User's Guide

TPS40193 Buck Controller Evaluation Module User's Guide

ABSTRACT

The TPS40193EVM-001 evaluation module is a 12-V to 1.8-V synchronous buck converter built around the TPS40193 synchronous buck controller. This module provides a convenient test platform for both evaluating the TPS40193 controller in a real application and prototyping synchronous buck converters using the TPS40193 controller.

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1 Introduction

The TPS40193EVM-001 evaluation module (EVM) is a synchronous buck converter that provides a fixed 1.8-V output at up to 10 A from a 12-V input bus. The EVM is designed to power up from a single supply, so no additional bias voltage is required for start-up. The demonstration module uses the TPS40193 reduced pin count mid-voltage synchronous buck controller.

1.1 Description

The TPS40193EVM-001 is designed to use a regulated 12-V (8V–14V) bus to produce a regulated 1.8-V output at up to 10 A of load current. The EVM is designed to demonstrate the capabilities of the TPS40193 in a typical 12-V bus to low-voltage application while providing a number of test points for evaluating the TPS40193 in a given application. The EVM can be modified to support output voltages from 0.9 V to 3.3 V by changing a single set resistor.

1.2 Applications

- Non-isolated medium current point-of-load and low voltage bus converters
- Networking equipment
- Telecommunications equipment
- Computer peripherals
- Digital set-top box

1.3 Features

- 8-V to 14-V input range
- 1.8-V fixed output, adjustable with single resistor
- 10-A_{DC} steady state output current
- 300-kHz switching frequency (fixed by the TPS40193)
- Single SO-8 MOSFETs for both the main switch and synchronous rectifier
- Double-sided, two active layer printed circuit board (PCB) with all components on top side
  - Test point signals routed on internal layers
- Active converter area of less than 1.2 $inch^2$(<1.54 inch × 0.76 inch)
- Convenient test points for probing switching waveforms and non-invasive loop response testing

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2 TPS40193EVM-001 Electrical Performance Specifications

Table 2-1 summarizes the electrical specifications of the TPS40193EVM-001.

Table 2-1. TPS40193EVM-001 Electrical and Performance Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNITS
Input Characteristics						
Input Voltage	V_{IN}		8	12	14	V
Input Current	I_{IN}	V_{IN} = Min, I_{OUT} = Max		2.7	2.85	A
No Load Input Current		V_{IN} = Min, I_{OUT} = 0A		48	60	mA
Input UVLO	V_{IN_UVLO}	I_{OUT} = Min to Max	3.9	4.2	4.4	V
Input OV	V_{IN_OV}	I_{OUT} = Min to Max		N/A		V
Output Characteristics						
Output Voltage	V_{OUT}	V_{IN} = NOM, I_{OUT} = NOM	1.86	1.8	1.84	V
Line Regulation		V_{IN} = Min to Max, I_{OUT} = NOM			0.5	%
Load Regulation		V_{IN} = NOM, I_{OUT} = Min to Max			0.5	%
Output Voltage Ripple	V_{OUT_Ripple}	V_{IN} = NOM, I_{OUT} = MAX			40	mV_{PP}
Output Current	I_{OUT}	V_{IN} = Min to Max	0	6	10	A
Output Over Current Inception Point	I_{OCP}	V_{IN} = NOM, V_{OUT} = (V_{OUT} – 5%)		19		A
Output OVP	V_{OVP}	I_{OUT} = Min to Max		N/A		V
Transient Response Load Step	ΔI	0.75 × I_{OUT_Max} to 0.25 × I_{OUT_Max}		5		A
Load Slew Rate				5		A/µs
Overshoot					50	mV
Settling Time						ms
System Characteristics						
Switching Frequency	F_{SW}		250	300	350	kHz
Peak Efficiency	η_{PK}	V_{IN} = NOM, I_{OUT} = Min to Max		95		%
Full Load Efficiency	η	V_{IN} = NOM, I_{OUT} = Max		92		%
Operating Temperature Range	T_{OP}	V_{IN} = Min to Max, I_{OUT} = Min to Max	–40	+25	+60	°C
Mechanical Characteristics						
Dimensions (Active Area)	W	Width		1.54		in
	L	Length		0.76		in

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3 Schematic

Figure 3-1 shows the schematic for this EVM. See Table 8-1, the Bill of Materials, for specific values.

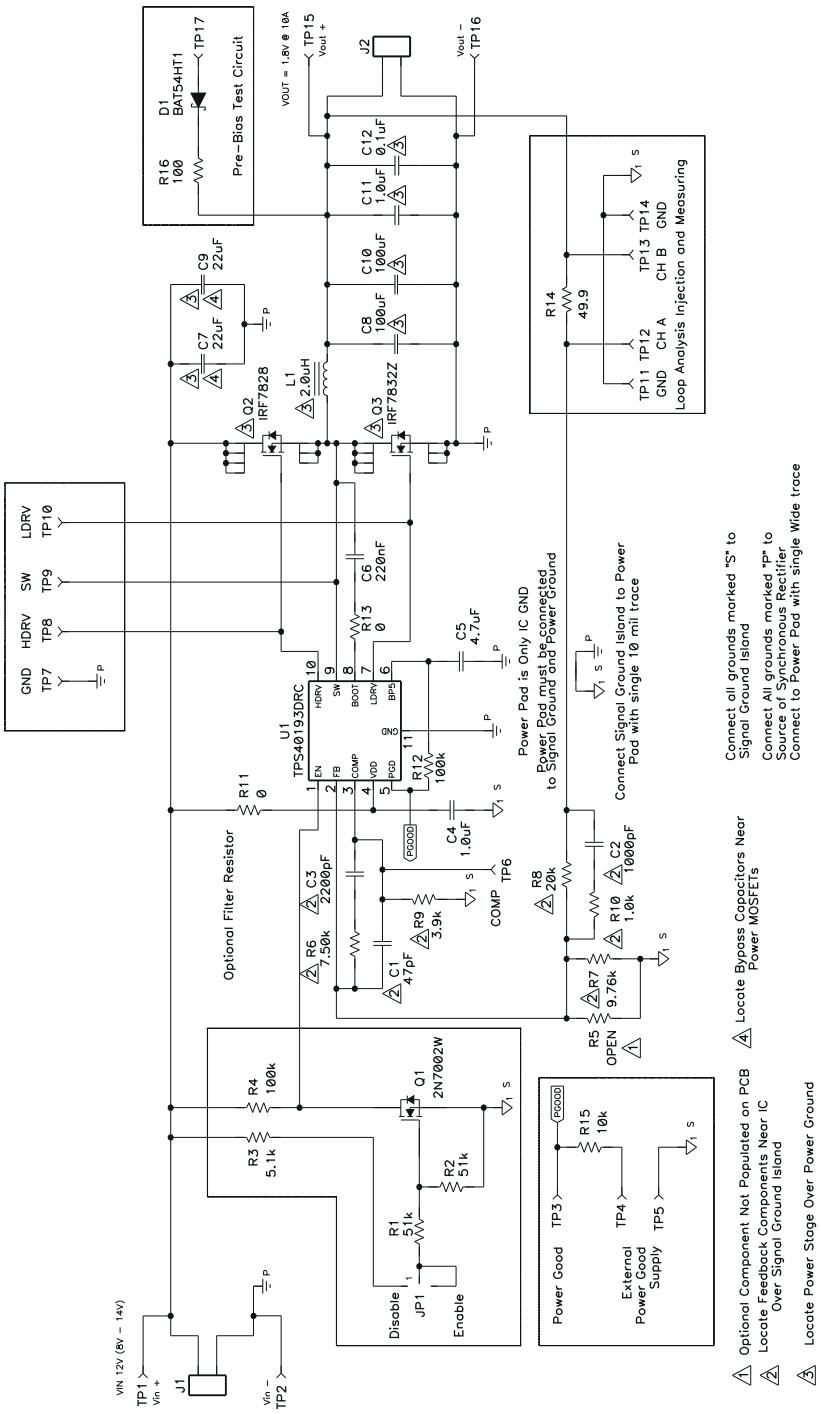


Figure 3-1. TPS40193EVM-001 Schematic

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4 General Configuration and Description

This section reviews the general configurations for using the TPS40193EVM-001.

4.1 Adjusting Output Voltage (R7)

The regulated output voltage can be adjusted within a limited range by changing the ground resistor in the feedback resistor divider (R7). The output voltage is given by the formula shown in Equation 1:

$$V_{VOUT} = V_{VREF} \times \frac{R_8 + R_7}{R_7} \quad (1)$$

where

- V_{VREF} = 0.591 V
- R_8 = 20 kΩ

Table 4-1 contains common values for R7 to generate popular output voltages. The TPS40193EVM-001 is stable through these output voltages, but efficiency may suffer because the power stage is optimized for 1.8V output.

Table 4-1. Adjusting V_{OUT} with R7

V_{OUT}	R7 (kΩ)
3.3V	4.32
2.5V	6.19
2.25V	7.15
2.0V	8.25
1.8V	9.76
1.5V	13.0
1.2V	19.1
1.0V	28.7
0.9V	38.3

The values in Table 4-1 provide less than 1% nominal set-point error in the output voltage. If a tighter nominal value is required, R5 can be used in parallel with R7 to obtain a wider range of resistor values, using commonly available E96 resistors.

4.2 Adjusting Short-Circuit Protection (R9)

The TPS40193 uses a selectable current limit for short-circuit protection. The current limit is selected from three predefined levels by placing a resistor at R9. The TPS40193 compares the voltage drop across the high-side FET (VDD to SW) to an internal reference voltage selected during start-up. Table 4-2 shows the voltage levels.

Table 4-2. Adjusting V_{SCP} with R9

V_{SCP} (min)	R7 (kΩ)
88mV	3.9
160mV	Open
228mV	12

The current before declaring short-circuit protection can be determined by dividing the V_{SCP} by the $R_{DS(ON)}$ of the high-side FET (Q2).

4.3 Disable Jumper (JP1)

The TPS40193EVM-001 provides a three-pin, 100-mil (0.100 in) header and shunt for testing the TPS40193 disable function.

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Placing the JP1 shunt in the Left Position 

drives the Q1 FET to pull the TPS40193 EN pin low, disabling the controller. Removing the JP1 shunt or installing it in the Right Position 

shorts the Q1 gate to ground and enables the TPS40193EVM-001 output.

4.4 Test Point Descriptions

Table 4-3 describes the TPS40196EVM-001 test points and identifies the respective sections of this user guide that discuss each test point.

Table 4-3. Test Point Descriptions

Test Point	Label	Use/Function	Section
TP1	V_{IN+}	Monitor input voltage to the module	Section 4.4.1
TP2	$V_{IN–}$	Monitor input voltage to the module	
TP3	Power-Good	Power-Good output voltage	Section 4.4.2
TP4	Ext Source	External source for Power-Good circuit	
TP5	GND	Ground for external source for Power-Good	
TP6	COMP	Monitor COMP voltage	Section 4.4.3, Section 4.4.5
TP7	GND	Ground for SW, LDRV and HDRV measurements	Section 4.4.4
TP8	HDRV	Monitor high-side gate drive (Q2)	
TP9	SW	Monitor switch node waveforms	
TP10	LDRV	Monitor low-side gate drive (Q3)	
TP11	GND	Ground for Loop Monitoring Probe	Section 4.4.5
TP12	CH1	Loop injection point and injection monitoring point	
TP13	CH2	Loop injection point and output response monitoring point	
TP14	GND	Ground for Loop Monitoring Probe	
TP15	V_{OUT+}	Monitor output voltage from the module	Section 4.4.6
TP16	$V_{OUT–}$	Monitor output voltage from the module	
TP17	Pre-Bias	Injection point to test pre-bias load compliance	Section 4.4.7

4.4.1 Input Voltage Monitoring (TP1, TP2)

The TPS40193EVM-001 provides two test points for measuring the voltage applied to the module. These test points allow the user to measure the actual module voltage without losses from input cables and connector losses. All input voltage measurements should be made between TP1 and TP2. To use TP1 and TP2, connect a voltmeter positive terminal to TP1 and negative terminal to TP2.

4.4.2 Power-Good (TP3, TP4, TP5)

The TPS40193EVM-001 has three test points to allow the user to evaluate the TPS40193 power-good function. TP4 provides access to the power-good output of the TPS40193. It has a 100-kΩ pullup resistor to the TPS40193 5-V regulator, and can be used as a logic signal with no additional requirements. TP3 provides a connection for an external power-good source for 3.3-V logic. TP3 is connected to the power-good circuit through a 10-kΩ pullup resistor. TP5 provides a local ground access to connect a remote disable circuit.

4.4.3 Compensation and Initialization (TP6)

The TPS40193EVM-001 also provides a test point connection to the COMP pin of the TPS40193 controller. This test point can be used to monitor the COMP voltage during the controller power-on initialization that sets the controller short-circuit protection (SCP) threshold. The test point can also be used to monitor the pulse-width

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modulator (PWM) comparator input voltage (COMP) during operation, or used to measure the power stage gain by following the loop analysis directions but moving Channel A probe from TP12 to TP6.

4.4.4 Switching Waveforms (TP7, TP8, TP9, TP10)

The TPS40193EVM-001 has three test points and a local ground connection (TP7) to monitor the main switching waveforms. Connect an oscilloscope probe to TP8 to monitor the high-side gate drive applied to the gate of Q2. Connect an oscilloscope probe to TP9 to monitor the switch node voltage. The gate-to-source voltage (V_{GS}) of the high-side FET can be determined by a math function TP8—TP9 if both channels use the same scale. Connect an oscilloscope probe to TP9 to monitor the low-side gate drive applied to the gate of Q3. Because the source of Q3 is connected directly to ground, no math function is required to determine the gate-to-source voltage of the low-side FET.

4.4.5 Loop Analysis (TP11, TP12, TP13, TP14)

The TPS40193EVM-001 contains a 49.9-Ω series resistor (R14) in the feedback loop to allow for matched impedance signal injection into the feedback for loop response analysis. An isolation transformer should be used to apply a small (30 mV or less) signal across R14 through TP12 and TP13. By monitoring the AC injection level at TP13 and the returned AC level at TP14, the power-supply loop response can be determined. Moving Channel A from TP12 to TP6 (COMP) the control-to-output response of the power stage (also referred to as the *power stage transfer function*) can be directly measured. See Section 3.9xx for a detailed procedure to perform loop response measurements.

4.4.6 Output Voltage and Monitoring (TP15, TP16)

There are two test points on the TPS40193EVM-001 for measuring the voltage generated by the module. These test points allow the user to measure the actual module output voltage without losses from output cables and connector losses. All output voltage measurements should be made between TP15 and TP16. To use TP1 and TP2, connect a voltmeter positive terminal to TP15 and negative terminal to TP16. For output ripple measurements, TP15 and TP16 allow a user to limit the ground loop area by using the tip and barrel measurement technique shown in Figure 5-2 (All output ripple measurements should be made using this method of measurement).

4.4.7 Pre-Bias Input (TP17)

The TPS40193EVM-001 contains a pre-bias injection circuit with 100-Ω resistor and series diode to allow testing and evaluation of the TPS40193 pre-bias support compatibility. Apply a voltage less than the target output voltage to TP17. Monitoring the output voltage during start-up demonstrates the ability of the TPS40193 to power up without drawing current from a pre-biased output. D2 prevents the output voltage from back-driving the pre-bias source.

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5 Test Setup

5.1 Equipment

5.1.1 Voltage Source

V_{IN}: The input voltage source (V_{IN}) should be a 0-V to 15-V variable DC source capable of 5 A_{DC}. Connect V_{IN} to J1 as shown in Figure 5-1.

5.1.2 Meters

A1: 0 A_{DC}–5 A_{DC}, ammeter

V1: V_{IN}, 0-V to 15-V voltmeter

V2: V_{OUT}, 0-V to 5-V voltmeter

5.1.3 Loads

LOAD1: The output load (LOAD1) should be an electronic constant current mode load capable of 0 A_{DC}–10 A_{DC} at 1.8 V.

5.1.4 Oscilloscope

Oscilloscope: A digital or analog oscilloscope can be used to measure the ripple voltage on V_{OUT}. The oscilloscope should be set for taking output ripple measurements:

- 1-MΩ impedance
- 20-MHz bandwidth
- AC coupling
- 1-µs/division horizontal resolution
- 10-mV/division vertical resolution

TP15 and TP16 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP15 and holding the ground barrel to TP16, as shown in Figure 5-2. For a hands-free approach, the loop in TP16 can be cut and opened to cradle the probe barrel. Using a leaded ground connection may induce additional noise because of the large ground loop area.

5.1.5 Recommended Wire Gauge

V_{IN} to J1: The connection between the source voltage, V_{IN}, and J1 of HPA238 can carry as much as 5 A_{DC}. The minimum recommended wire size is AWG #16 with the total length of wire less than four feet (two feet input, two feet return maximum recommended).

J2 to LOAD1 (Power): The power connection between J2 of HPA238 and LOAD1 can carry as much as 10 A_{DC}. The minimum recommended wire size is 2× AWG #16, with the total length of wire less than two feet (one foot output, one foot return maximum recommended).

5.1.6 Other

Fan: This evaluation module includes components that can become hot to the touch. Because this EVM is not enclosed (to allow probing of circuit nodes), a small fan capable of 200lfm–400lfm is required to reduce component surface temperatures to prevent user injury.

CAUTION

The EVM should not be left unattended while powered.

WARNING

The EVM should not be probed while the fan is not running.

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5.2 Equipment Setup

Figure 5-1 through Figure 5-3 show the basic test setup recommended to evaluate the TPS40193EVM-001. Please note that although the return for J1 and J2 are the same, the connections should remain separate, as shown in Figure 5-1.

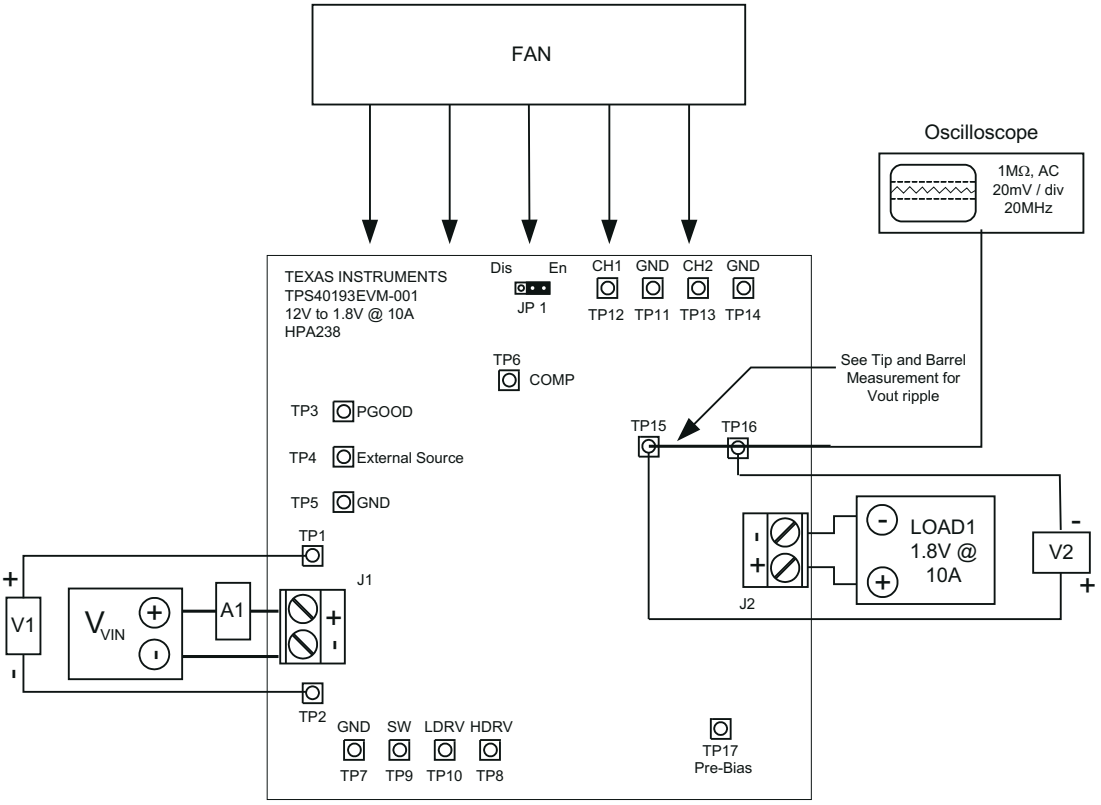


Figure 5-1. TPS40193EVM-001 Recommended Test Setup

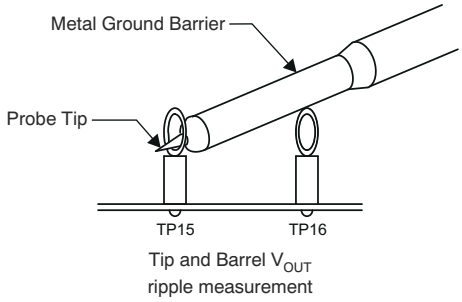


Figure 5-2. TPS40193EVM-001 Output Ripple Measurement—Tip and Barrel Using TP15 and TP16

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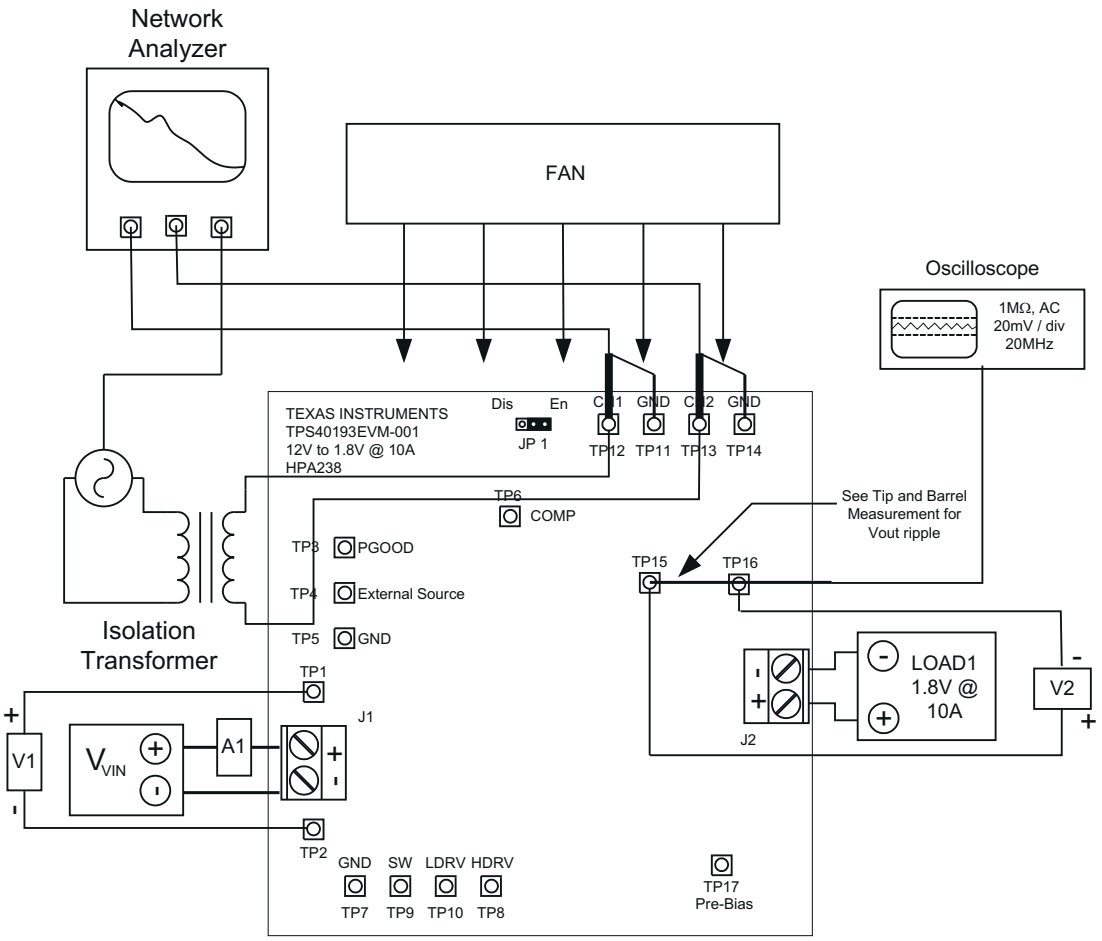


Figure 5-3. TPS40193EVM-001 Control Loop Measurement Setup

5.3 Start-Up/Shutdown Procedure

Follow these steps to start up and shut down the TPS40193EVM-001.

1. Increase V_{IN} from 0 V to 12 V_{DC}.
2. Vary LOAD1 from 0 A_{DC} to 10 A_{DC}.
3. Vary V_{IN} from 8.0 V_{DC} to 14 V_{DC}.
4. Decrease V_{IN} to 0 V_{DC}.
5. Decrease LOAD1 to 0 A.

5.4 Output Ripple Voltage Measurement Procedure

Follow these steps to measure the output ripple voltage on the TPS40193EVM-001.

1. Increase V_{IN} from 0 V_{DC} to 12 V_{DC}.
2. Adjust LOAD1 to desired load between 0 A_{DC} and 10 A_{DC}.
3. Adjust V_{IN} to desired load between 8.0 V_{DC} and 14 V_{DC}.
4. Connect oscilloscope probe to TP15 and TP16 as shown in Figure 5-2.
5. Measure output ripple.
6. Decrease V_{IN} to 0 V_{DC}.
7. Decrease LOAD1 to 0 A.

5.5 Control Loop Gain and Phase Measurement Procedure

Follow these steps to measure the control loop gain and phase on the TPS40193EVM-001.

1. Connect 1-kHz to 1-MHz isolation transformer to TP12 and TP13 as shown in Figure 5-3.
2. Connect input signal amplitude measurement probe (Channel A) to TP12 as shown in Figure 5-3.
3. Connect output signal amplitude measurement probe (Channel B) to TP13 as shown in Figure 5-3.

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4. Connect ground lead of Channel A and Channel B to TP11 and TP14 as shown in Figure 5-3.
5. Inject 30-mV (or less) signal across R14 through isolation transformer.
6. Sweep frequency from 1 kHz to 1 MHz, with 1-0Hz or lower post filter.
7. Control loop gain can be measured by Equation 2:

$$20 \times \text{LOG}\left(\frac{\text{Channel B}}{\text{Channel A}}\right) \tag{2}$$

8. Control loop phase is measured by the phase difference between Channel A and Channel B.
9. Control to output response (power stage transfer function) can be measured by connecting Channel A probe to TP6 (COMP) and Channel B probe to TP13.
10. Output to control response (error amplifier transfer function) can be measured by connecting Channel B probe to TP6 (COMP) and Channel A probe to TP12.
11. Disconnect isolation transformer from TP12 and TP13 before making other measurements (signal injection into feedback may interfere with accuracy of other measurements).

5.6 Equipment Shutdown

Follow these steps to power down the EVM.

1. Shut down the oscilloscope.
2. Shut down V_{IN}.
3. Shut down LOAD1.
4. Shut down the fan.

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6 TPS40193EVM-001 Typical Performance Data and Characteristic Curves

Figure 6-1 through Figure 6-7 present typical performance curves for the TPS40193EVM-001. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference only and may differ from actual field measurements.

6.1 Efficiency

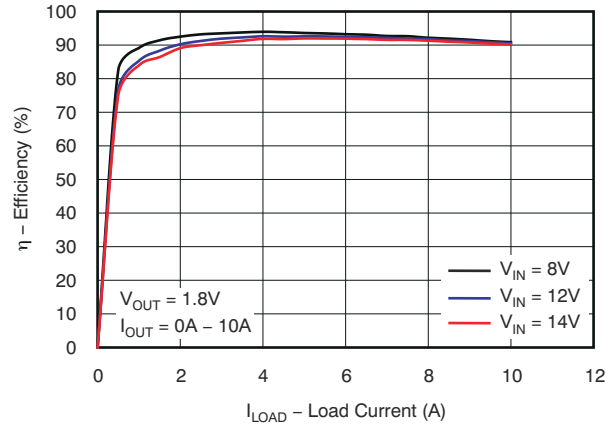


Figure 6-1. TPS40193EVM-001 Efficiency vs Load Current

6.2 Line and Load Regulation

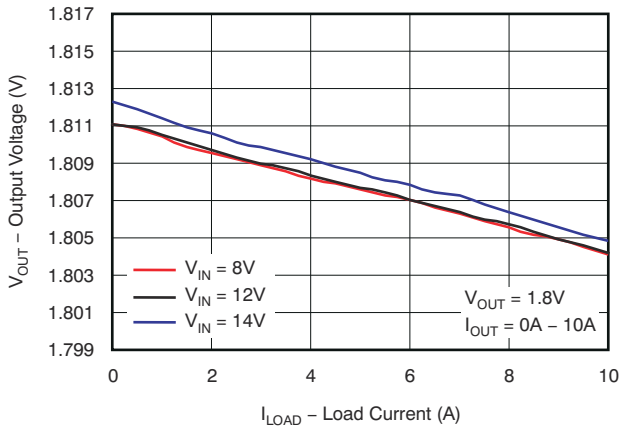


Figure 6-2. TPS40193EVM-001 Output Voltage vs Load Current (±0.5% Window Shown)

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6.3 Output Voltage Ripple

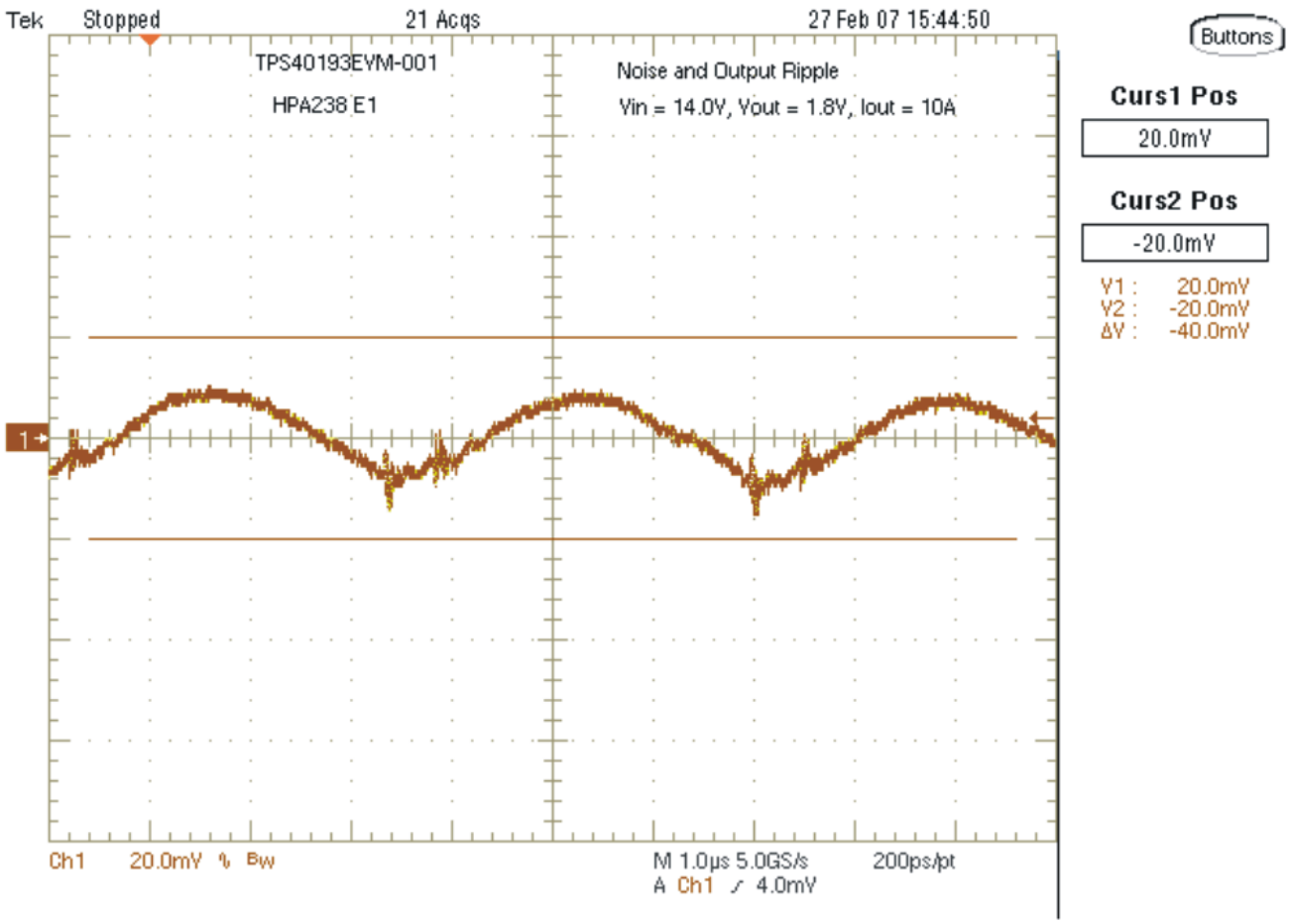
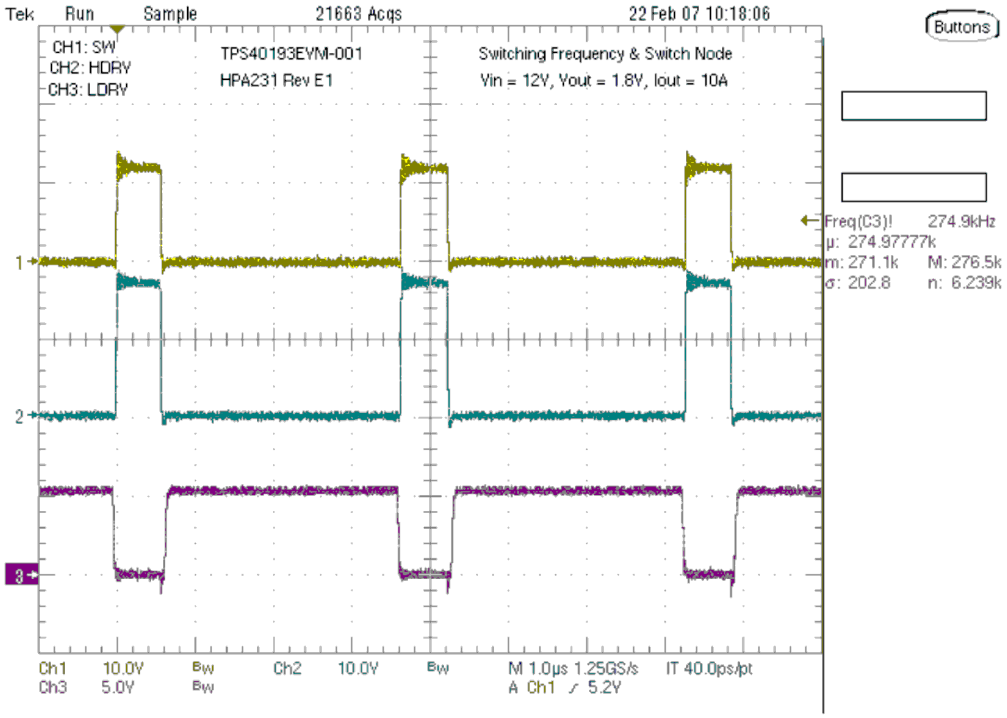


Figure 6-3. TPS40193EVM-001 Output Voltage Ripple

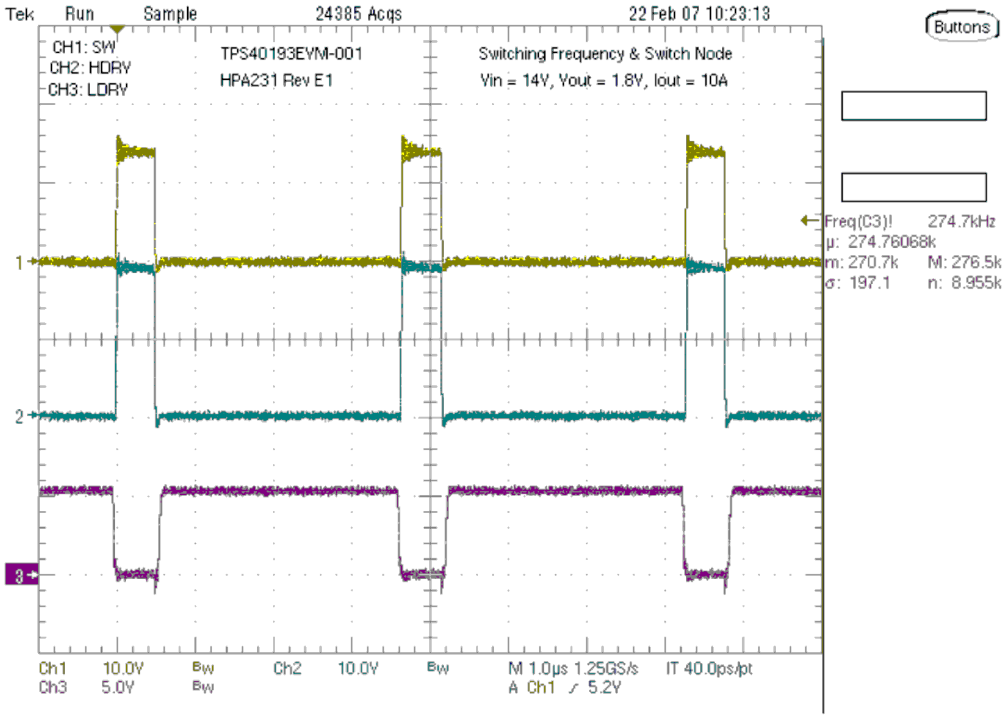
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6.4 Switch Node



Ch1: TP9 (SW); Ch2: TP8 (HDRV); Ch3: TP10 (LDRV)

Figure 6-4. TPS40193EVM-001 Switching Waveforms (V_{IN} = 8 V, I_{OUT} = 10 A)



Ch1: TP9 (SW); Ch2: TP8 (HDRV); Ch3: TP10 (LDRV)

Figure 6-5. TPS40193EVM-001 Switching Waveforms (V_{IN} = 14 V, I_{OUT} = 10 A)

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6.5 Control Loop Bode Plot

6.5.1 Low Line (V_{IN} = 8 V)

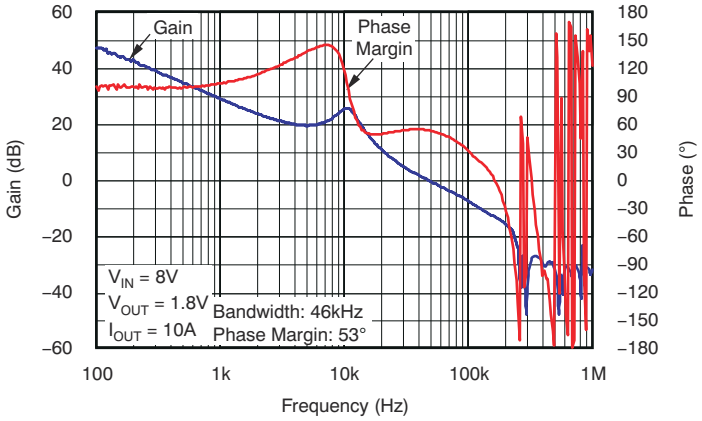


Figure 6-6. TPS40193EVM-001 Gain and Phase vs Frequency

6.5.2 High Line (V_{IN} = 14 V)

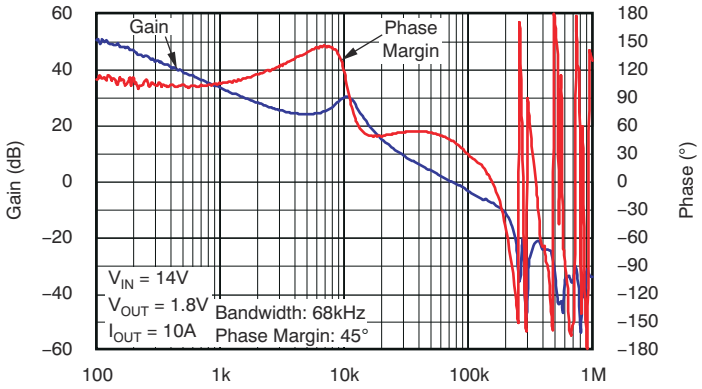


Figure 6-7. TPS40193EVM-001 Gain and Phase vs Frequency

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7 EVM Assembly Drawings and Layout

Figure 7-1 through Figure 7-6 show the design of the TPS40193EVM-001 printed circuit board (PCB). The EVM has been designed using a 4-layer, 2oz, copper-clad PCB (2.5 inch × 2.5 inch), with all components in a 1.54-inch × 0.76-inch active area on the top side and all active traces to the top and bottom layers of the board. This configuration allows the user to easily view, probe, and evaluate the TPS40193 control IC in a practical, double-sided application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space-constrained systems.

Unless otherwise specified, these figures illustrate the view from the top side of the PCB.

Note

Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing TPS40193EVM-001 PCBs.

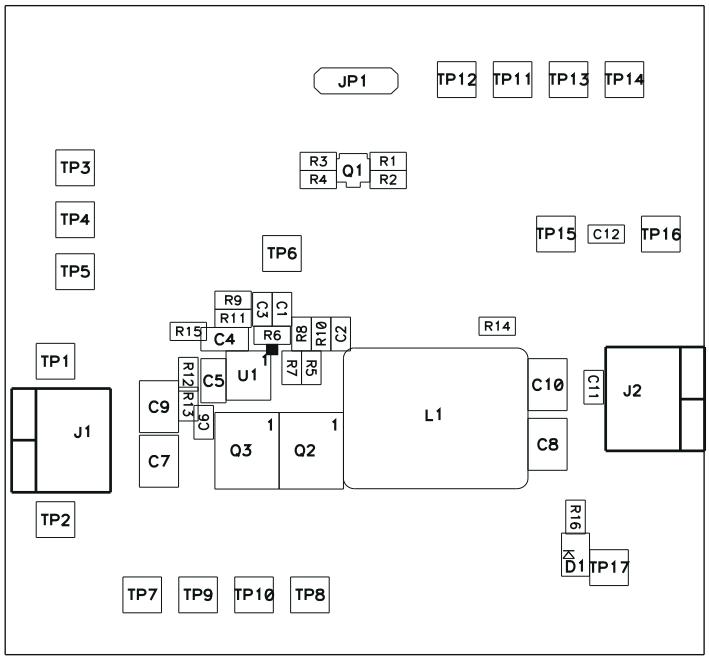


Figure 7-1. TPS40193EVM-001 Component Placement

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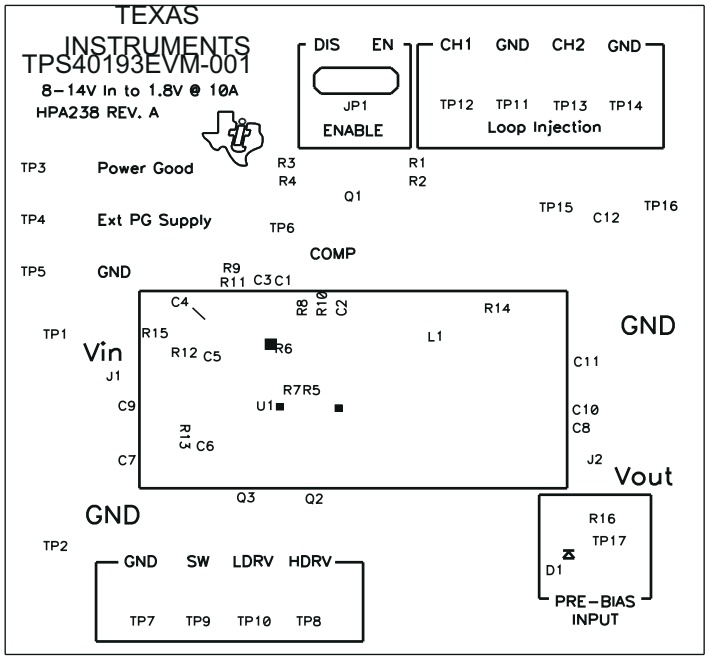


Figure 7-2. TPS40193EVM-001 Silkscreen

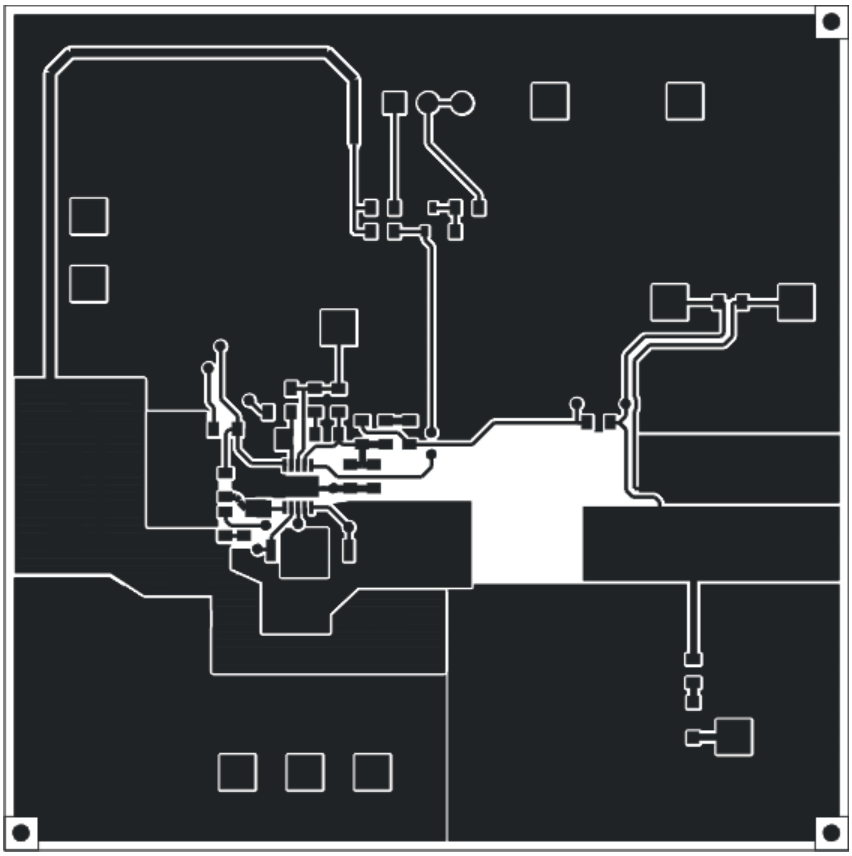


Figure 7-3. TPS40193EVM-001 Top Copper Layer

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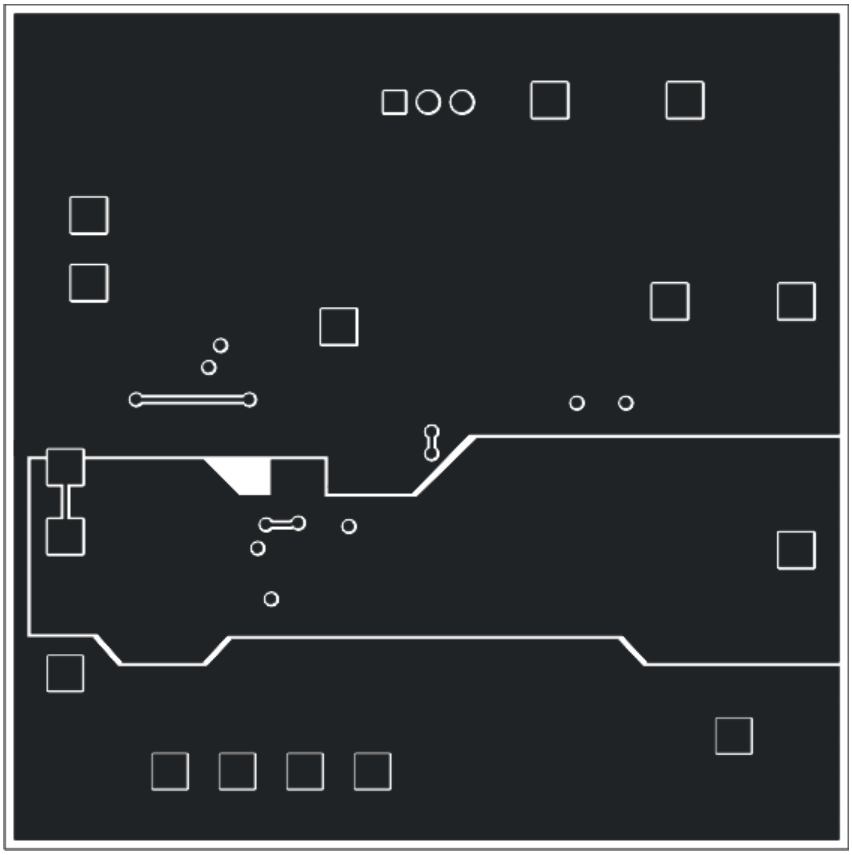


Figure 7-4. TPS40193EVM-001 Bottom Copper Layer

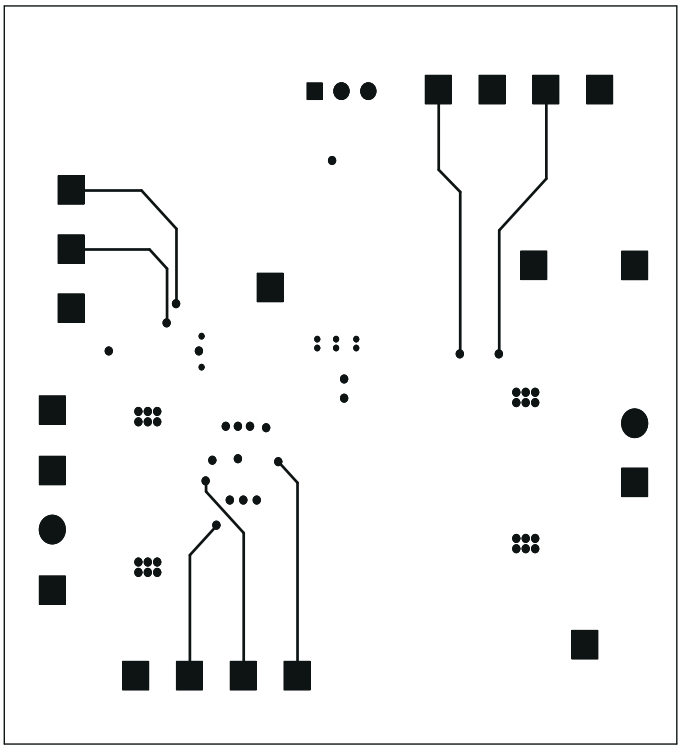


Figure 7-5. TPS40193EVM-001 Internal Layer 1

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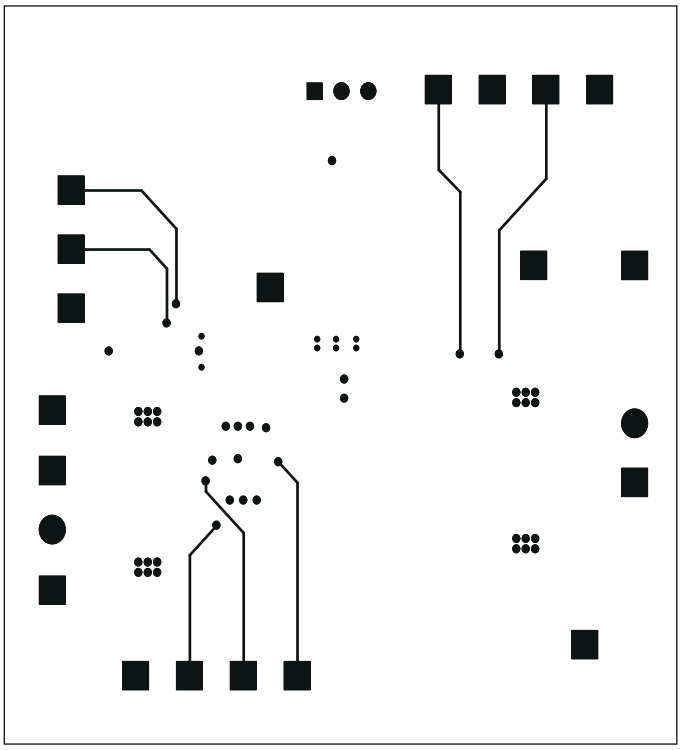


Figure 7-6. TPS40193EVM-001 Internal Layer 2

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8 Bill of Materials

Table 8-1 lists the EVM components as configured according to the schematic (see Figure 3-1).

Table 8-1. Bill of Materials

Qty	RefDes	Value	Description	Size	Part Number	MFR
1	C1	47 pF	Capacitor, Ceramic, 10 V, C0G, 10%	0603	STD	STD
1	C11	1.0 µF	Capacitor, Ceramic, 6.3 V, X5R, 20%	0603	STD	STD
1	C12	0.1 µF	Capacitor, Ceramic, 6.3 V, X5R, 20%	0603	STD	STD
1	C2	1000 pF	Capacitor, Ceramic, 10 V, C0G, 10%	0603	STD	STD
1	C3	2200 pF	Capacitor, Ceramic, 10 V, C0G, 10%	0603	STD	STD
1	C4	1.0 µF	Capacitor, Ceramic, 25 V, X5R, 20%	0805	STD	STD
1	C5	4.7 µF	Capacitor, Ceramic, 10 V, X5R, 20%	0805	STD	STD
1	C6	220 nF	Capacitor, Ceramic, 10 V, X5R, 20%	0603	Std	Std
2	C7, C9	22 µF	Capacitor, Ceramic, 25 V, X5R, 20%	1210	C3225X7R1E106M	TDK
2	C8, C10	100 µF	Capacitor, Ceramic, 6.3 V, X5R, 20%	1210	C3225X5R0J107M	TDK
1	D2	BAT54HT1	Diode, Schottky, 200-mA, 30-V	SOD323	BAT54HT1	On Semi
2	J1, J2	ED1609-ND	Terminal Block, 2-pin, 15-A, 5.1 mm	0.40in x 0.35in	ED1609	OST
1	JP1	PTC36SAAN	Header, 3-pin, 100-mil spacing, (36-pin strip)	0.100in x 3in	PTC36SAAN	Sullins
1	L1	2	Inductor, SMT, xxA	0.512in x 0.571in	PG0077.xxx	Pulse
1	Q1	2N7002W	Mosfet, N-Ch, VDS 60v, RDS 2 ohms, ID 115 mA	SOT-323 (SC-70)	2N7002W-7	Diodes Inc
1	Q2**	IRF7828	XSTR, MOSFET, N-Chan, 30 V, Rds(ON) 9.5 mΩ	SO8	IRF7828	IR
1	Q3**	IRF7832Z	XSTR, MOSFET, N-Chan, 30 V, Rds(ON) 4.8 mΩ	SO8	IRF7832Z	IR
2	R1, R2	51 k	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R10	1.0 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R11, R13	0	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R12	100 k	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R14	49.9	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R15	10 k	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R16	100	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R3	5.1 k	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R4	100 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R5	Open	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	7.50 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	9.76 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	20 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	3.9 k	Resistor, Chip, 1/16W, 5%	0603	Std	Std
4	TP1, TP4, TP15, TP17	5010	Test Point, Red, Thru Hole	0.125in x 0.125in	5010	Keystone
6	TP2, TP5, TP7, TP11, TP14, TP16	5011	Test Point, Black, Thru Hole	0.125in x 0.125in	5011	Keystone
7	TP3, TP6, TP8, TP9, TP10, TP12, TP13	5012	Test Point, White, Thru Hole	0.125in x 0.125in	5012	Keystone
1	U1	TPS40193DRC	IC, Cost Optimized Mid Vin Freq. 300kHz Sync. Buck controller	DRC10	TPS40193DRC	Texas Instruments
1	—–	—	PCB, 3 In x 3 In x 0.062 In	—	HPA238	Any
1	—	—	Shunt, 100-mil, Black	0.100	929950-00	3M

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9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2017) to Revision A (January 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	3
• Updated the user's guide title.	3

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