32.768 KHZ CLOCK OSCILLATOR

MK3200

Description

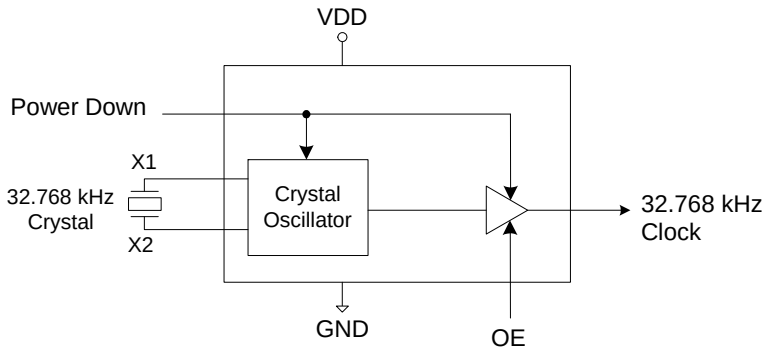
The MK3200 is IDT's lowest cost, low power clock oscillator that generates a low power 32.768 kHz output from an inexpensive 32.768 kHz crystal. This part includes a power down pin and allows you to tri-state the output clock for in-circuit testing.

IDT manufactures the largest variety of clock synthesizers for all applications. If more clock outputs are needed, including MHz frequencies, see the MK32xx family of parts. Consult IDT to eliminate VCXOs, crystals and oscillators from your board.

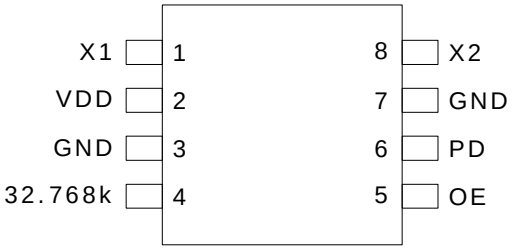
Features

- Packaged in 8-pin SOIC or 8-pin MSOP (3.00 mm body)
- Pb (lead) free package
- Operates from 2.5 V to 5 V
- Consumes only 3.5 µA in normal operation
- Accepts an inexpensive 32.768 kHz crystal input
- Offers power down mode
- Includes an Output Enable pin to tri-state the output for in-circuit testing
- Advanced, low power, sub-micron CMOS process
- For other 32.768 kHz-based clocks with MHz outputs, please consult IDT
- Industrial temperature version available

Block Diagram



Pin Assignment



8-pin (150 mil) SOIC or
8-pin MSOP (3.00 mm body)

Power Down Select Table

PD	32.768k	Oscillator
0	On	On
1	Low	Off

Output Enable Select Table

OE	32.768k	Oscillator
0	Tri state (Hi-Z)	On
1	On	On

0 = connect directly to GND.

1 = connect directly to VDD.

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	Input	Crystal connection. Connect to a 32.768 kHz crystal.
2	VDD	Power	Connect to +3.3 V.
3	GND	Power	Connect to ground.
4	32.768k	Input	32.768 kHz clock output.
5	OE	Output	Output Enable.
6	PD	Input	Power down pin. Turns off entire chip when high.
7	GND	Input	Connect to ground.
8	X2	Output	Crystal connection. Connect to a 32.768 kHz crystal.

External Components

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Decoupling Capacitor

As with any high-performance mixed-signal IC, the MK3200 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and the PCB ground plane.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the MK3200. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

4) The input crystal must be connected as close to the chip as possible. The input crystal should be a parallel mode crystal with a 12 pF load capacitance.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK3200. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+ 0.5	V
Clock Outputs	Referenced to GND	-0.5		VDD+ 0.5	V
Storage Temperature		-65		150	°C
Soldering Temperature	Max 10 seconds			260	°C
Junction Temperature				125	°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.15	+3.3	+3.45	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		5.250	V
Supply Current	IDD	No load, OE=1		3.5		µA
		PD = 0		3.5		µA
Output High Voltage (CMOS level)	V_{OH}	I_{OH} = -1.5 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -3 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Short Circuit Current	I_{OS}			±6		mA

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}			32.768		kHz
Output Rise Time	t_{OR}	20% to 80%, Note 1		8		ns
Output Fall Time	t_{OF}	80% to 20%, Note 1		8		ns
Duty Cycle		at VDD/2	40	50	60	%
Input Crystal Accuracy				0	±30	ppm

Thermal Characteristics (8SOIC)

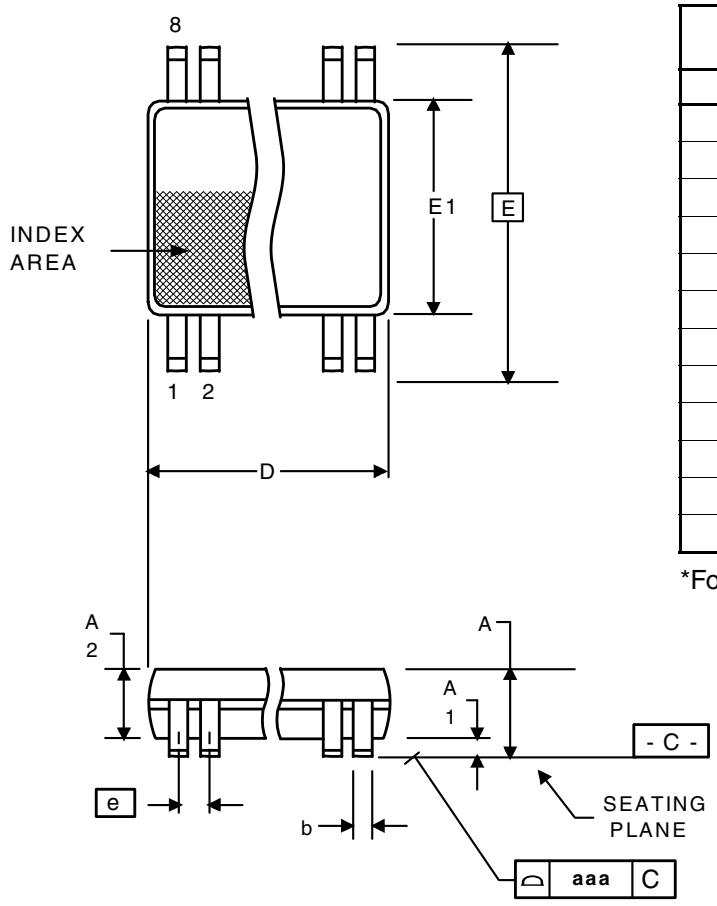
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		135		°C/W
	θ_{JA}	1 m/s air flow		93		°C/W
	θ_{JA}	3 m/s air flow		78		°C/W
Thermal Resistance Junction to Case	θ_{JC}			60		°C/W

Thermal Characteristics (8MSOP)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		95		°C/W
Thermal Resistance Junction to Case	θ_{JC}			48		°C/W

Package Outline and Package Dimensions (8-pin MSOP, 3.00 mm Body)

Package dimensions are kept current with JEDEC Publication No. 95

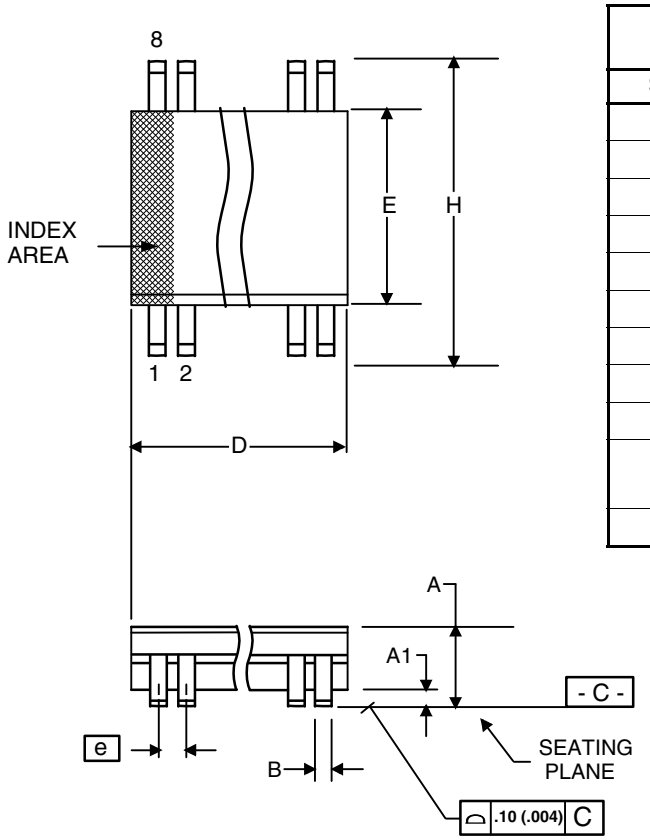


	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.10	--	0.043
A1	0	0.15	0	0.006
A2	0.79	0.97	0.031	0.038
b	0.22	0.38	0.008	0.015
C	0.08	0.23	0.003	0.009
D	3.00 BASIC		0.118 BASIC	
E	4.90 BASIC		0.193 BASIC	
E1	3.00 BASIC		0.118 BASIC	
e	0.65 Basic		0.0256 Basic	
L	0.40	0.80	0.016	0.032
α	0°	8°	0°	8°
aaa	-	0.10	-	0.004

*For reference only. Controlling dimensions in mm.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.0	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK3200SLF	MK3200SL	Tubes	8-pin SOIC	0 to +70° C
MK3200SLFTR	MK3200SL	Tape and Reel	8-pin SOIC	0 to +70° C
MK3200SILF	MK3200IL	Tubes	8-pin SOIC	-40 to +85° C
MK3200SILFTR	MK3200IL	Tape and Reel	8-pin SOIC	-40 to +85° C
MK3200GLF	3200GL	Tubes	8-pin MSOP	0 to +70° C
MK3200GLFT	3200GL	Tape and Reel	8-pin MSOP	0 to +70° C

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(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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