MOSFETs Silicon P-Channel MOS (U-MOSⅥ)

SSM6J422TU

1. Applications

- Power Management Switches

2. Features

(1) AEC-Q101 qualified (Please see the orderable part number list)

(2) 1.5-V gate drive voltage.

(3) Low drain-source on-resistance

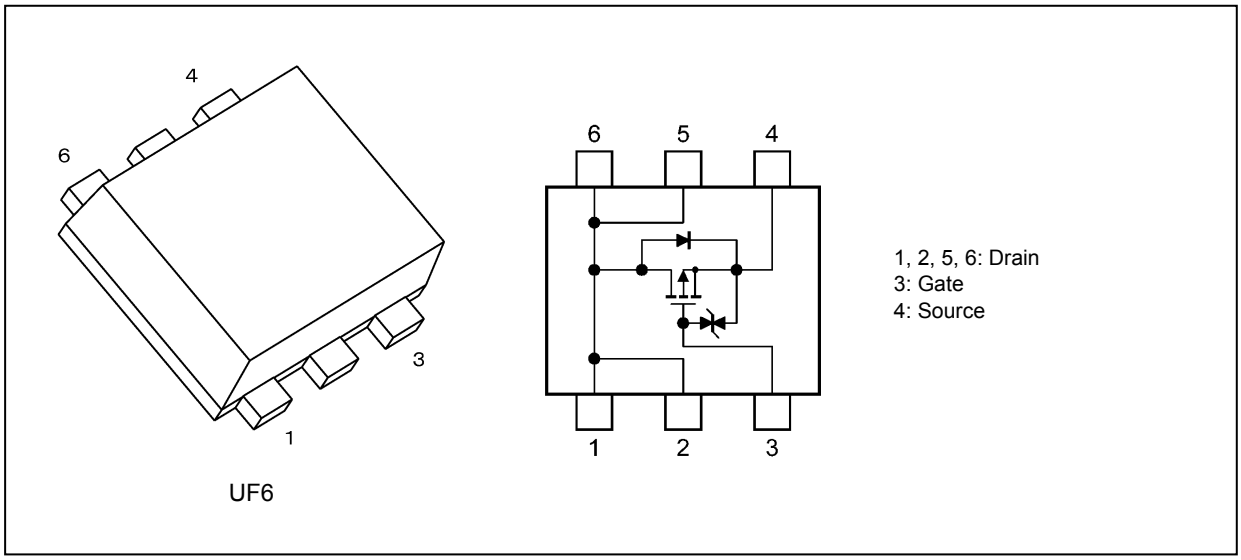
: $R_{DS(ON)}$ = 99.6 mΩ (max) (@V_{GS} = -1.5 V)

$R_{DS(ON)}$ = 67.8 mΩ (max) (@V_{GS} = -1.8 V)

$R_{DS(ON)}$ = 51.4 mΩ (max) (@V_{GS} = -2.5 V)

$R_{DS(ON)}$ = 42.7 mΩ (max) (@V_{GS} = -4.5 V)

3. Packaging and Pin Configuration



4. Orderable part number

Orderable part number	AEC-Q101	Note
SSM6J422TU,LF	—	General Use
SSM6J422TU,LXGF	YES (Note 1)	Unintended Use (Note 1)
SSM6J422TU,LXHF	YES	Automotive Use

Note 1: For more information, please contact our sales or use the inquiry form on our website.

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5. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	-20	V
Gate-source voltage		V_{GSS}	-8/+6	
Drain current (DC)	(Note 1)	I_D	-4	A
Drain current (pulsed)	(Note 1,2)	I_{DP}	-16	
Power dissipation	(Note 3)	P_D	1	W
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: Pulse width (PW) ≤ 10 μs, duty ≤ 1%

Note 3: Device mounted on an FR4 board.(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance, $R_{th(ch-a)}$, and the power dissipation, P_D, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

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6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = -8/+6 V, V_{DS} = 0 V	—	—	±1	μA
Drain cut-off current		I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V	—	—	-1	
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = -1 mA, V_{GS} = 0 V	-20	—	—	V
Drain-source breakdown voltage	(Note 1)	$V_{(BR)DSX}$	I_D = -1 mA, V_{GS} = 5 V	-15	—	—	
Gate threshold voltage	(Note 2)	V_{th}	V_{DS} = -3 V, I_D = -1 mA	-0.3	—	-1.0	
Drain-source on-resistance	(Note 3)	$R_{DS(ON)}$	I_D = -3.0 A, V_{GS} = -4.5 V	—	36.9	42.7	mΩ
			I_D = -2.5 A, V_{GS} = -2.5 V	—	42.8	51.4	
			I_D = -1.5 A, V_{GS} = -1.8 V	—	50.6	67.8	
			I_D = -0.5 A, V_{GS} = -1.5 V	—	58.6	99.6	
Forward transfer admittance	(Note 3)	$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -1.0 A	4.5	9.1	—	S

Note 1: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (-1 mA for this device). Then, for normal switching operation, $V_{GS(ON)}$ must be higher than V_{th}, and $V_{GS(OFF)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.
Take this into consideration when using the device.

Note 3: Pulse measurement.

6.2. Dynamic Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	—	840	—	pF
Reverse transfer capacitance	C_{rss}		—	99	—	
Output capacitance	C_{oss}		—	118	—	
Switching time (turn-on time)	t_{on}	V_{DD} = -10 V, I_D = -2.0 A V_{GS} = 0 to -2.5 V, R_G = 4.7 Ω, Duty ≤ 1%, Input: t_r, t_f < 5 ns Common source	—	32	—	ns
Switching time (turn-off time)	t_{off}		—	107	—	

6.3. Switching Time Test Circuit

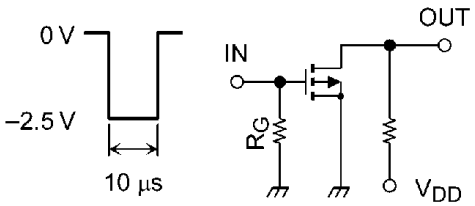


Fig. 6.3.1 Test Circuit of Switching Time

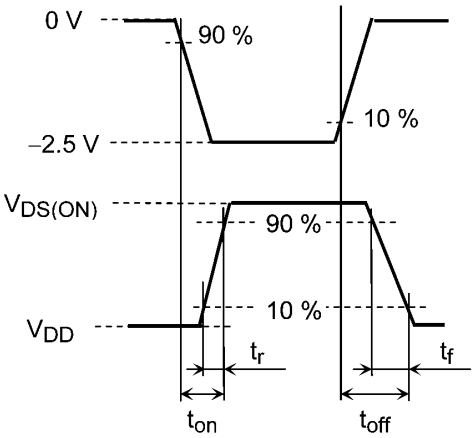


Fig. 6.3.2 Input Waveform/Output Waveform

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6.4. Gate Charge Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} = -10 V, V_{GS} = -4.5 V, I_D = -4.0 A	—	12.8	—	nC
Gate-source charge 1	Q_{gs1}		—	1.4	—	
Gate-drain charge	Q_{gd}		—	3.0	—	

6.5. Source-Drain Characteristics (T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	(Note 1)	V_{DSF}	I_D = 4.0 A, V_{GS} = 0 V	—	0.88	1.2	V

Note 1: Pulse measurement.

7. Marking

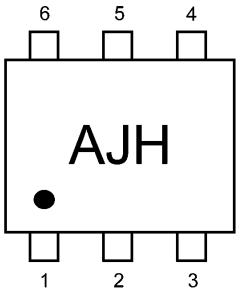


Fig. 7.1 Marking

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8. Characteristics Curves (Note)

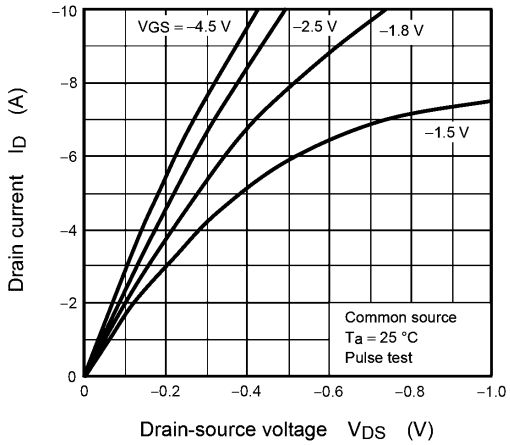


Fig. 8.1 I_D - V_{DS}

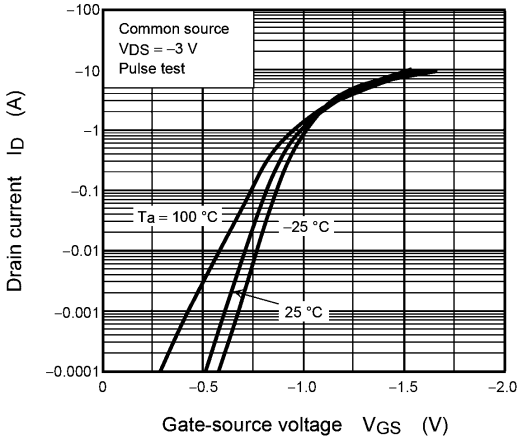


Fig. 8.2 I_D - V_{GS}

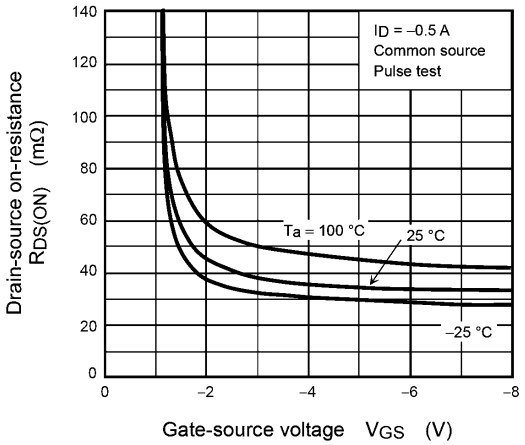


Fig. 8.3 $R_{DS(ON)}$ - V_{GS}

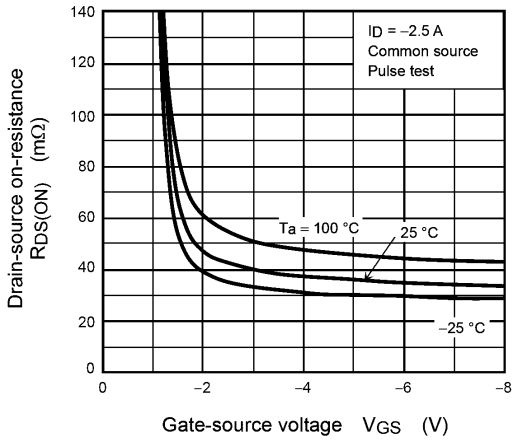


Fig. 8.4 $R_{DS(ON)}$ - V_{GS}

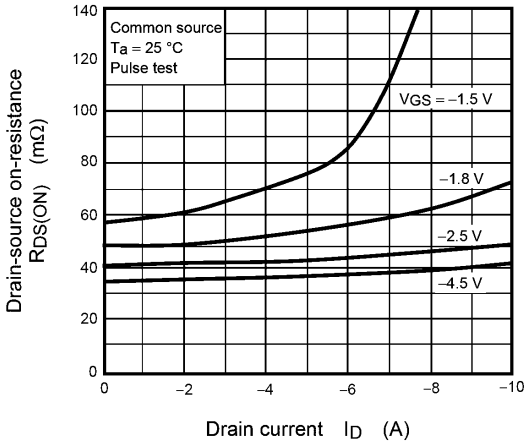


Fig. 8.5 $R_{DS(ON)}$ - I_D

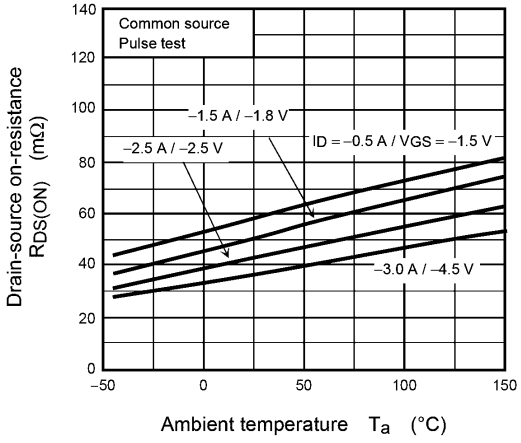


Fig. 8.6 $R_{DS(ON)}$ - T_a

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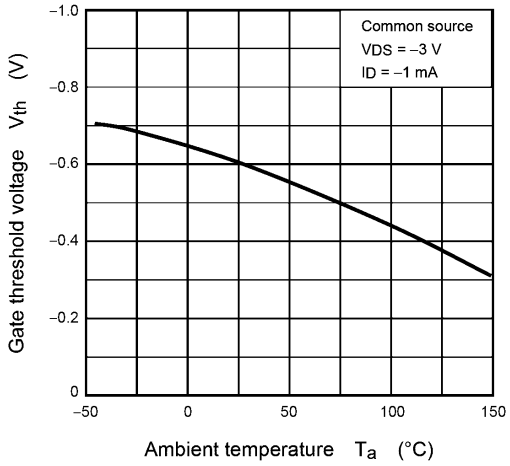


Fig. 8.7 V_{th} - T_a

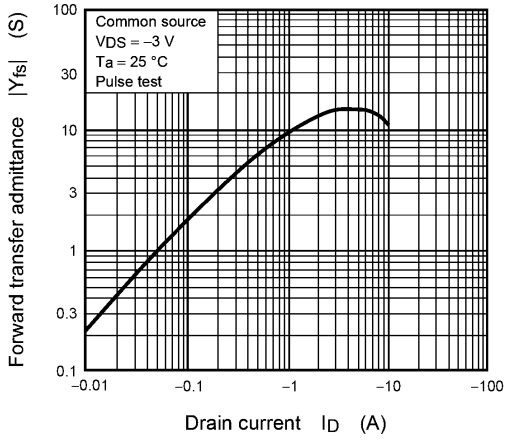


Fig. 8.8 $|Y_{fs}|$ - I_D

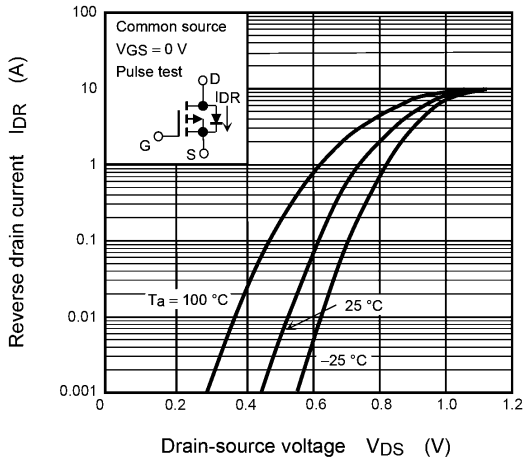


Fig. 8.9 I_{DR} - V_{DS}

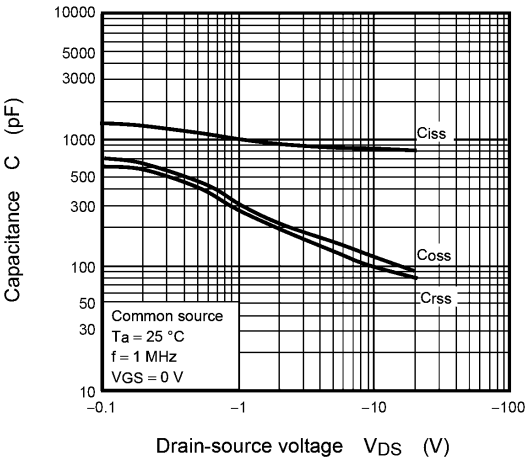


Fig. 8.10 C - V_{DS}

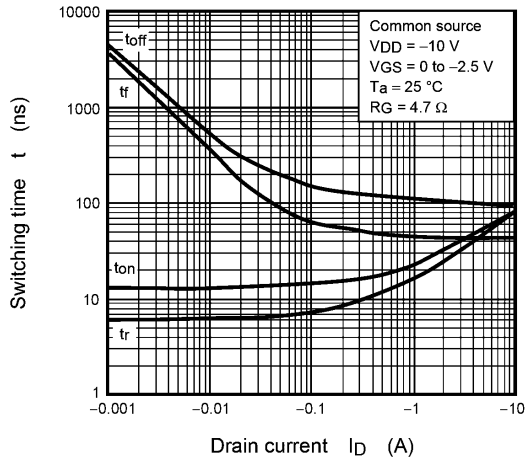


Fig. 8.11 t - I_D

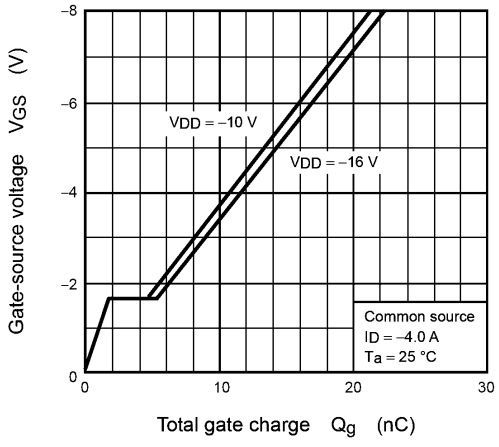


Fig. 8.12 Dynamic Input Characteristics

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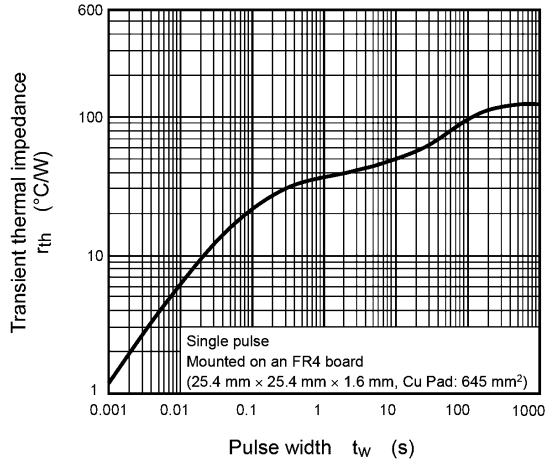


Fig. 8.13 r_{th} - t_w

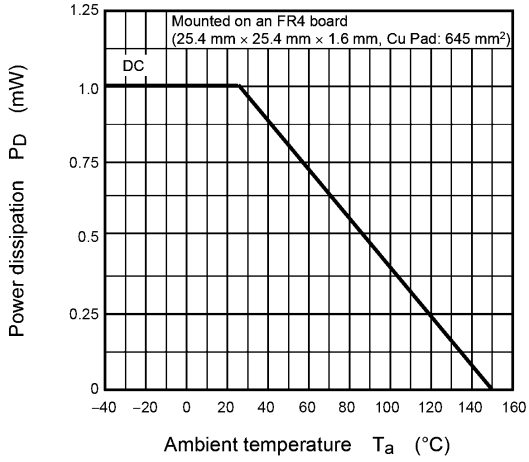


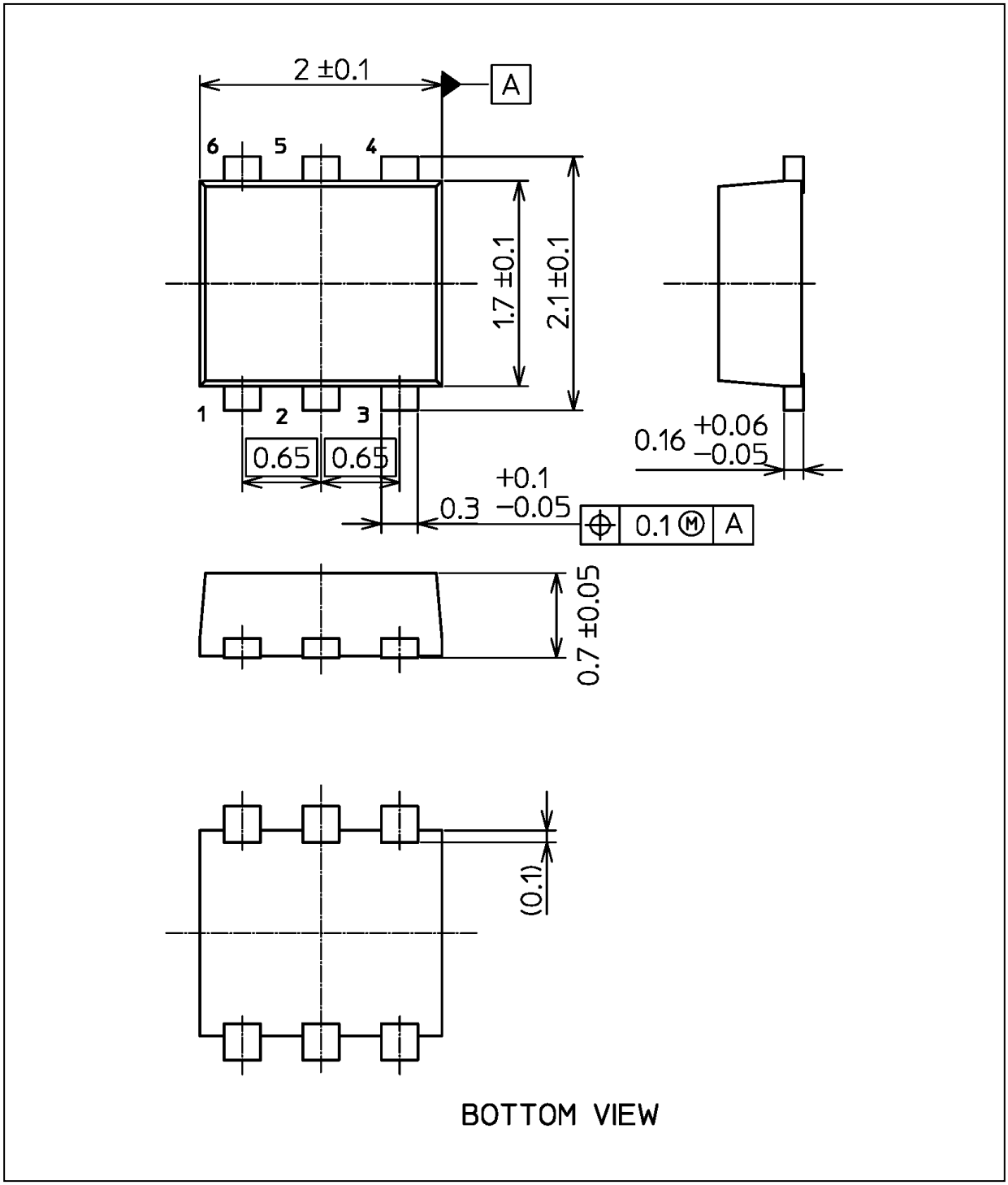
Fig. 8.14 P_D - T_a

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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Package Dimensions

Unit: mm



Weight: 7.0 mg (typ.)

Package Name(s)
TOSHIBA: 2-2T1S
Nickname: UF6

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