

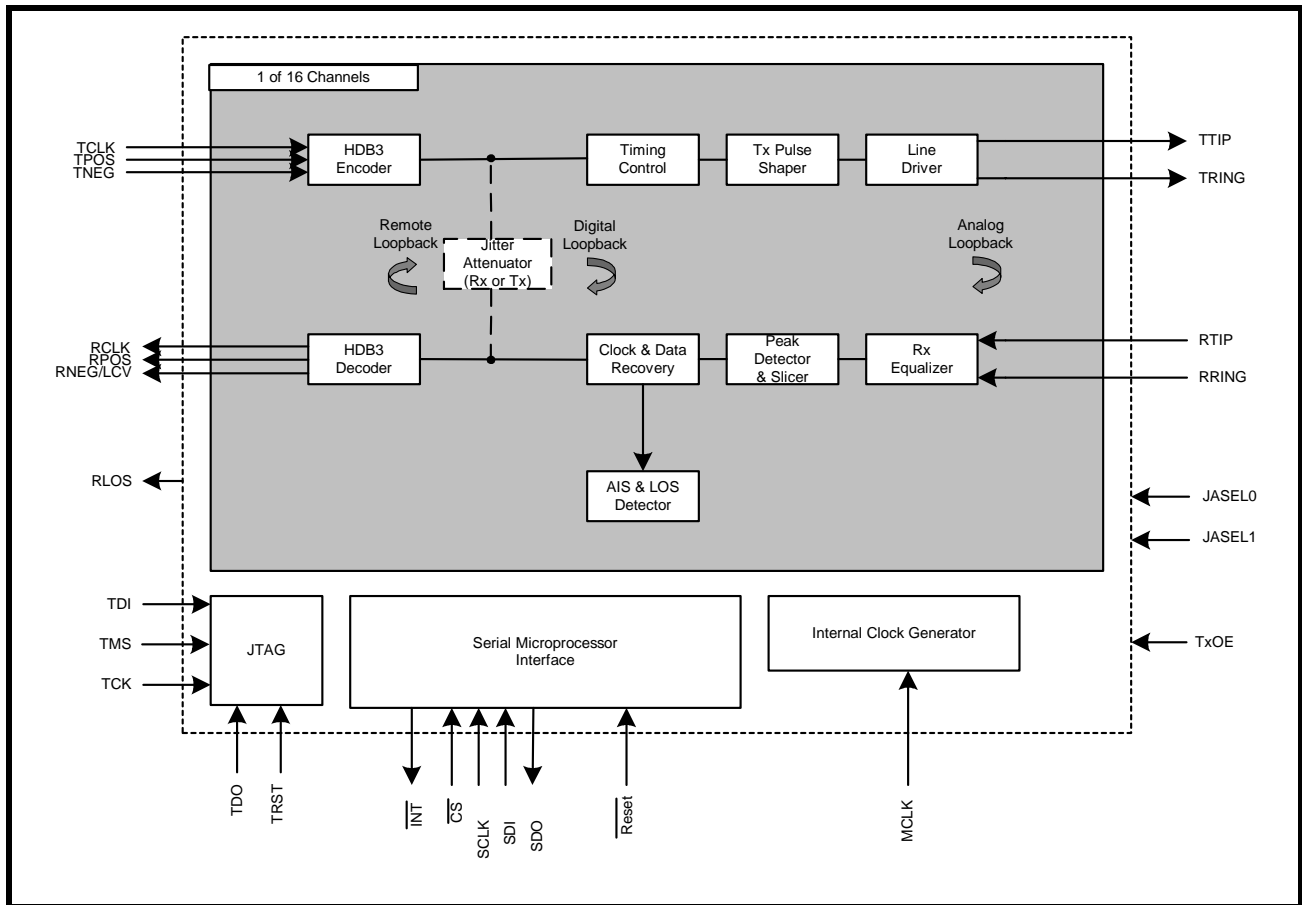
GENERAL DESCRIPTION

The XRT83SL216 is a fully integrated 16-channel E1 short-haul LIU which optimizes system cost and performance by offering key design features. The XRT83SL216 operates from a single 3.3V power supply. The LIU features are programmed through a standard serial microprocessor interface. EXAR's LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be placed in a high impedance mode when experiencing a power failure or when the LIU is powered off. Additional features include TAOS for transmit and receive, RLOS, LCV, on chip Jitter Attenuator, AIS detector, and diagnostic loopback modes.

APPLICATIONS

- ISDN Primary Rate Interface
- CSU/DSU E1 Interface
- E1 LAN/WAN Routers
- Public Switching Systems and PBX Interfaces
- E1 Multiplexer and Channel Banks
- Integrated Multi-Service Access Platforms (IMAPs)
- Integrated Access Devices (IADs)
- Inverse Multiplexing for ATM (IMA) Wireless Base Stations

FIGURE 1. BLOCK DIAGRAM OF THE XRT83SL216



XRT83SL216

16-CHANNEL E1 SHORT-HAUL LINE INTERFACE UNIT

FEATURES

- Fully integrated 16-Channel short haul transceivers for E1 (2.048MHz) applications
- Tri-State on a per channel basis for the transmit selection
- Crystal-Less digital jitter attenuators (JA) with 32-Bit or 64-Bit FIFO for the receive or transmit paths
- Transmit outputs and receive inputs stay in the High Impedance mode upon power failure
- Support for automatic protection switching
- RLOS/AIS according to ITU-T G.775 or ETSI-300-233
- On-Chip HDB3 encoder/decoder for each channel
- On-Chip digital clock recovery circuit for high input jitter tolerance
- On-Chip per channel driver failure monitoring circuit
- On-Chip transmit pulse shaper for CEPT 75Ω and 120Ω line terminations
- High receiver interference immunity
- Transmit return loss meets or exceeds ETS1 300-166
- Meets or exceeds ITU G.703, G,775, G.736 and G.823
- Line code error and bipolar violation detection
- Transmit all ones (TAOS) for the Transmit and Receive Outputs
- Supports local analog, remote, and digital loopback modes
- Supports gapped clocks for mapper/multiplexer applications
- Low Power dissipation
- Single 3.3V supply operation (3V to 5V I/O tolerant)
- 289-Pin STBGA package
- -40°C to +85°C Temperature Range

PRODUCT ORDERING INFORMATION

| PRODUCT NUMBER | PACKAGE TYPE | OPERATING TEMPERATURE RANGE |
|----------------|----------------|-----------------------------|
| XRT83SL216IB | 289 Ball STBGA | -40°C to +85°C |

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PIN DESCRIPTIONS

HOST MODE INTERFACE

SERIAL MICROPROCESSOR INTERFACE

| NAME | PIN | TYPE | DESCRIPTION |
|---------------------------|-----|------|---|
| $\overline{\text{CS}}$ | J4 | I | Chip Select Input Active low signal. This signal enables the serial microprocessor interface by pulling chip select "Low". The serial interface is disabled when the chip select signal returns "High". |
| SCLK | J5 | I | Serial Clock Input The serial clock input samples SDI on the rising edge and updates SDO on the falling edge. See the Serial Microprocessor section of this datasheet for more details. |
| SDI | K5 | I | Serial Data Input The serial data input pin is used to supply an address and data string to program the internal registers within the device. See the Serial Microprocessor section of this datasheet for more details. |
| SDO | L5 | O | Serial Data Output The serial data output pin is used to retrieve the internal contents of a selected register in readback mode. See the Microprocessor section of this datasheet for more details. |
| $\overline{\text{Reset}}$ | J6 | I | Hardware Reset Input Active low signal. When this pin is pulled "Low" for more than 10 μ S, all internal registers and state machines are set to their default state. NOTE: Internally pulled "High" with 50k Ω . |
| $\overline{\text{INT}}$ | K4 | O | Interrupt Output Active low signal. This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". GIE (Global Interrupt Enable) must be set "High" in the appropriate global register to enable interrupt generation. NOTE: This pin is an open-drain output that requires an external 10K Ω pull-up resistor. |

RECEIVER SECTION

| NAME | PIN | TYPE | DESCRIPTION |
|--------|-----|------|---|
| RLOS15 | B10 | O | Receive Loss of Signal When a receive loss of signal occurs, the RLOS pin will go "High" for a minimum of one RCLK cycle. RLOS will remain "High" until the loss of signal condition clears. See the Receive Loss of Signal section of this datasheet for more details. |
| RLOS14 | D11 | | |
| RLOS13 | F10 | | |
| RLOS12 | B12 | | |
| RLOS11 | T12 | | |
| RLOS10 | T11 | | |
| RLOS9 | M10 | | |
| RLOS8 | R10 | | |
| RLOS7 | U8 | | |
| RLOS6 | R7 | | |
| RLOS5 | M8 | | |
| RLOS4 | T6 | | |
| RLOS3 | B6 | | |
| RLOS2 | B7 | | |
| RLOS1 | F8 | | |
| RLOS0 | C8 | | |
| RCLK15 | A10 | O | Receive Clock Output RCLK is the recovered clock from the incoming data stream. If the incoming signal is absent, RCLK maintains its timing by using an internal master clock as its reference. RPOS/RNEG data can be updated on either edge of RCLK selected by RCLKinv in the appropriate channel register. |
| RCLK14 | A11 | | |
| RCLK13 | E10 | | |
| RCLK12 | A12 | | |
| RCLK11 | U12 | | |
| RCLK10 | U11 | | |
| RCLK9 | N10 | | |
| RCLK8 | P10 | | |
| RCLK7 | T8 | | |
| RCLK6 | P7 | | |
| RCLK5 | N8 | | |
| RCLK4 | U6 | | |
| RCLK3 | A6 | | |
| RCLK2 | A7 | | |
| RCLK1 | E8 | | |
| RCLK0 | D8 | | |

RECEIVER SECTION

| NAME | PIN | TYPE | DESCRIPTION |
|------------|-----|------|--|
| RPOS15 | C10 | O | RPOS/RDATA Output Receive digital output pin. In dual rail mode, this pin is the receive positive data output. In single rail mode, this pin is the receive non-return to zero (NRZ) data output. |
| RPOS14 | C11 | | |
| RPOS13 | E11 | | |
| RPOS12 | C12 | | |
| RPOS11 | R12 | | |
| RPOS10 | R11 | | |
| RPOS9 | M11 | | |
| RPOS8 | T10 | | |
| RPOS7 | R8 | | |
| RPOS6 | T7 | | |
| RPOS5 | N7 | | |
| RPOS4 | R6 | | |
| RPOS3 | C6 | | |
| RPOS2 | C7 | | |
| RPOS1 | F7 | | |
| RPOS0 | A8 | | |
| RNEG/LCV15 | D10 | O | RNEG/LCV Output In dual rail mode, this pin is the receive negative data output. In single rail mode, this pin is a Line Code Violation indicator. If a line code violation or a bipolar violation occur, the LCV pin will pull "High" for a minimum of one RCLK cycle. LCV will remain "High" until there are no more violations. If AMI coding is selected, every bipolar violation will cause this pin to go "High". |
| RNEG/LCV14 | B11 | | |
| RNEG/LCV13 | F11 | | |
| RNEG/LCV12 | D12 | | |
| RNEG/LCV11 | P12 | | |
| RNEG/LCV10 | P11 | | |
| RNEG/LCV9 | N11 | | |
| RNEG/LCV8 | U10 | | |
| RNEG/LCV7 | P8 | | |
| RNEG/LCV6 | U7 | | |
| RNEG/LCV5 | M7 | | |
| RNEG/LCV4 | P6 | | |
| RNEG/LCV3 | D6 | | |
| RNEG/LCV2 | D7 | | |
| RNEG/LCV1 | E7 | | |
| RNEG/LCV0 | B8 | | |

RECEIVER SECTION

| NAME | PIN | TYPE | DESCRIPTION |
|---------|-----|------|---|
| RTIP15 | B17 | I | Receive Differential Tip Input RTIP is the positive differential input from the line interface. Along with the RRING signal, these pins should be coupled to a 2:1 transformer for proper operation. |
| RTIP14 | D17 | | |
| RTIP13 | F17 | | |
| RTIP12 | H17 | | |
| RTIP11 | K17 | | |
| RTIP10 | M17 | | |
| RTIP9 | P17 | | |
| RTIP8 | T17 | | |
| RTIP7 | T1 | | |
| RTIP6 | P1 | | |
| RTIP5 | M1 | | |
| RTIP4 | K1 | | |
| RTIP3 | H1 | | |
| RTIP2 | F1 | | |
| RTIP1 | D1 | | |
| RTIP0 | B1 | | |
| RRING15 | C17 | I | Receive Differential Ring Input RRING is the negative differential input from the line interface. Along with the RTIP signal, these pins should be coupled to a 2:1 transformer for proper operation. |
| RRING14 | E17 | | |
| RRING13 | G17 | | |
| RRING12 | J17 | | |
| RRING11 | L17 | | |
| RRING10 | N17 | | |
| RRING9 | R17 | | |
| RRING8 | T16 | | |
| RRING7 | T2 | | |
| RRING6 | R1 | | |
| RRING5 | N1 | | |
| RRING4 | L1 | | |
| RRING3 | J1 | | |
| RRING2 | G1 | | |
| RRING1 | E1 | | |
| RRING0 | C1 | | |

TRANSMITTER SECTION

| NAME | PIN | TYPE | DESCRIPTION |
|--|--|------|---|
| TxOE | K14 | I | <p>Transmit Output Enable</p> <p>Upon power up, the transmitters are tri-stated. Enabling the transmitters is selected through the serial microprocessor interface by programming the appropriate channel register if this pin is pulled "High". If the TxOE pin is pulled "Low", all 16 transmitters are tri-stated.</p> <p><i>NOTE: TxOE is ideal for redundancy applications. See the Redundancy Applications Section of this datasheet for more details. Internally pulled "Low" with a 50kΩ resistor.</i></p> |
| TCLK15 TCLK14 TCLK13 TCLK12 TCLK11 TCLK10 TCLK9 TCLK8 TCLK7 TCLK6 TCLK5 TCLK4 TCLK3 TCLK2 TCLK1 TCLK0 | A14 D13 C14 E14 N14 P13 U16 R13 R5 U2 P5 N4 E4 A3 F5 C5 | I | <p>Transmit Clock Input</p> <p>TCLK is the input facility clock used to sample the incoming TPOS/TNEG data. TPOS/TNEG data can be sampled on either edge of TCLK selected by TCLK-inv in the appropriate channel register.</p> |
| TPOS15 TPOS14 TPOS13 TPOS12 TPOS11 TPOS10 TPOS9 TPOS8 TPOS7 TPOS6 TPOS5 TPOS4 TPOS3 TPOS2 TPOS1 TPOS0 | B13 E13 A15 F13 M14 N13 U15 T13 T5 U3 N5 M4 D4 B4 D5 B5 | I | <p>TPOS/TDATA Input</p> <p>Transmit digital input pin. In dual rail mode, this pin is the transmit positive data input. In single rail mode, this pin is the transmit non-return to zero (NRZ) data input.</p> |

TRANSMITTER SECTION

| NAME | PIN | TYPE | DESCRIPTION |
|--------|-----|------|--|
| TNEG15 | A13 | I | Transmit Negative Data Input In dual rail mode, this pin is the transmit negative data input. In single rail mode, this pin can be tied to ground. |
| TNEG14 | C13 | | |
| TNEG13 | B14 | | |
| TNEG12 | D14 | | |
| TNEG11 | L14 | | |
| TNEG10 | M13 | | |
| TNEG9 | U14 | | |
| TNEG8 | U13 | | |
| TNEG7 | U5 | | |
| TNEG6 | U4 | | |
| TNEG5 | M5 | | |
| TNEG4 | L4 | | |
| TNEG3 | C4 | | |
| TNEG2 | A4 | | |
| TNEG1 | E5 | | |
| TNEG0 | A5 | | |

TRANSMITTER SECTION

| NAME | PIN | TYPE | DESCRIPTION |
|---------|-----|------|--|
| TTIP15 | B15 | ○ | Transmit Differential Tip Output TTIP is the positive differential output to the line interface. Along with the TRING signal, these pins should be coupled to a 1:2 step up transformer for proper operation. |
| TTIP14 | D15 | | |
| TTIP13 | F15 | | |
| TTIP12 | H15 | | |
| TTIP11 | K15 | | |
| TTIP10 | M15 | | |
| TTIP9 | P15 | | |
| TTIP8 | T14 | | |
| TTIP7 | T4 | | |
| TTIP6 | P3 | | |
| TTIP5 | M3 | | |
| TTIP4 | K3 | | |
| TTIP3 | H3 | | |
| TTIP2 | F3 | | |
| TTIP1 | D3 | | |
| TTIP0 | B3 | | |
| TRING15 | C15 | ○ | Transmit Differential Ring Output TRING is the negative differential output to the line interface. Along with the TTIP signal, these pins should be coupled to a 1:2 step up transformer for proper operation. |
| TRING14 | E15 | | |
| TRING13 | G15 | | |
| TRING12 | J15 | | |
| TRING11 | L15 | | |
| TRING10 | N15 | | |
| TRING9 | R15 | | |
| TRING8 | R14 | | |
| TRING7 | R4 | | |
| TRING6 | R3 | | |
| TRING5 | N3 | | |
| TRING4 | L3 | | |
| TRING3 | J3 | | |
| TRING2 | G3 | | |
| TRING1 | E3 | | |
| TRING0 | C3 | | |

CONTROL FUNCTION

| NAME | PIN | TYPE | DESCRIPTION | | | | | | | | | | | | | | | |
|------------------|------------|--|--|--------|--------|-------------------------|---|---|-------------|---|---|---------------|---|---|---------------|---|---|--|
| JASEL0 JASEL1 | G13 H13 | I | <p>Jitter Attenuator Select: The Jitter Attenuator can be selected to be in the Transmit or Receive path.</p> <table border="1"> <thead> <tr> <th>JASEL1</th> <th>JASEL0</th> <th>Jitter Attenuator State</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>JA Disabled</td> </tr> <tr> <td>0</td> <td>1</td> <td>JA in Tx Path</td> </tr> <tr> <td>1</td> <td>0</td> <td>JA in Rx Path</td> </tr> <tr> <td>1</td> <td>1</td> <td>JA Select is enabled through μP Control</td> </tr> </tbody> </table> <p><i>NOTE: Internally pulled "High" with a 50kΩ resistor.</i></p> | JASEL1 | JASEL0 | Jitter Attenuator State | 0 | 0 | JA Disabled | 0 | 1 | JA in Tx Path | 1 | 0 | JA in Rx Path | 1 | 1 | JA Select is enabled through μ P Control |
| JASEL1 | JASEL0 | Jitter Attenuator State | | | | | | | | | | | | | | | | |
| 0 | 0 | JA Disabled | | | | | | | | | | | | | | | | |
| 0 | 1 | JA in Tx Path | | | | | | | | | | | | | | | | |
| 1 | 0 | JA in Rx Path | | | | | | | | | | | | | | | | |
| 1 | 1 | JA Select is enabled through μ P Control | | | | | | | | | | | | | | | | |
| MCLK | L6 | I | <p>Master Clock Input This pin is used as the internal reference to the LIU. This clock must be 2.048MHz +/-50ppm.</p> | | | | | | | | | | | | | | | |

JTAG SECTION

| NAME | PIN | TYPE | DESCRIPTION |
|------|-----|------|---|
| TCK | G5 | I | JTAG Test Clock input, Boundary Scan Clock input: |
| TDI | G4 | I | <p>JTAG Test Data input, Boundary Scan Test Data Input: <i>NOTE: Internally pulled "High" with a 50kΩ resistor.</i></p> |
| TDO | H5 | O | <p>JTAG Test Data output: Boundary Scan Test Data Output:</p> |
| TMS | G6 | I | <p>JTAG Test Mode Select, Boundary Scan Test Mode Select input pin: <i>NOTE: Internally pulled "High" with a 50kΩ resistor.</i></p> |
| TRST | H4 | I | <p>JTAG Test Mode Reset, Boundary Scan Mode Reset Input pin: <i>NOTE: This input pin should be pulled "Low" for normal operation. Internally pulled "High" with a 50kΩ resistor.</i></p> |

POWER AND GROUND

| NAME | PIN | TYPE | DESCRIPTION |
|--|--|------|--|
| TVDD15 TVDD14 TVDD13 TVDD12 TVDD11 TVDD10 TVDD9 TVDD8 TVDD7 TVDD6 TVDD5 TVDD4 TVDD3 TVDD2 TVDD1 TVDD0 | C16 E16 G16 J16 L16 N16 R16 P14 P4 R2 N2 L2 J2 G2 E2 C2 | PWR | Transmit Analog Power Supply (3.3V ±5%) TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1µF capacitor and a 10µF capacitor. |
| RefVDD AVDD_pll | K12 K6 | PWR | Analog Power Supply (3.3V ±5%) These analog supply pins should not be shared with other power supplies. It is recommended that they be isolated from the digital power supply, DVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1µF capacitor. |
| DVDD | A2 A17 C9 D9 H6 H12 P9 R9 | PWR | Digital Power Supply (3.3V ±5%) DVDD should be isolated from the analog power supplies except for TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1µF capacitor. |
| RVDD_1 RVDD_2 | E9 F6 F9 F12 M6 M9 M12 N9 | PWR | Receive Power Supply (3.3V ±5%) RVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1µF capacitor and a 10µF capacitor. |

POWER AND GROUND

| NAME | PIN | TYPE | DESCRIPTION |
|--------|--|------|---|
| TGND15 | B16 | GND | Transmit Analog Ground It's recommended that all ground pins of this device be tied together and to a ground plane. |
| TGND14 | D16 | | |
| TGND13 | F16 | | |
| TGND12 | H16 | | |
| TGND11 | K16 | | |
| TGND10 | M16 | | |
| TGND9 | P16 | | |
| TGND8 | T15 | | |
| TGND7 | T3 | | |
| TGND6 | P2 | | |
| TGND5 | M2 | | |
| TGND4 | K2 | | |
| TGND3 | H2 | | |
| TGND2 | F2 | | |
| TGND1 | D2 | | |
| TGND0 | B2 | | |
| DGND | A1 A9 A16 B9 T9 U1 U9 U17 | GND | Digital Ground It's recommended that all ground pins of this device be tied together and to a ground plane. |

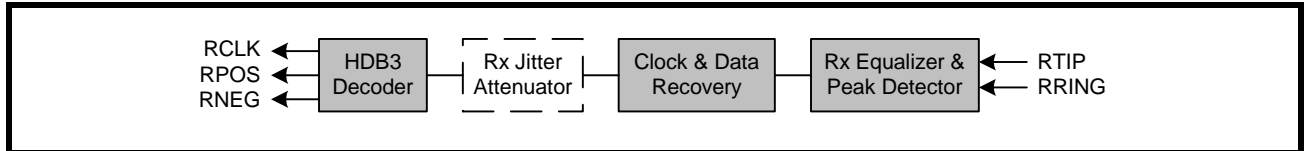
POWER AND GROUND

| NAME | PIN | TYPE | DESCRIPTION |
|------|---|------|--|
| AGND | G7 G8 G9 G10 G11 H7 H8 H9 H10 H11 J7 J8 J9 J10 J11 K7 K8 K9 K10 K11 L7 L8 L9 L10 L11 J14 | GND | <p>Analog Ground</p> <p>It's recommended that all ground pins of this device be tied together and to a ground plane.</p> <p><i>NOTE: J14 is a factory test pin and MUST be grounded for normal operation.</i></p> |
| NC | E6 E12 F4 F14 G12 G14 H14 J12 J13 K13 L12 L13 N6 N12 | NC | <p>No Connects</p> |

1.0 RECEIVE PATH LINE INTERFACE

The receive path consists of 16 independent E1 receivers. The following section describes the complete receive path from RTIP/RRING inputs to RCLK/RPOS/RNEG outputs. A simplified block diagram of the receive path is shown in **Figure 3**.

FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH LINE TERMINATION (RTIP/RRING)



1.1 Peak Detector/Data Slicer

In the receive path, the line signal is coupled into the RTIP and RRING pins via a 2:1 transformer and are converted into digital pulses by an equalizer and an adaptive data slicer. Clock and data signals are recovered from the output of the slicer with the help of a digital PLL that provides excellent jitter accommodation for high input jitter tolerance.

1.2 Clock and Data Recovery

The receive clock (RCLK) is recovered by the clock and data recovery circuitry. An internal PLL locks on the incoming data stream and outputs a clock that's in phase with the incoming signal. In the absence of an incoming signal, RCLK maintains its timing by using MCLK as its reference. The recovered data can be updated on either edge of RCLK. By default, data is updated on the rising edge of RCLK. To update data on the falling edge of RCLK, set RCLKinv to "1" in the appropriate global register. **Figure 4** is a timing diagram of the receive data updated on the rising edge of RCLK. **Figure 5** is a timing diagram of the receive data updated on the falling edge of RCLK. The timing specifications are shown in **Table 1**.

FIGURE 4. RECEIVE DATA UPDATED ON THE RISING EDGE OF RCLK

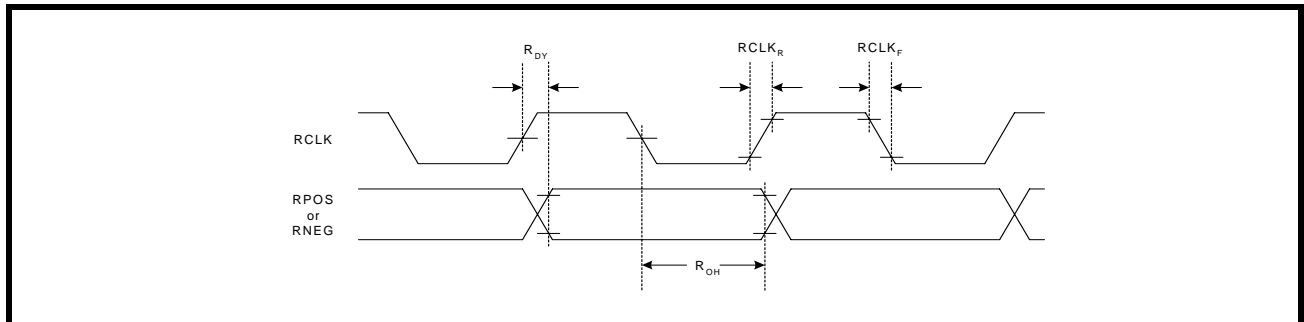


FIGURE 5. RECEIVE DATA UPDATED ON THE FALLING EDGE OF RCLK

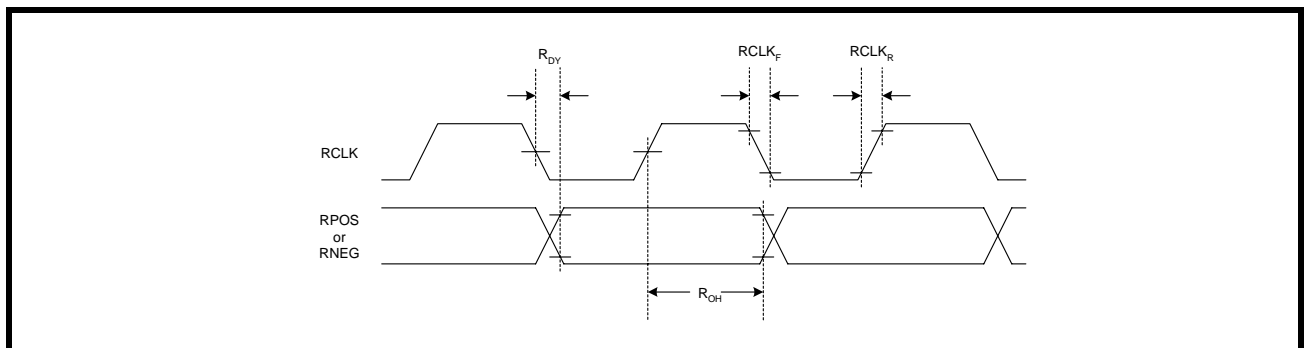


TABLE 1: TIMING SPECIFICATIONS FOR RCLK/RPOS/RNEG

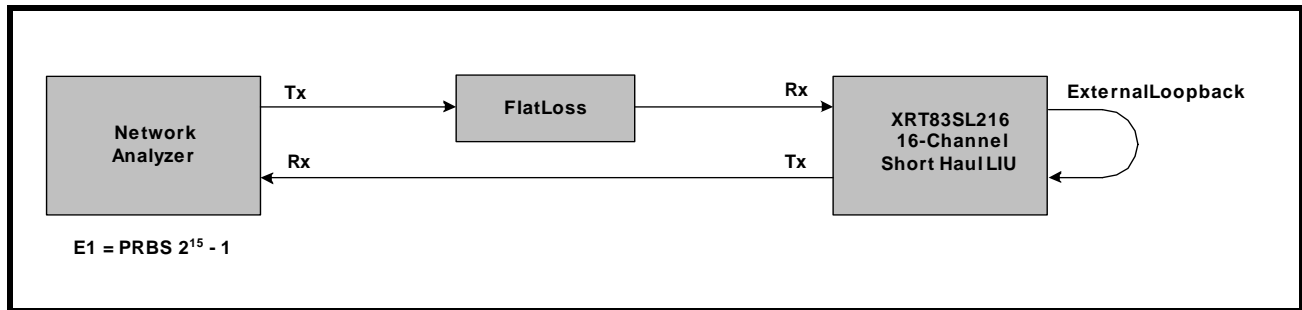
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|-------------------|-----|-----|-----|-------|
| RCLK Duty Cycle | R _{CDU} | 45 | 50 | 55 | % |
| Receive Data Setup Time | R _{SU} | 150 | - | - | ns |
| Receive Data Hold Time | R _{HO} | 150 | - | - | ns |
| RCLK to Data Delay | R _{DY} | - | - | 40 | ns |
| RCLK Rise Time (10% to 90%) with 25pF Loading | RCLK _R | - | - | 40 | ns |
| RCLK Fall Time (90% to 10%) with 25pF Loading | RCLK _F | - | - | 40 | ns |

NOTE: VDD=3.3V ±5%, T_A=25°C, Unless Otherwise Specified

1.3 Receive Sensitivity

To meet short haul requirements, the XRT83SL216 can accept E1 signals that have been attenuated by 11dB of flat loss in E1 mode. The test configuration for measuring the receive sensitivity is shown in Figure 6.

FIGURE 6. TEST CONFIGURATION FOR MEASURING RECEIVE SENSITIVITY



1.4 General Alarm Detection and Interrupt Generation

The receive path detects RLOS and AIS. These alarms can be individually masked to prevent the alarm from triggering an interrupt. To enable interrupt generation, the Global Interrupt Enable (GIE) bit must be set "High" in the appropriate global register. Any time a change in status occurs (if the alarms are enabled), the interrupt pin will pull "Low" to indicate an alarm has occurred. Once the status registers have been read, the INT pin will return "High". The status registers are Reset Upon Read (RUR).

NOTE: The interrupt pin is an Open-Drain output that requires a 10kΩ pull-up resistor.

1.4.1 RLOS (Receiver Loss of Signal)

The XRT83SL216 supports both G.775 or ETSI-300-233 RLOS detection scheme.

In G.775 mode, RLOS is declared when the received signal is less than 320mV for more than 32 consecutive pulse periods (typical). The device clears RLOS when the receive signal achieves 12.5% ones density with no more than 15 consecutive zeros in a 32 bit sliding window and the signal level exceeds 550mV (typical).

In ETSI-300-233 mode the device declares RLOS when the input level drops below 320mV (typical) for more than 2048 pulse periods (1msec). The device clears RLOS when the receive signal achieves 12.5% ones density with no more than 15 consecutive zeros in a 32 bit sliding window and the signal level exceeds 550mV (typical).

1.4.2 AIS (Alarm Indication Signal)

The XRT83SL216 adheres to ITU-T G.775 or ETSI-300-233 specifications for an all ones pattern detection by programming the appropriate channel register. The alarm indication signal is set to "1" if an all ones pattern is detected. In G.775 mode, AIS is defined as 2 or less zeros in 2 consecutive double frame (512-bit window) periods. AIS will clear when the incoming signal has 3 or more zeros in the same time period. In ETSI-300-233 mode, AIS is defined as less than 3 zeros in a 512-bit window.

1.4.3 LCV (Line Code Violation Detection)

In HDB3 mode, the LCV pin will be set to "High" if the receiver detects excessive zero's, bipolar violations or HDB3 code violations. If the device is configured in AMI mode, any bipolar violations will cause the LCV pin to go "High".

1.5 Receive Jitter Attenuator

The jitter attenuator can be configured in the receive path to reduce phase and frequency jitter in the recovered clock. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth of 32-bit or 64-bit. If the LIU is used for line synchronization (loop timing systems), the JA should be enabled. When the Read and Write pointers of the FIFO are within 2-Bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this condition occurs, the jitter attenuator will not attenuate input jitter until the Read/Write pointer's position is outside the 2-Bit window. The JA has a typical clock delay equal to ½ of the FIFO bit depth.

NOTE: *If the LIU is used in a multiplexer/mapper application where stuffing bits are typically removed, the JA can be configured in the transmit path to smooth out the gapped clock. See the Transmit Section of this datasheet.*

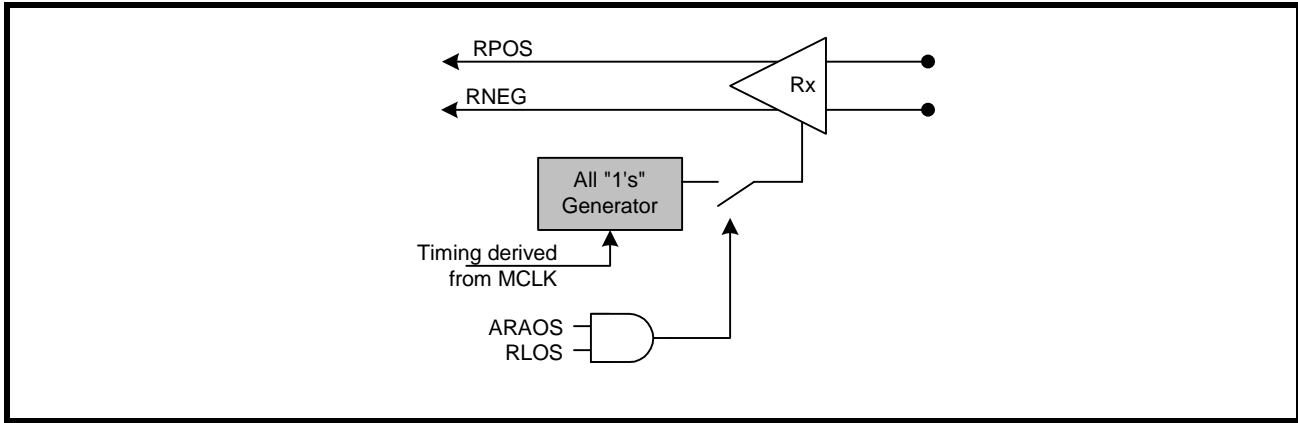
1.6 HDB3 Decoder

In single rail mode, RPOS is the output of decoded AMI or HDB3 signals and RNEG is the LCV output. HDB3 data is defined as any block of 4 successive zeros replaced with OOOV or BOOV, so that two successive V pulses are of opposite polarity to achieve zero DC offset. If the HDB3 decoder is selected, the receive path removes the V and B pulses so that the original data is output to RPOS.

1.7 ARAOS (Automatic Receive All Ones)

If ARAOS is enabled in the appropriate channel register and an RLOS condition occurs, the Receiver outputs will generate an All Ones pattern using MCLK as reference. When RLOS clears, the All Ones pattern ends and the Receive path returns to normal operation.

FIGURE 7. SIMPLIFIED BLOCK DIAGRAM OF THE ARAOS FUNCTION



1.8 RPOS/RNEG/RCLK

The digital output data can be programmed to either single rail or dual rail formats. **Figure 8** is a timing diagram of a repeating "0011" pattern in single-rail mode. **Figure 9** is a timing diagram of the same fixed pattern in dual rail mode.

FIGURE 8. SINGLE RAIL MODE WITH A FIXED REPEATING "0011" PATTERN

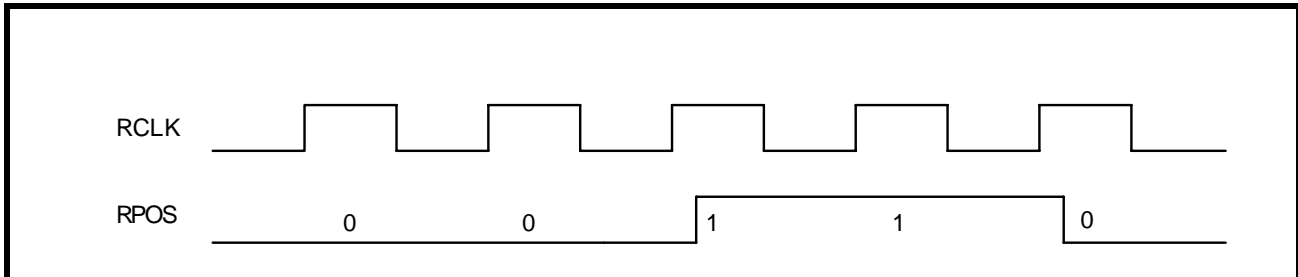
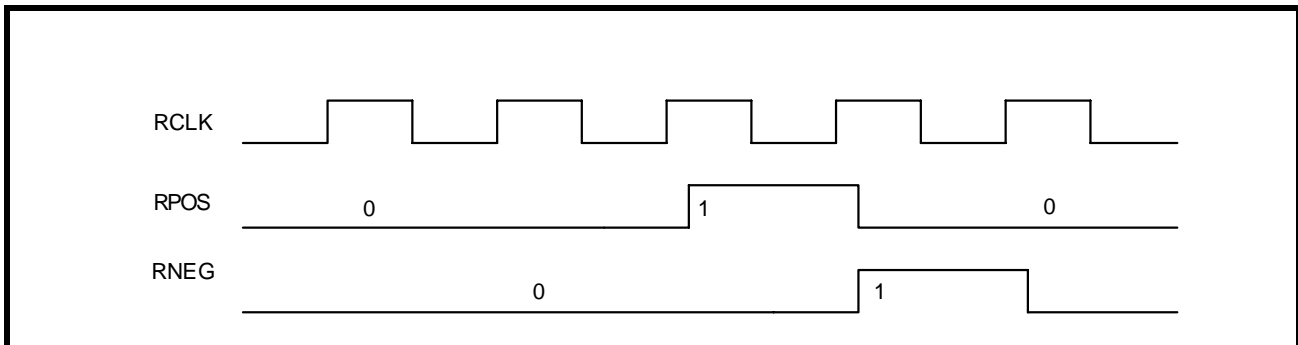


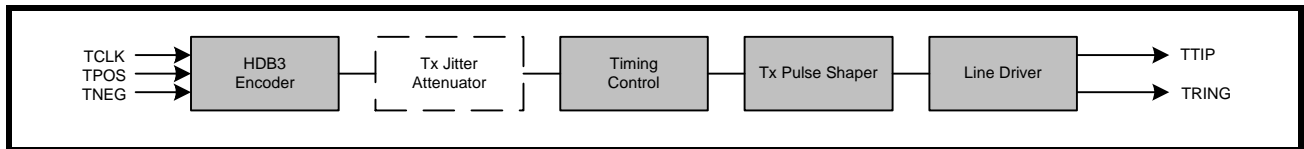
FIGURE 9. DUAL RAIL MODE WITH A FIXED REPEATING "0011" PATTERN



2.0 TRANSMIT PATH LINE INTERFACE

The transmit path consists of 16 independent E1 transmitters. The following section describes the complete transmit path from TCLK/TPOS/TNEG inputs to TTIP/TRING outputs. A simplified block diagram of the transmit path is shown in **Figure 10**.

FIGURE 10. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT PATH



2.1 TCLK/TPOS/TNEG Digital Inputs

In dual rail mode, TPOS and TNEG are the digital inputs for the transmit path. In single rail mode, TNEG can be tied to ground. The XRT83SL216 can be programmed to sample the inputs on either edge of TCLK. By default, data is sampled on the falling edge of TCLK. To sample data on the rising edge of TCLK, set TCLKinv to "1" in the appropriate global register. **Figure 11** is a timing diagram of the transmit input data sampled on the falling edge of TCLK. **Figure 12** is a timing diagram of the transmit input data sampled on the rising edge of TCLK. The timing specifications are shown in **Table 2**.

FIGURE 11. TRANSMIT DATA SAMPLED ON FALLING EDGE OF TCLK

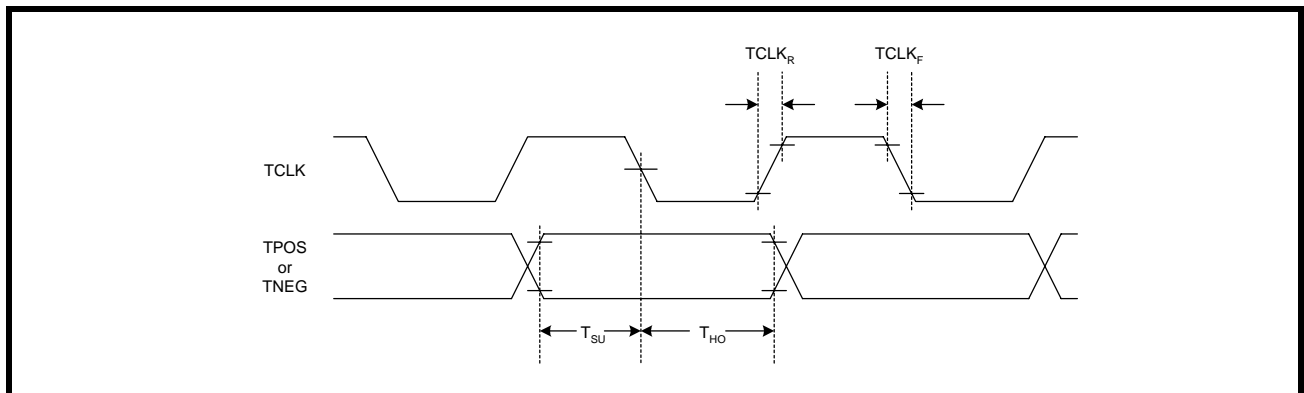


FIGURE 12. TRANSMIT DATA SAMPLED ON RISING EDGE OF TCLK

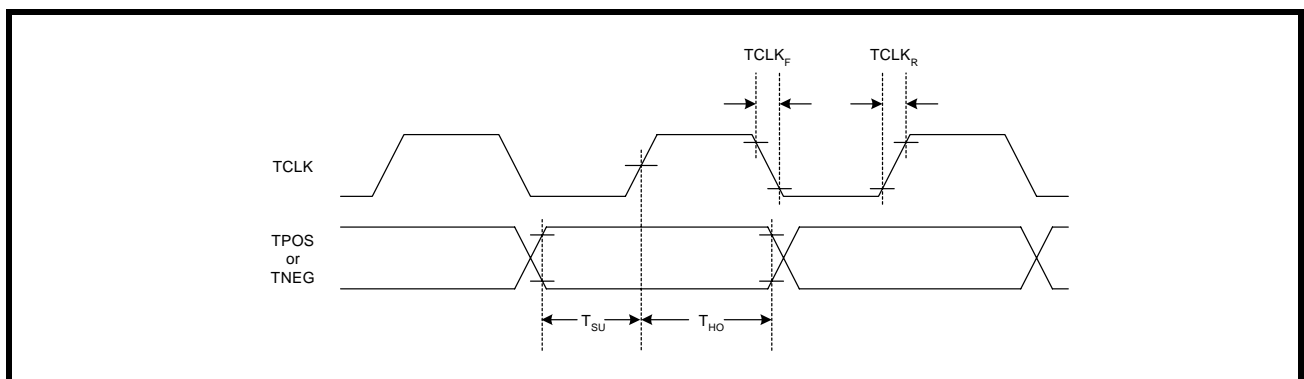


TABLE 2: TIMING SPECIFICATIONS FOR TCLK/TPOS/TNEG

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|-----------------------------|-------------------|-----|-----|-----|-------|
| TCLK Duty Cycle | T _{CDU} | 30 | 50 | 70 | % |
| Transmit Data Setup Time | T _{SU} | 50 | - | - | ns |
| Transmit Data Hold Time | T _{HO} | 30 | - | - | ns |
| TCLK Rise Time (10% to 90%) | TCLK _R | - | - | 40 | ns |
| TCLK Fall Time (90% to 10%) | TCLK _F | - | - | 40 | ns |

NOTE: VDD=3.3V ±5%, T_A=25°C, Unless Otherwise Specified

2.2 HDB3 Encoder

In single rail mode, the LIU can encode the TPOS input signal to AMI or HDB3 data. If HDB3 encoding is selected, any sequence with four or more consecutive zeros in the input will be replaced with 000V or B00V, where "B" indicates a pulse conforming to the bipolar rule and "V" representing a pulse violating the rule. An example of HDB3 encoding is shown in **Table 3**.

TABLE 3: EXAMPLES OF HDB3 ENCODING

| | NUMBER OF PULSES BEFORE NEXT 4 ZEROS | |
|---------------|--------------------------------------|------|
| Input | | 0000 |
| HDB3 (Case 1) | Odd | 000V |
| HDB3 (Case 2) | Even | B00V |

2.3 Transmit Jitter Attenuator

The XRT83SL216 LIU is ideal for multiplexer or mapper applications where the network data crosses multiple timing domains. As the higher data rates are de-multiplexed to E1 data, stuffing bits are typically removed which can leave gaps in the incoming data stream. The JA can be configured in the transmit path with a 32-Bit or 64-Bit FIFO that is used to smooth the gapped clock into a steady E1 output. The maximum gap width the JA in the Transmit path can tolerate is shown in **Table 4**.

TABLE 4: MAXIMUM GAP WIDTH FOR MULTIPLEXER/MAPPER APPLICATIONS

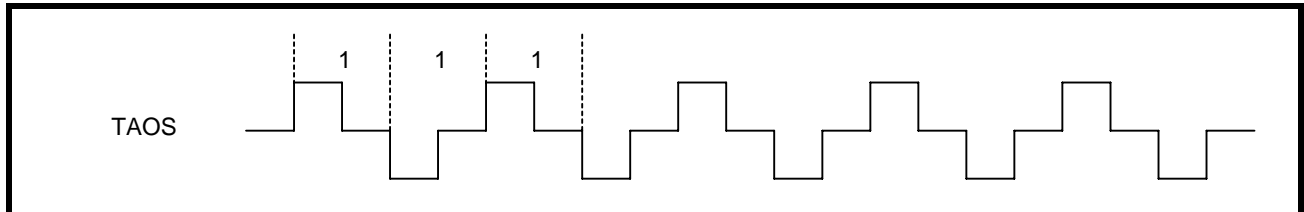
| FIFO DEPTH | MAXIMUM GAP WIDTH |
|------------|-------------------|
| 32-Bit | 20 UI |
| 64-Bit | 50 UI |

NOTE: If the LIU is used in a loop timing system, the JA should be configured in the receive path. See the Receive Section of this datasheet.

2.4 TAOS (Transmit All Ones)

The XRT83SL216 has the ability to transmit all ones on a per channel basis by programming the appropriate channel register. If TAOS is enabled, the Transmitter outputs will generate an All Ones pattern regardless of the Transmit Input data. The Remote Loop Back mode has priority over TAOS. **Figure 13** is a diagram showing the all ones signal at TTIP and TRING.

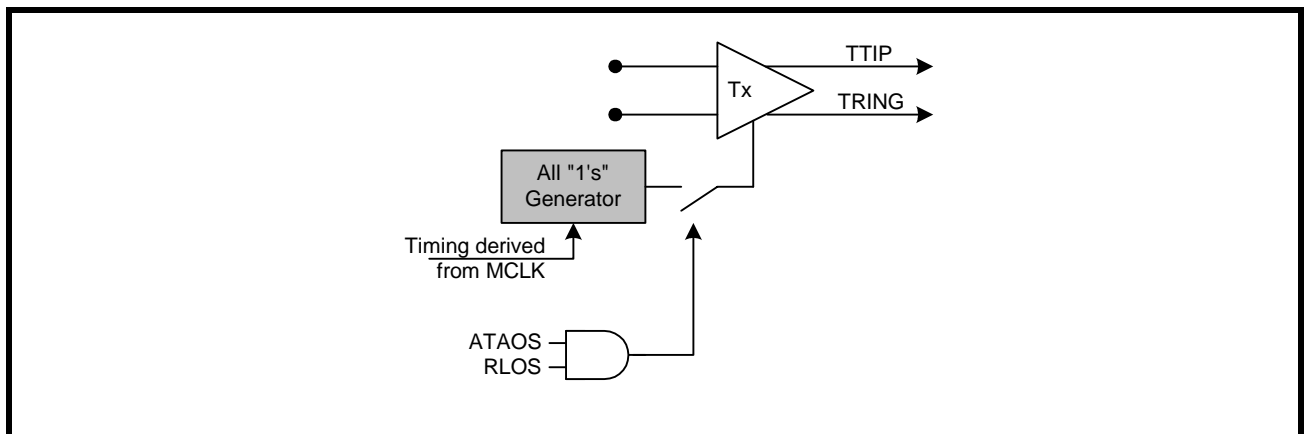
FIGURE 13. TAOS (TRANSMIT ALL ONES)



2.5 ATAOS (Automatic Transmit All Ones)

ATAOS is used to generate an All Ones signal only when an RLOS condition occurs. If ATAOS is enabled, any channel that experiences an RLOS condition will automatically cause the transmitter on that channel to send an All Ones Pattern to the line using MCLK as reference. When RLOS clears, the All Ones pattern ends and the Transmit path returns to normal operation.

FIGURE 14. SIMPLIFIED BLOCK DIAGRAM OF THE ATAOS FUNCTION



3.0 APPLICATIONS

This applications section describes system considerations along with references to application notes available for reference where applicable.

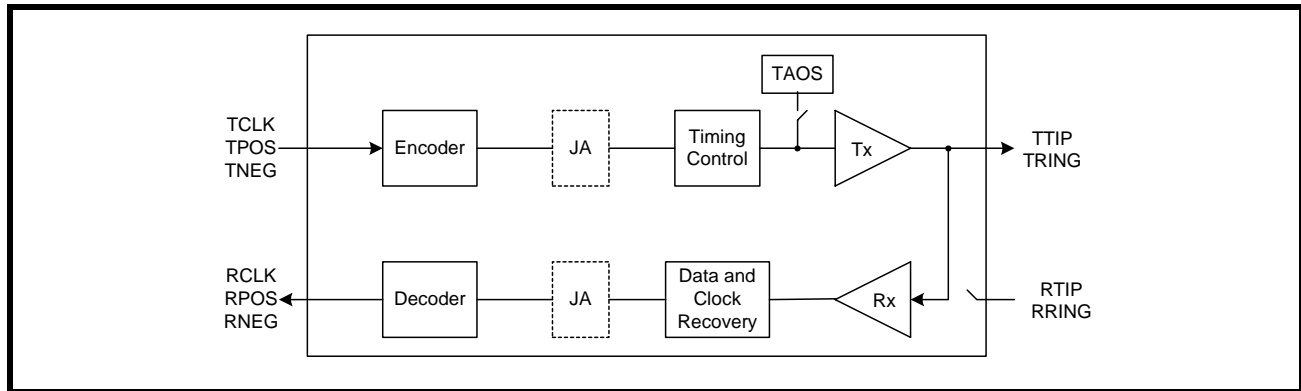
3.1 Loopback Diagnostics

The XRT83SL216 supports several loopback modes for diagnostic testing. The following section describes the local analog loopback, remote loopback, and digital loopback.

3.1.1 Local Analog Loopback

With local analog loopback activated, the transmit output data at TTIP/TRING is internally looped back to the analog inputs at RTIP/RRING. External inputs at RTIP/RRING are ignored while valid transmit output data continues to be sent to the line. A simplified block diagram of local analog loopback is shown in **Figure 15**.

FIGURE 15. SIMPLIFIED BLOCK DIAGRAM OF LOCAL ANALOG LOOPBACK

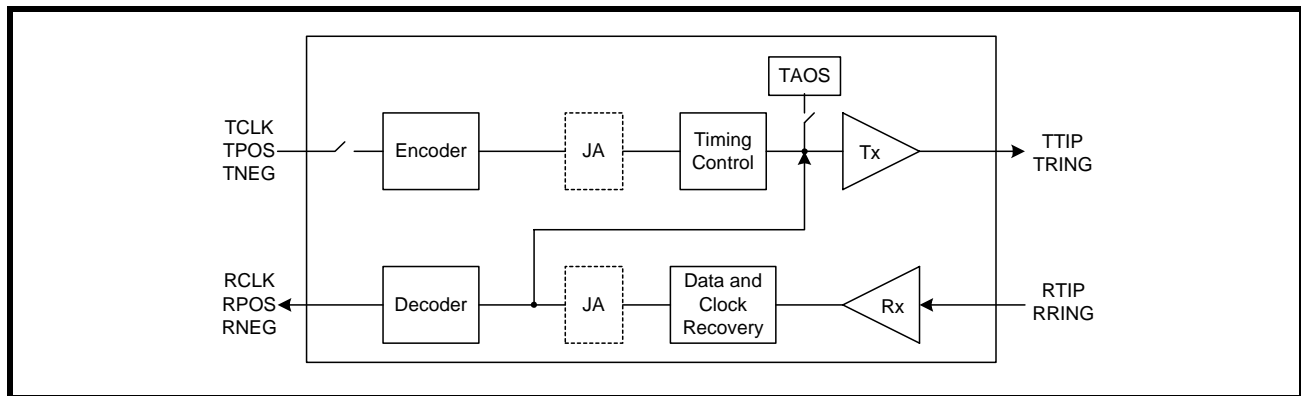


NOTE: TAOS takes priority over the transmit input data at TPOS/TNEG.

3.1.2 Remote Loopback

With remote loopback activated, the receive input data at RTIP/RRING is internally looped back to the transmit output data at TTIP/TRING. The transmit input data at TCLK/TPOS/TNEG are ignored while valid receive output data continues to be sent to the system. A simplified block diagram of remote loopback is shown in **Figure 16**.

FIGURE 16. SIMPLIFIED BLOCK DIAGRAM OF REMOTE LOOPBACK

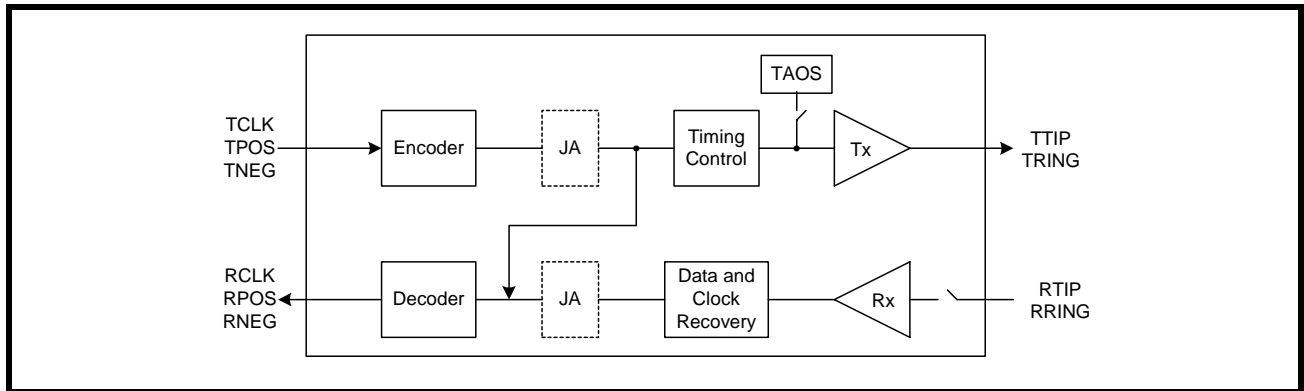


NOTE: Remote Loop Back takes priority over TAOS.

3.1.3 Digital Loopback

With digital loopback activated, the transmit input data at TCLK/TPOS/TNEG is looped back to the receive output data at RCLK/RPOS/RNEG. The receive input data at RTIP/RRING is ignored while valid transmit output data continues to be sent to the line. A simplified block diagram of digital loopback is shown in **Figure 17**.

FIGURE 17. SIMPLIFIED BLOCK DIAGRAM OF DIGITAL LOOPBACK



3.2 Interfacing the Transmit Section of the XRT83L216 to the Line

ITU-T G.703 specifies that the E1 line signal can be transmitted over coaxial cable and terminated with 75Ω or transmitted over twisted-pair and terminated with 120Ω .

In both applications (e.g., 75Ω or 120Ω), the user is advised to interface the Transmitter to the Line, in the manner as depicted in **Figure 18** and **Figure 19**, respectively.

FIGURE 18. INTERFACING THE XRT83L216 TO THE LINE FOR 75Ω APPLICATIONS (1 CHANNEL SHOWN)

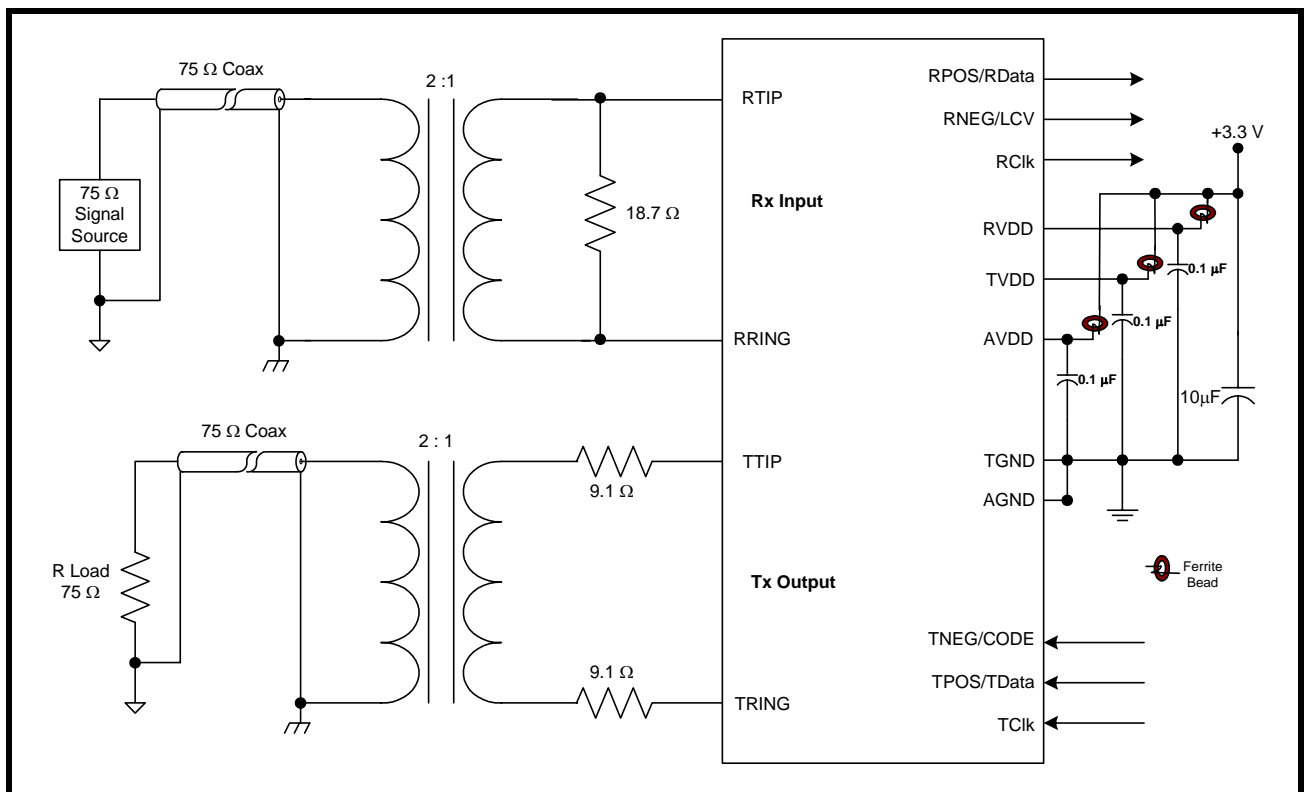
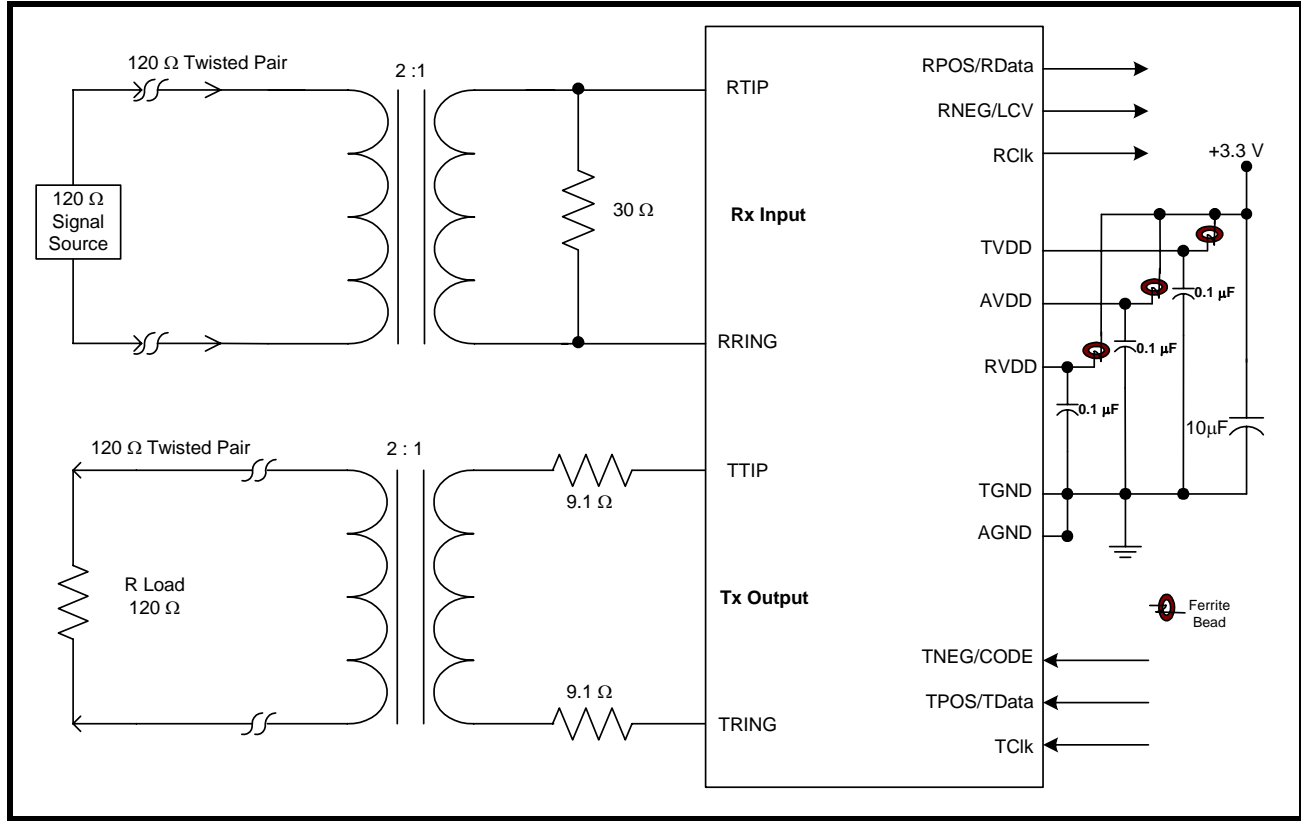


FIGURE 19. INTERFACING THE XRT83L216 TO THE LINE FOR 120 Ω APPLICATIONS (1 CHANNEL SHOWN)



THE FOLLOWING FERRITE BEAD IS RECOMMENDED FOR USE

| PART NUMBER | VENDOR | TYP. IMPEDANCE @ 100MHZ | TYP. IMPEDANCE @ 200MHZ |
|----------------|---------|-------------------------|-------------------------|
| HZ0402A601r-00 | Steward | 600Ω | 925Ω |

Supplier Information

| Steward | | |
|--|---|---|
| Corporate Office | Europe | Asia |
| P.O. Box 510 Chattanooga, TN 37401-510 Phone: +1 (423) 308-1690 Phone: (800) 634-2673 - Toll Free Fax: +1 (423) 308-1622 | Brucefield Industrial Park Livingston EH9 9DR Scotland, UK Phone +44-[0]1-506-414200 Fax: +44-[0]1-506-410694 | 3791 Jalan Bukit Merah #10-14 E-Centre @ Redhill Singapore 159471 Phone: +65-6272-2646 Fax: +65-6272-6165 |

THE FOLLOWING TRANSFORMER IS RECOMMENDED FOR USE

| PART NUMBER | VENDOR | TURNS RATIO | PACKAGE TYPE |
|-------------|--------|-----------------------------|--------------|
| T1113 | Pulse | 1:2 Transmit 2:1 Receive | TOU 2 |

Magnetic Supplier Information

Supplier Information

| PULSE | | |
|--|--|---|
| <i>Corporate Office</i> | <i>Europe</i> | <i>Asia</i> |
| 12220 World Trade Drive San Diego, CA 92128 Tel: (619)-674-8100 FAX: (619)-674-8262 | 1 & 2 Huxley Road The Surrey Research Park Guildford, Surrey GU2 5RE United Kingdom Tel: 44-1483-401700 FAX: 44-1483-401701 | 150 Kampong Ampat #07-01/02 KA Centre Singapore 368324 Tel: 65-287-8998 FAX: 65-280-0080 |

4.0 SERIAL MICROPROCESSOR INTERFACE BLOCK

The serial microprocessor uses a standard 3-pin serial port with \overline{CS} , SCLK, and SDI for programming the LIU. Optional pins such as SDO, \overline{INT} , and \overline{RESET} allow the ability to read back contents of the registers, monitor the LIU via an interrupt pin, and reset the LIU to its default configuration by pulling reset "Low" for more than 10 μ S. A simplified block diagram of the Serial Microprocessor is shown in **Figure 20**.

FIGURE 20. SIMPLIFIED BLOCK DIAGRAM OF THE SERIAL MICROPROCESSOR INTERFACE

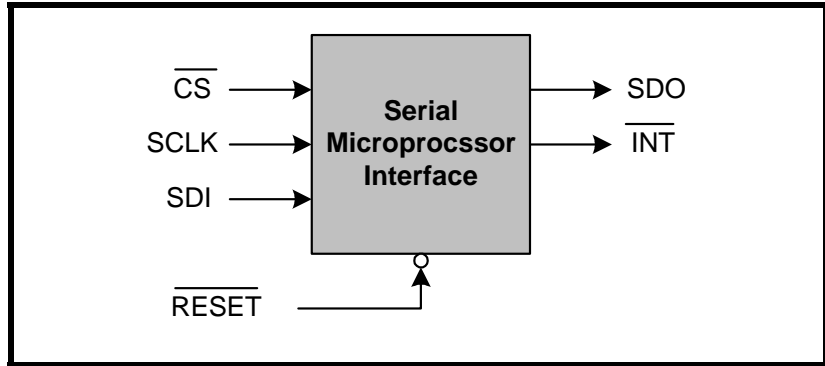
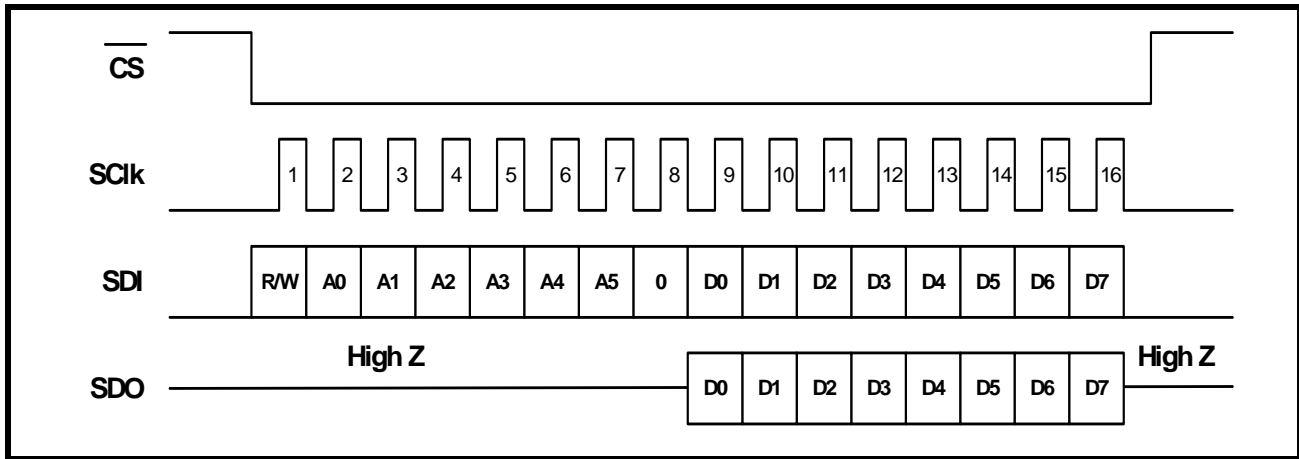


FIGURE 21. MICROPROCESSOR SERIAL INTERFACE STRUCTURE



NOTE: If the R/W bit is set to "1", then this denotes a "READ" operation with the Microprocessor Serial Interface. Conversely, if the R/W bit is set to "0", then this denotes a "WRITE" operation.

FIGURE 22. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

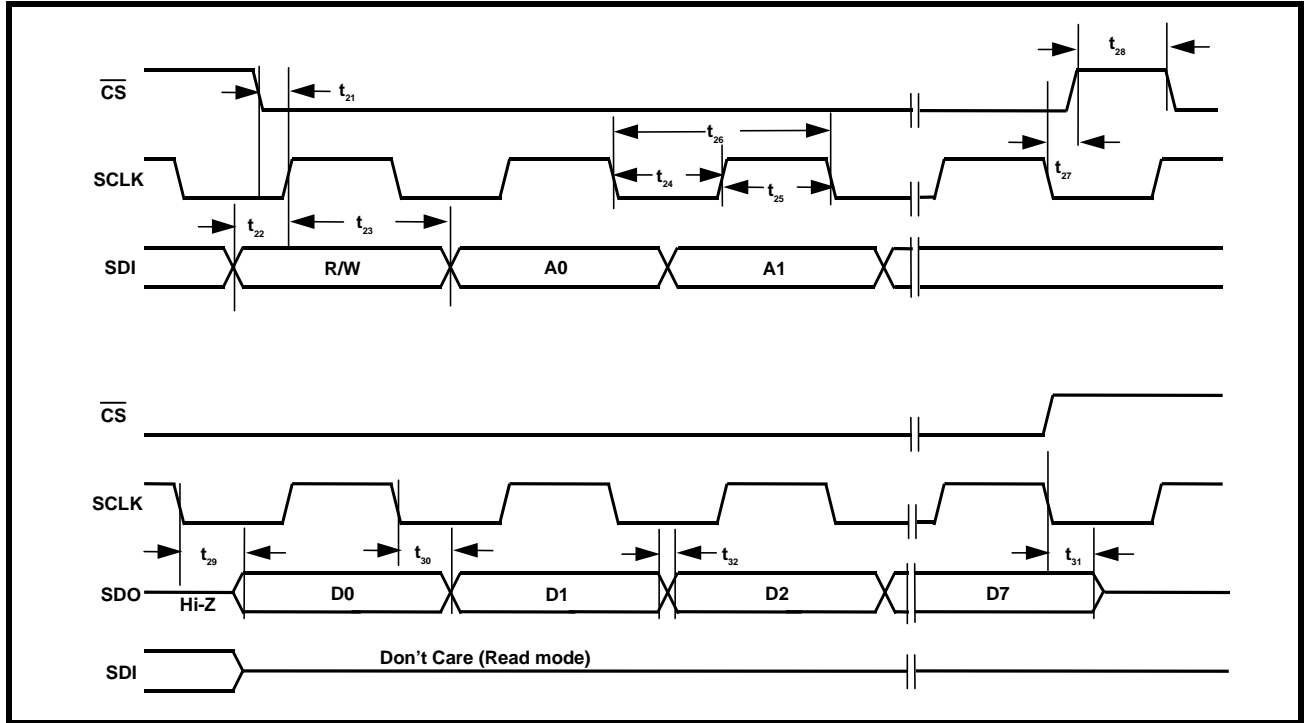


TABLE 5: MICROPROCESSOR SERIAL INTERFACE TIMINGS ($T_A = 25^{\circ}\text{C}$, $V_{DD}=3.3\text{V}\pm 5\%$ AND LOAD = 10PF)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX | UNITS |
|----------|--|------|------|-----|-------|
| t_{21} | \overline{CS} Low to Rising Edge of SClk | 5 | | | ns |
| t_{22} | SDI to Rising Edge of SClk | 5 | | | ns |
| t_{23} | SDI to Rising Edge of SClk Hold Time | 5 | | | ns |
| t_{24} | SClk "Low" Time | 50 | | | ns |
| t_{25} | SClk "High" Time | 50 | | | ns |
| t_{26} | SClk Period | 100 | | | ns |
| t_{27} | Falling Edge of SClk to rising edge of \overline{CS} | 0 | | | ns |
| t_{28} | \overline{CS} Inactive Time | 50 | | | ns |
| t_{29} | Falling Edge of SClk to SDO Valid Time | | | 20 | ns |
| t_{30} | Falling Edge of SClk to SDO Invalid Time | | | 10 | ns |
| t_{31} | Rising edge of \overline{CS} to High Z | | | 25 | ns |
| t_{32} | Rise/Fall time of SDO Output | | | 5 | ns |

TABLE 6: MICROPROCESSOR REGISTER DESCRIPTION

| REG | ADDR | TYPE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--|------|------------|--|----------|---------|----------|----------|----------|-----------|-----------|
| Global Control Register for All 16 Channels (0x00h) | | | | | | | | | | |
| 0 | 0x00 | R/W | GIE | Reserved | SR/DR | CODE | FIFO | JABW | JASEL1 | JASEL0 |
| 1 | 0x01 | RO | INTS7 | INTS6 | INTS5 | INTS4 | INTS3 | INTS2 | INTS1 | INTS0 |
| 2 | 0x02 | RO | INTS15 | INTS14 | INTS13 | INTS12 | INTS11 | INTS10 | INTS9 | INTS8 |
| 3 | 0x03 | RO | Revision ID (See Bit Description) | | | | | | | |
| 4 | 0x04 | RO | Device ID (See Bit Description) | | | | | | | |
| 5 | 0x05 | RO | Device ID (See Bit Description) | | | | | | | |
| Channel 0 Control Register (0x04h - 0x06h) | | | | | | | | | | |
| 6 | 0x06 | R/W | SRES_0 * | ARAOS_0 | ATAOS_0 | TAOS_0 | RLAM_0 | TXOE_0 | RCLKinv_0 | TCLKinv_0 |
| 7 | 0x07 | R/W | Reserved | AISIE_0 | DMOIE_0 | RLOSIE_0 | Reserved | Reserved | LPB1 | LPB0 |
| 8 | 0x08 | RUR/ RO | Reserved | AISIS_0 | DMOIS_0 | RLOIS_0 | Reserved | AISS_0 | DMOS_0 | RLOSS_0 |
| Channel 1 Control Register (0x07h - 0x09h) | | | | | | | | | | |
| 9 | 0x09 | R/W | SRES_1 * | ARAOS_1 | ATAOS_1 | TAOS_1 | RLAM_1 | TXOE_1 | RCLKinv_1 | TCLKinv_1 |
| 10 | 0x0A | R/W | Reserved | AISIE_1 | DMOIE_1 | RLOSIE_1 | Reserved | Reserved | LPB1 | LPB0 |
| 11 | 0x0B | RUR/ RO | Reserved | AISIS_1 | DMOIS_1 | RLOIS_1 | Reserved | AISS_1 | DMOS_1 | RLOSS_1 |
| Channel 2 Control Register (0x0Ah - 0x0Ch) | | | | | | | | | | |
| 12 | 0x0C | R/W | SRES_2 * | ARAOS_2 | ATAOS_2 | TAOS_2 | RLAM_2 | TXOE_2 | RCLKinv_2 | TCLKinv_2 |
| 13 | 0x0D | R/W | Reserved | AISIE_2 | DMOIE_2 | RLOSIE_2 | Reserved | Reserved | LPB1 | LPB0 |
| 14 | 0x0E | RUR/ RO | Reserved | AISIS_2 | DMOIS_2 | RLOIS_2 | Reserved | AISS_2 | DMOS_2 | RLOSS_2 |
| Channel 3 Control Register (0x0Dh - 0x0Fh) | | | | | | | | | | |
| 15 | 0x0F | R/W | SRES_3 * | ARAOS_3 | ATAOS_3 | TAOS_3 | RLAM_3 | TXOE_3 | RCLKinv_3 | TCLKinv_3 |
| 16 | 0x10 | R/W | Reserved | AISIE_3 | DMOIE_3 | RLOSIE_3 | Reserved | Reserved | LPB1 | LPB0 |
| 17 | 0x11 | RUR/ RO | Reserved | AISIS_3 | DMOIS_3 | RLOIS_3 | Reserved | AISS_3 | DMOS_3 | RLOSS_3 |
| Channel 4 Control Register (0x10h - 0x12h) | | | | | | | | | | |
| 18 | 0x12 | R/W | SRES_4 * | ARAOS_4 | ATAOS_4 | TAOS_4 | RLAM_4 | TXOE_4 | RCLKinv_4 | TCLKinv_4 |
| 19 | 0x13 | R/W | Reserved | AISIE_4 | DMOIE_4 | RLOSIE_4 | Reserved | Reserved | LPB1 | LPB0 |
| 20 | 0x14 | RUR/ RO | Reserved | AISIS_4 | DMOIS_4 | RLOIS_4 | Reserved | AISS_4 | DMOS_4 | RLOSS_4 |
| Channel 5 Control Register (0x13h - 0x15h) | | | | | | | | | | |
| 21 | 0x15 | R/W | SRES_5 * | ARAOS_5 | ATAOS_5 | TAOS_5 | RLAM_5 | TXOE_5 | RCLKinv_5 | TCLKinv_5 |
| 22 | 0x16 | R/W | Reserved | AISIE_5 | DMOIE_5 | RLOSIE_5 | Reserved | Reserved | LPB1 | LPB0 |
| 23 | 0x17 | RUR/ RO | Reserved | AISIS_5 | DMOIS_5 | RLOIS_5 | Reserved | AISS_5 | DMOS_5 | RLOSS_5 |
| Channel 6 Control Register (0x16h - 0x18h) | | | | | | | | | | |

TABLE 6: MICROPROCESSOR REGISTER DESCRIPTION

| REG | ADDR | TYPE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--|------|------------|-----------|----------|----------|-----------|----------|----------|------------|------------|
| 24 | 0x18 | R/W | SRES_6 * | ARAOS_6 | ATAOS_6 | TAOS_6 | RLAM_6 | TXOE_6 | RCLKinv_6 | TCLKinv_6 |
| 25 | 0x19 | R/W | Reserved | AISIE_6 | DMOIE_6 | RLOSIE_6 | Reserved | Reserved | LPB1 | LPB0 |
| 26 | 0x1A | RUR/ RO | Reserved | AISIS_6 | DMOIS_6 | RLOSIS_6 | Reserved | AISS_6 | DMOS_6 | RLOSS_6 |
| Channel 7 Control Register (0x19h - 0x1Bh) | | | | | | | | | | |
| 27 | 0x1B | R/W | SRES_7 * | ARAOS_7 | ATAOS_7 | TAOS_7 | RLAM_7 | TXOE_7 | RCLKinv_7 | TCLKinv_7 |
| 28 | 0x1C | R/W | Reserved | AISIE_7 | DMOIE_7 | RLOSIE_7 | Reserved | Reserved | LPB1 | LPB0 |
| 29 | 0x1D | RUR/ RO | Reserved | AISIS_7 | DMOIS_7 | RLOSIS_7 | Reserved | AISS_7 | DMOS_7 | RLOSS_7 |
| Channel 8 Control Register (0x1Ch - 0x1Eh) | | | | | | | | | | |
| 30 | 0x1E | R/W | SRES_8 * | ARAOS_8 | ATAOS_8 | TAOS_8 | RLAM_8 | TXOE_8 | RCLKinv_8 | TCLKinv_8 |
| 31 | 0x1F | R/W | Reserved | AISIE_8 | DMOIE_8 | RLOSIE_8 | Reserved | Reserved | LPB1 | LPB0 |
| 32 | 0x20 | RUR/ RO | Reserved | AISIS_8 | DMOIS_8 | RLOSIS_8 | Reserved | AISS_8 | DMOS_8 | RLOSS_8 |
| Channel 9 Control Register (0x1Fh - 0x21h) | | | | | | | | | | |
| 33 | 0x21 | R/W | SRES_9 * | ARAOS_9 | ATAOS_9 | TAOS_9 | RLAM_9 | TXOE_9 | RCLKinv_9 | TCLKinv_9 |
| 34 | 0x22 | R/W | Reserved | AISIE_9 | DMOIE_9 | RLOSIE_9 | Reserved | Reserved | LPB1 | LPB0 |
| 35 | 0x23 | RUR/ RO | Reserved | AISIS_9 | DMOIS_9 | RLOSIS_9 | Reserved | AISS_9 | DMOS_9 | RLOSS_9 |
| Channel 10 Control Register (0x22h - 0x24h) | | | | | | | | | | |
| 36 | 0x24 | R/W | SRES_10 * | ARAOS_10 | ATAOS_10 | TAOS_10 | RLAM_10 | TXOE_10 | RCLKinv_10 | TCLKinv_10 |
| 37 | 0x25 | R/W | Reserved | AISIE_10 | DMOIE_10 | RLOSIE_10 | Reserved | Reserved | LPB1 | LPB0 |
| 38 | 0x26 | RUR/ RO | Reserved | AISIS_10 | DMOIS_10 | RLOSIS_10 | Reserved | AISS_10 | DMOS_10 | RLOSS_10 |
| Channel 11 Control Register (0x25h - 0x27h) | | | | | | | | | | |
| 39 | 0x27 | R/W | SRES_11 * | ARAOS_11 | ATAOS_11 | TAOS_11 | RLAM_11 | TXOE_11 | RCLKinv_11 | TCLKinv_11 |
| 40 | 0x28 | R/W | Reserved | AISIE_11 | DMOIE_11 | RLOSIE_11 | Reserved | Reserved | LPB1 | LPB0 |
| 41 | 0x29 | RUR/ RO | Reserved | AISIS_11 | DMOIS_11 | RLOSIS_11 | Reserved | AISS_11 | DMOS_11 | RLOSS_11 |
| Channel 12 Control Register (0x28h - 0x2Ah) | | | | | | | | | | |
| 42 | 0x2A | R/W | SRES_12 * | ARAOS_12 | ATAOS_12 | TAOS_12 | RLAM_12 | TXOE_12 | RCLKinv_12 | TCLKinv_12 |
| 43 | 0x2B | R/W | Reserved | AISIE_12 | DMOIE_12 | RLOSIE_12 | Reserved | Reserved | LPB1 | LPB0 |
| 44 | 0x2C | RUR/ RO | Reserved | AISIS_12 | DMOIS_12 | RLOSIS_12 | Reserved | AISS_12 | DMOS_12 | RLOSS_12 |
| Channel 13 Control Register (0x2Bh - 0x2Dh) | | | | | | | | | | |
| 45 | 0x2D | R/W | SRES_13 * | ARAOS_13 | ATAOS_13 | TAOS_13 | RLAM_13 | TXOE_13 | RCLKinv_13 | TCLKinv_13 |
| 46 | 0x2E | R/W | Reserved | AISIE_13 | DMOIE_13 | RLOSIE_13 | Reserved | Reserved | LPB1 | LPB0 |
| 47 | 0x2F | RUR/ RO | Reserved | AISIS_13 | DMOIS_13 | RLOSIS_13 | Reserved | AISS_13 | DMOS_13 | RLOSS_13 |
| | | | | | | | | | | |

TABLE 6: MICROPROCESSOR REGISTER DESCRIPTION

| REG | ADDR | TYPE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--|------|------------|-----------|----------|----------|-----------|----------|----------|------------|------------|
| Channel 14 Control Register (0x2Eh - 0x30h) | | | | | | | | | | |
| 48 | 0x30 | R/W | SRES_14 * | ARAOS_14 | ATAOS_14 | TAOS_14 | RLAM_14 | TXOE_14 | RCLKinv_14 | TCLKinv_14 |
| 49 | 0x31 | R/W | Reserved | AISIE_14 | DMOIE_14 | RLOSIE_14 | Reserved | Reserved | LPB1 | LPB0 |
| 50 | 0x32 | RUR/ RO | Reserved | AISIS_14 | DMOIS_14 | RLOIS_14 | Reserved | AISS_14 | DMOS_14 | RLOSS_14 |
| Channel 15 Control Register (0x31h - 0x33h) | | | | | | | | | | |
| 51 | 0x33 | R/W | SRES_15 * | ARAOS_15 | ATAOS_15 | TAOS_15 | RLAM_15 | TXOE_15 | RCLKinv_15 | TCLKinv_15 |
| 52 | 0x34 | R/W | Reserved | AISIE_15 | DMOIE_15 | RLOSIE_15 | Reserved | Reserved | LPB1 | LPB0 |
| 53 | 0x35 | RUR/ RO | Reserved | AISIS_15 | DMOIS_15 | RLOIS_15 | Reserved | AISS_15 | DMOS_15 | RLOSS_15 |

NOTE: * Indicates that these bits are WRITE-ONLY Reset for that channel register only.

TABLE 7: MICROPROCESSOR REGISTER 0x00H BIT DESCRIPTION

| GLOBAL CONTROL REGISTER FOR ALL 16 CHANNELS (0x00H) | | | | |
|---|----------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | GIE | Global Interrupt Enable The global interrupt enable is used to enable/disable all interrupt activity for all 16 channels. This bit must be set "High" for the interrupt pin to operate. "0" = Disable all interrupt generation "1" = Enable interrupt generation to the individual channel registers | R/W | 0 |
| D6 | Reserved | This Register Bit is Not Used | R/W | 0 |
| D5 | SR/DR | Single Rail / Dual Rail Select This bit is used to configure the receive outputs and transmit inputs to single rail or dual rail data formats. "0" = Dual Rail "1" = Single Rail | R/W | 0 |
| D4 | CODE | Encoding / Decoding Select (Single Rail Mode Only) This bit is used to select between AMI or HDB3. "0" = HDB3 "1" = AMI | R/W | 0 |
| D3 | FIFOS | FIFO Depth Select The FIFO depth select is used to configure the part for a 32-bit or 64-bit FIFO (Within the Jitter Attenuator Block). The delay of the FIFO is typically equal to ½ the FIFO depth. "0" = 32-bit FIFO "1" = 64-bit FIFO | R/W | 0 |

TABLE 7: MICROPROCESSOR REGISTER 0x00H BIT DESCRIPTION

| GLOBAL CONTROL REGISTER FOR ALL 16 CHANNELS (0x00H) | | | | |
|---|------------------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D2 | JABW | <p>JA Band width Select</p> <p>This bit is used to select the band with of the JA PLL.</p> <p>"0" = 10 Hz "1" = 1.5Hz</p> <p><i>NOTE: If a "1" is written into this bit, JA FIFO size of 64 bit wide is automatically selected.</i></p> | R/W | 0 |
| D1 D0 | JASEL1 JASEL0 | <p>Jitter Attenuator Select</p> <p>These bits are used to configure the Jitter Attenuator into the Receive or Transmit path.</p> <p>"00" = Disabled "01" = Transmit Path "10" = Receive Path "11" = Disabled</p> | R/W | 0 0 |

TABLE 8: MICROPROCESSOR REGISTERS 0x01H & 0x02H BIT DESCRIPTION

| INTERRUPT STATUS REGISTERS (0x01H) & 0x02H | | | | |
|--|--------|---|---------------|--------------------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 D6 D5 D4 D3 D2 D1 D0 | INTS_n | <p>Interrupt Status</p> <p>These 2 registers are ready only to determine when an interrupt event occurs, the channel that generates interrupt can be identified with minimum read/write operation.</p> | RO | 0 0 0 0 0 0 0 0 |

TABLE 9: MICROPROCESSOR REGISTER 0x03H BIT DESCRIPTION

| REVISION "ID" REGISTER (0x03H) | | | | |
|--|---------------|---|---------------|--------------------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 D6 D5 D4 D3 D2 D1 D0 | Revision "ID" | The revision "ID" of the XRT83SL216 LIU is used to enable software to identify which revision of silicon is currently being tested. The revision "ID" for the first revision of silicon (Revision A) will be 0x01h. | RO | 0 0 0 0 0 0 0 1 |

TABLE 10: MICROPROCESSOR REGISTERS 0x04H & 0x05H BIT DESCRIPTION

| DEVICE "ID" REGISTERS (0x04H & 0x05H) | | | | |
|--|-------------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 D6 D5 D4 D3 D2 D1 D0 | Device "ID" | The device for this chip consists of 2 read only registers. The ID for the XR T83SL216 is 0x8004h. | RO | |

TABLE 11: MICROPROCESSOR REGISTER BIT DESCRIPTION

| CHANNEL CONTROL REGISTER (CHANNEL_n, where n = 0:15) (0x06H, 0x09H, 0x0CH, 0x0FH, 0x12H, 0x15H, 0x18H, 0x1BH, 1EH, 0x21H, 0x24H, 0x27H, 0x2AH, 0x2DH, 0x30H, 0x33H) | | | | |
|--|---------|---|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | SRES_n | Software Reset Writing a "1" to this bit will cause the channel register to reset to it's default value. <i>NOTE: This is a Write-Only bit.</i> | WO | X |
| D6 | ARAOS_n | Automatic Receive All Ones If ARAOS_n is selected, an all ones pattern will be sent to the RPOS/RNEG outputs if the channel experiences an RLOS condition. If RLOS does not occur, ARAOS_n will remain inactive. "0" = Disabled "1" = Enabled | R/W | 0 |

TABLE 11: MICROPROCESSOR REGISTER BIT DESCRIPTION

| CHANNEL CONTROL REGISTER (CHANNEL_n, where n = 0:15) (0x06H, 0x09H, 0x0CH, 0x0FH, 0x12H, 0x15H, 0x18H, 0x1BH, 1EH, 0x21H, 0x24H, 0x27H, 0x2AH, 0x2DH, 0x30H, 0x33H) | | | | |
|--|-------------|--|----------------------|---------------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D5 | ATAOS_n | Automatic Transmit All Ones If ATAOS_n is selected, an all ones pattern will be transmitted from TTIP/TRING if the channel experiences an RLOS condition. If RLOS does not occur, ATAOS_n will remain inactive. "0" = Disabled "1" = Enabled | R/W | 0 |
| D4 | TAOS_n | Transmit All Ones If TAOS_n is selected, an all ones pattern will be transmitted from TTIP/TRING if the transmitter is turned on. Remote Loop Back has priority over TAOS. "0" = Disabled "1" = Enabled | R/W | 0 |
| D3 | RLAM_n | RLOS/AIS Mode Select for channel n This bit is used to select the industry standard for declaring / clearing RLOS and AIS functionality. See the Receive section of the Line Interface description. "0" = ITU G.775 "1" =ETSI300233 | R/W | 0 |
| D2 | TXOE_n | Transmit Output Enable Upon power up, the transmitters are tri-stated. This bit is used to enable the transmitter for this channel if the TxOE pin is pulled "High". If the TxOE pin is pulled "Low", all 8 transmitters are tri-stated. "0" = Transmitter is disabled "1" = Transmitter is enabled if TxOE pin is pulled "High" | R/W | 0 |
| D1 | RCLKinv_n | Receiver Clock Invert This bit is used to invert receive clock update edge with respect to RPOS/RNEG output data. "0" =RPOS/RNEG data is updated on the rising edge of RCLK "1" =RPOS/RNEG data is updated on the falling edge of RCLK. | R/W | 0 0 |
| D0 | TCLKinv_n | Transmit Clock Invert This bit is used to invert transmit clock sampling edge with respect to TPOS/TNEG input data. "0" =TPOS/TNEG data is sampled on the falling edge of TCLK "1" =TPOS/TNEG data is sampled on the rising edge of TCLK. | R/W | 0 |

TABLE 12: MICROPROCESSOR REGISTER BIT DESCRIPTION

| CHANNEL CONTROL REGISTER (CHANNEL_n, where n = 0:15) (0x07H, 0x0AH, 0x0DH, 0x10H, 0x13H, 0x16H, 0x19H, 0x1CH, 0x1FH, 0x22H, 0x25H, 0x28H, 0x2BH, 0x2EH, 0x31H, 0x34H) | | | | | | | | | | | | | | | | | | | |
|--|--------------|---|---------------|--------------------------|---------------|---|---|-------------|---|---|-----------------|---|---|-----------------|---|---|------------------|-----|---|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) | | | | | | | | | | | | | | | |
| D7 | Reserved | This Register Bit is Not Used | X | X | | | | | | | | | | | | | | | |
| D6 | AISIE_n | Alarm Indication Signal Interrupt Enable "0" = Masks the AIS interrupt generation "1" = Enables Interrupt generation | R/W | 0 | | | | | | | | | | | | | | | |
| D5 | DMOIE_n | Driver Monitor Output Interrupt Enable "0" = Masks the DMO interrupt generation "1" = Enables Interrupt generation | R/W | 0 | | | | | | | | | | | | | | | |
| D4 | RLOSIE_n | Receiver Loss of Signal Interrupt Enable "0" = Masks the RLOS interrupt generation "1" = Enables Interrupt generation | R/W | 0 | | | | | | | | | | | | | | | |
| D3 | Reserved | This Register Bit is Not Used | X | X | | | | | | | | | | | | | | | |
| D2 | Reserved | This Register Bit is Not Used | X | X | | | | | | | | | | | | | | | |
| D1 D0 | LPB1 LPB0 | Loop Back Select These bits are used to configure the channel in one of three loop-back modes. For additional information on loopback modes, see the Application Section of this datasheet. <table border="1" data-bbox="441 1129 873 1369"> <thead> <tr> <th>LPB1</th> <th>LPB0</th> <th>Loopback Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>No Loopback</td> </tr> <tr> <td>0</td> <td>1</td> <td>Analog Loopback</td> </tr> <tr> <td>1</td> <td>0</td> <td>Remote Loopback</td> </tr> <tr> <td>1</td> <td>1</td> <td>Digital Loopback</td> </tr> </tbody> </table> | LPB1 | LPB0 | Loopback Mode | 0 | 0 | No Loopback | 0 | 1 | Analog Loopback | 1 | 0 | Remote Loopback | 1 | 1 | Digital Loopback | R/W | 0 |
| LPB1 | LPB0 | Loopback Mode | | | | | | | | | | | | | | | | | |
| 0 | 0 | No Loopback | | | | | | | | | | | | | | | | | |
| 0 | 1 | Analog Loopback | | | | | | | | | | | | | | | | | |
| 1 | 0 | Remote Loopback | | | | | | | | | | | | | | | | | |
| 1 | 1 | Digital Loopback | | | | | | | | | | | | | | | | | |

TABLE 13: MICROPROCESSOR REGISTER BIT DESCRIPTION

| CHANNEL CONTROL REGISTER (CHANNEL_n, where n = 0:15) (0x08H, 0x0BH, 0x0EH, 0x11H, 0x14H, 0x17H, 0x1AH, 0x1DH, 0x20H, 0x23H, 0x26H, 0x29H, 0x2CH, 0x2FH, 0x32H, 0x35H) | | | | |
|--|----------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D7 | Reserved | This Register Bit is Not Used | R/W | X |
| D6 | AISIS_n | Alarm Indication Signal Interrupt Status "0" = No Change "1" = Change in Status Occured | RUR | 0 |

TABLE 13: MICROPROCESSOR REGISTER BIT DESCRIPTION

| CHANNEL CONTROL REGISTER (CHANNEL_n, where n = 0:15) (0x08H, 0x0BH, 0x0EH, 0x11H, 0x14H, 0x17H, 0x1AH, 0x1DH, 0x20H, 0x23H, 0x26H, 0x29H, 0x2CH, 0x2FH, 0x32H, 0x35H) | | | | |
|--|----------|--|---------------|--------------------------|
| BIT | NAME | FUNCTION | Register Type | Default Value (HW reset) |
| D5 | DMOIS_n | Driver Monitor Output Interrupt Status "0" = No Change "1" = Change in Status Occured | RUR | 0 |
| D4 | RLOSSI_n | Receiver Loss of Signal Interrupt Status "0" = No Change "1" = Change in Status Occured | RUR | 0 |
| D3 | Reserved | This Register Bit is Not Used | R/W | X |
| D2 | AISS_n | AIS Alarm Status This alarm indication signal detection is always active regardless if the interrupt generation is disabled. This bit indicates the AIS activity at the time of reading. "0" = No Alarm "1" = An All "Ones" Signal is detected. | RO | 0 |
| D1 | DMOS_n | Driver Monitor Output Status The Driver Monitor output is always active regardless if the interrupt generation is disabled. This bit indicates the DMO output activity at the time of reading. "0" = No alarm "1" = Failure at the transmit output is detected. | RO | 0 |
| D0 | RLOSS_n | Receive Loss of Signal Status The receiver loss of signal detection is always active regardless if the interrupt generation is disabled. This bit indicates the RLOS activity at the time of reading. "0" = No Alarm "1" = Loss of Signal condition is detected. | RO | 0 |

ELECTRICAL CHARACTERISTICS

TABLE 14: ABSOLUTE MAXIMUM RATINGS

| | |
|-----------------------|-----------------|
| Storage Temperature | -65°C to +150°C |
| Operating Temperature | -40°C to +85°C |
| Supply Voltage | -0.5V to +6.0V |

TABLE 15: DC DIGITAL INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS

| VDD=3.3V ±5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED | | | | | |
|--|-----------------|------|-----|------|-------|
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
| Power Supply Voltage | VDD | 3.13 | 3.3 | 3.46 | V |
| Input High Voltage | V _{IH} | 2.0 | - | 5.0 | V |
| Input Low Voltage | V _{IL} | -0.5 | - | 0.8 | V |
| Output High Voltage IOH=2.0mA | V _{OH} | 2.4 | - | | V |
| Output Low Voltage IOL=2.0mA | V _{OL} | - | - | 0.4 | V |
| Input Leakage Current | I _L | - | - | ±10 | µA |
| Input Capacitance | C _I | - | 5.0 | | pF |
| Output Lead Capacitance | C _L | - | - | 25 | pF |

NOTE: Input leakage current excludes pins that are internally pulled "Low" or "High".

TABLE 16: AC ELECTRICAL CHARACTERISTICS

| VDD=3.3V ±5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED | | | | | |
|--|--------|-----|-----|-----|-------|
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
| MCLK Clock Duty Cycle | | 40 | - | 60 | % |
| MCLK Clock Tolerance | | - | ±50 | - | ppm |

TABLE 17: POWER CONSUMPTION

| VDD=3.3V ±5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED | | | | | | | |
|--|-----------|----------|-------------|------------|-----|------|-----------------------|
| MODE | IMPEDANCE | RECEIVER | TRANSMITTER | TYP | MAX | UNIT | TEST CONDITION |
| E1 | 75Ω | 2:1 | 1:2 | 1.6 2.3 | | W | 50% ones 100% ones |
| E1 | 120Ω | 2:1 | 1:2 | 1.4 1.9 | | W | 50% ones 100% ones |
| E1 | 75Ω/120Ω | 2:1 | 1:2 | 400 | | mW | Transmitter OFF |

TABLE 18: RECEIVER ELECTRICAL CHARACTERISTICS

| VDD=3.3V ±5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED | | | | | |
|--|------|------|------|-------------------------------|--|
| PARAMETER | MIN | TYP | MAX | UNIT | TEST CONDITION |
| Receiver Loss of Signal | | | | | |
| Number of consecutive zeros before RLOS is declared | - | 32 | - | | G.775 |
| | - | 2048 | - | | ETSI 300 233 |
| Input signal level at RLOS | 15 | 20 | - | dB | Cable attenuation @ 1024kHz |
| RLOS clear | 12.5 | - | - | % ones | ITU-G.775, ETSI 300 233 |
| Receiver Sensitivity (flat loss only) | 11 | 13 | - | dB | With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω. With -18dB interference signal added. |
| Interference Margin | -18 | -14 | | | With 6dB cable loss. |
| Input Impedance | - | 15 | - | kΩ | |
| Input Jitter Tolerance | | | | | |
| 1Hz | 37 | - | - | U _I _{p-p} | ITU-G.823 |
| 10kHz - 100kHz | 0.2 | - | - | U _I _{p-p} | |
| Recovered Clock Jitter | | | | | |
| Transfer Corner Frequency | - | 36 | - | kHz | |
| Peaking Amplitude | - | - | +0.5 | dB | |
| Jitter Attenuator Corner Frequency | | | | | |
| JABW = "0" | - | 10 | - | Hz | |
| JABW = "1" | - | 1.5 | - | Hz | |
| Return Loss | | | | | |
| 51kHz - 102kHz | 14 | - | - | dB | ITU-G.703 |
| 102kHz - 2048kHz | 20 | - | - | dB | |
| 2048kHz - 3072kHz | 16 | - | - | dB | |

TABLE 19: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

| VDD=3.3V ±5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED | | | | | |
|--|------|-------|------|------------------|--|
| PARAMETER | MIN | TYP | MAX | UNIT | TEST CONDITION |
| AMI Output Pulse Amplitude | | | | | |
| 75Ω | 2.13 | 2.37 | 2.60 | V | 1:2 Transformer |
| 120Ω | 2.70 | 3.00 | 3.30 | V | |
| Output Pulse Width | 224 | 244 | 264 | ns | |
| Output Pulse Width Ratio | 0.95 | - | 1.05 | | ITU-G.703 |
| Output Pulse Amplitude Ratio | 0.95 | - | 1.05 | | ITU-G.703 |
| Jitter Added by the Transmitter Output | - | 0.025 | 0.05 | U _{Ipp} | Broad Band with jitter free TCLK applied to the input. |
| Output Return Loss | | | | | |
| 51kHz - 102kHz | 12 | - | - | dB | ETSI 300 166 |
| 102kHz - 2048kHz | 10 | - | - | dB | |
| 2048kHz - 3072kHz | 8 | - | - | dB | |

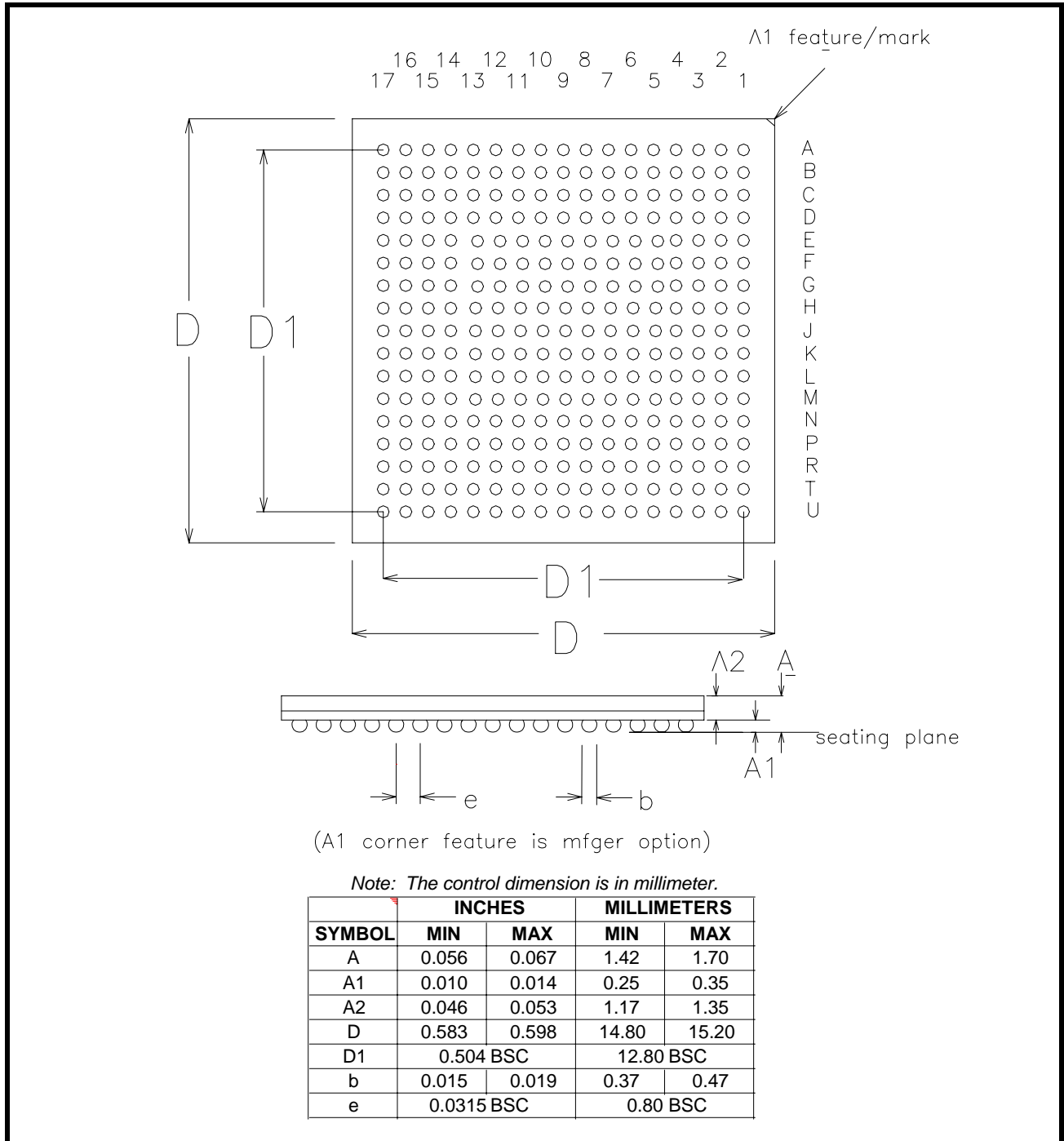
NOTE: Transmit output return loss is dependent on the transformer characteristics.

ORDERING INFORMATION

| PRODUCT NUMBER | PACKAGE | OPERATING TEMPERATURE RANGE |
|----------------|----------------|-----------------------------|
| XRT83SL216IB | 289 ball STBGA | -40°C to +85°C |

PACKAGE DIMENSIONS

FIGURE 23. 15X15MM 289 BALL STBGA



16-CHANNEL E1 SHORT-HAUL LINE INTERFACE UNIT
REVISION HISTORY

| REVISION # | DATE | DESCRIPTION |
|------------|----------|---|
| P1.0.0 | 07/07/05 | First release of the 16-Channel LIU Preliminary Datasheet |
| P1.0.1 | 08/04/05 | Edits to features, RNEG description, figure 6,, electrical supply voltage. |
| P1.0.2 | 11/05 | Edits |
| P1.0.3 | 12/06/05 | Changed receive transformer turns ratio from 1:1 to 2:1. Added register information. Table 16: Power Consumption added TYP values. |
| 1.0.0 | 08/02/06 | Removed TBD's from electrical, removed preliminary and updated document format. Added timing diagram and timing info for the microprocessor serial interface. |

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