2.5V LVDS 1:6 Clock Buffer Terabuffer™ II

IDT5T9306

DATA SHEET

FEATURES:

- **Guaranteed Low Skew < 40ps (max)**
- **Very low duty cycle distortion < 125ps (max)**
- **High speed propagation delay < 1.75ns (max)**
- **Additive phase jitter, RMS 0.159ps (typical) @ 125MHz**
- **Up to 1GHz operation**
- **Selectable inputs**
- **Hot insertable and over-voltage tolerant inputs**
- **3.3V / 2.5V LVTTL, HSTL, eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML, or LVDS input interface**
- **Selectable differential inputs to six LVDS outputs**
- **Power-down mode**
- **2.5V VDD**
- **Available in VFQFPN package**

APPLICATIONS:

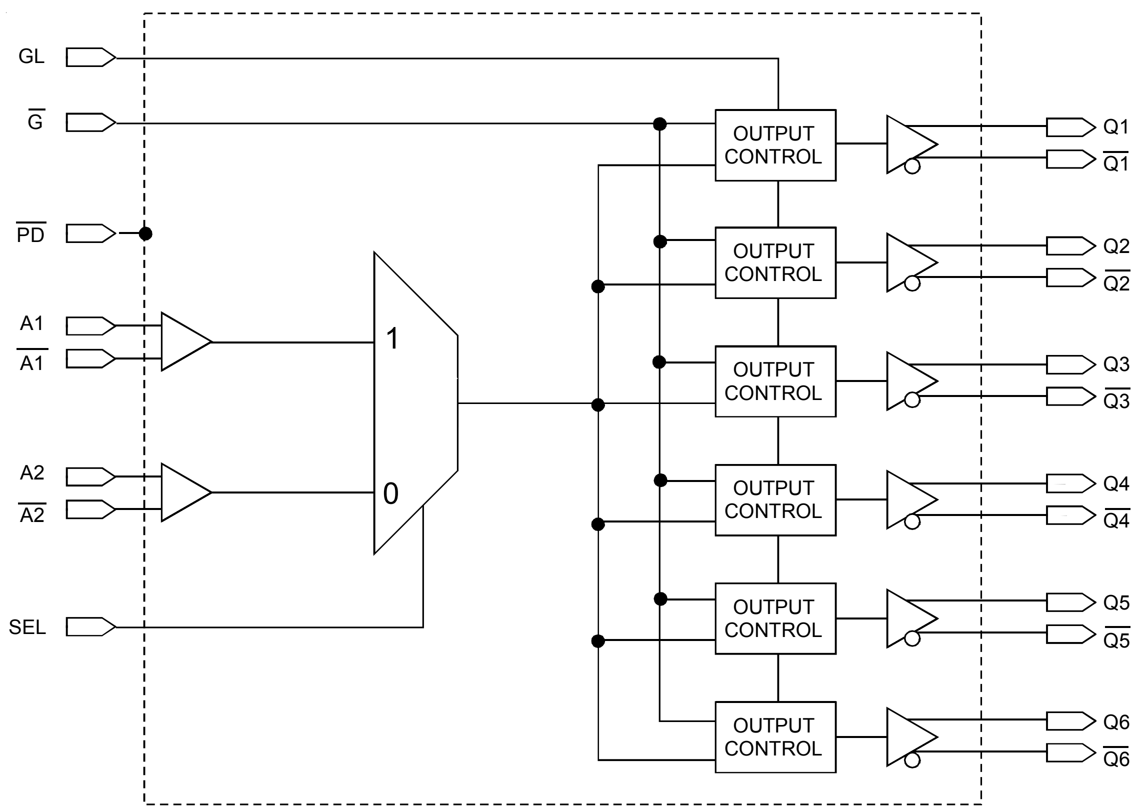
- **Clock distribution**

DESCRIPTION:

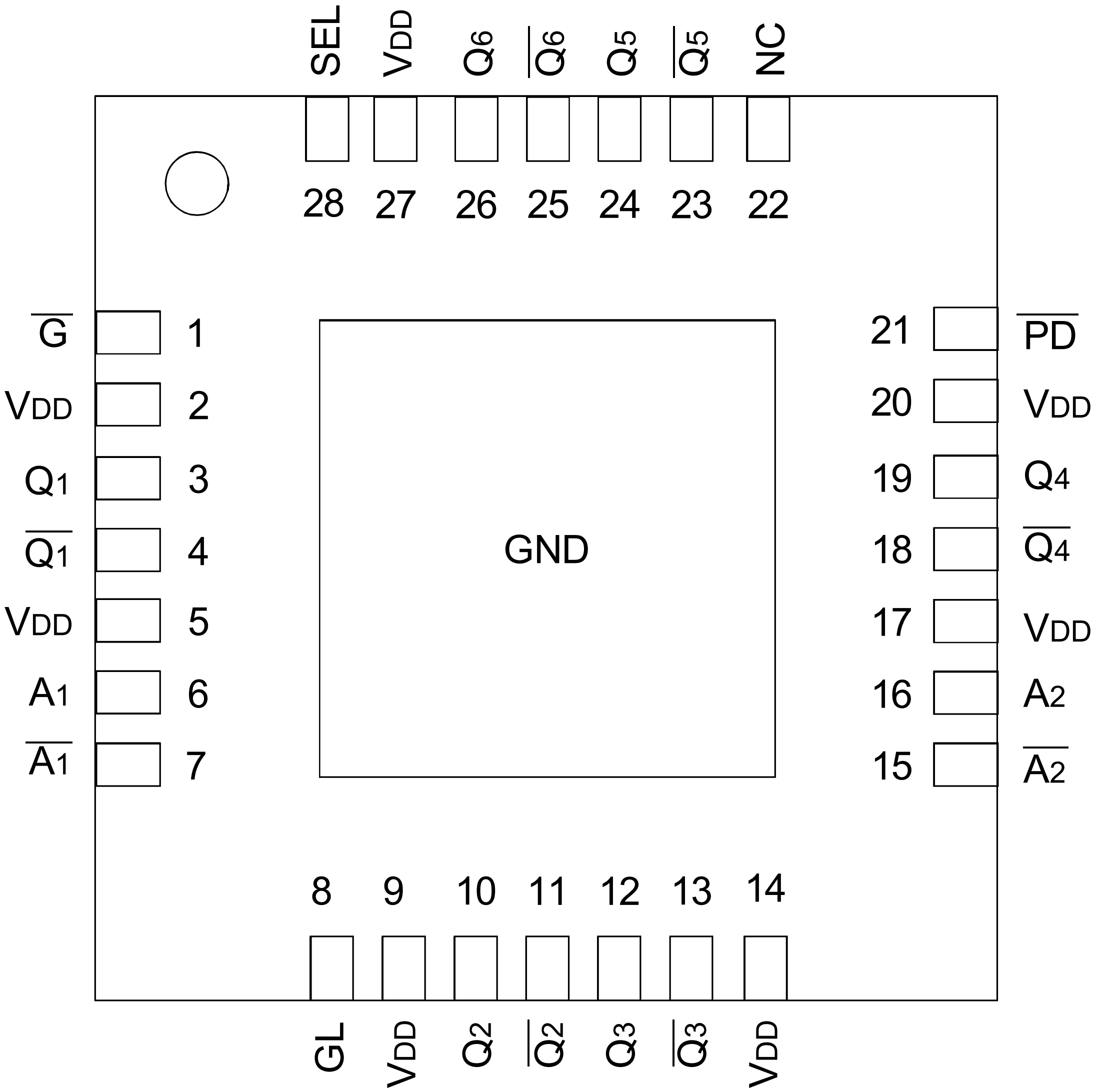
The IDT5T9306 2.5V differential clock buffer is a user-selectable differential input to six LVDS outputs. The fanout from a differential input to six LVDS outputs reduces loading on the preceding driver and provides an efficient clock distribution network. The IDT5T9306 can act as a translator from a differential HSTL, eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML, or LVDS input to LVDS outputs. A single-ended 3.3V / 2.5V LVTTL input can also be used to translate to LVDS outputs. The redundant input capability allows for an asynchronous change-over from a primary clock source to a secondary clock source. Selectable reference inputs are controlled by SEL.

The IDT5T9306 outputs can be asynchronously enabled/disabled. When disabled, the outputs will drive to the value selected by the GL pin. Multiple power and grounds reduce noise.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



VFQFPN
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max	Unit
V_{DD}	Power Supply Voltage	–0.5 to +3.6	V
V_I	Input Voltage	–0.5 to +3.6	V
V_O	Output Voltage[2]	–0.5 to V_{DD} +0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_J	Junction Temperature	150	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Not to exceed 3.6V.

CAPACITANCE[1] (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Min	Typ.	Max.	Unit
C_{IN}	Input Capacitance	—	—	3	pF

NOTE:

1. This parameter is measured at characterization but not tested

RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	–40	+25	+85	°C
V_{DD}	Internal Power Supply Voltage	2.3	2.5	2.7	V

PIN DESCRIPTION

Symbol	I/O	Type	Description
$A_{[1:2]}$	I	Adjustable[1,4]	Clock input. $A_{[1:2]}$ is the "true" side of the differential clock input.
$\overline{A}_{[1:2]}$	I	Adjustable[1,4]	Complementary clock inputs. $\overline{A}_{[1:2]}$ is the complementary side of $A_{[1:2]}$. For LVTTL single-ended operation, $\overline{A}_{[1:2]}$ should be set to the desired toggle voltage for $A_{[1:2]}$: 3.3V LVTTL V_{REF} = 1650mV 2.5V LVTTL V_{REF} = 1250mV
$\overline{G}$	I	LVTTL	Gate control for differential outputs Q_1 and $\overline{Q}_1$ through Q_6 and $\overline{Q}_6$. When $\overline{G}$ is LOW, the differential outputs are active. When $\overline{G}$ is HIGH, the differential outputs are asynchronously driven to the level designated by GL[2].
GL	I	LVTTL	Specifies output disable level. If HIGH, "true" outputs disable HIGH and "complementary" outputs disable LOW. If LOW, "true" outputs disable LOW and "complementary" outputs disable HIGH.
Qn	O	LVDS	Clock outputs
$\overline{Qn}$	O	LVDS	Complementary clock outputs
SEL	I	LVTTL	Reference clock select. When LOW, selects A_2 and $\overline{A}_2$. When HIGH, selects A_1 and $\overline{A}_1$.
$\overline{PD}$	I	LVTTL	Power-down control. Shuts off entire chip. If LOW, the device goes into low power mode. Inputs and outputs are disabled. Both "true" and "complementary" outputs will pull to V_{DD}. Set HIGH for normal operation.[3]
V_{DD}		PWR	Power supply for the device core and inputs
GND		PWR	Power supply return for all power
NC			No connect; recommended to connect to GND

NOTES:

1. Inputs are capable of translating the following interface standards:
   Single-ended 3.3V and 2.5V LVTTL levels
   Differential HSTL and eHSTL levels
   Differential LVEPECL (2.5V) and LVPECL (3.3V) levels
   Differential LVDS levels
   Differential CML levels
2. Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.
3. It is recommended that the outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting $\overline{PD}$.
4. The user must take precautions with any differential input interface standard being used in order to prevent instability when there is no input signal.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVTTL[1]

Symbol	Parameter	Test Conditions	Min.	Typ.[2]	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current	V_{DD} = 2.7V	—	—	±5	µA
I_{IL}	Input LOW Current	V_{DD} = 2.7V	—	—	±5	
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.3V, I_{IN} = -18mA	—	- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		- 0.3	—	+3.6	V
V_{IH}	DC Input HIGH		1.7	—	—	V
V_{IL}	DC Input LOW		—	—	0.7	V
V_{THI}	DC Input Threshold Crossing Voltage		—	V_{DD} /2	—	V
V_{REF}	Single-Ended Reference Voltage[3]	3.3V LVTTL	—	1.65	—	V
		2.5V LVTTL	—	1.25	—	

NOTES:
1. See RECOMMENDED OPERATING RANGE table.
2. Typical values are at V_{DD} = 2.5V, +25°C ambient.
3. For $A_{[1:2]}$ single-ended operation, $\overline{A}_{[1:2]}$ is tied to a DC reference voltage.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR DIFFERENTIAL INPUTS[1]

Symbol	Parameter	Test Conditions	Min.	Typ.[2]	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current	V_{DD} = 2.7V	—	—	±5	µA
I_{IL}	Input LOW Current	V_{DD} = 2.7V	—	—	±5	
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.3V, I_{IN} = -18mA	—	- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		- 0.3	—	+3.6	V
V_{DIF}	DC Differential Voltage[3]		0.1	—	—	V
V_{CM}	DC Common Mode Input Voltage[4]		0.05	—	V_{DD}	V

NOTES:
1. See RECOMMENDED OPERATING RANGE table.
2. Typical values are at V_{DD} = 2.5V, +25°C ambient.
3. V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
4. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2.

DC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING RANGE FOR LVDS[1]

Symbol	Parameter	Test Conditions	Min.	Typ.[2]	Max	Unit
Output Characteristics						
V_{OT}(+)	Differential Output Voltage for the True Binary State		247	—	454	mV
V_{OT}(-)	Differential Output Voltage for the False Binary State		247	—	454	mV
ΔV_{OT}	Change in V_{OT} Between Complementary Output States		—	—	50	mV
V_{OS}	Output Common Mode Voltage (Offset Voltage)		1.125	1.2	1.375	V
ΔV_{OS}	Change in V_{OS} Between Complementary Output States		—	—	50	mV
I_{OS}	Outputs Short Circuit Current	V_{OUT} + and V_{OUT} - = 0V	—	12	24	mA
I_{OSD}	Differential Outputs Short Circuit Current	V_{OUT} + = V_{OUT} -	—	6	12	mA

NOTES:
1. See RECOMMENDED OPERATING RANGE table.
2. Typical values are at V_{DD} = 2.5V, T_A = +25°C ambient.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR HSTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing(1)	1	V
V_X	Differential Input Signal Crossing Point(2)	750	mV
D_H	Duty Cycle	50	%
V_{THI}	Input Timing Measurement Reference Level(3)	Crossing Point	V
t_R, t_F	Input Signal Edge Rate(4)	2	V/ns

NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.
2. A 750mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR eHSTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing(1)	1	V
V_X	Differential Input Signal Crossing Point(2)	900	mV
D_H	Duty Cycle	50	%
V_{THI}	Input Timing Measurement Reference Level(3)	Crossing Point	V
t_R, t_F	Input Signal Edge Rate(4)	2	V/ns

NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.
2. A 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR LVEPECL (2.5V) AND LVPECL (3.3V)

Symbol	Parameter		Value	Units
V_{DIF}	Input Signal Swing(1)		732	mV
V_X	Differential Input Signal Crossing Point(2)	LVEPECL	1082	mV
		LVPECL	1880	
D_H	Duty Cycle		50	%
V_{THI}	Input Timing Measurement Reference Level(3)		Crossing Point	V
t_R, t_F	Input Signal Edge Rate(4)		2	V/ns

NOTES:

1. The 732mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.
2. 1082mV LVEPECL (2.5V) and 1880mV LVPECL (3.3V) crossing point levels are specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR LVDS

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing[1]	400	mV
V_X	Differential Input Signal Crossing Point[2]	1.2	V
D_H	Duty Cycle	50	%
V_{THI}	Input Timing Measurement Reference Level[3]	Crossing Point	V
t_R, t_F	Input Signal Edge Rate[4]	2	V/ns

NOTES:

1. The 400mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.
2. A 1.2V crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

AC DIFFERENTIAL INPUT SPECIFICATIONS[1]

Symbol	Parameter	Min.	Typ.	Max	Unit
V_{DIF}	AC Differential Voltage[2]	0.1	—	3.6	V
V_{IX}	Differential Input Crosspoint Voltage	0.05	—	V_{DD}	V
V_{CM}	Common Mode Input Voltage Range[3]	0.05	—	V_{DD}	V
V_{IN}	Input Voltage	- 0.3		+3.6	V

NOTES:

1. The output will not change state until the inputs have crossed and the minimum differential voltage range defined by V_{DIF} has been met or exceeded.
2. V_{DIF} specifies the minimum input voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. The AC differential voltage must be achieved to guarantee switching to a new state.
3. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2.

POWER SUPPLY CHARACTERISTICS FOR LVDS OUTPUTS[1]

Symbol	Parameter	Test Conditions	Typ.	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current	V_{DD} = Max., All Input Clocks = LOW[2] Outputs enabled	—	240	mA
I_{TOT}	Total Power V_{DD} Supply Current	V_{DD} = 2.7V., $F_{REFERENCE\ CLOCK}$ = 1GHz	—	250	mA
I_{PD}	Total Power Down Supply Current	$\overline{PD}$ = LOW	—	5	mA

NOTES:

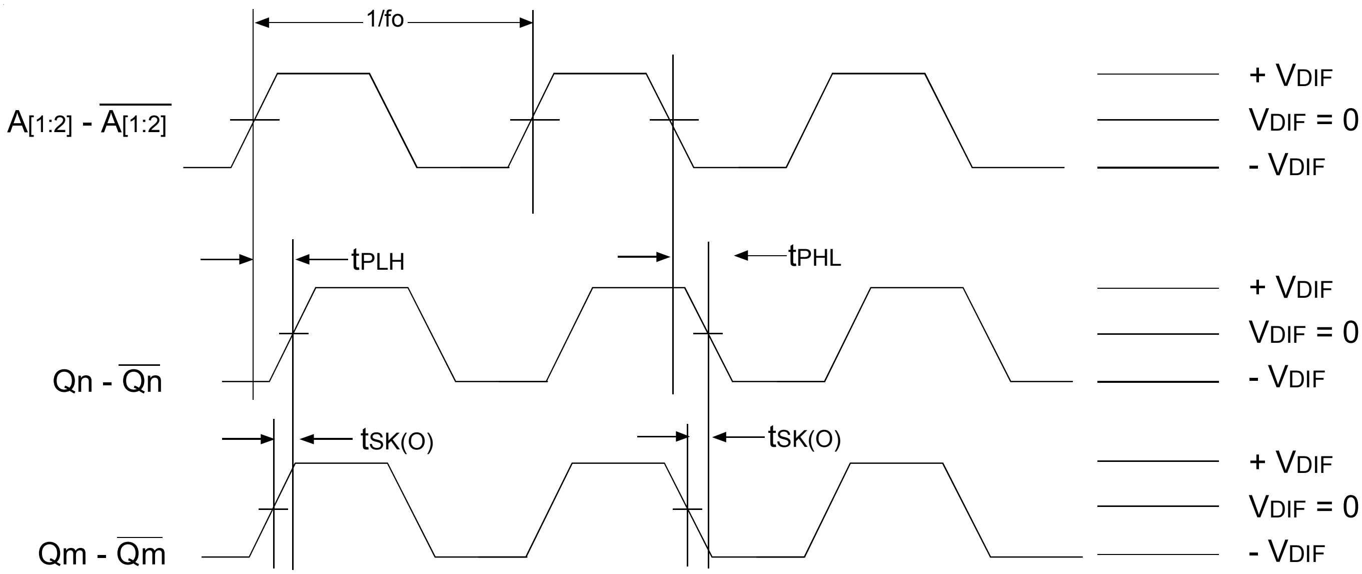
1. These power consumption characteristics are for all the valid input interfaces and cover the worst case conditions.
2. The true input is held LOW and the complementary input is held HIGH.

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE(1,5)

Symbol	Parameter	Min.	Typ.	Max	Unit
Skew Parameters					
$t_{SK(O)}$	Same Device Output Pin-to-Pin Skew(2)	—	—	40	ps
$t_{SK(P)}$	Pulse Skew(3)	—	—	125	ps
$t_{SK(PP)}$	Part-to-Part Skew(4)	—	—	300	ps
Propagation Delay					
t_{PLH} t_{PHL}	Propagation Delay A, $\overline{A}$ Crosspoint to Qn, $\overline{Qn}$ Crosspoint	—	1.25	1.75	ns
f_O	Frequency Range(6)	—	—	1	GHz
Output Gate Enable/Disable Delay					
t_{PGE}	Output Gate Enable Crossing V_{THI} to Qn/$\overline{Qn}$ Crosspoint	—	—	3.5	ns
t_{PGD}	Output Gate Disable Crossing V_{THI} to Qn/$\overline{Qn}$ Crosspoint Driven to GL Designated Level	—	—	3.5	ns
Power Down Timing					
t_{PWRDN}	$\overline{PD}$ Crossing V_{THI} to Qn = V_{DD}, $\overline{Qn}$ = V_{DD}	—	—	100	µS
t_{PWRUP}	Output Gate Disable Crossing V_{THI} to Qn/$\overline{Qn}$ Driven to GL Designated Level	—	—	100	µS
RMS Additive Phase Jitter					
t_{JIT}	RMS Additive Phase Jitter @ 25MHz (12kHz – 10MHz Integration Range)		0.541		ps
	RMS Additive Phase Jitter @ 125MHz (12kHz – 20MHz Integration Range)		0.159		ps
	RMS Additive Phase Jitter @ 156.25MHz (12kHz – 20MHz Integration Range)		0.185		ps
Output Rise/Fall Time					
t_R/t_F	Output Rise/Fall Time(6), (20% - 80%)	125		600	ps

NOTES:
1. AC propagation measurements should not be taken within the first 100 cycles of startup.
2. Skew measured between crosspoints of all differential output pairs under identical input and output interfaces, transitions and load conditions on any one device.
3. Skew measured is the difference between propagation delay times t_{PHL} and t_{PLH} of any differential output pair under identical input and output interfaces, transitions and load conditions on any one device.
4. Skew measured is the magnitude of the difference in propagation times between any single differential output pair of two devices, given identical transitions and load conditions at identical V_{DD} levels and temperature.
5. All parameters are tested with a 50% input duty cycle.
6. Guaranteed by design but not production tested.

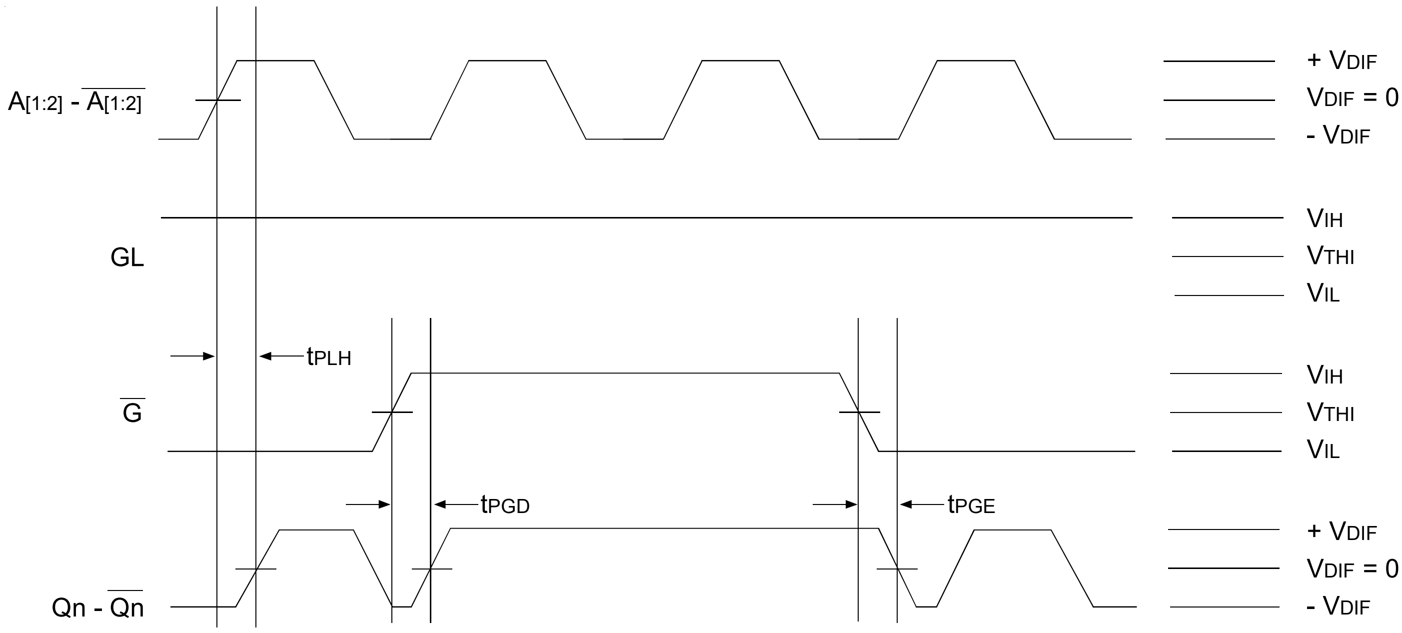
DIFFERENTIAL AC TIMING WAVEFORMS



Output Propagation and Skew Waveforms

NOTES:

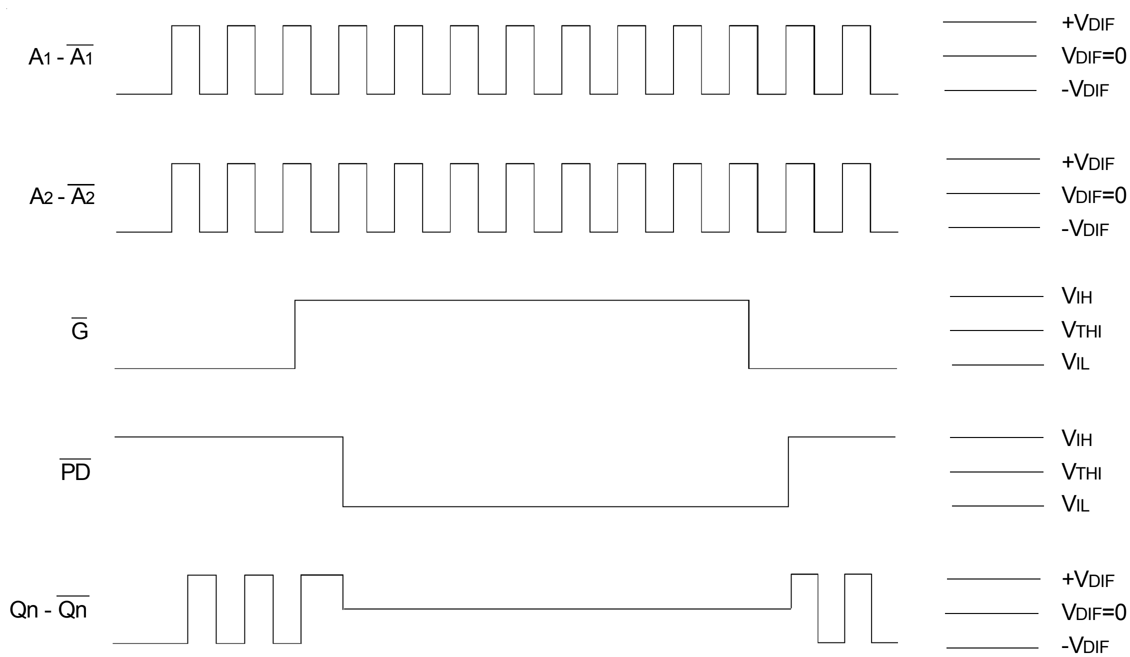
1. Pulse skew is calculated using the following expression:
   $t_{SK(P)} = | t_{PHL} - t_{PLH} |$
   Note that the t_{PHL} and t_{PLH} shown above are not valid measurements for this calculation because they are not taken from the same pulse.
2. AC propagation measurements should not be taken within the first 100 cycles of startup.



Differential Gate Disable/Enable Showing Runt Pulse Generation

NOTE:

1. As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time the $\overline{G}$ signal to avoid this problem.

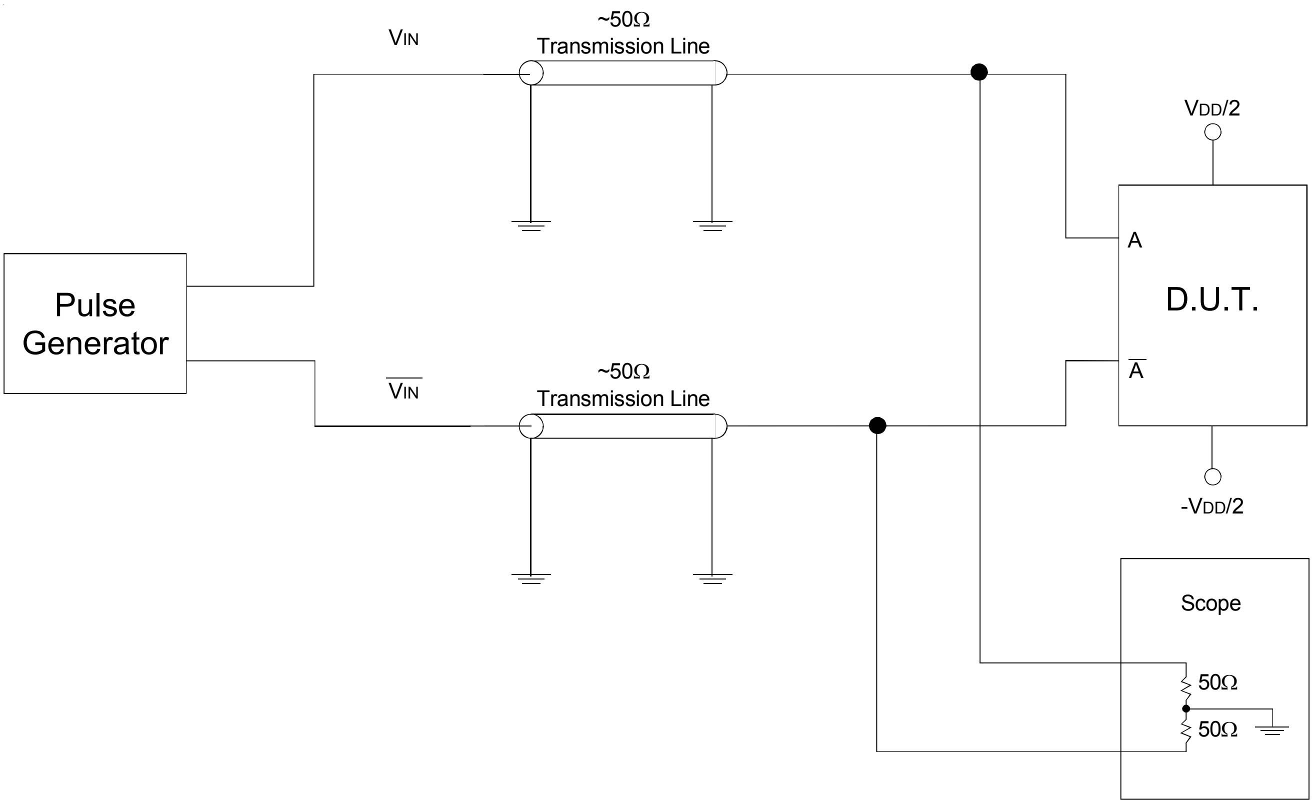


Power Down Timing

NOTES:

1. It is recommended that outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting $\overline{PD}$.
2. The POWER DOWN TIMING diagram assumes that GL is HIGH.
3. It should be noted that during power-down mode, the outputs are both pulled to V_{DD}. In the POWER DOWN TIMING diagram this is shown when Qn-$\overline{Qn}$ goes to $V_{DIF} = 0$.

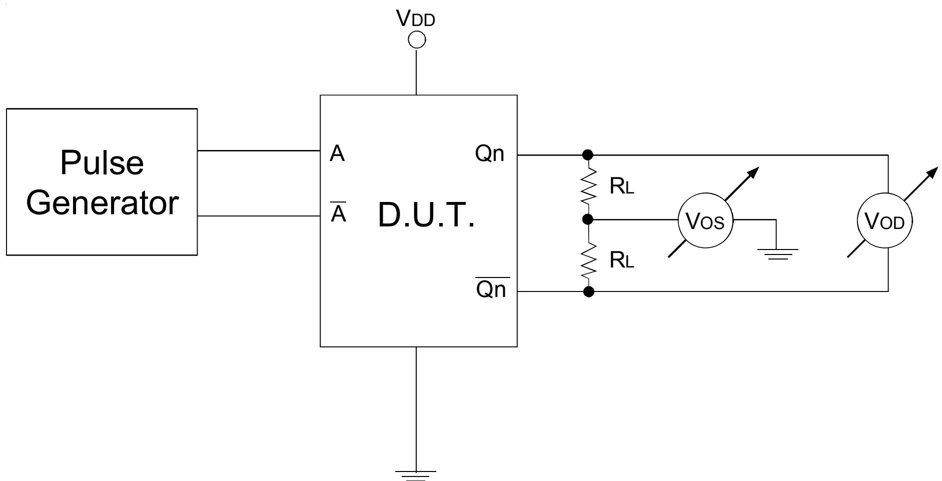
TEST CIRCUITS AND CONDITIONS



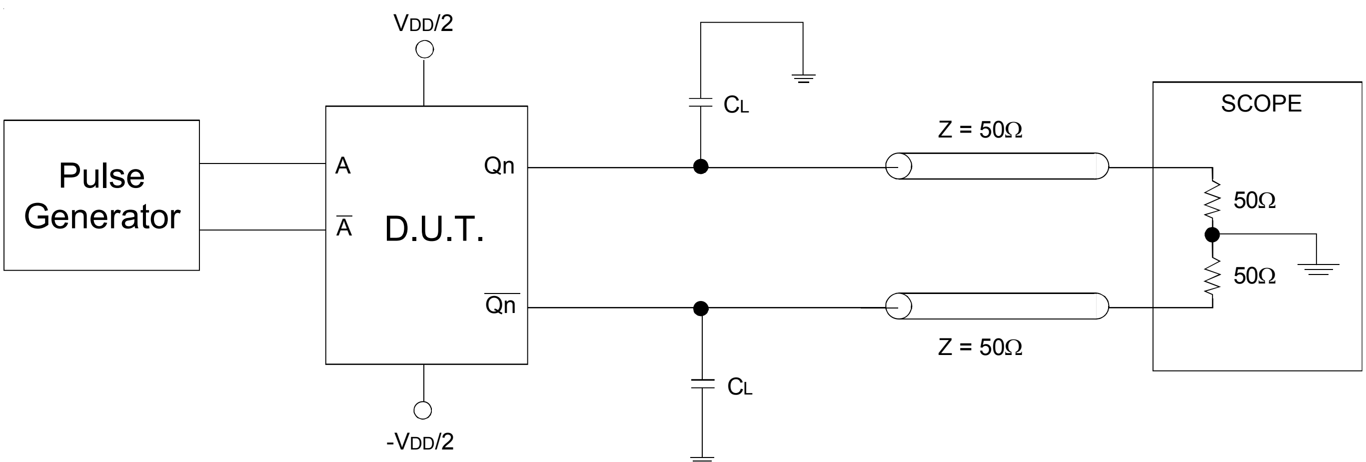
Test Circuit for Differential Input

DIFFERENTIAL INPUT TEST CONDITIONS

Symbol	V_{DD} = 2.5V ± 0.2V	Unit
V_{THI}	Crossing of A and $\overline{A}$	V



Test Circuit for DC Outputs and Power Down Tests



Test Circuit for Propagation, Skew, and Gate Enable/Disable Timing

LVDS OUTPUT TEST CONDITION

Symbol	V_{DD} = 2.5V ± 0.2V	Unit
C_L	0(1)	pF
	8(1,2)	
R_L	50	Ω

NOTES:

1. Specifications only apply to "Normal Operations" test condition. The TIA/EIA specification load is for reference only.
2. The scope inputs are assumed to have a 2pF load to ground. TIA/EIA - 644 specifies 5pF between the output pair. With C_L = 8pF, this gives the test circuit appropriate 5pF equivalent load.

VFQFPN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 1.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/ slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

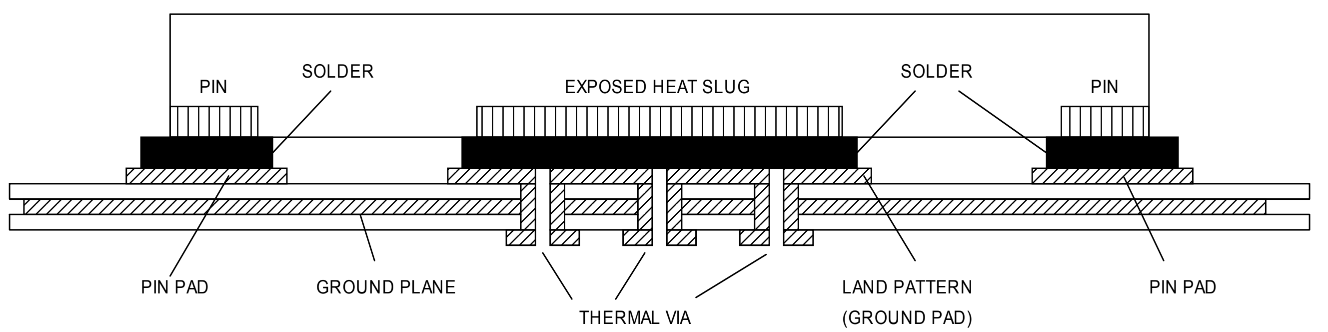


FIGURE 1. P.C.ASSEMBLY FOR EXPOSED PAD THERMAL RELEASE PATH –SIDE VIEW (DRAWING NOT TO SCALE)

SCHEMATIC LAYOUT

Figure 2 shows an example of IDT5T9306 schematic. In this example, the device is operated at V_{DD} = 2.5V. As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

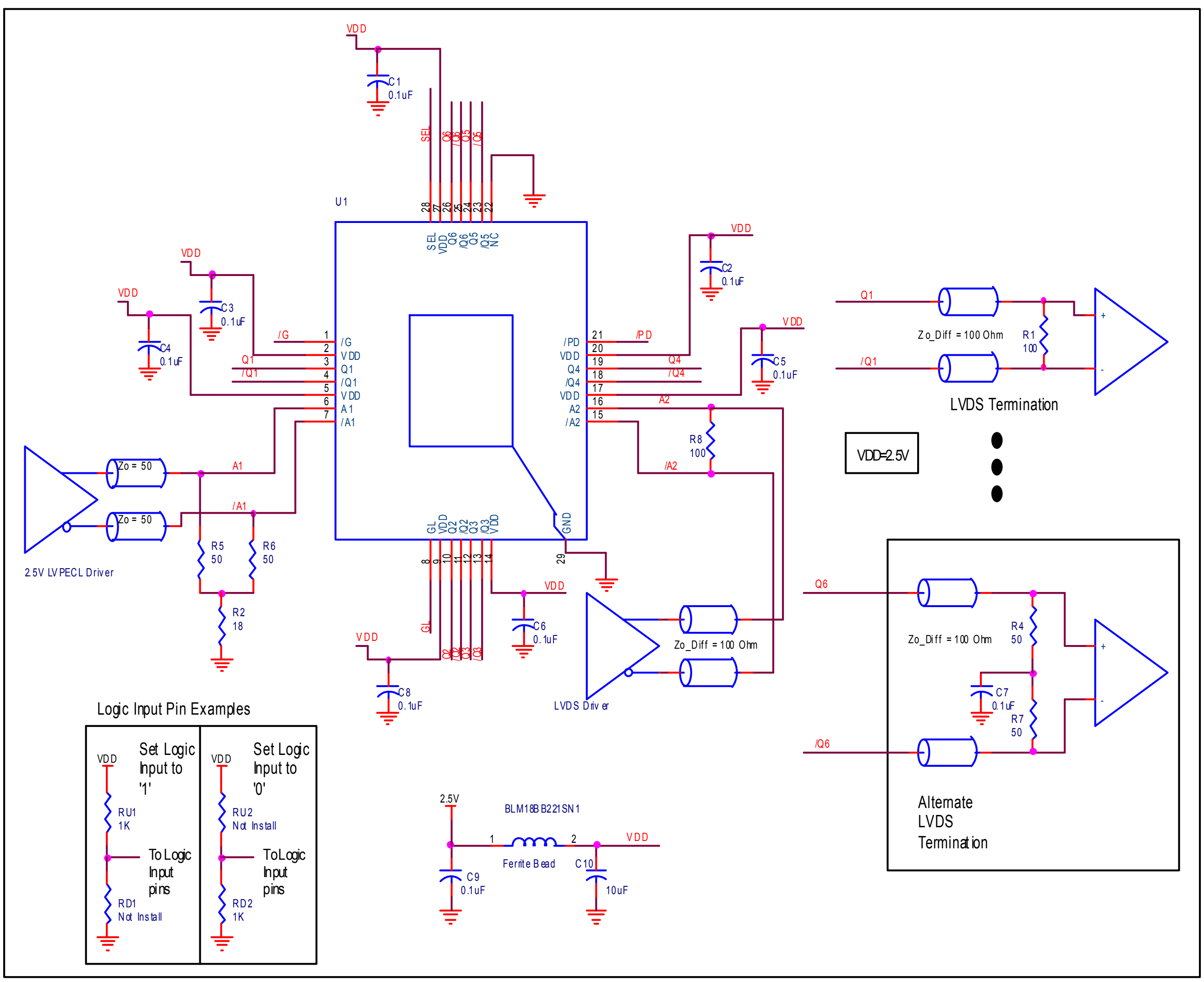
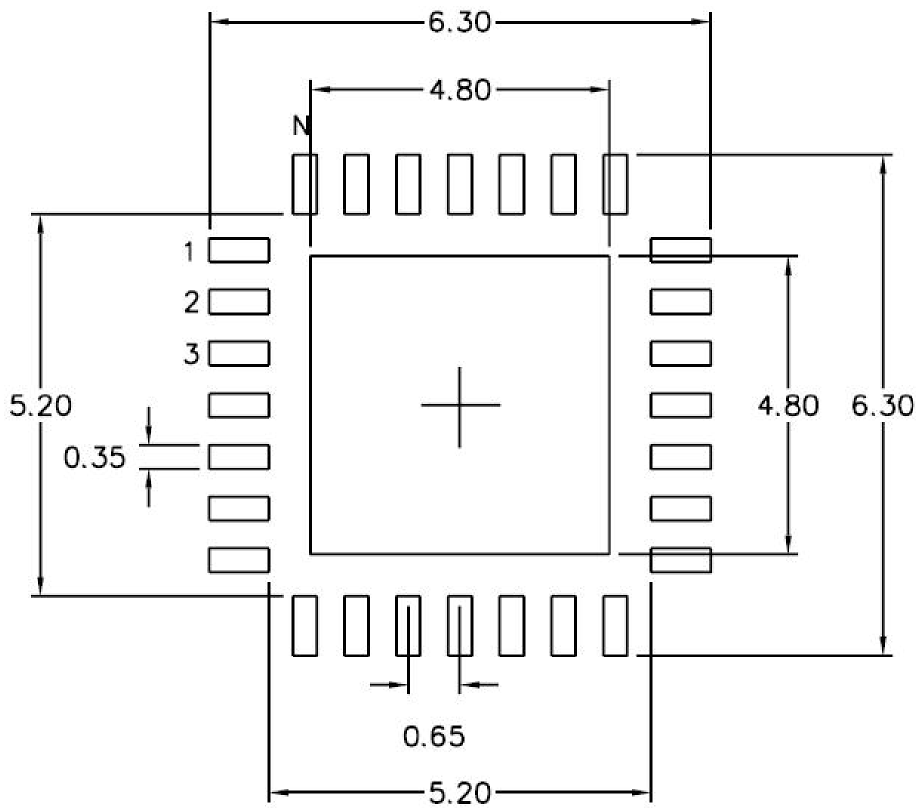


FIGURE 2. IDT5T3906 SCHEMATIC EXAMPLE

RECOMMENDED LANDING PATTERN



NL 28 pin

NOTE: All dimensions are in millimeters.

REVISION HISTORY SHEET

July 23, 2002	Datasheet creation
October 8, 2002	Page 1, entire page changed; page 2, both diagrams; page 3, Pin Description and notes; page 4, DC Cha. for LVPECL and Differential Input tables; page 6, DC Cha. and Power Supply tables; page 7, entire page; page 9, added note 3; page 10, entire page; page 10, entire page; page 11, entire page; page 12, Ordering Info; added 3 new pages (10 thru 12) of diagrams.
October 10, 2002	Page 1, entire page changed; page 2, both diagrams; page 3, Pin Description and notes; page 7, AC Cha. table; page 8, added new LVPECL table; page 10, removed Input Clock Switching diagram; page 11, deleted entire page; page 12, changed Power Down Timing; page 15, Ordering Info.
October 24, 2002	Page 2, added note 1 to TQFP TOP VIEW text; page3, aded note 4 to Pin Description; page 4, replaced "Compliant devices must meet" with the text "This device meets" in four instances; page 5, Differential Input table, note 1, changed 1V to 732mV and replaced "Compliant devices must meet" with the text "This device meets"; page 6, DC Electrical table, Vdif row, changed Min. value to 0.1, and under Differential Input table replaced "Compliant devices must meet" with the text "This device meets" page 7, Power Supply table, replaced ((TBD)) with 800MHz, and under AC Electrical table, replaced ((TBD)) with 500; page 8, completely altered AC DIfferential table; page 12, LVDS Output table, replaced ((TBD)) with 3.
November 1, 2002	Radical changes to entire document.
December 12, 2002	Radical changes to entire document, using 5T9316 as a base.
December 16, 2002	Throughout document, removed "Differential" from title; page 7, Power Supply table, changed Max values, changed $F_{REFERENCE}$ value; page 10, note 1, changed $\overline{G}$x to $\overline{G}$.
May 8, 2003	Page 2, corrected pinout diagram.
August 7, 2003	Page 1, Features text, 3rd bullet, changed 2ns to 1.75ns, 4th bullet, changed 800MHz to 1GHz, and 7th bullet, added CML, on Description, 3rd line, added CML to list; page 4, Pin Descr., note 1, added "Differential CML levels", for Description of PD row, replaced 2nd sentence with "Both 'true' and 'complementary' output will pull to Vdd"; page 5, DC... for Differential Inputs table, removed note 5 and changed Vcm Max. from 3.5 to Vdd; page 7, Power Supply table, changed 800MHz to 1GHz; page 8, AC Differential table, changed Vix and Vcm Max specs from 3.5V to Vdd, removed notes 4 and 5, and placed entire table on page 7, for AC Elect. table, added notes 5 and 6, changed ((TBD)) to 300ps, tplh Type to 1.25ns, and Max from 2ns to 1.75ns, and changed fo Max from 800MHz to 1GHz.
October 2, 2003	Page 1, Features, 7th bullet, added "3.3V / 2,5V LVTTL" to front, Description, added to 1st paragraph "A single-ended 3.3V / 2.5V LVTTL input can also be used to translate to LVDS outputs."; page 4, Pin Description table, added large block of text to 2nd row, added "Single-ended 3.3V and 2.5V LVTTL levels" to note 1; page 5, DC for LVTTL table, added Vref row and note 3, for DC for LVDS table, changed Ios ratings from 5 Typ, 7.5 Max to 12 Typ, 24 Max, and changed Iosd ratings from 5 Typ, 7.5 Max to 6 Typ, 12 Max; page 7, Power Supply table, changed Ipd from 3 to 5.
March 26, 2004	Page 2, changed pin 22 to NC; page 3, changed pin 25 to NC; page 4, added NC row to Pin Description.
June 22, 2004	Removed TQFP package.
October 26, 2004	Inserted a page before Ordering Info and added Landing Pattern.
October 27, 2004	Added note to Landing Pattern.
October 29, 2004	Changed landing pattern diagram.
March 9, 2005	Page 6, switched Iddq and Itot values.
October 23, 2007	Page 7, added Additive Phase Jitter, RMS specs to the AC Electrical Characterisitcs Table.
April 15, 2008	Page 7, added Rise/Fall Time spec. to the AC Electrical Characteristics Table.
January 31, 2011	Page 12, added VFQFPN Thermal Release Path application note. Updated to header/footer to new format.
March 13, 2012	Page 13, added schematic layout. Page 16, corrected ordering information table.
May 30, 2012	Page 1, Features Section - changed Low Skew spec to <40ps (max) from <25ps. Page 7, AC Charastics Table - tsk(o) Max from 25ps to 40ps.
November 29, 2012	Page 16, Removed leaded parts from Ordering Information

ORDERING INFORMATION

IDT XXXXX XX X

Device Type, Package, Package

I	-40ºC to +85ºC (Industrial)
NLG	VFQFPN - Green
5T9306	2.5V 1:6 LVDS Clock Buffer Terrabuffer™ II

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/