20V_{IN}, Dual 5A or Single 10A Step-Down DC/DC µModule Regulator

FEATURES

- **Complete Solution in <1cm^2 (Single-Sided PCB) or 0.5cm^2 (Dual-Sided PCB)**
- Wide Input Voltage Range: 3.1V to 20V
- 0.6V to 5.5V Output Voltage
- Dual 5A or Single 10A Output Current
- ±1.5% Maximum Total Output Voltage Regulation Error Over Load, Line and Temperature
- Current Mode Control, Fast Transient Response
- External Frequency Synchronization
- Multiphase Parallelable with Current Sharing
- Output Voltage Tracking and Soft-Start Capability
- Selectable Burst Mode® Operation
- Overvoltage Input and Overtemperature Protection
- Power Good Indicators
- 6.25mm × 7.5mm × 3.22mm BGA package

APPLICATIONS

- General Purpose Point-of-Load Conversion
- Telecom, Networking and Industrial Equipment
- Medical Diagnostic Equipment
- Test and Debug Systems

DESCRIPTION

The LTM®4705 is a complete dual 5A step-down switching mode µModule® (micromodule) regulator in a tiny 6.25mm × 7.5mm × 3.22mm BGA package. Included in the package are the switching controller, power MOSFETs, inductor and support components. Operating over an input voltage range of 3.1V to 20V, the LTM4705 supports an output voltage range of 0.6V to 5.5V, set by a single external resistor. Its high efficiency design delivers dual 5A continuous output current. Only a few ceramic input and output capacitors are needed.

The LTM4705 supports selectable Burst Mode operation and output voltage tracking for supply rail sequencing. Its high switching frequency and current mode control enable a very fast transient response to line and load changes without sacrificing stability.

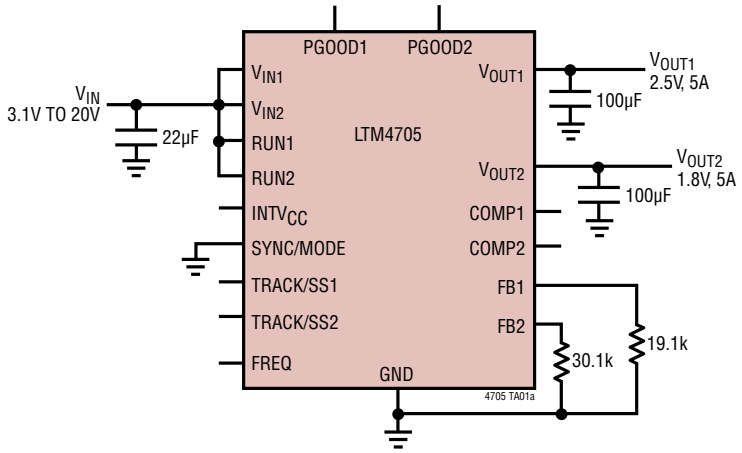
Fault protection features include input overvoltage, output overcurrent and overtemperature protection.

The LTM4705 is available with RoHS compliant terminal finish.

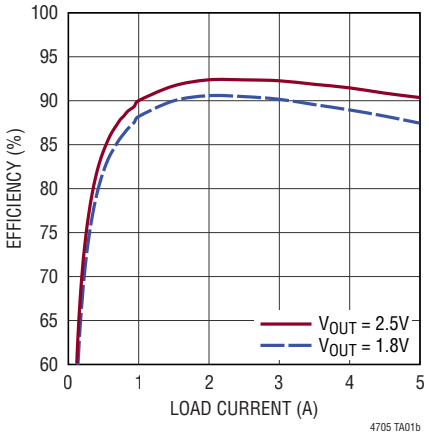
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TYPICAL APPLICATION

2.5V and 1.8V Dual Output DC/DC Step-Down µModule Regulator



12V Input, Efficiency vs Load Current

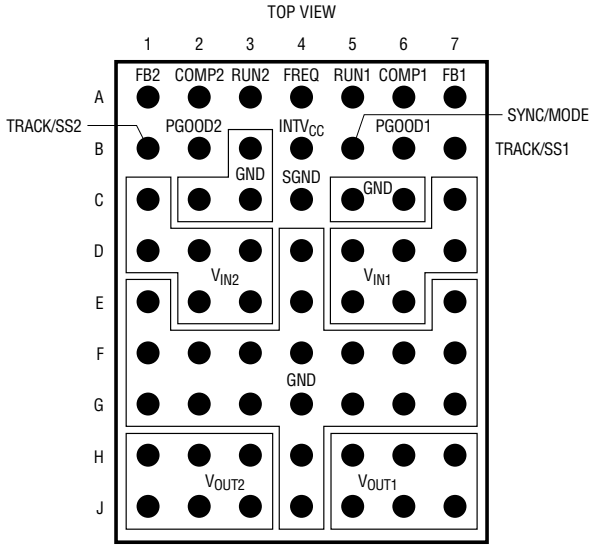


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1}, V_{IN2} ..... –0.3V to 22V
V_{OUT1}, V_{OUT2}, PGOOD1, PGOOD2 ..... –0.3V to 6V
RUN1, RUN2 ..... –0.3V to 22V
$INTV_{CC}$, TRACK/SS1, TRACK/SS2 ..... –0.3V to 3.6V
SYNC/MODE, COMP1, COMP2,
FB1, FB2, ... –0.3V to $INTV_{CC}$
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 250°C

PIN CONFIGURATION



BGA PACKAGE
63-PIN (6.25mm × 7.5mm × 3.22mm)
T_{JMAX} = 125°C, θ_{JCtop} = 22°C/W, $\theta_{JCbottom}$ = 4°C/W,
θ_{JA} = 17°C/W, WEIGHT = 0.46g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4705EY#PBF	Au (RoHS)	LTM4705Y	e1	BGA	3	–40°C to 125°C
LTM4705IY#PBF		LTM4705Y				

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range (Note 2), otherwise specifications are at T_A = 25°C (Note 2), V_{IN1} = V_{IN2} = 12V, unless otherwise noted per the typical application shown in Figure 23.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator Section: Per Channel							
V_{IN1}	Input DC Voltage		●	3.1		20	V
V_{IN2}	Input DC Voltage	3.1V < V_{IN1} < 20V	●	1.5		20	V
$V_{OUT(RANGE)}$	Output Voltage Range		●	0.6		5.5	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF, C_{OUT} = 100µF Ceramic, R_{FB} = 40.2k, MODE = $INTV_{CC}$, V_{IN1} = V_{IN2} = 3.1V to 20V, I_{OUT} = 0A to 5A	●	1.477	1.5	1.523	V
V_{RUN}	RUN Pin On Threshold	RUN Threshold Rising RUN Threshold Falling		1.16 0.96	1.27 1	1.35 1.06	V V
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V, MODE = GND V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V, MODE = $INTV_{CC}$, I_{OUT} = 0.5A Shutdown, RUN1 = RUN2 = 0			15 79 75		mA mA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range (Note 2), otherwise specifications are at T_A = 25°C (Note 2), V_{IN1} = V_{IN2} = 12V, unless otherwise noted per the typical application shown in Figure 23.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{S(VIN)}$	Input Supply Current	V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V, I_{OUT} = 5A			0.74		A
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V (Note 3)	●	0		5	A
$\Delta V_{OUT(Line)}/V_{OUT}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN1} = V_{IN2} = 3.1V to 20V, I_{OUT} = 0A	●		0.01	0.1	%/V
$\Delta V_{OUT(Load)}/V_{OUT}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 5A	●		0.2	0.8	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V			8		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.5V			15		mV
t_{START}	Turn-On Time	C_{OUT} = 100µF Ceramic, No Load, TRACK/SS = 0.01µF, V_{IN} = 12V, V_{OUT} = 1.5V			5		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 25% to 0% of Full Load, C_{OUT} = 100µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V			30		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 25% to 0% of Full Load, C_{OUT} = 100µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V			70		µs
I_{OUTPK}	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.5V		6			A
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.592	0.6	0.608	V
I_{FB}	Current at V_{FB} Pin	(Note 4)				±30	nA
R_{FBHI}	Resistor Between V_{OUT} and V_{FB} Pins			60	60.4	60.8	kΩ
UVLO	V_{IN} Undervoltage Lockout	V_{IN} Falling Hysteresis		2.2	2.4 0.5	2.6	V V
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V			1.4		µA
t_{ss}	Internal Soft-Start Time	10% to 90% Rise Time (Note 4)			1000		µs
$t_{ON(MIN)}$	Minimum On-Time	(Note 4)			30		ns
$t_{OFF(MIN)}$	Minimum Off-Time	(Note 4)			100		ns
V_{PGOOD}	PGOOD Trip Level	V_{FB} with Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive		 –10	 –8 8	 –5 10	 % %
R_{PGOOD}	PGOOD Pull-Down Resistance	10mA Load			25		Ω
V_{INTVCC}	Internal V_{CC} Voltage	V_{IN1} = V_{IN2} = 3.6V to 20V		3.1	3.3	3.5	V
V_{INTVCC} Load Reg	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA			1.3		%
FREQ	Default Switching Frequency				1		MHz
$V_{SYNC/MODE}$	SYNC/MODE High Threshold SYNC/MODE Low Threshold	MODE V_{IH} MODE V_{IL}		1		 0.3	V V
I_{MODE}	SYNC/MODE Input Current	MODE = 0V MODE = $INTV_{CC}$			1.5 –1.5		µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4705 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4705E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4705I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

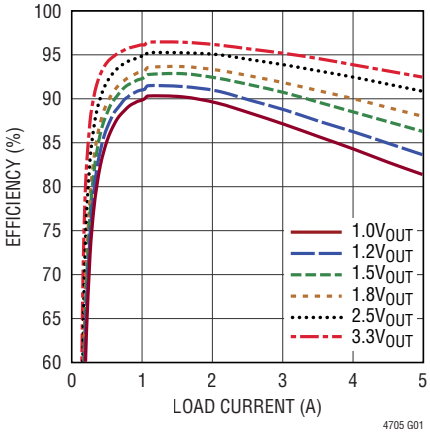
Note 3: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

Note 4: 100% tested at wafer level.

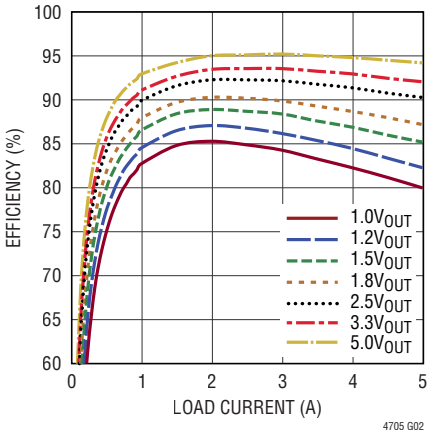
Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

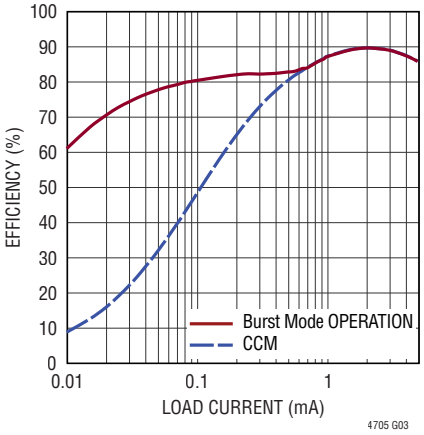
Efficiency vs Load Current from $5V_{IN}$



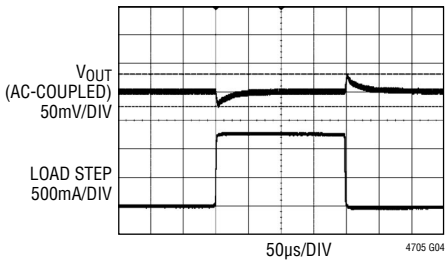
Efficiency vs Load Current from $12V_{IN}$



Burst Mode Efficiency, $12V_{IN}$, $1.5V_{OUT}$

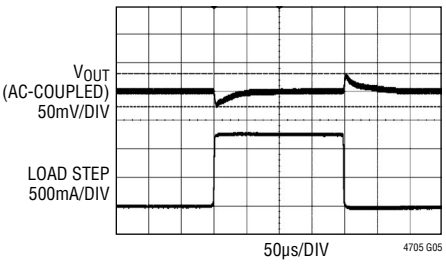


1.0V Output Transient Response



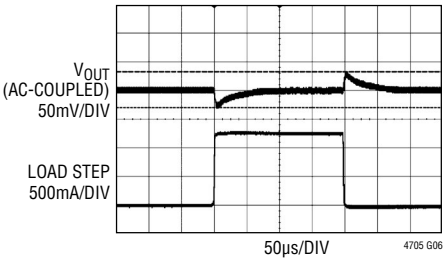
V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF
1.25A (25%) LOAD STEP, 1A/µs

1.2V Output Transient Response



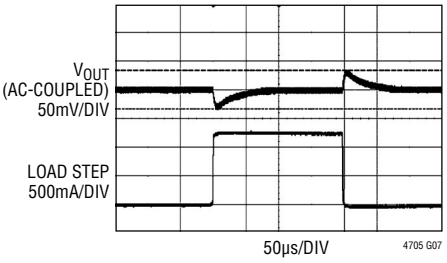
V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF
1.25A (25%) LOAD STEP, 1A/µs

1.5V Output Transient Response



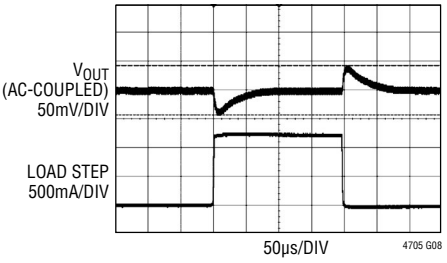
V_{IN} = 12V, V_{OUT} = 1.5V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF
1.25A (25%) LOAD STEP, 1A/µs

1.8V Output Transient Response



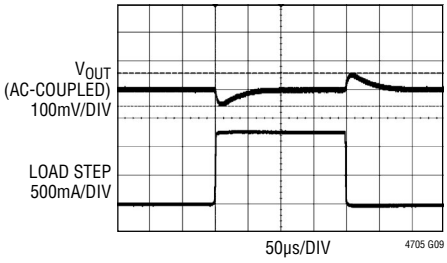
V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF
1.25A (25%) LOAD STEP, 1A/µs

2.5V Output Transient Response



V_{IN} = 12V, V_{OUT} = 2.5V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF
1.25A (25%) LOAD STEP, 1A/µs

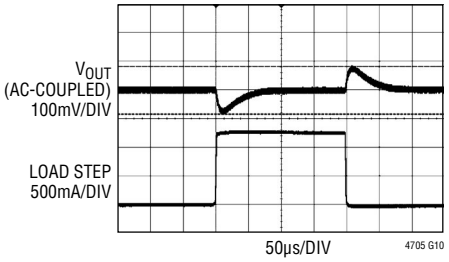
3.3V Output Transient Response



V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF
1.25A (25%) LOAD STEP, 1A/µs

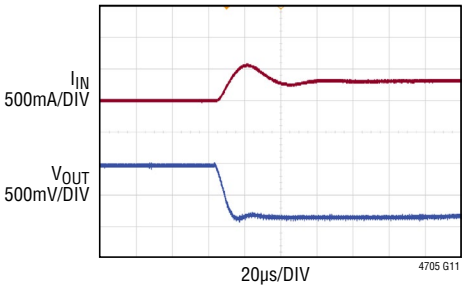
TYPICAL PERFORMANCE CHARACTERISTICS

5V Output Transient Response



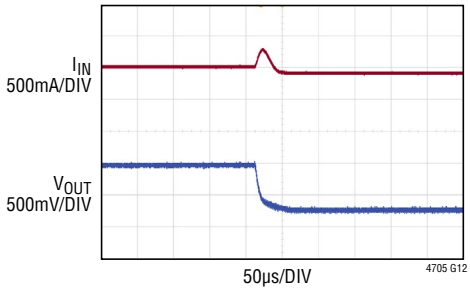
V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF
1.25A (25%) LOAD STEP, 1A/µs

Short-Circuit with No Load Current



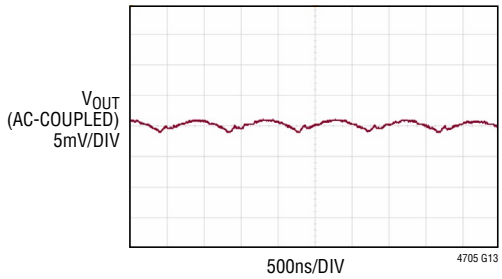
V_{IN} = 12V, V_{OUT} = 1.0V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF

Short-Circuit with 5A Load Current



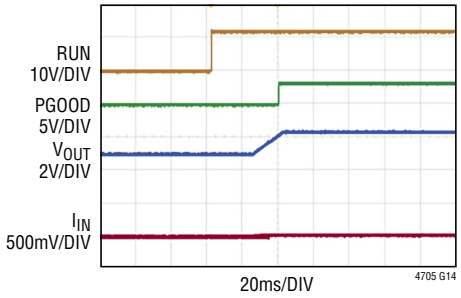
V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF

Steady-State Output Voltage Ripple



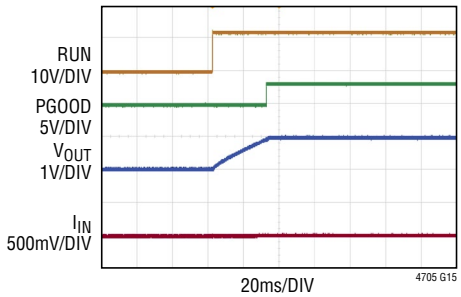
V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF

Start-Up into Pre-Biased Output



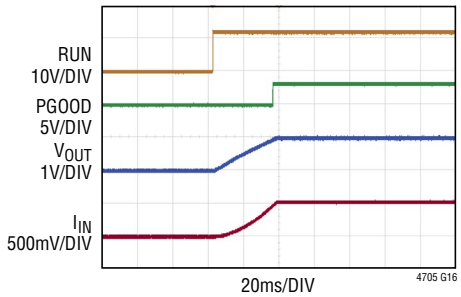
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1MHz,
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF

Start-Up with No Load Current



V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 1MHz,
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF

Start-Up with 5A Load Current



V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 1MHz,
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

FREQ (A4): Frequency is set internally to 1MHz. An external resistor can be placed from this pin to GND to increase frequency, or from this pin to $INTV_{CC}$ to reduce frequency. See the Applications Information section for frequency adjustment.

RUN1 (A5), RUN2 (A3): Run Control Input of Each Switching Mode Regulator Channel. Enables chip operation by tying RUN above 1.27V. Tying this pin below 1V shuts down the specific regulator channel. Do not float this pin.

COMP1 (A6), COMP2 (A2): Current Control Threshold and Error Amplifier Compensation Point of each Switching Mode Regulator Channel. The current comparator's trip threshold is linearly proportional to this voltage, whose normal range is from 0.3V to 1.8V. Tie the COMP pins together for parallel operation. The device is internally compensated.

FB1 (A7), FB2 (A1): The Negative Input of the Error Amplifier for Each Switching Mode Regulator Channel. Internally, this pin is connected to V_{OUT} with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between FB and GND pins. In PolyPhase operation, tying the FB pins together allows for parallel operation. See the Applications Information section for details.

GND (B3, C2, C3, C5, C6, D4, E1, E4, E7, F1 - F7, G1 - G7, H4, J4): Power Ground Pins for Both Input and Output Returns.

$INTV_{CC}$ (B4): Internal 3.3V Regulator Output of the Switching Mode Regulator Channel. The internal power drivers and control circuits are powered from this voltage. This pin is internally decoupled to GND with a 2.2µF low ESR ceramic capacitor. No additional external decoupling capacitor is needed.

SYNC/MODE (B5): Mode Select and External Synchronization Input. Tie this pin to ground to force continuous synchronous operation at all output loads. Floating this pin or tying it to $INTV_{CC}$ enables high efficiency Burst Mode operation at light loads. Drive this pin with a clock to synchronize the LTM4705 switching frequency. An internal phase-locked loop will force the bottom power N-channel MOSFET's turn on signal to be synchronized with the rising edge of the clock signal. When this pin is driven with a clock, forced continuous mode is automatically selected.

PGOOD1 (B6), PGOOD2 (B2): Output Power Good with Open-Drain Logic of Each Switching Mode Regulator Channel. PGOOD is pulled to ground when the voltage on the FB pin is not within ±8% (typical) of the internal 0.6V reference.

TRACK/SS1 (B7), TRACK/SS2 (B1): Output Tracking and Soft-Start Pin of Each Switching Mode Regulator Channel. It allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 1.4µA pull-up current from $INTV_{CC}$ on this pin, so putting a capacitor here provides soft-start function.

SGND (C4): Signal Ground Connection. Tie to GND with minimum distance. Connect COMP component, MODE, TRACK/SS component, FB resistor to this pin as needed.

V_{IN1} (C7, D5 - D7, E5 - E6), V_{IN2} (C1, D1 - D3, E2 - E3): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between BOTH V_{IN1} and V_{IN2} pins and GND pins. Please note the module internal control circuitry is running off V_{IN1}. Channel 2 will not work without a voltage higher than 3.1V present at V_{IN1}.

V_{OUT1} (H5 - H7, J5 - J7), V_{OUT2} (H1 - H3, J1 - J3): Power Output Pins of Each Switching Mode Regulator. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

BLOCK DIAGRAM

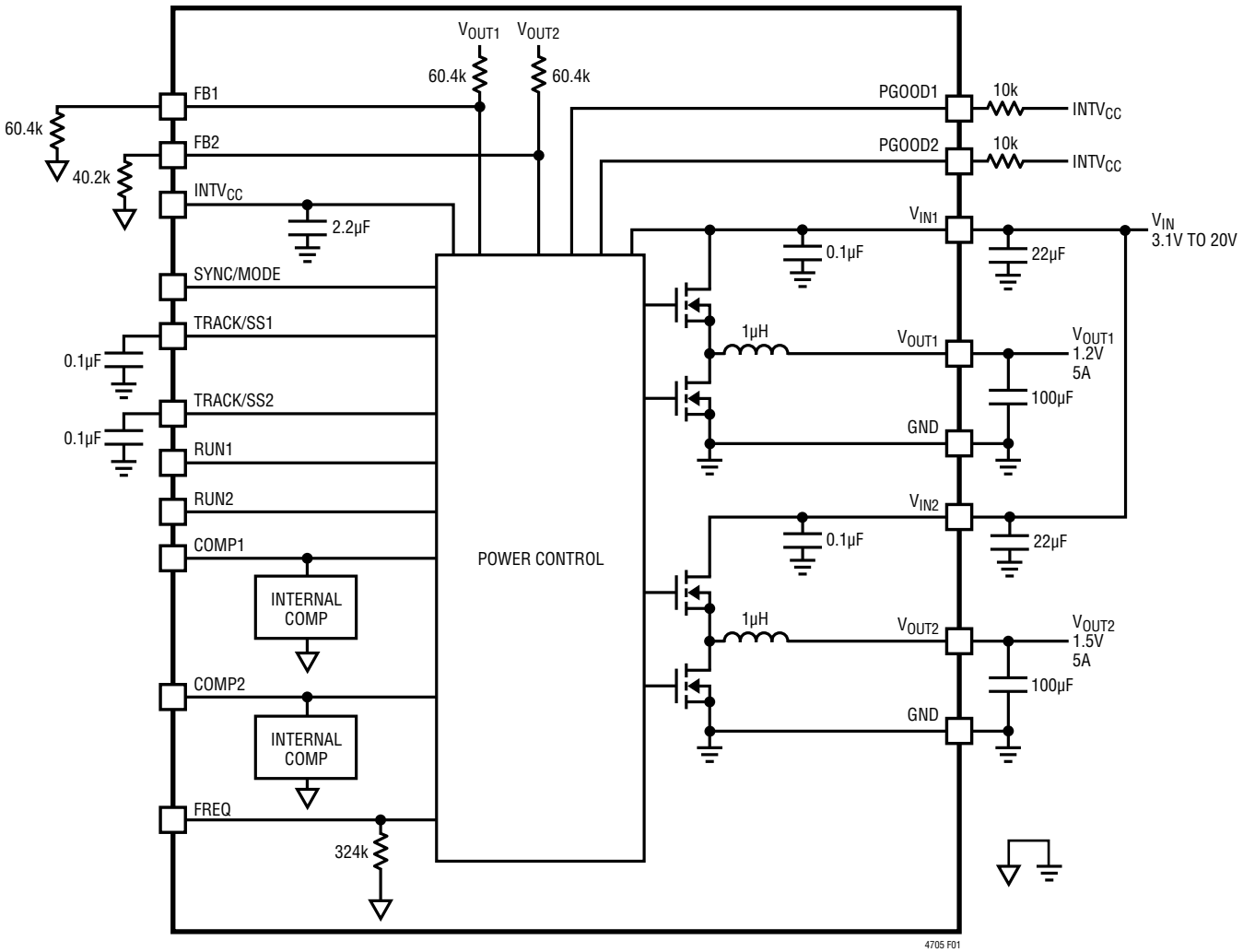


Figure 1. Simplified LTM4705 Block Diagram

DECOUPLING REQUIREMENTS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 3.1V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 5A	10	22		µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 3.1V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 5A	47	100		µF

OPERATION

The LTM4705 is a dual output standalone nonisolated switch mode DC/DC power supply. It can deliver two 5A DC outputs with few external input and output ceramic capacitors. This module provides dual precisely regulated output voltages programmable via two external resistors from 0.6V to 5.5V over 3.1V to 20V input voltage range. Both channels share the same clock and run 180° out of phase. The typical application schematic is shown in Figure 23.

The LTM4705 contains an integrated controlled on-time valley current mode regulator, power MOSFETs, inductor and other supporting discrete components. The default switching frequency is 1MHz. For output voltages between 2.5V and 5V, an external resistor is required between FREQ and GND pins to set the operating frequency to higher frequency to optimize inductor current ripple. For switching noise-sensitive applications, the µModule can be externally synchronized to a clock. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4705 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limiting. An internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±8% window around the regulation point. Furthermore, the input overvoltage protection will be activated by shutting down both power MOSFETs when V_{IN} rises above 22.5V to protect internal devices.

Multiphase operation can be easily employed by connecting the SYNC pin to an external oscillator. Multiple LTM4705s can be paralleled to run simultaneously with good current sharing guaranteed by the current mode control loop.

Pulling the RUN pin below 1V forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load currents, burst mode operation can be enabled to achieve higher efficiency compared to continuous current mode (CCM) by setting MODE pin to $INTV_{CC}$. The TRACK/SS pin is used for power supply tracking and soft-start programming. See the Applications Information section.

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The typical LTM4705 application circuit is shown in Figure 23. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current. Refer to Table 8 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step down ratio that can be achieved for a given input voltage due to the minimum off-time and minimum on-time limits of the regulator. The minimum off-time limit imposes a maximum duty cycle which can be calculated by Equation 1.

$$D_{MAX} = 1 - t_{OFF(MIN)} \bullet f_{SW} \quad (1)$$

where $t_{OFF(MIN)}$ is the minimum off-time, 100ns typical for LTM4705, and f_{SW} is the switching frequency. Conversely the minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated by Equation 2.

$$D_{MIN} = t_{ON(MIN)} \bullet f_{SW} \quad (2)$$

where $t_{ON(MIN)}$ is the minimum on-time, 30ns typical for LTM4705. In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. Note that additional thermal derating may be applied. See the Thermal Considerations and Output Current Derating section in this data sheet.

Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4k 0.5% internal feedback resistor connects V_{OUT} and FB pins together.

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Adding a resistor R_{FB} from FB pin to GND programs the output voltage (Equation 3).

$$R_{FB} = \frac{0.6V}{V_{OUT} - 0.6V} \bullet 60.4k \quad (3)$$

Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT} (V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3	5.0
R_{FB} (k)	OPEN	90.9	60.4	40.2	30.1	19.1	13.3	8.25

For parallel operation of N-channels LTM4705, Equation 4 can be used to solve for R_{FB}:

$$R_{FB} = \frac{0.6V}{V_{OUT} - 0.6V} \bullet \frac{60.4k}{N} \quad (4)$$

Input Decoupling Capacitors

The LTM4705 module should be connected to a low AC-impedance DC source. For each regulator channel, one piece 10µF input ceramic capacitor is required for RMS ripple current decoupling. A bulk input capacitor is only needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capacitor and/or polymer capacitor.

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated using Equation 5.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)} \quad (5)$$

where is the estimated efficiency of the power module.

Output Decoupling Capacitors

With an optimized high frequency, high bandwidth design, only a single piece of 47µF low ESR output ceramic capacitor is required for each LTM4705 output to achieve low output voltage ripple and very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 8 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 2.5A (50%) load step transient. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance will be more a function of stability and transient response. The Analog Devices LTpowerCAD® Design Tool is available to download online for output ripple, stability and transient response analysis and calculating the output ripple reduction as the number of phases implemented increases by N times.

Burst Mode Operation

In applications where high efficiency at intermediate current is preferred over lower output voltage ripple, Burst Mode operation could be used by connecting SYNC/MODE pin to $INTV_{CC}$ to improve light load efficiency. In Burst Mode operation, a current reversal comparator (I_{REV}) detects the negative inductor current and shuts off the bottom power MOSFET, resulting in discontinuous operation and increased efficiency. Both power MOSFETs will remain off and the output capacitor will supply the load current until the COMP voltage rises above the zero current level to initiate another cycle.

Forced Continuous Current Mode (CCM) Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the SYNC/MODE pin to GND. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4705's output voltage is in regulation.

Operating Frequency

The operating frequency of the LTM4705 is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency. The default operating frequency is internally set to 1MHz. In most applications, no additional frequency adjusting is required.

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If any operating frequency other than 1MHz is required by application, the operating frequency can be increased by adding a resistor, R_{FSET}, between the FREQ pin and GND, as shown in Figure 26. The operating frequency can be calculated by Equation 6.

$$f(Hz) = \frac{3.2e11}{324k \,||\, R_{FSET}(\Omega)} \quad (6)$$

To reduce switching current ripple, 1.5MHz to 2.5MHz operating frequency can be used for 2.5V to 5V output with R_{FSET} to GND.

Table 2.

V_{OUT}	0.6V TO 1.8V	2.5V	3.3V	5V
f_{SW}	1MHz	1.5MHz	2MHz	2.5MHz
R_{FSET}	Open	649kΩ	324kΩ	215kΩ

The operating frequency can also be decreased by adding a resistor between the FREQ pin and $INTV_{CC}$, calculated as:

$$f(Hz) = 1\,MHz - \frac{5.67e11}{R_{FSET}(\Omega)} \quad (7)$$

The programmable operating frequency range is from 800kHz to 3MHz.

Frequency Synchronization

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows the internal bottom MOSFET turn-on to be locked to the rising edge of the external clock. The synchronization frequency range for the LTM4705 is 700kHz to 3MHz. A pulse detection circuit is used to detect a clock on the SYNC/MODE pin to turn on the phase locked loop. The pulse width of the clock has to be at least 100ns. The clock high level must be above 1V and clock low level below 0.3V. The presence of an external clock will place both regulator channels into forced continuous mode operation. During the start-up of the regulator, the phase-locked loop function is disabled.

Multiphase Operation

For output loads that demand more than 5A of current, two outputs in the LTM4705 or even multiple LTM4705s can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripples.

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design.

The two switching mode regulator channels inside the LTM4705 are internally set to operate 180° out of phase. Multiple LTM4705s could easily operate 90 degrees, 60 degrees or 45 degrees shift which corresponds to 4-phase, 6-phase or 8-phase operation by letting SYNC/MODE of the LTM4705 synchronize to an external multiphase oscillator like LTC6902. Figure 2 shows a 4-phase design example for clock phasing.

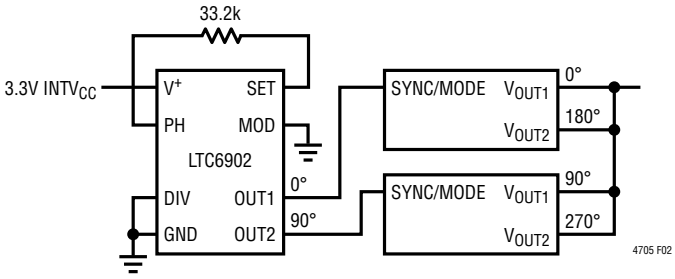


Figure 2. Example of Clock Phasing for 4-Phase Operation with LTC6902

The LTM4705 is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Please tie RUN, TRACK/SS, FB and COMP pin of each paralleling channel together. Figure 24 shows an example of parallel operation and pin connection.

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INPUT RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 3 shows this graph.

Soft-Start and Output Voltage Tracking

The TRACK/SS pin provides a means to either soft-start the regulator or track it to a different power supply. A capacitor on the TRACK/SS pin will program the ramp rate of the output voltage. An internal 1.4µA current source will charge up the external soft-start capacitor towards $INTV_{CC}$ voltage. When the TRACK/SS voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage. The total soft-start time can be calculated by Equation 8.

$$t_{SS} = 0.6 \bullet \frac{C_{SS}}{1.4\mu A} \quad (8)$$

where C_{SS} is the capacitance on the TRACK/SS pin. Current foldback and force continuous mode are disabled during the soft-start process.

Output voltage tracking can also be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. Figure 4 and Figure 5 show an example waveform and schematic of a Ratiometric tracking where the slave regulator's output slew rate is proportional to the master's.

Since the slave regulator's TRACK/SS is connected to the master's output through a $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider and its voltage used to regulate the slave output voltage when TRACK/SS voltage is below 0.6V, the slave output voltage and the master output voltage should satisfy Equation 9 during the start-up.

$$V_{OUT(SL)} \bullet \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = V_{OUT(MA)} \bullet \frac{R_{TR(TOP)}}{R_{TR(TOP)} + R_{TR(BOT)}} \quad (9)$$

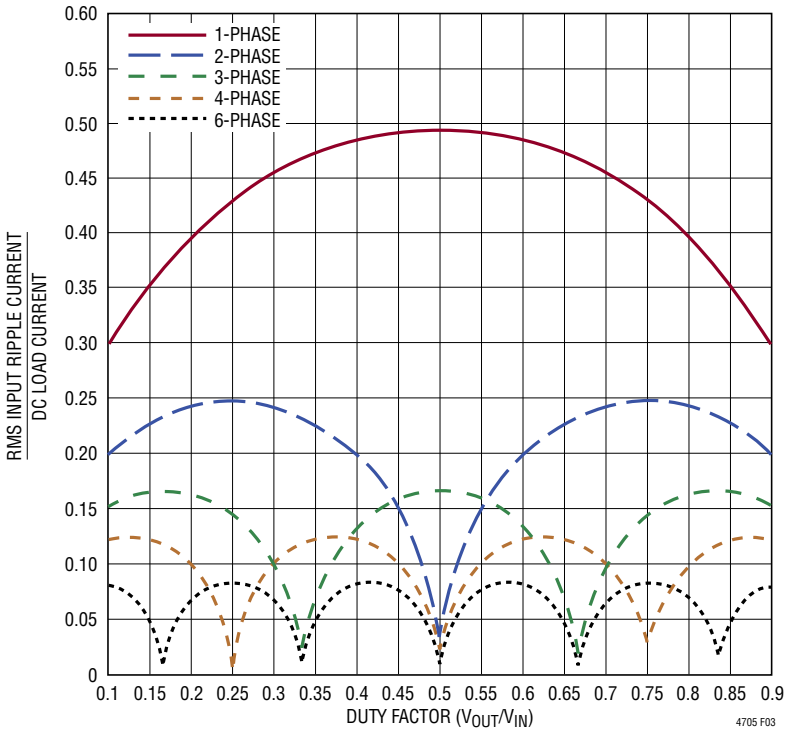


Figure 3. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

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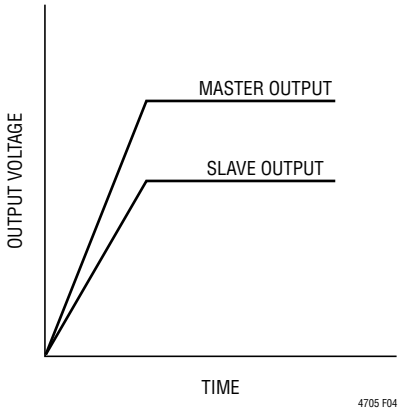


Figure 4. Output Ratiometric Tracking Waveform

The $R_{FB(SL)}$ is the feedback resistor and the $R_{TR(TOP)}$/$R_{TR(BOT)}$ is the resistor divider on the TRACK/SS pin of the slave regulator, as shown in Figure 5.

Following Equation 9, the master's output slew rate (MR) and the slave's output slew rate (SR) in Volts/Time is determined by Equation 10.

$$\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}} \quad (10)$$

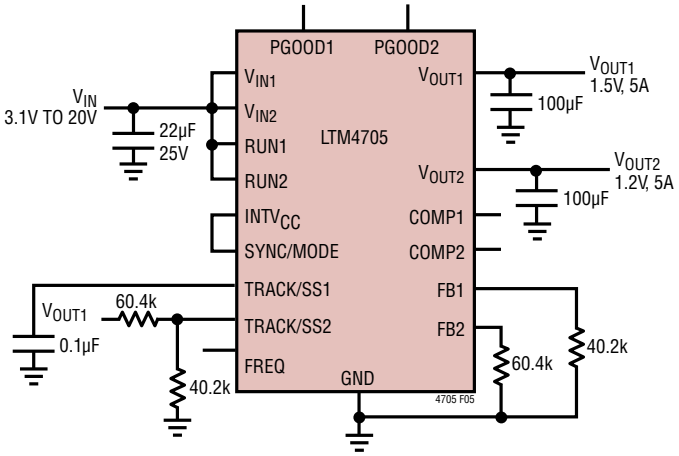


Figure 5. Example Schematic of Ratiometric Output Voltage Tracking

For example, $V_{OUT(MA)}$ = 1.5V, MR = 1.5V/1ms and $V_{OUT(SL)}$ = 1.2V, SR = 1.2V/1ms as shown in Figure 5. From the equation, we could solve out that $R_{TR(TOP)}$ = 60.4k and $R_{TR(BOT)}$ = 40.2k is a good combination for the Ratiometric tracking.

The TRACK pins will have the 1.5µA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK pin input. Smaller value resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK pin offset to a negligible value.

The Coincident output tracking can be recognized as a special Ratiometric output tracking which the master's output slew rate (MR) is the same as the slave's output slew rate (SR), as waveform shown in Figure 6.

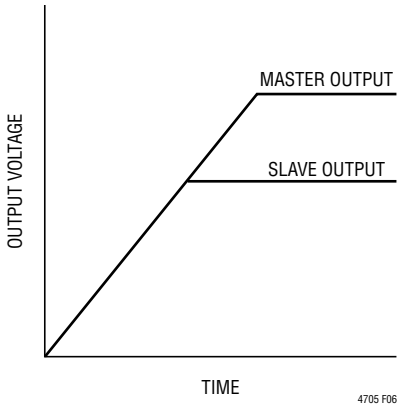


Figure 6. Output Coincident Tracking Waveform

From Equation 10, we could easily find out that, in the Coincident tracking, the slave regulator's TRACK/SS pin resistor divider is always the same as its feedback divider (Equation 11).

$$\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}} \quad (11)$$

For example, $R_{TR(TOP)}$ = 60.4k and $R_{TR(BOT)}$ = 60.4k is a good combination for Coincident tracking for $V_{OUT(MA)}$ = 1.5V and $V_{OUT(SL)}$ = 1.2V application.

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Power Good

The PGOOD pins are open drain pins that can be used to monitor valid output voltage regulation. This pin monitors a ±8% window around the regulation point. A resistor can be pulled up to a particular supply voltage for monitoring. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTM4705's PGOOD falling edge includes a blanking delay of approximately 40µs.

Stability compensation

The LTM4705 module internal compensation loop is designed and optimized for low ESR ceramic output capacitors only applications. Please note that for applications that need to achieve high bandwidth control loop compensation with enough phase margin, a feed forward capacitor between 33pF – 100pF is recommended from V_{OUT} to V_{FB} pin. Table 8 is provided for most application requirements. The LTpowerCAD Design Tool is available to download online for control loop optimization.

RUN Enable

Pulling the RUN pin to ground forces the LTM4705 into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Tying the RUN pin voltage above 1.27V will turn on the entire chip.

Pre-Biased Output Start-Up

There may be situations that require the power supply to start up with a pre-bias on the output capacitors. In this case, it is desirable to start up without discharging that output pre-bias. The LTM4705 can safely power up into a pre-biased output without discharging it.

The LTM4705 accomplishes this by forcing discontinuous mode (DCM) operation until the TRACK/SS pin voltage reaches 0.6V reference voltage. This will prevent the bottom MOSFET from turning on during the pre-biased output start-up which would discharge the output.

Overtemperature Protection

The internal overtemperature protection monitors the junction temperature of the module. If the junction temperature reaches approximately 160°C, both power switches will be turned off until the temperature drops about 15°C cooler.

Input Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LTM4705 constantly monitors each V_{IN} pin for an overvoltage condition. When V_{IN} rises above 22.5V, the regulator suspends operation by shutting off both power MOSFETs on the corresponding channel. Once V_{IN} drops below 21.5V, the regulator immediately resumes normal operation. The regulator executes its soft-start function when exiting an overvoltage condition.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The motivation for providing these thermal coefficients in found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in and of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application usage, and can be adapted to correlate thermal performance to one's own application.

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The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 7; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSED51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same

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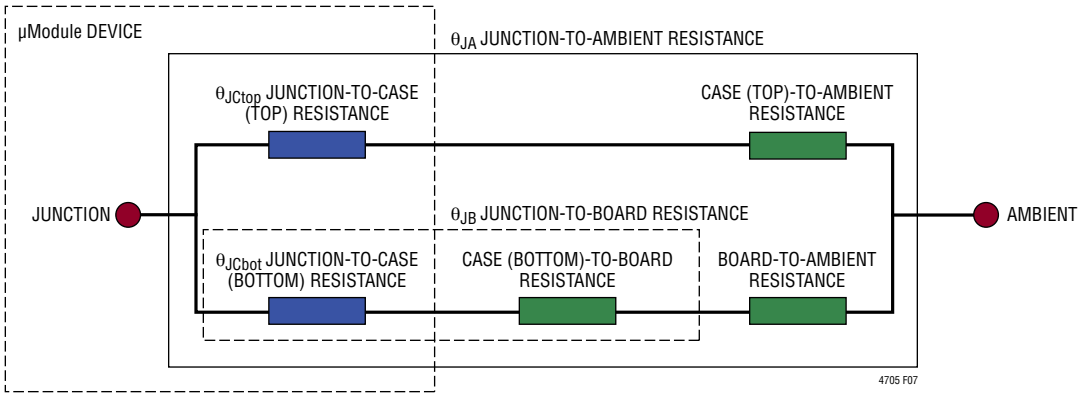


Figure 7. Graphical Representation of JESD51-12 Thermal Coefficients

power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory test have been performed and correlated to the µModule model, then the θ_{JB} and θ_{BA} are summed together to correlate quite well with the µModule model with no airflow or heat sinking in a properly define chamber. This $\theta_{JB} + \theta_{BA}$ value is shown in the Pin Configuration section and should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The 1.0V, 1.5V, 2.5V, 3.3V and 5V power loss curves in Figure 8 to Figure 12 can be used in coordination with the load current derating curves in Figure 13 to Figure 21 for calculating an approximate θ_{JA} thermal resistance for the LTM4705 with no heat sinking and various airflow conditions. The power loss curves are taken at room temperature, and are increased with multiplicative factors of 1.35 assuming junction temperature at 120°C. The derating curves are plotted with the output current starting at 10A and the ambient temperature at 40°C. These output voltages are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 15 the load current is derated to ~4A at ~110°C with no air or heat sink and the power loss for the 5V to 1.5V at 10A output is about 0.6W. The 0.6W loss is calculated with the ~0.5W room temperature loss from the 5V to 1.5V power loss curve at 10A, and the 1.2 multiplying factor at 110°C ambient. If the 110°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 10°C divided by 0.6W equals a 16.7°C/W θ_{JA} thermal resistance. Table 3 specifies a 17°C/W value which is very close. Table 3 to Table 7 provide equivalent thermal resistances for 1.0V, 1.5V, 2.5V, 3.3V and 5V outputs with and without airflow. The derived thermal resistances in Table 3 to Table 7 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one

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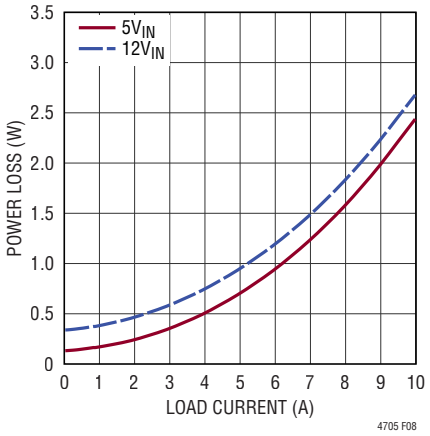


Figure 8. 1.0V Output Power Loss

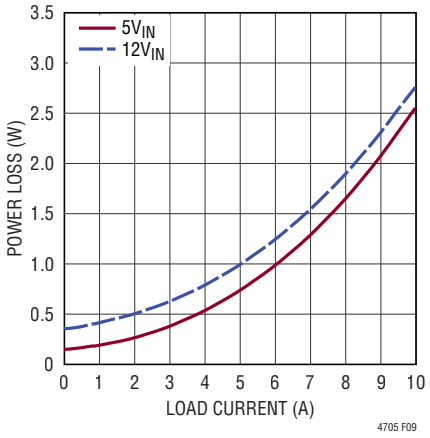


Figure 9. 1.5V Output Power Loss

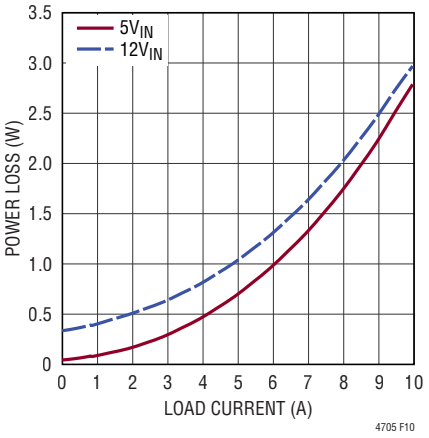


Figure 10. 2.5V Output Power Loss

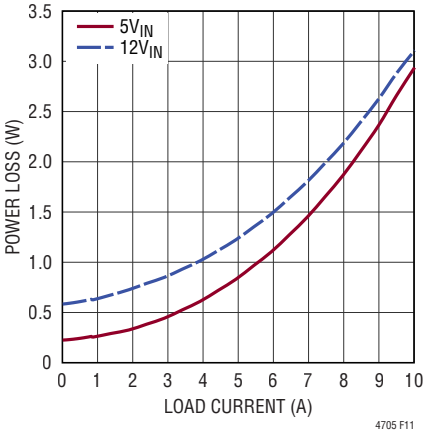


Figure 11. 3.3V Output Power Loss

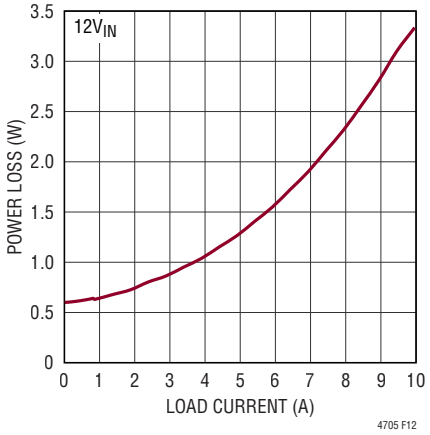


Figure 12. 5V Output Power Loss

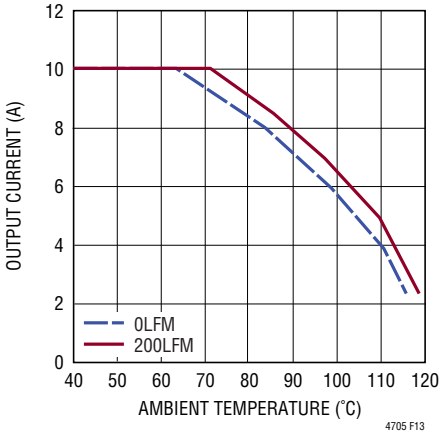


Figure 13. 5V to 1.0V Derating Curve, No Heat Sink

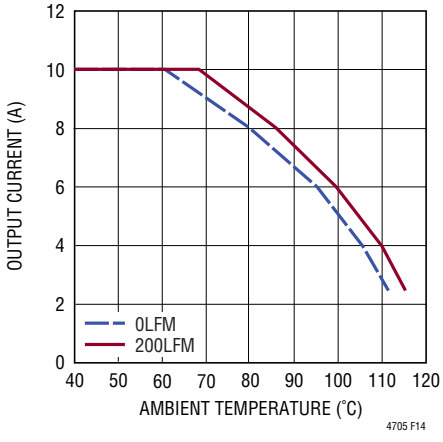


Figure 14. 12V to 1.0V Derating Curve, No Heat Sink

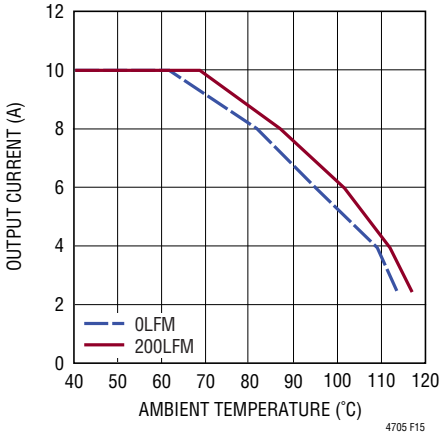


Figure 15. 5V to 1.5V Derating Curve, No Heat Sink

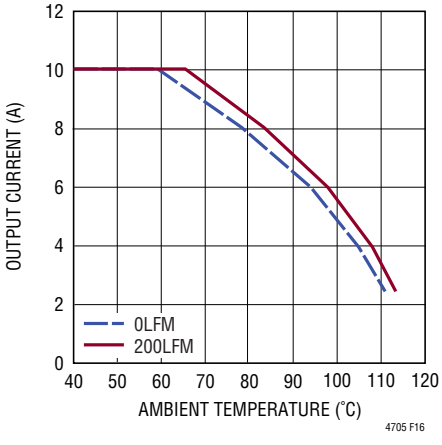


Figure 16. 12V to 1.5V Derating Curve, No Heat Sink

APPLICATIONS INFORMATION

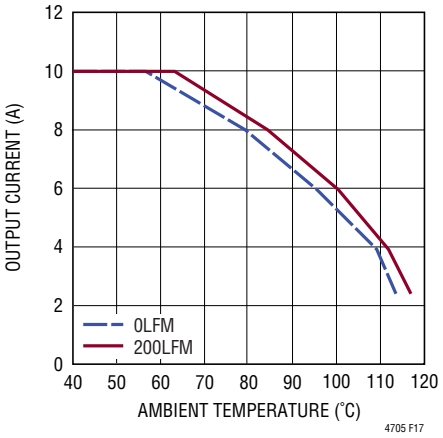


Figure 17. 5V to 2.5V Derating Curve, No Heat Sink

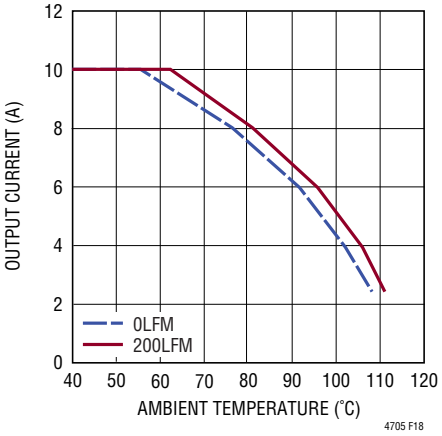


Figure 18. 12V to 2.5V Derating Curve, No Heat Sink

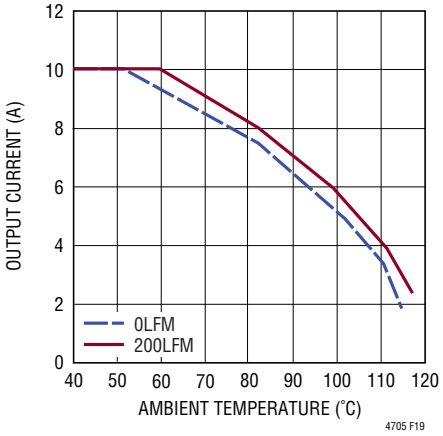


Figure 19. 5V to 3.3V Derating Curve, No Heat Sink

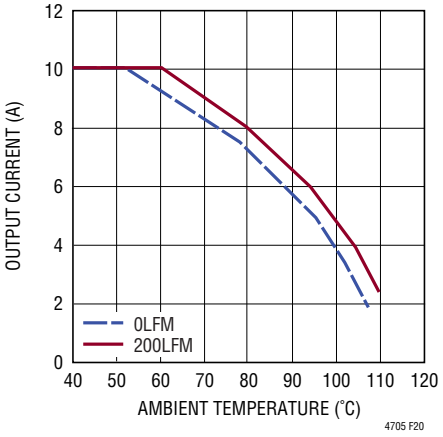


Figure 20. 12V to 3.3V Derating Curve, No Heat Sink

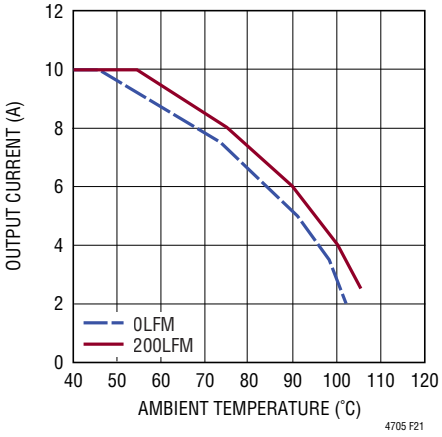


Figure 21. 12V to 5V Derating Curve, No Heat Sink

Table 3. 1V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA}(°C/W)
Figure 13, Figure 14	5, 12	Figure 8	0	None	17
Figure 13, Figure 14	5, 12	Figure 8	200	None	14

Table 4. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA}(°C/W)
Figure 15, Figure 16	5, 12	Figure 9	0	None	17
Figure 15, Figure 16	5, 12	Figure 9	200	None	14

APPLICATIONS INFORMATION

Table 5. 2.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	$\theta_{JA(°C/W)}$
Figure 17, Figure 18	5, 12	Figure 10	0	None	17
Figure 17, Figure 18	5, 12	Figure 10	200	None	14

Table 6. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	$\theta_{JA(°C/W)}$
Figure 19, Figure 20	5, 12	Figure 11	0	None	17
Figure 19, Figure 20	5, 12	Figure 11	200	None	14

Table 7. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	$\theta_{JA(°C/W)}$
Figure 21	12	Figure 12	0	None	17
Figure 21	12	Figure 12	200	None	14

Table 8. Output Voltage Response for Each Regulator Channel vs Component Matrix (Refer to Figure 23)
1.25A Load Step Typical Measured Values

V_{OUT} (V)	C_{IN} (CERAMIC) (µF)	C_{OUT1} (CERAMIC) (µF)	C_{FF} (pF)	V_{IN} (V)	P-P DERIVATION (mV)	RECOVERY TIME (µS)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µS)	R_{FB} (kΩ)
1	22	100	100	5, 12	60	50	1.25	1	90.9
1.2	22	100	100	5, 12	60	50	1.25	1	60.4
1.5	22	100	100	5, 12	60	50	1.25	1	40.2
1.8	22	100	100	5, 12	60	50	1.25	1	30.1
2.5	22	100	100	5, 12	68	50	1.25	1	19.1
3.3	22	100	100	5, 12	90	50	1.25	1	13.3
5	22	100	100	12	133	50	1.25	1	8.25

APPLICATIONS INFORMATION

ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm.

Safety Considerations

The LTM4705 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and overcurrent protection.

Layout Checklist/Example

The high integration of LTM4705 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND, V_{OUT1} and V_{OUT2}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the V_{OUT}, V_{FB}, and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 22 gives a good example of the recommended layout.

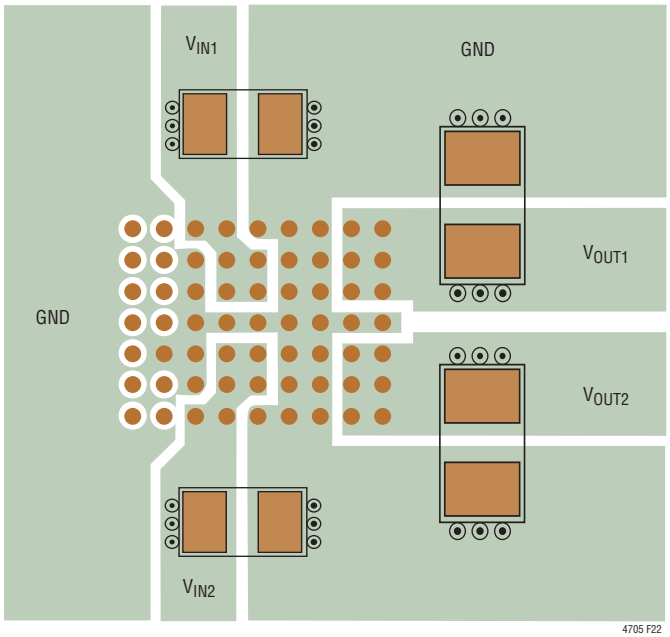


Figure 22. Recommended PCB Layout

TYPICAL APPLICATIONS

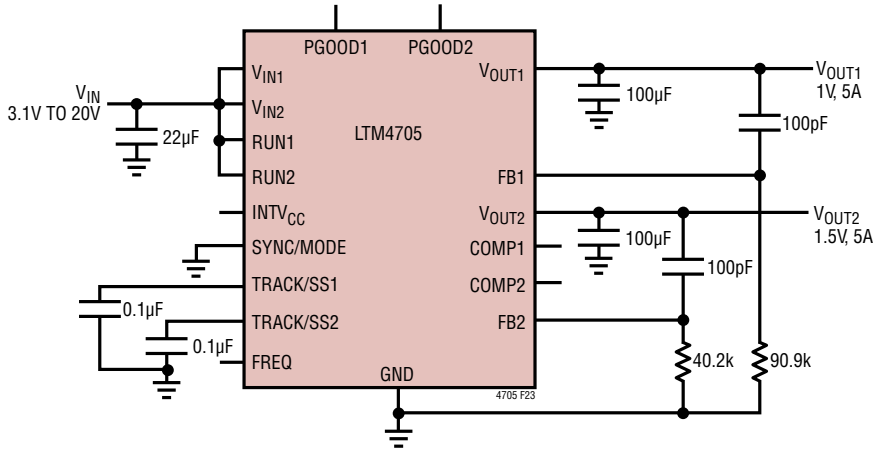


Figure 23. 3.1V_{IN} to 20V_{IN}, 1V and 1.5V Output at 5A Design

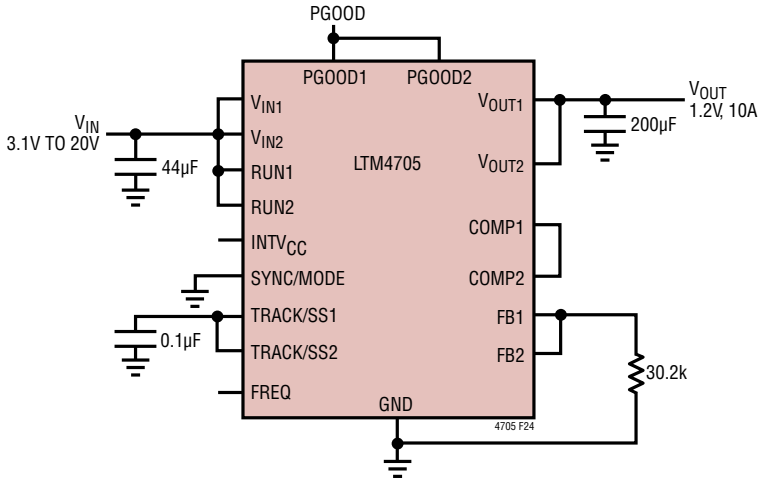


Figure 24. 3.1V_{IN} to 20V_{IN}, 1.2V Two Phase in Parallel 10A Design

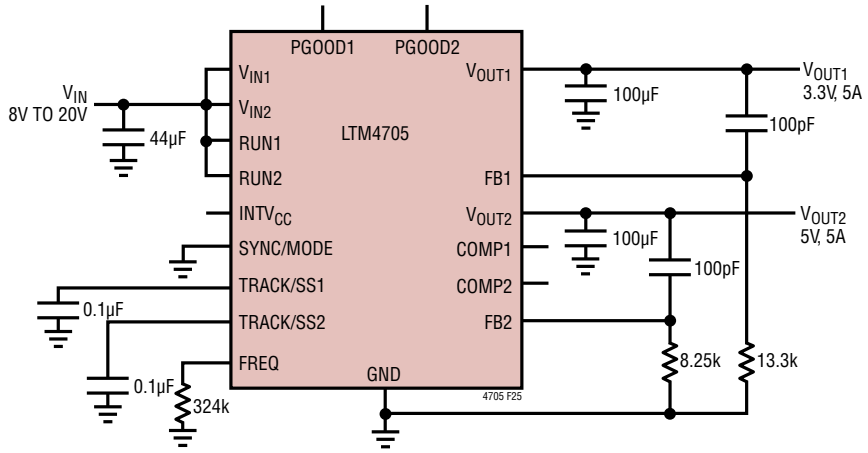


Figure 25. 8V_{IN} to 20V_{IN}, 3.3V and 5V Output at 5A with 2MHz Switching Frequency

TYPICAL APPLICATIONS

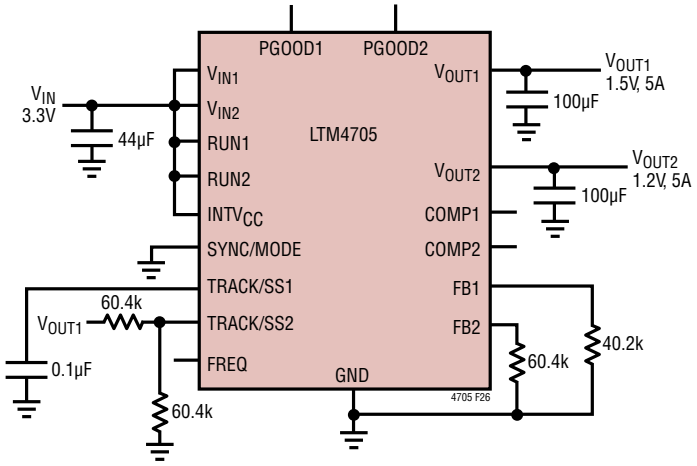


Figure 26. 3.3V_{IN}, 1.5V and 1.2V Output at 5A Design with Output Coincident Tracking

PACKAGE DESCRIPTION

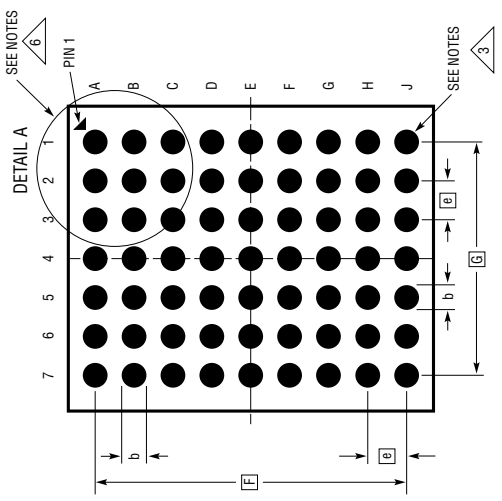
PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

LTM4705 Component BGA Pinout

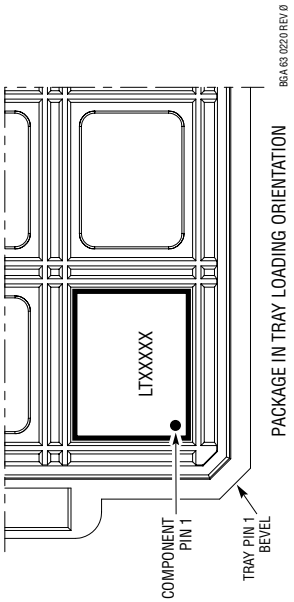
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	FB2	A2	COMP2	A3	RUN2	A4	FREQ	A5	RUN1	A6	COMP1	A7	FB1
B1	TRACK/SS2	B2	PGOOD2	B3	GND	B4	$INTV_{CC}$	B5	SYNC/MODE	B6	PGOOD1	B7	TRACK/SS1
C1	V_{IN2}	C2	GND	C3	GND	C4	SGND	C5	GND	C6	GND	C7	V_{IN1}
D1	V_{IN2}	D2	V_{IN2}	D3	V_{IN2}	D4	GND	D5	V_{IN1}	D6	V_{IN1}	D7	V_{IN1}
E1	GND	E2	V_{IN2}	E3	V_{IN2}	E4	GND	E5	V_{IN1}	E6	V_{IN1}	E7	GND
F1	GND	F2	GND	F3	GND	F4	GND	F5	GND	F6	GND	F7	GND
G1	GND	G2	GND	G3	GND	G4	GND	G5	GND	G6	GND	G7	GND
H1	V_{OUT2}	H2	V_{OUT2}	H3	V_{OUT2}	H4	GND	H5	V_{OUT1}	H6	V_{OUT1}	H7	V_{OUT1}
J1	V_{OUT2}	J2	V_{OUT2}	J3	V_{OUT2}	J4	GND	J5	V_{OUT1}	J6	V_{OUT1}	J7	V_{OUT1}

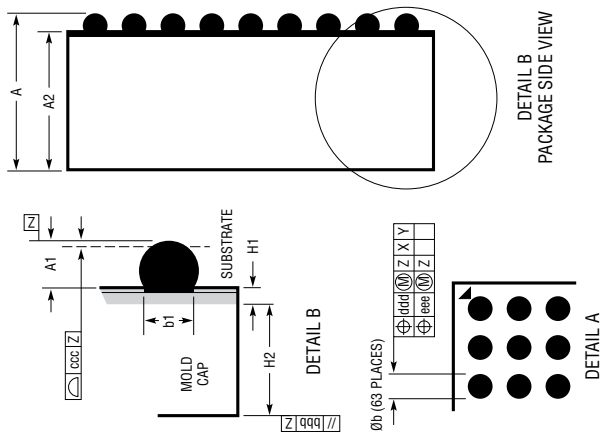
PACKAGE DESCRIPTION

BGA Package
63-Lead (6.25mm × 7.50mm × 3.22mm)
(Reference LTC DWG # 05-08-7023 Rev Ø)

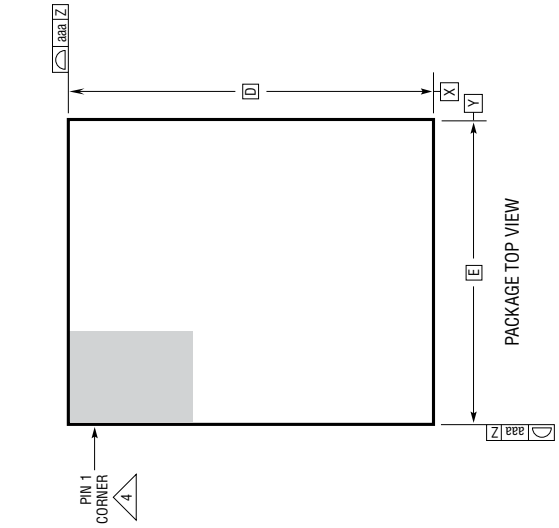


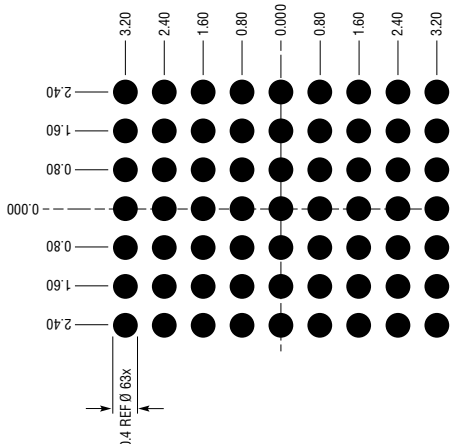
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY





DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	3.03	3.22	3.41	
A1	0.30	0.40	0.50	BALL HT
A2	2.73	2.82	2.91	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		7.50		
E		6.25		
e		0.80		
F		6.40		
G		4.80		
H1		0.32 REF		SUBSTRATE THK
H2		2.50 REF		MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.15	
eee			0.08	





Rev. A

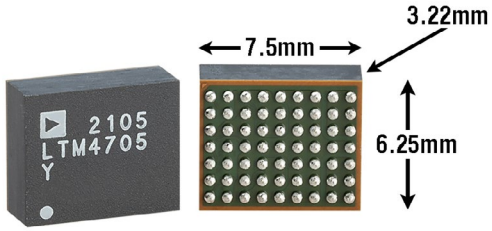
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/22	Changed reflow 260°C to 250°C.	2
		Added the synchronization frequency range for the LTM4705: 700kHz to 3MHz.	10
		Changed load step to 1.25A and load step slew rate to 1.	18
		Added ink marking statement to package photos.	24

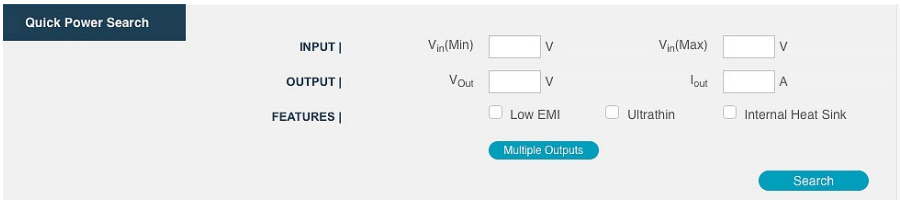
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PACKAGE PHOTOS

Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4622	Dual 2.5A or Single 5A µModule Regulator	$3.6V \le V_{IN} \le 20V$; $0.6V \le V_{OUT} \le 5.5V$; 6.25mm × 6.25mm × 1.82mm LGA, 2.42mm BGA
LTM4668/ LTM4668A	Configurable Quad 1.2A µModule Regulator	$2.7V \le V_{IN} \le 17V$; $0.6V \le V_{OUT} \le 1.8V$ (5.5V for LTM4668A); 6.25mm × 6.25mm × 2.1mm BGA
LTM4643	Configurable Quad 3A µModule Regulator	$4V \le V_{IN} \le 20V$; $0.6V \le V_{OUT} \le 3.3V$; 9mm × 15mm × 1.82mm LGA, 2.42mm BGA
LTM4644	Configurable Quad 4A µModule Regulator	$4V \le V_{IN} \le 14V$; $0.6V \le V_{OUT} \le 5.5V$; 9mm × 15mm × 5.01mm BGA
LTM4657	8A µModule Regulator; Pin Compatible with LTM4626 and LTM4638	$3.1V \le V_{IN} \le 20V$; $0.5V \le V_{OUT} \le 5.5V$; 6.25mm × 6.25mm × 3.87mm BGA
LTM4626	12A µModule Regulator. Pin Compatible with LTM4657 and LTM4638	$3.1V \le V_{IN} \le 20V$; $0.6V \le V_{OUT} \le 5.5V$; 6.25mm × 6.25mm × 3.87mm BGA
LTM4638	15A µModule Regulator; Pin Compatible with LTM4657 and LTM4626	$3.1V \le V_{IN} \le 20V$; $0.6V \le V_{OUT} \le 5.5V$; 6.25mm × 6.25mm × 5.02mm BGA
LTM4691	Dual, Low V_{IN} 2A µModule Regulator	$2.25V \le V_{IN} \le 3.6V$; $0.5V \le V_{OUT} \le 2.5V$; 3mm × 4mm × 1.18mm LGA, 1.48mm BGA
LTM4646	Dual 10A or Single 20A µModule Regulator	$4.5V \le V_{IN} \le 20V$; $0.6V \le V_{OUT} \le 5.5V$; 11.25mm × 15mm × 5.01mm BGA
LTM4662	Dual 15A or Single 30A µModule Regulator	$4.5V \le V_{IN} \le 20V$; $0.6V \le V_{OUT} \le 5.5V$; 11.25mm × 15mm × 5.74mm BGA

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