BTS6110-1SJA

Smart High-Side Power Switch

Data Sheet

Rev. 1.1, 2014-11-24

Automotive Power

Table of Contents

1 Overview . . . 3

2 Block Diagram . . . 4

3 Application Information . . . 4

4 Pin Configuration . . . 5
4.1 Pin Assignment . . . 5
4.2 Pin Definitions and Functions . . . 5
4.3 Voltage and Current Definition . . . 5

5 General Product Characteristics . . . 6
5.1 Absolute Maximum Ratings . . . 6
5.2 Functional Range . . . 7
5.3 Thermal Resistance . . . 7
5.3.1 PCB set up . . . 7
5.3.2 Thermal Resistance . . . 8

6 Power Stage . . . 9
6.1 Output ON-state Resistance . . . 9
6.2 Turn ON/OFF Characteristics with Resistive Load . . . 9
6.3 Frequency Generator . . . 10
6.4 Timing Output . . . 10
6.5 Output Polarization . . . 11
6.6 CAP Pin . . . 13

7 Protection Functions . . . 14
7.1 Overvoltage Protection . . . 14
7.2 Reverse Polarity Protection . . . 14
7.3 Overload Protection . . . 15
7.3.1 Current Limitation . . . 15
7.3.2 Temperature Limitation in the Power DMOS . . . 15

8 Diagnostic Functions . . . 16
8.1 Load Current Measurement . . . 16
8.2 Under load Current . . . 17

9 Electrical Characteristics . . . 18
9.1 Electrical Characteristics Power Stage . . . 18
9.2 Electrical Characteristics CAP pin . . . 19
9.3 Electrical Characteristics for the Protection Functions . . . 20
9.4 Electrical Characteristics Diagnostic Function . . . 21

10 Package Outlines . . . 22

11 Revision History . . . 23

1 Overview

Package	Marking
PG-DSO-8-49	6110-SJA

Application

- Side Indicator 2 x R10W + 1 x R2W

Basic Features

- One channel device
- Very small external reservoir capacitor of 10 µF
- Electrostatic discharge protection (ESD)
- Optimized electromagnetic compatibility
- Green product (RoHS compliant)
- AEC qualified

Protection Functions

- Overtemperature protection with limited restart
- Overvoltage protection without external component

Diagnostic Functions

- Auto-failure detection of a failed main lamp (N-1 diagnosis), signalized by frequency doubling

Description

The BTS6110-1SJA is a single 80 mΩ channel Smart High-Side Power Switch, embedded in a PG-DSO-8-49 package, providing protective functions and diagnosis. It is designed to drive lamps 2 x R10W + 1 x R2W to realize the side indicators function for motorcycle.

Table 1 Product Summary

Parameter	Symbol	Value
Operating voltage range	$V_{S(OP)}$	9 V ... 16 V
Load dump voltage	$V_{S(LD)}$	65 V
Maximum ON state resistance at TJ = 150 °C	$R_{DS(ON)}$	200 mΩ
Flasher Frequency ; normal operation	f_4	85 ± 15 cycles / minute [1]
Flasher Frequency; loss of a main lamp / typical value	f_2	f_4 * 2.24
Minimum current limitation	$I_{L(SC)}$	20 A

1) With external capacitor CEXT = 10µF

2 Block Diagram

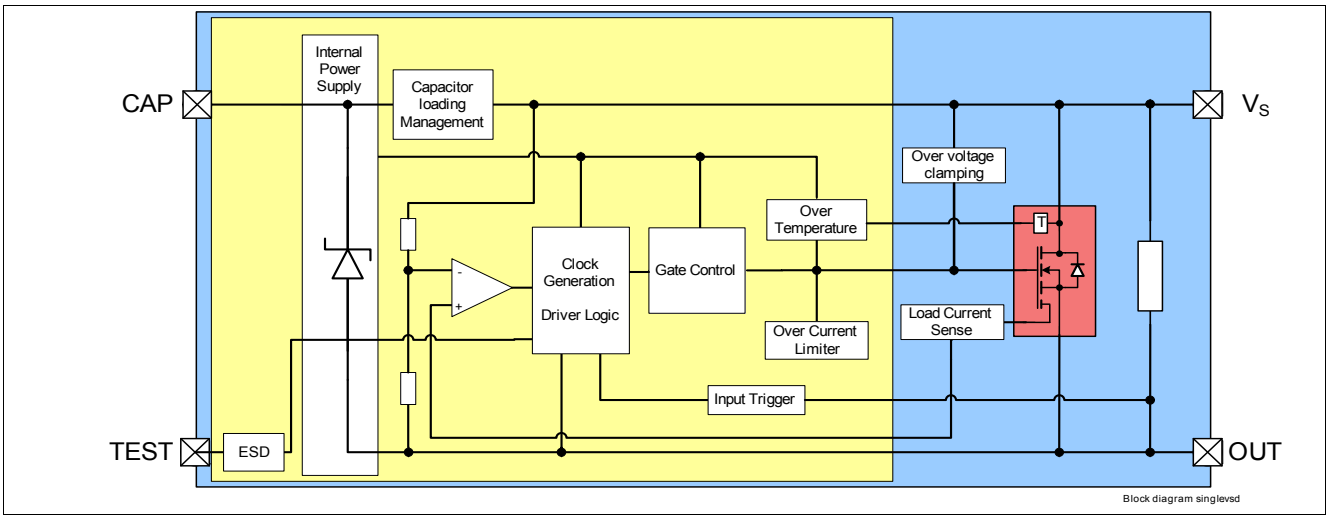

Figure 1 BTS6110-1SJA Block Diagram

3 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

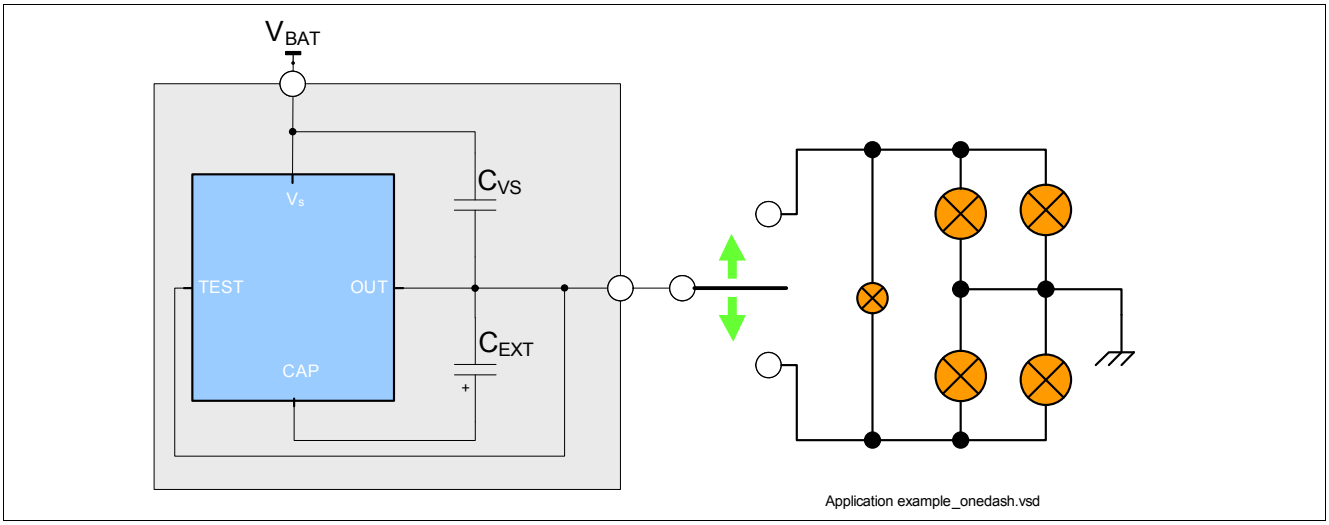

Figure 2 Application Example

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Table 2 Bill of Material

Reference	Value	Purpose
C_{VS}	10 nF / min. 100V	Reduction of voltage spikes. It is mandatory to place this component to assure correct device behavior.
C_{EXT}	10 µF	BTS6110-1SJA energy reservoir during ON state. It is mandatory to place this component to assure correct device behavior.

4 Pin Configuration

4.1 Pin Assignment

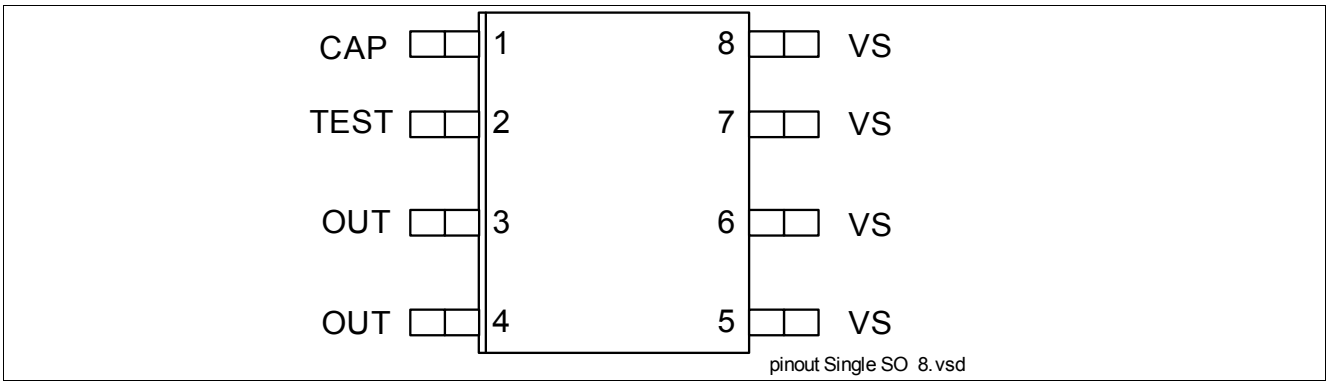

Figure 3 Pin Configuration

4.2 Pin Definitions and Functions

Pin	Symbol	Function
1	CAP	**CAPacitor;** Must be connected to OUT via a reservoir capacitor
2	TEST	**TEST MODE PIN;** Must be connected to OUT
3, 4	OUT	**OUTput;** Protected high side power output channel [1)]
5, 6, 7, 8	V_S	**Voltage Supply;** Battery voltage

1) All output pins must be connected together on the PCB. PCB traces have to be designed to withstand the maximum current which can flow.

4.3 Voltage and Current Definition

Figure 4 shows all terms used in this document, with associated convention for positive values.

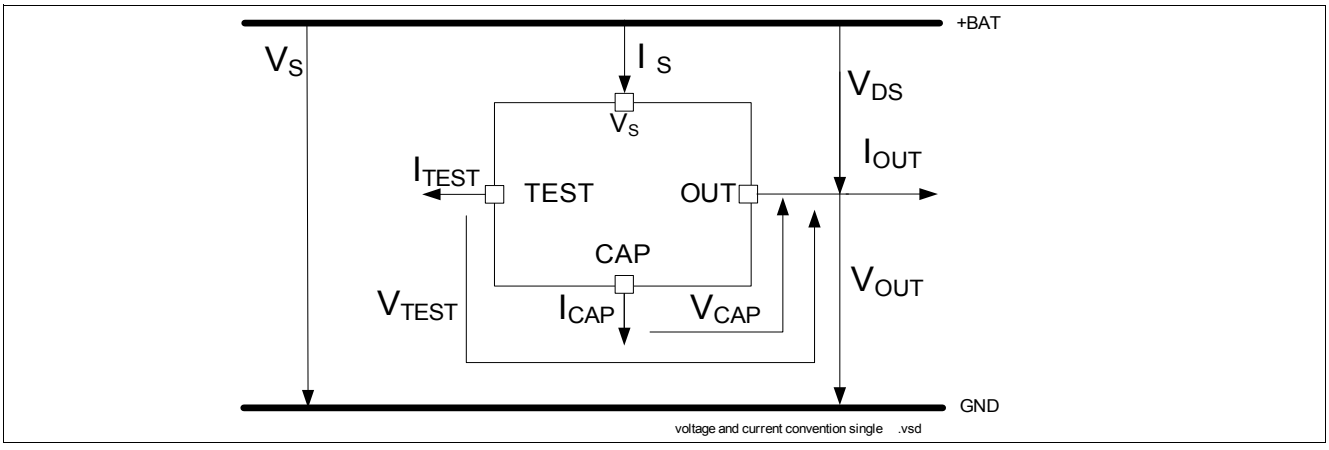

Figure 4 Voltage and Current Definition

5 General Product Characteristics

5.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings [1)]

T_J = -40 °C to +150 °C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Supply voltage	V_S	-0.3	–	18	V	–	P_5.1.1
Reverse polarity voltage	$-V_{S(REV)}$	0	–	16	V	t < 120 s T_A = 25 °C R_L ≥ 6 Ω	P_5.1.2
Supply voltage for Load dump protection	$V_{S(LD)}$	–	–	65	V	[2)] R_I = 2 Ω R_L = 6 Ω	P_5.1.3
CAP Pin							
Voltage at CAP pin	V_{CAP}	-0.3	–	8.0	V	–	P_5.1.4
Current through CAP pin	I_{CAP}	-2	–	15	mA	–	P_5.1.5
TEST Pin							
Voltage at TEST pin	V_{TEST}	-0.3	–	1	V	–	P_5.1.6
Current through TEST pin	I_{TEST}	-2	–	2	mA	–	P_5.1.7
Power Stage							
Load current	$\lvert I_L \rvert$	–	–	$I_{L(LIM)}$	A	–	P_5.1.8
Power dissipation (50% duty cycle)	P_{TOT}	–	–	1.4	W	T_A = 85 °C T_J < 150 °C	P_5.1.9
Voltage at power transistor	V_{DS}	–	–	65	V	–	P_5.1.10
Temperatures							
Junction temperature	T_J	-40	–	150	°C	–	P_5.1.11
Storage temperature	T_{STG}	-55	–	150	°C	–	P_5.1.12
ESD Susceptibility							
ESD susceptibility (all pins)	V_{ESD}	-2	–	2	kV	[3)] HBM	P_5.1.13
ESD susceptibility (OUT versus VS)	V_{ESD}	-4	–	4	kV	[3)] HBM	P_5.1.14

1) Not subject to production test. Specified by design.

2) $V_{S(LD)}$ is setup without the DUT connected to the generator per ISO 7637-1.

3) ESD susceptibility HBM according to EIA/JESD 22-A 114B

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

5.2 Functional Range

Table 4 Functional Range T_J = -40 °C to +150 °C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating voltage	V_{NOM}	9	13.5	16	V	V_{OUT} = 0 V	P_5.2.1
Extended operating voltage	$V_{S(OP)}$	8	–	24	V	1) 8 to 18 V: R_L = 6 Ω, 18 to 24 V: R_L = 12 Ω V_{DS} < 0.7 V	P_5.2.2

1) Not subject to production test. Specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

5.3 Thermal Resistance

Table 5 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to case (bottom)	R_{thJS}	–	40	–	K/W	1)	P_5.3.1
Junction to ambient	R_{thJA}	–	58	–	K/W	1) 2)	P_5.3.2

1) Not subject to production test. Specified by design.

2) Specified R_{thja} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board with thermal vias; The product (chip + package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35 µm Cu).

5.3.1 PCB set up

e = 1.27; A = 5.69; L = 1.31; B = 0.65

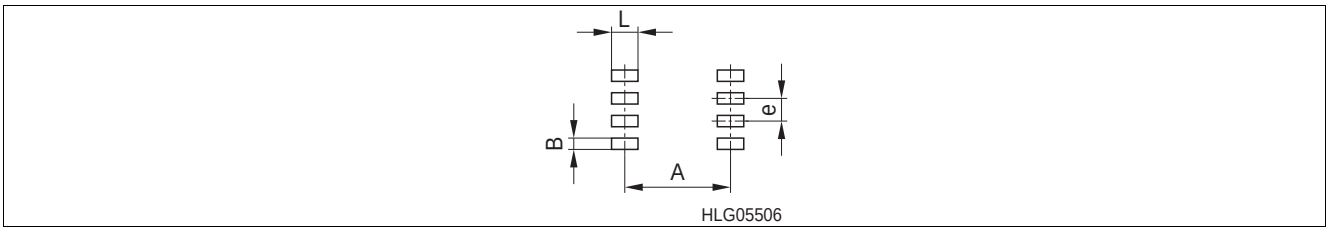

Figure 5 PCB Footprint for PG-DSO-8-49

5.3.2 Thermal Resistance

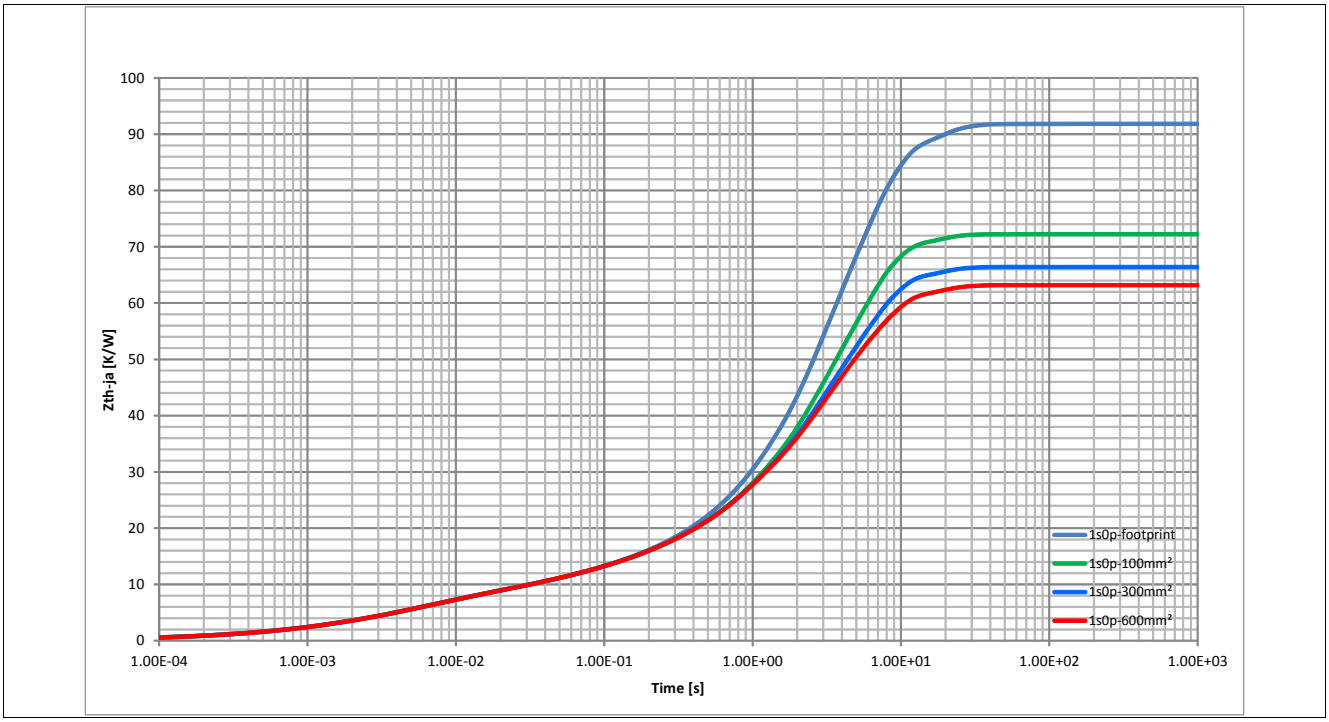

Figure 6 Typical Thermal Resistance for FR2 PCB

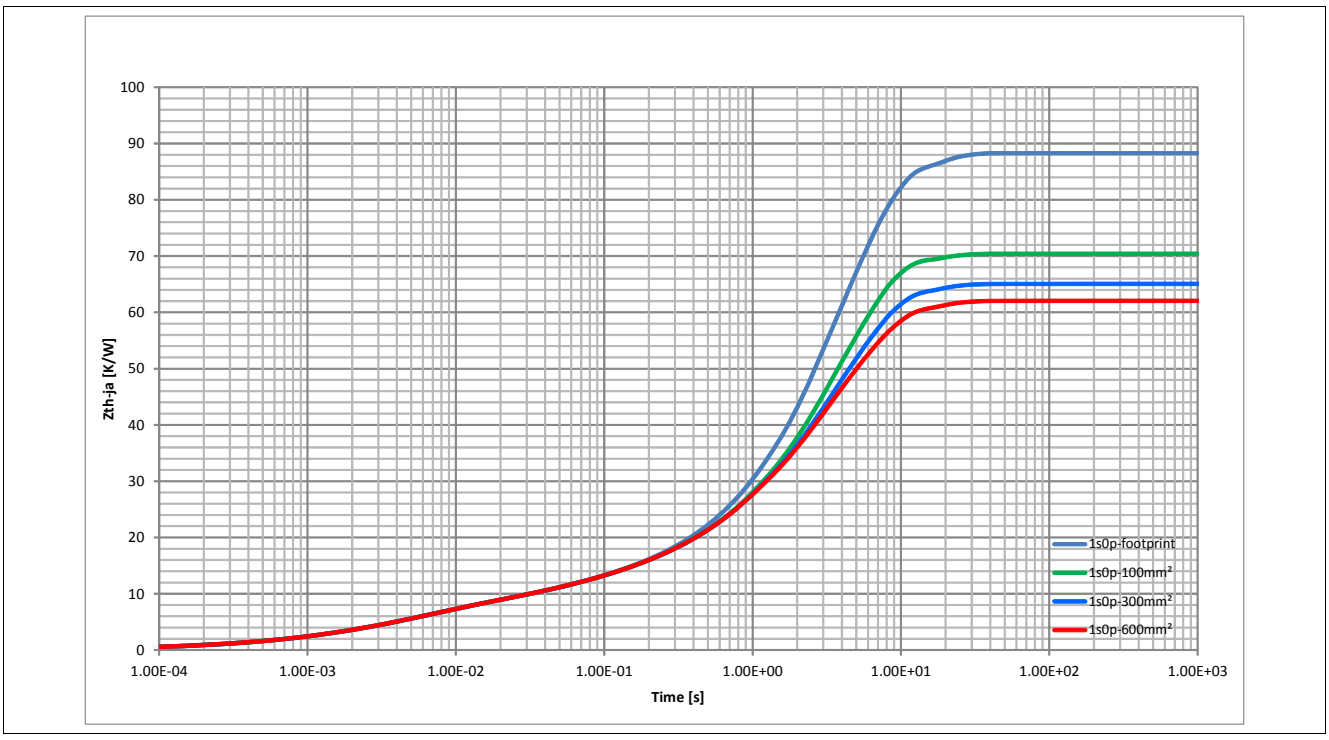

Figure 7 Typical Thermal Resistance for FR4 PCB

6 Power Stage

The power stage is built using an N-channel vertical power MOSFET (DMOS) with charge pump.

6.1 Output ON-state Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the junction temperature T_J. **Figure 8** shows the dependencies in terms of temperature for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 7.2**.

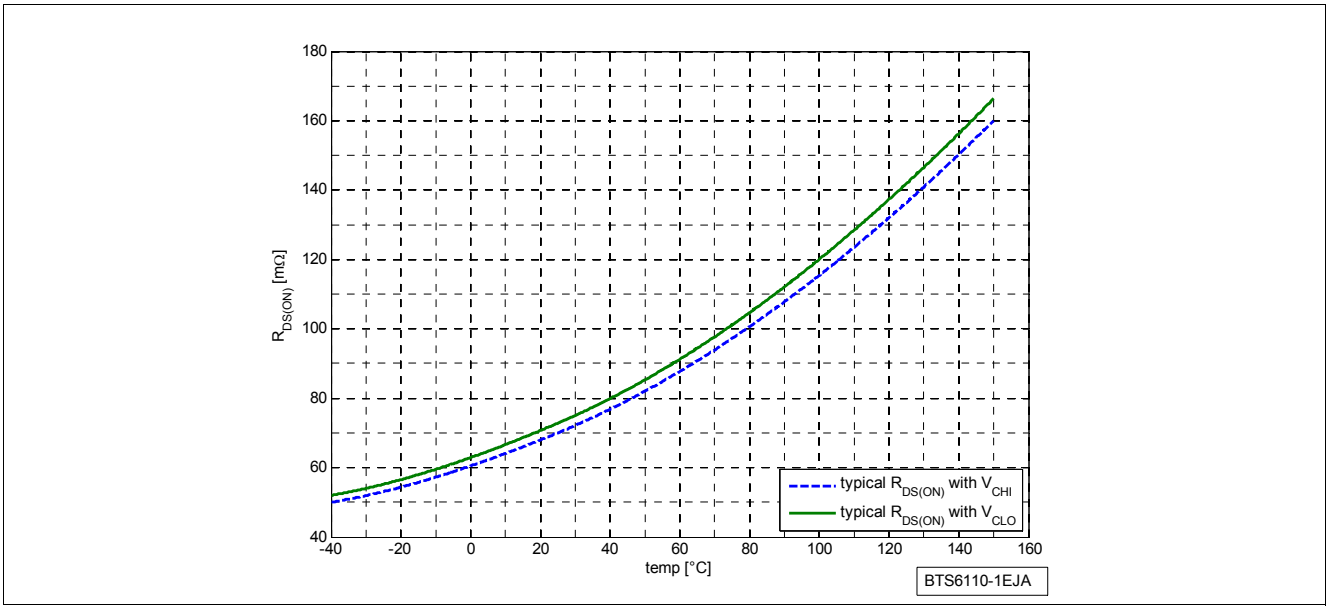

Figure 8 Typical ON-state Resistance

6.2 Turn ON/OFF Characteristics with Resistive Load

A low voltage event at the OUT pin causes the power DMOS to switch ON with a dedicated slope, optimized in terms of Electro Magnetic Emission.

Chapter 7.2 shows the typical timing when switching a resistive load.

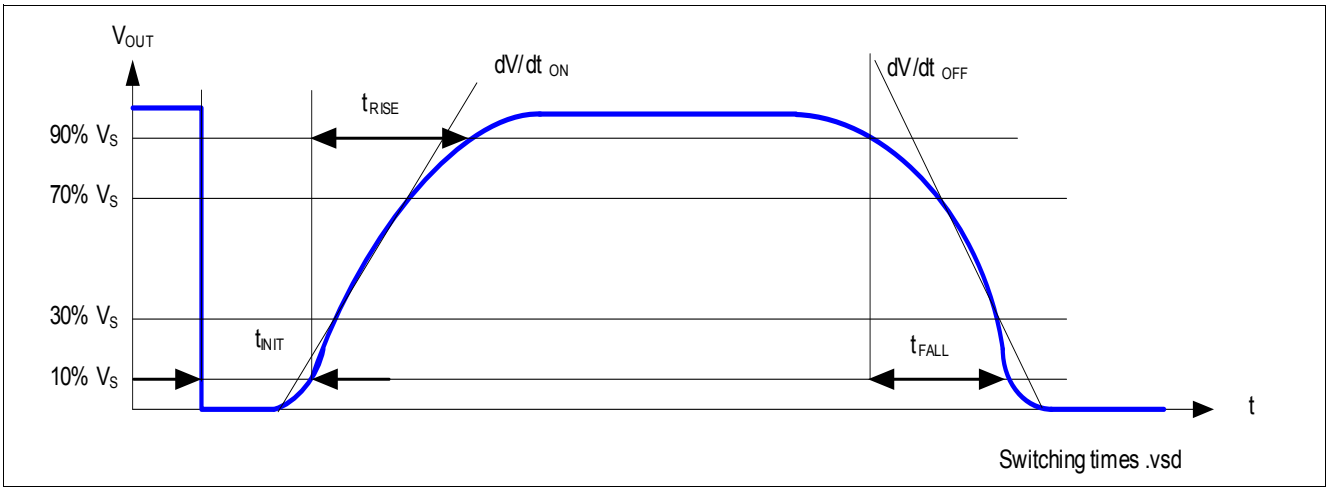

Figure 9 Switching a Resistive Load Timing

6.3 Frequency Generator

The BTS6110-1SJA is designed to manage side indicators functionality. As soon as a LOW voltage level is applied for more than t_{INIT}, at OUT pin, the clock generator is activated and the channel is switched ON. At t1, the device starts diagnosis. Refer to **Figure 10**. In case of underload detection, the device switches OFF and operates the failure frequency based on T_{2FAIL}. Otherwise, the device stays ON and runs on frequency based on T_4. The duty cycle is fixed to d.

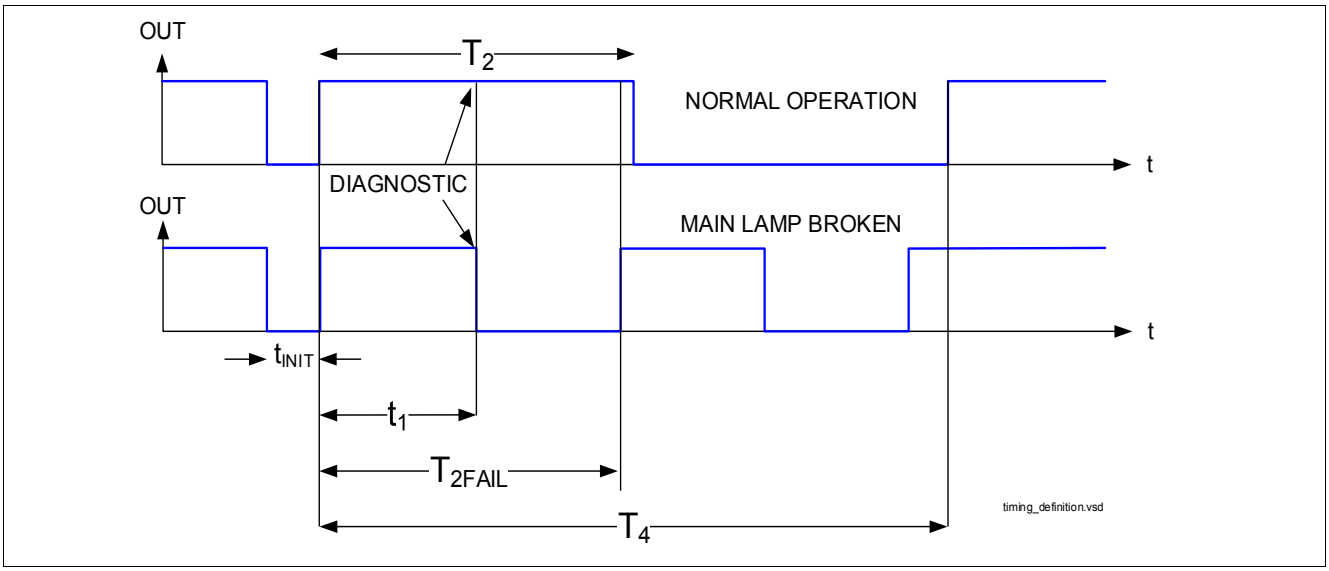

Figure 10 Frequency Generation Timing

6.4 Timing Output

The BTS6110-1SJA is dedicated to side indicators function on vehicle. The frequency f2 (resp T_{2FAIL} period) is tuned to be the failure indication frequency. At t1 time, the BTS6110-1SJA measures the load current. Refer to **Figure 11**. Depending on the measurement results, three possible actions will be done (see **Chapter 8** for the details diagnosis definition).

If an underload is detected, it provokes immediate switch OFF to run at f2 frequency, indicating the failure. A normal diagnosis keep the power output ON for t1 to run at f4 frequency. A short circuit will latch the device.

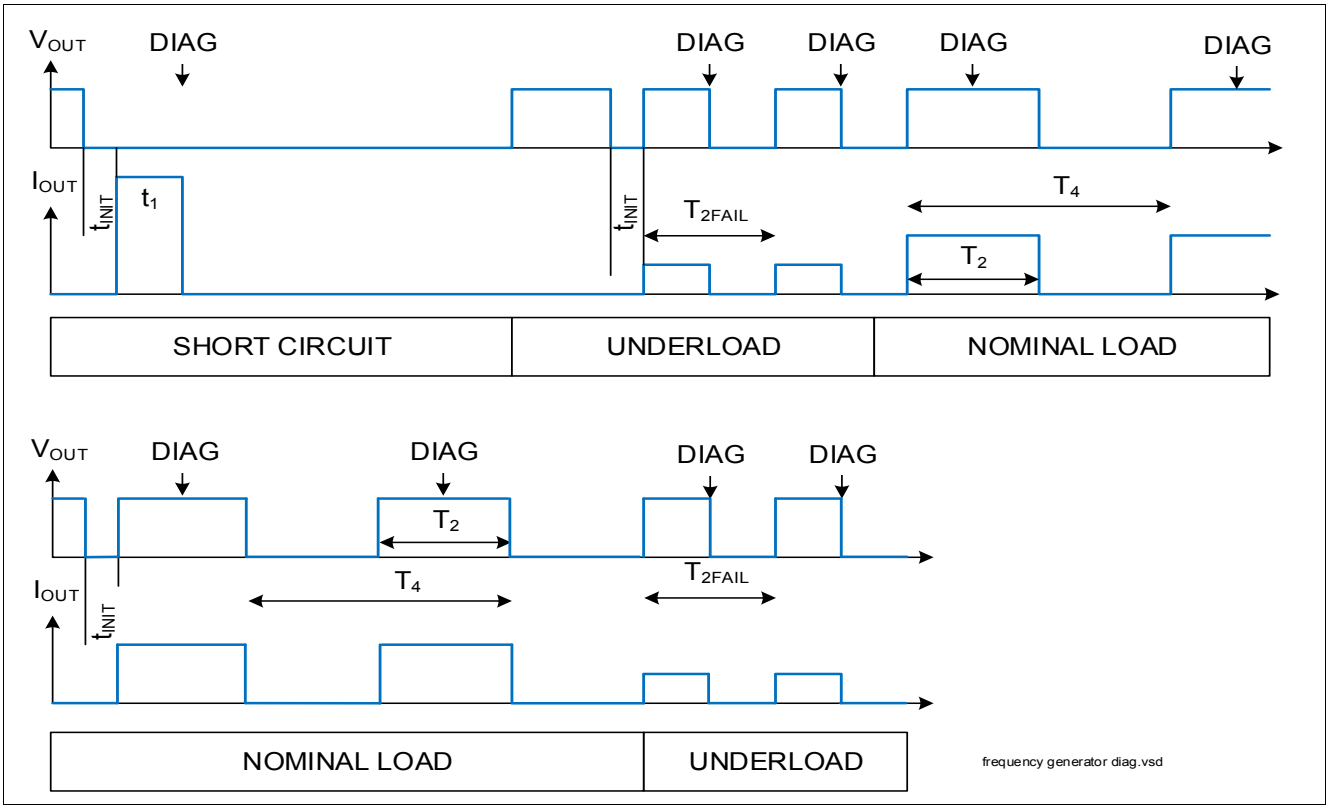

Figure 11 Frequency Generation Timing

6.5 Output Polarization

The BTS6110-1SJA includes from V_S to OUT a pull up resistor $R_{L(OFF)}$. This pull-up resistor compensates the I_{DIRT} leakage current due to the humidity and dust at the handle bar selector. It forces supply voltage VS at the output until a load is connected. The BTS6110-1SJA starts as soon as V_{DS} is detected between V_S and OUT by charging the external reservoir capacitor C_{EXT}. Refer to **Figure 12**.

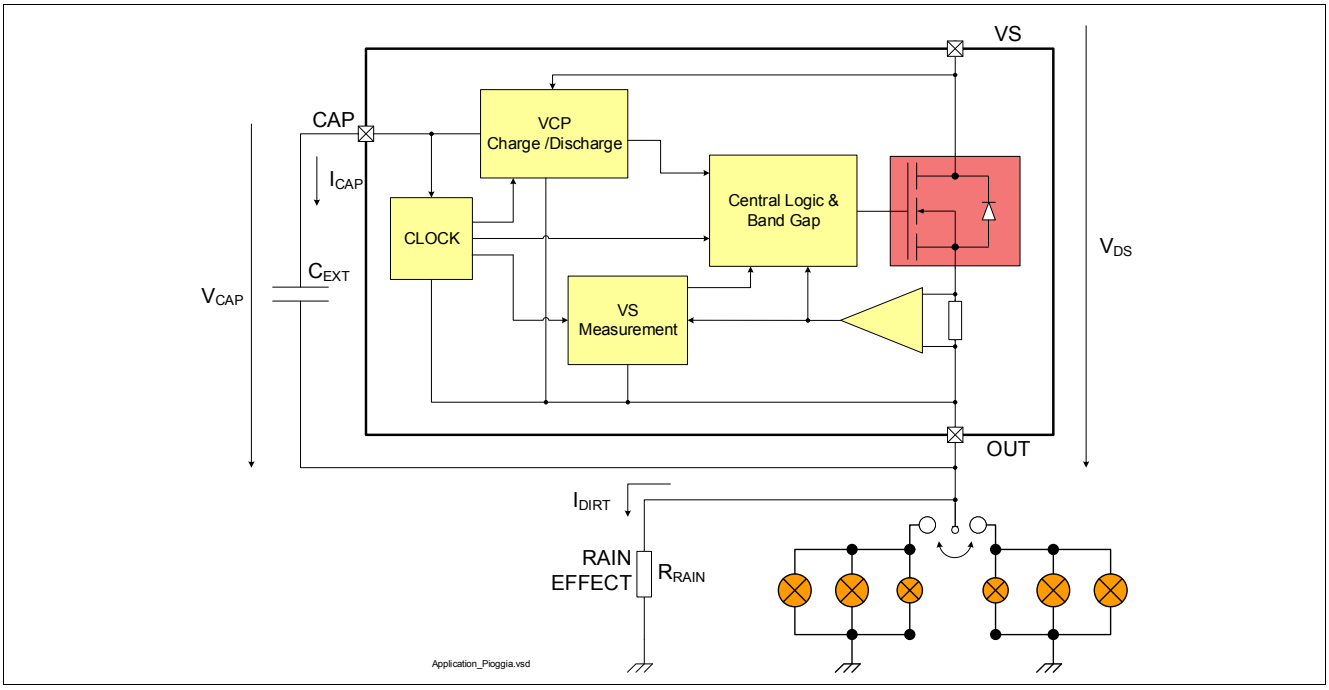

Figure 12 Output Polarization Circuitry

In case of leakage at the output, due to rain for example, the BTS6110-1SJA might start parasitically. To limit the effect, a load current measurement is implemented to estimate the impedance connected at the output. An impedance lower than R_{RAIN} will activate the switch while an impedance above (see maximum value P_9.1.11) will keep the device in sensing mode. Refer to **Figure 13**.

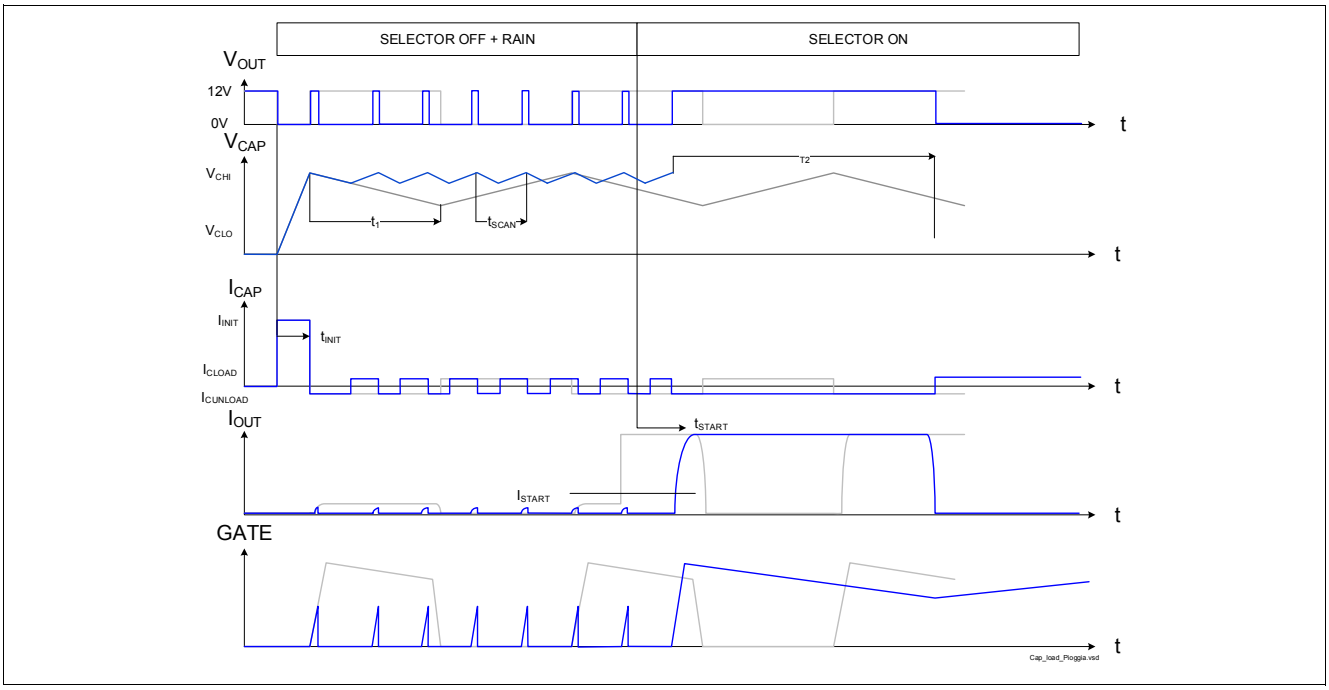

Figure 13 Output Timing during Leakage

6.6 CAP Pin

The BTS6110-1SJA stores the needed energy to keep the DMOS ON during T_2 phase, in the capacitor C_{EXT}. This capacitor is loaded initially with I_{INT} while OUT is grounded. I_{INT} is relatively important to reduce t_{INIT}, initialization time. During the next successive activations, the charging / discharging currents are controlled to I_{CLOAD} and $I_{CUNLOAD}$ whom are significantly lower to improve EMC and capacitor aging.
The loading is stopped when the voltage at the capacitor V_{CHI} is reached, and restarted by V_{CLO}. This oscillation provides the reference clock to the flasher functionality. In the case V_S - V_{OUT} is below $V_{S(OP)}$, the device doesn't start. Refer from **Equation (1)** to **Equation (4)** and **Figure 14** and **Figure 15**.

$$t_{INIT} = C_{EXT} \times \frac{V_S - 1V}{I_{INIT}} \times \ln\left(\frac{V_S - 1V}{V_S - 7{,}5V}\right) \quad (1)$$

$$T_{2FAIL} = T_4 \times d_f \quad (2)$$

$$d = \frac{T_2}{T_4} = \frac{1}{1 + \frac{I_{CUNLOAD}}{I_{CLOAD}}} \quad (3)$$

$$T_4 = C_{EXT} \times R_{CAP} \quad (4)$$

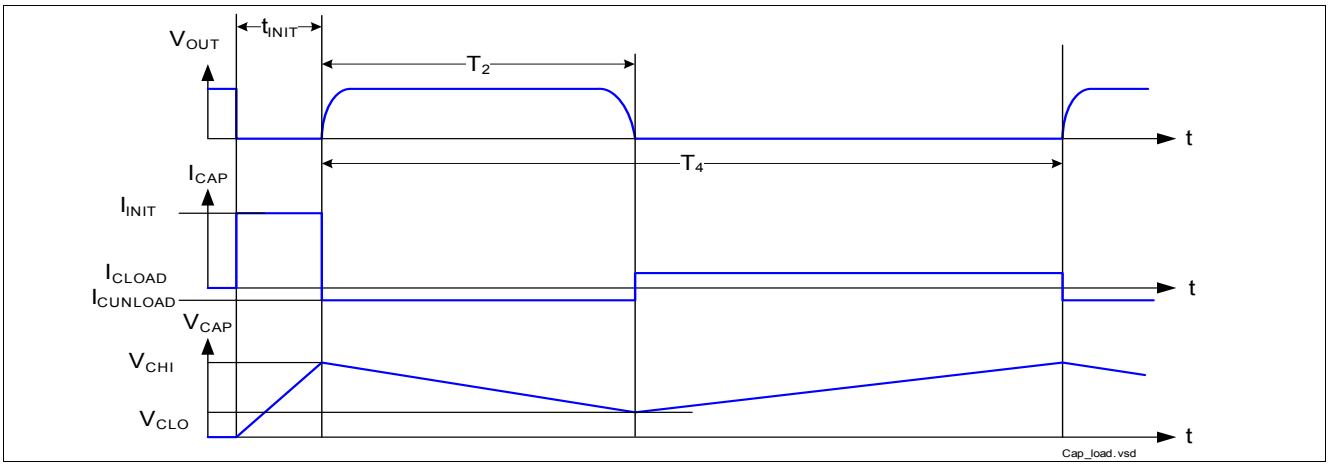

Figure 14 Capacitor Charge and Discharge Timing

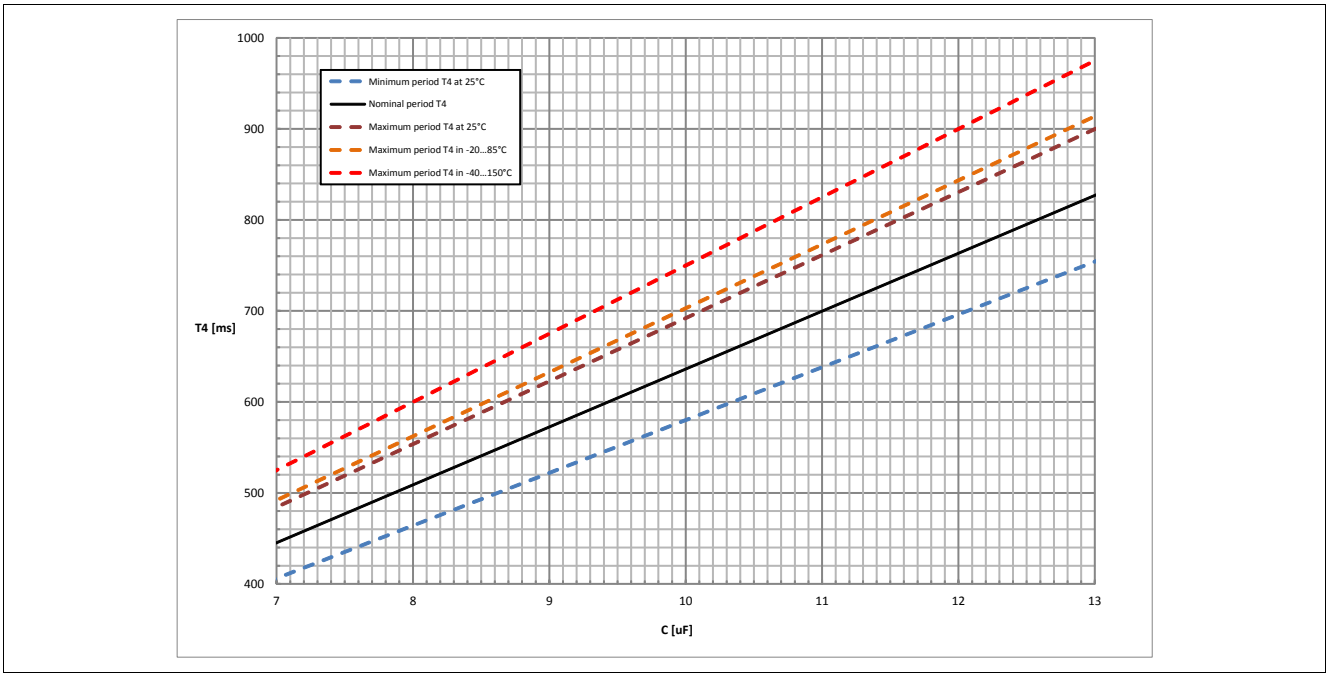

Figure 15 Normal Period T4 Dependency in Regards to Capacitor Value (typical behavior)

7 Protection Functions

The BTS6110-1SJA provides integrated protection functions. These functions are designed to prevent the destruction of the IC from fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed for neither continuous nor repetitive operation.

7.1 Overvoltage Protection

The BTS6110-1SJA is protected against overvoltage. In case of a voltage $V_S > V_{S(AZ)}$, if the handle bar selector switch is ON, the $Z_{DS(AZ)}$ will activate the power DMOS and some current will flow, limited by the load.

7.2 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diodes of the power DMOS causes power dissipation. The current in this intrinsic body diode is limited by the load itself. **Figure 16** shows the application schematic.

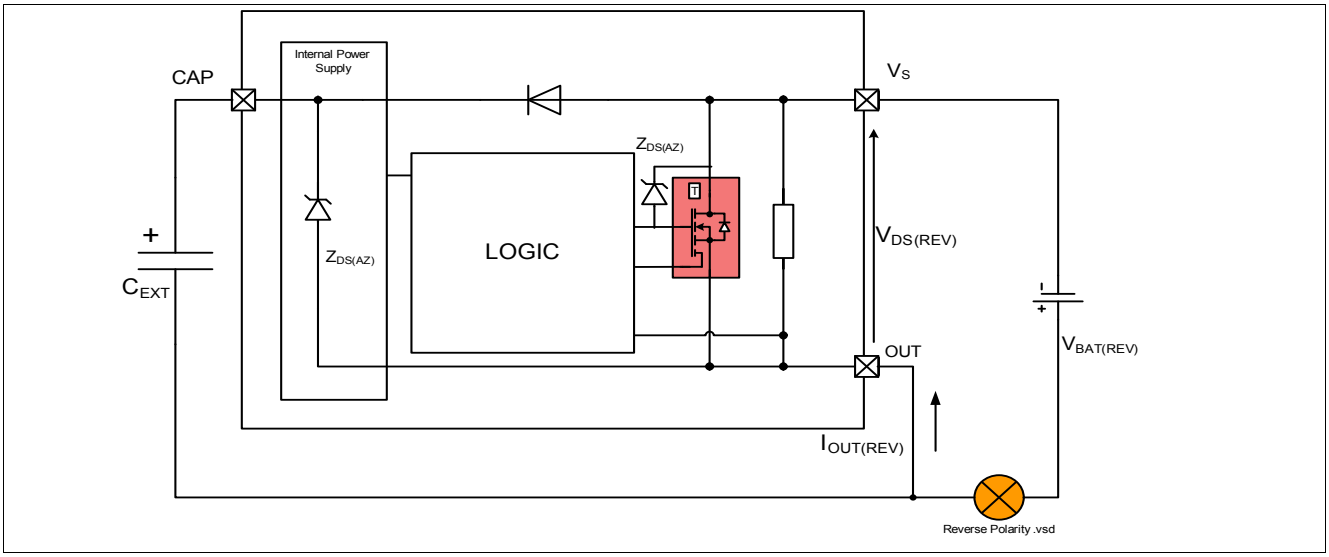

Figure 16 Reverse Polarity Protection

7.3 Overload Protection

In case of overload, such as high inrush of cold lamp filament, or short circuit to ground, the BTS6110-1SJA offers protection mechanisms.

7.3.1 Current Limitation

At first step, the instantaneous power in the switch is maintained to a safe value by limiting the current to $I_{L(SC)}$. During this time, the DMOS temperature is increasing.

7.3.2 Temperature Limitation in the Power DMOS

The channel incorporates an absolute ($T_{J(SC)}$) and a dynamic ($T_{J(SW)}$) temperature sensor. Activation of either sensor will cause the overheated channel to switch OFF to prevent destruction. Any protective switch OFF latches the output until the temperature has reached an acceptable value. To ensure the lamps to be turned ON, the DMOS restarts after cool down until t_1. **Figure 17** sketches the situation. The restart takes place for maximum t_1 of the flasher in fault condition, around 130ms. If after this time, the device is still in restart conditions, the switch is latched until the OUT voltage goes to HIGH again.

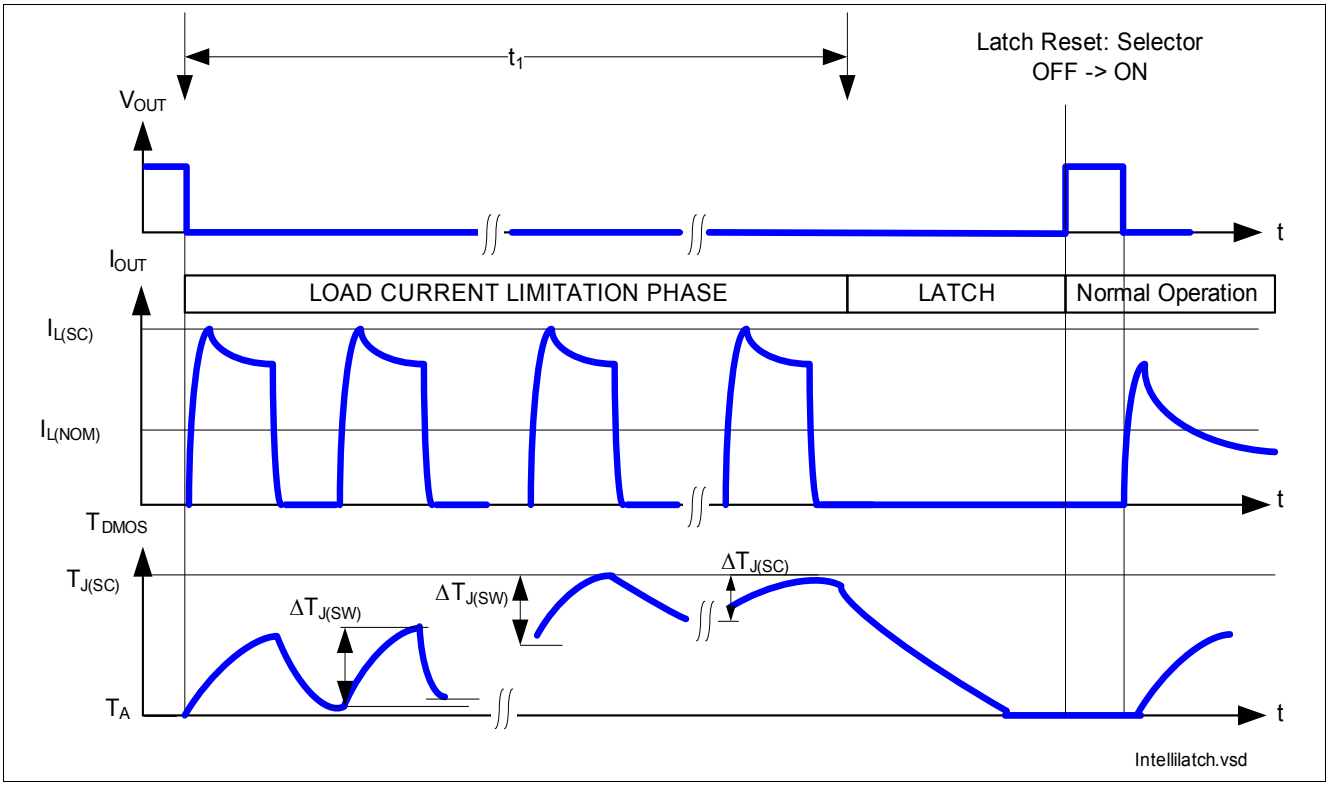

Figure 17 Overload Protection

8 Diagnostic Functions

For diagnosis purpose, the BTS6110-1SJA measures the load current.

8.1 Load Current Measurement

The BTS6110-1SJA integrates a sense signal called I_{IS}. As long as no “hard” failure mode occurs (current limitation / overtemperature / excessive dynamic temperature increase) a proportional signal to the load current (ratio $k_{ILIS} = I_L / I_{IS}$) is measured. To reduce current consumption, the diagnosis is only realized periodically. Refer to the **Figure 11**. The complete sense circuit and diagnostic mechanism is described on **Figure 18**. In the case $V_{IS} < V_{REF}$, the device raises an internal fault signal, to double the flashing frequency. Just before the switch ON event, the device measures the supply voltage VS, via a voltage divider.

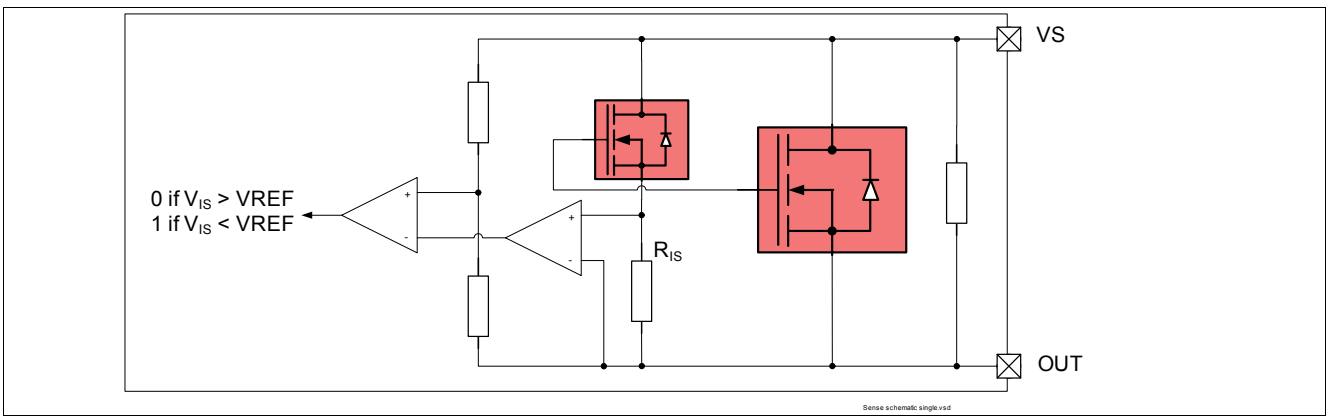

Figure 18 Diagnostic Block Diagram

8.2 Under load Current

Figure 19 shows the load current I_{df_L} considered as a function of the load current in the power DMOS. The blue curve represents the typical current threshold, assuming ideal device. The red curves show the accuracy the device provide accross full temperature range, at a defined current [1].

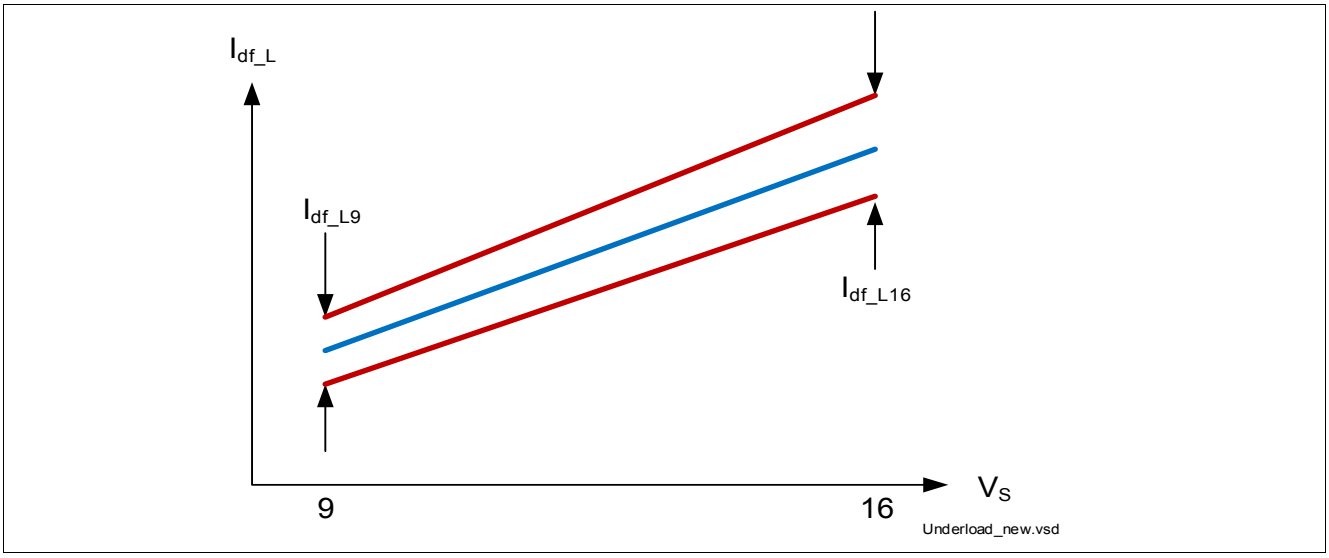

Figure 19 Current Sense for Nominal Load

1) Only Idf_L9 and Idf_L16 are tested in production. The red curves between these points are specified by design.

9 Electrical Characteristics

9.1 Electrical Characteristics Power Stage

Table 6 Electrical Characteristics: Power Stage

V_S = 9 V to 16 V, T_J = -40 °C to +150 °C (unless otherwise specified).
Typical values are given at V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
ON-state resistance per channel	$R_{DS(ON)\_150}$	–	–	200	mΩ	R_L = 6 Ω V_{CAP} = V_{CHI} T_J = 150 °C See **Figure 8**	P_9.1.1
ON-state resistance per channel	$R_{DS(ON)\_25}$	–	80	–	mΩ	1) T_J = 25 °C	P_9.1.2
Drain to source clamping voltage $V_{DS(AZ)}$ = [V_S - V_{OUT}]	$V_{DS(AZ)}$	65	70	75	V	I_{DS} = 2 mA	P_9.1.3
Output Leakage resistor	R_{RAIN}	0.04	0.4	1	kΩ	1)	P_9.1.11
Slew rate 30% to 70% V_S	dV/dt_{ON}	0.1	0.25	0.5	V/µs	R_L = 6 Ω V_S = 13.5 V See **Figure 9**	P_9.1.5
Slew rate 70% to 30% V_S	-dV/dt_{OFF}	0.1	0.25	0.5	V/µs		P_9.1.6
Turn-ON time to V_{OUT} = 10 to 90% V_S	t_{RISE}	–	70 1)	–	µs		P_9.1.7
Turn-OFF time to V_{OUT} = 90 to 10% V_S	t_{FALL}	–	70 1)	–	µs		P_9.1.8
Switch ON energy	E_{ON}	–	450	–	µJ	1) R_L = 6 Ω V_{OUT} = 90% V_S V_S = 16 V	P_9.1.9
Switch OFF energy	E_{OFF}	–	470	–	µJ	1) R_L = 6 Ω V_{OUT} = 10% V_S V_S = 16 V	P_9.1.10

1) Not subject to production test, specified by design

9.2 Electrical Characteristics CAP pin

Table 7 Electrical Characteristics: CAP pin

V_S = 9 V to 16 V, T_J = -40 °C to +150 °C (unless otherwise specified).
Typical values are given at V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Load Current							
Initialization Load current	I_{INIT}	3	4.5	10	mA	See **Figure 14** V_S = 9 V	P_9.2.1
Charging current	I_{CLOAD}		76.4		µA	1) See **Figure 14** V_{CAP} = 5.37 V	P_9.2.2
Discharging current	$I_{CUNLOAD}$		-74.4		µA	1) See **Figure 14** V_{CAP} = 5.37 V	P_9.2.3
Load current matching	I_{CRATIO} = $\lvert I_{CUNLOAD} \rvert$ / I_{CLOAD}		0.97		–	1) See **Figure 14**	P_9.2.4
Voltage Threshold							
CAP voltage High threshold	V_{CHI}		6.4		V	1) See **Figure 14**	P_9.2.5
CAP voltage Low threshold	V_{CLO}		4		V	1) See **Figure 14**	P_9.2.6
CAP voltage diagnostic threshold	V_{CDIAG}		5.37		V	1) See **Figure 14**	P_9.2.7
CAP voltage threshold Matching	V_{OSC} = V_{CHI} - V_{CLO}		2.4		V	1) See **Figure 14**	P_9.2.8
Flasher duty cycle Device dependency	R_{LOAD} = V_{OSC} / I_{CLOAD}	–	32	–	kΩ	1) See **Figure 14**	P_9.2.10
Flasher duty cycle Device dependency	R_{UNLOAD} = V_{OSC} / $I_{CUNLOAD}$	–	31.6	–	kΩ	1) See **Figure 14**	P_9.2.11
Flasher duty cycle Device dependency	R_{CAP} = R_{UNLOAD} + R_{LOAD}	58	63.6	75	kΩ		P_9.2.17
Flasher duty cycle Device dependency	R_{CAP_USAGE}	58	63.6	70.3	kΩ	1) 2) T_J = -20°C to 85°C	P_9.2.19
Flasher duty cycle Device dependency	R_{CAP_AMB}	58	63.6	69.2	kΩ	1) 2) T_J = +25°C	P_9.2.20
Time Generator							
Duty Cycle	d	45	50	55	%	–	P_9.2.14
Double frequency factor	df = T_{2FAIL} / T_4	0.40	0.45	0.50	–	–	P_9.2.18
Initialisation Time	t_{INIT}	–	30	–	ms	– 1)2) V_S = 9V	P_9.2.13
Impedance sensing Time	t_{SCAN}	–	25	–	ms	– 1)2)	P_9.2.16

1) Not subject to production test, specified by design

2) With a CEXT of 10 µF

9.3 Electrical Characteristics for the Protection Functions

Table 8 Electrical Characteristics: Protection

V_S = 9 V to 16 V, T_J = -40 °C to +150 °C (unless otherwise specified).
Typical values are given at V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Reverse Polarity							
Drain source diode voltage during reverse polarity	$V_{DS(REV)}$	200	600	700	mV	R_L = 6 Ω T_J = 150 °C See **Figure 16**	P_9.3.1
Overload Condition							
Load current limitation	$I_{L(SC)}$	20	27	36	A	1) V_{DS} = 5 V	P_9.3.2
Dynamic temperature increase while switching	$\Delta T_{J(SW)}$	–	80	–	K	2) See **Figure 17**	P_9.3.5
Thermal shutdown temperature	$T_{J(SC)}$	150	170 2)	200 2)	°C	See **Figure 17**	P_9.3.3
Thermal shutdown hysteresis	$\Delta T_{J(SC)}$	–	30	–	K	2) See **Figure 17**	P_9.3.4

1) Test at TJ = -40°C only

2) Not subject to production test, specified by design.

9.4 Electrical Characteristics Diagnostic Function

Table 9 Electrical Characteristics: Diagnostics

V_S = 9 V to 16 V, T_J = -40 °C to +150 °C (unless otherwise specified).
Typical values are given at V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Load Current Underload Threshold							
Load current threshold Low battery operation	Idf_L9	0.782	0.924	1.067	A	V_S at 9 V step See **Figure 19**	P_9.4.1
Load current threshold High battery operation	Idf_L16	1.074	1.269	1.464	A	V_S at 16 V step See **Figure 19**	P_9.4.2

10 Package Outlines

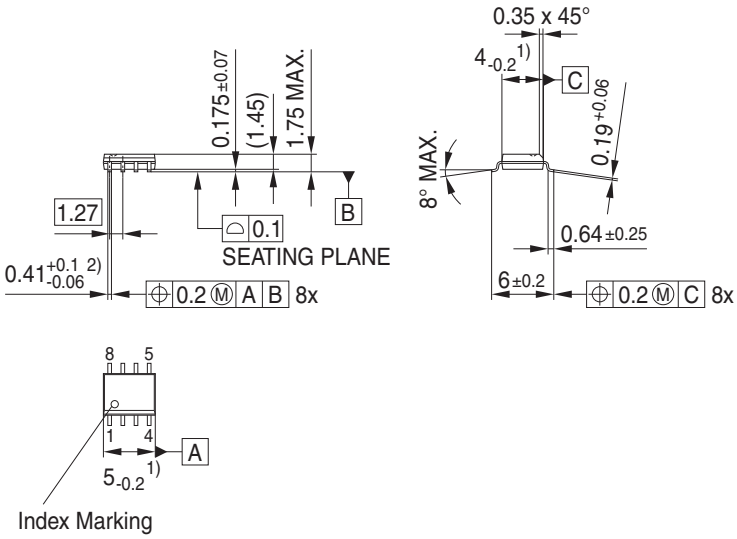

Figure 20 PG-DSO-8-49 (Plastic Dual Small Outline Package) (RoHS-Compliant)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant. For the soldering of this device the appropriate temperature profile as described in J-STD-020 is to be used.

Table 10 Package Classification

Value	Purpose
MSL3	JEDEC humidity category acc. J-STD-020-D
260°C	JEDEC classification temperature acc. J-STD-020-D

11 Revision History

Version	Date	Changes
1.1	2014-11-24	Chapter 3 - Changed position of the Notes Chapter 5.3 - Removed the hint for exposed pad packages in footnote of table 5 Chapter 6.3 - Minor text change and update of Figure 10 Chatper 6.4 - Minor text change and update of Figure 11 Chatper 6.5 - Typo in text and update of Figure 12 and 13 (typo and headline) Chapter 7.3.2 - Typo in text corrected Chapter 8.2 - Update of Figure 19 Chapter 9.2 - P_9.2.2 and P_9.2.3 changed test condition from V_{CAP} - V_{OUT} = 5.37 V to V_{CAP} = 5.37 V Chapter 10 - Updated package drawing Figure 20
1.0	2014-02-27	Creation of the Document

Edition 2014-11-24

Published by
Infineon Technologies AG
81726 Munich, Germany

© 2014 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.