MPM54504

16V, Quad DC/DC Power Module with 5A Output Array

DESCRIPTION

The MPM54504 is a 16V input, quad-output step-down power module. The device can provide up to 5A of continuous output current per output, with excellent load and line regulation across a wide input range.

The MPM54504 has internal auto-compensation, which means that external compensation components are not required. The output voltage is adjustable from 0.6V to 5.5V, and can be set via a single resistor.

Constant-on-time (COT) control provides ultra-fast transient response and eases loop stabilization. Full protection features include over-current protection (OCP), short-circuit protection (SCP), under-voltage lockout (UVLO), over-voltage protection (OVP), and thermal shutdown.

The MPM54504 integrates a monolithic power stage, inductors, and supports passive components for high efficiency. It is available in a BGA (9mmx15mmx5mm) package.

FEATURES

- Quad-Output Step-Down Power Module with 5A per Output
- Wide 3V to 16V Input Voltage Range
- 0.6 to 5.5V Output Voltage
- 5A Output Current per Channel
- Fixed 1MHz Switching Frequency
- Constant-On-Time (COT) Control for Fast Transient, No External Compensation Required
- External Configurable Soft Start-Up Time
- EN and Power Good for Power Sequencing
- OVP, UVP, OCP, SCP, and OTP
- Available in a BGA (9mmx15mmx5mm) Package

APPLICATIONS

- FPGAs, DSPs and ASIC Applications
- Multi-Rail Point-of-Loads (PoLs)

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION

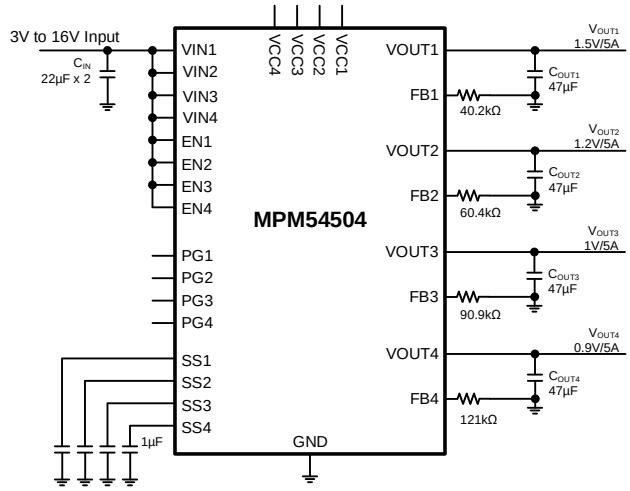
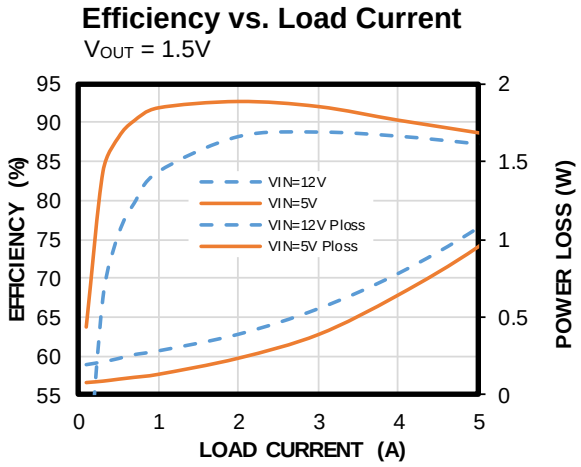


Figure 1: 3V to 16V Input, Quad Output (5A Applications)



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM54504GBS	BGA (9mmx15mmx5mm)	*See Below*	*3*

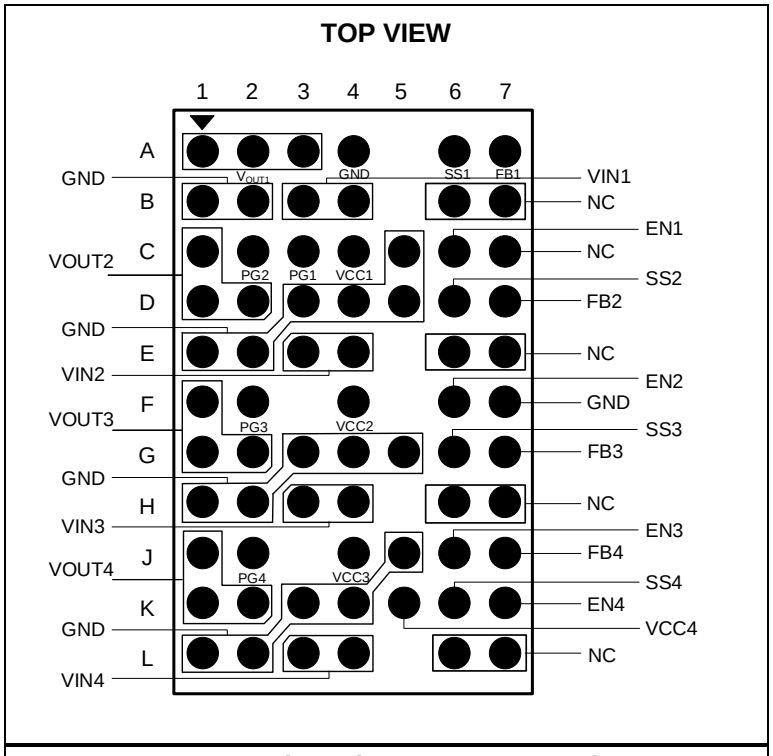
* For Tray, add suffix –T (e.g. MPM54504GBS–T).

TOP MARKING

MPSYYWW
MP54504
LLLLLLLLL
M

MPS: MPS prefix
YY: Year code
WW: Week code
MP54504: Part number
LLLLLLLLL: Lot number
M: Module

PACKAGE REFERENCE



BGA Package (9mmx15mmx5mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PIN ASSIGNMENT

Table 1: Pins A1–F7

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	VOUT1	B1	GND	C1	VOUT2	D1	VOUT2	E1	GND	F1	VOUT3
A2	VOUT1	B2	GND	C2	PG2	D2	VOUT2	E2	GND	F2	PG3
A3	VOUT1	B3	VIN1	C3	PG1	D3	GND	E3	VIN2	-	-
A4	GND	B4	VIN1	C4	VCC1	D4	GND	E4	VIN2	F4	VCC2
-	-	-	-	C5	GND	D5	GND	-	-	-	-
A6	SS1	B6	NC	C6	EN1	D6	SS2	E6	NC	F6	EN2
A7	FB1	B7	NC	C7	NC	D7	FB2	E7	NC	F7	GND

Table 2: Pins G1–L7

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
G1	VOUT3	H1	GND	J1	VOUT4	K1	VOUT4	L1	GND
G2	VOUT3	H2	GND	J2	PG4	K2	VOUT4	L2	GND
G3	GND	H3	VIN3	-	-	K3	GND	L3	VIN4
G4	GND	H4	VIN3	J4	VCC3	K4	GND	L4	VIN4
G5	GND	-	-	J5	GND	K5	VCC4	-	-
G6	SS3	H6	NC	J6	EN3	K6	SS4	L6	NC
G7	FB3	H7	NC	J7	FB4	K7	EN4	L7	NC

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
B3–B4, E3–E4, H3–H4, L3–L4	VIN1, VIN2, VIN3, VIN4	**Power input pins for the MPM54504.** The ceramic capacitors between VIN and ground are required to decouple the input rail. Connect VIN to the PCB using a wide copper plane.
A4, B1–B2, C5, D3–D5, E1–E2, F7, G3–G5, H1–H2, J5, K3–K4, L1–L2	GND	**Power ground pins for both input and output returns.** Use large copper areas on the PCB to connect all the GND pins together.
A1–A3	VOUT1	**Power output for channel 1.** Apply an output load between these pins and GND. It is recommend to directly connect the ceramic capacitors from these pins to GND.
C1, D1–D2	VOUT2	**Power output for channel 2.** Apply an output load between these pins and GND. It is recommend to directly connect the ceramic capacitors from these pins to GND.
F1, G1–G2	VOUT3	**Power output for channel 3.** Apply an output load between these pins and GND. It is recommend to directly connect the ceramic capacitors from these pins to GND.
J1, K1–K2	VOUT4	**Power output for channel 4.** Apply an output load between these pins and GND. It is recommend to directly connect the ceramic capacitors from these pins to GND.
A7, D7, G7, J7	FB1, FB2, FB3, FB4	**Output voltage feedback pin for each channel.** Internally, this pin is the negative input of the error amplifier for each channel. There is a 60.4kΩ resistor connected between the output and this pin. Connect a single resistor from this pin to GND to set the output voltage.
A6, D6, G6, K6	SS1, SS2, SS3, SS4	**Soft start.** Connect a capacitor across the SS pin and GND to set the soft-start time and avoid an inrush current during start-up.
C4, F4, J4, K5	VCC1, VCC2, VCC3, VCC4	**Internal 3.3V LDO output.** The driver and control circuit are powered from this pin. Each pin is internally decoupled to GND with a 1µF ceramic capacitor. This pin can be floated.
C6, F6, J6, K7	EN1, EN2, EN3, EN4	**Enable control for the four channels.** When this pin is pulled up high to VIN or VCC, the MPM54540 starts up with a pre-configured start-up sequence. Do not leave this pin floating.
C3, C2, F2, J2	PG1, PG2, PG3, PG4	**Power good output.** The output of this pin is an open drain. This pin changes states if under-voltage protection (UVP), over-voltage protection (OVP), over-current protection (OCP), short-circuit protection (SCP), or over-temperature protection (OTP) occurs.
B6–B7, C7, E6–E7, H6–H7, L6–L7	NC	**No connection.** Do not short the NC pins, or make any connections with them. Leave these pins floating.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} 20V
V_{EN} ..... V_{IN}
V_{OUT}..... 7V
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2)
..... 11.8W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +125°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....3V to 16V
Output voltage (V_{OUT}).....0.6V to 5.5V
Operating junction (T_J)..... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

BGA (9mmx15mmx5mm)
EVM54504-BS-00A (4)……..10.6……2.8…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside its operation conditions.
4) Measured on EVM54504-BS-00A, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [5], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		3		16	V
Supply Current						
Shutdown supply current	I_{IN}	V_{EN} = 0V		10	20	μA
Quiescent supply current	I_Q	V_{EN} = 2V, V_{FB} = 0.65V		400	600	μA
Current Limit						
Valley current limit	I_{LIMIT_VY}			7		A
Short hiccup duty cycle [6]	D_{HICCUP}			10		%
Switching Frequency and Minimum On/Off Time						
Switching frequency	f_{SW}			1		MHz
Minimum on time [6]	t_{ON-MIN}			50		ns
Minimum off time [6]	$t_{OFF-MIN}$			100		ns
Reference and Soft Start						
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C		600		
Integrated upper feedback resistor				60.4		kΩ
Feedback current	I_{FB}	V_{FB} = 700mV		10	50	nA
Soft start current	I_{SS_START}		4	6	8	μA
Enable and UVLO						
EN rising threshold	V_{EN_RISING}		1.1	1.25	1.4	V
EN falling threshold	$V_{EN_FALLING}$		0.9	1	1.1	V
EN pin pull-down resistor	V_{EN_PD}			1.2		MΩ
VCC						
VCC under-voltage lockout threshold rising	VCC_{VTH}		2.6	2.8	3	V
VCC under-voltage lockout threshold hysteresis	VCC_{HYS}			300		mV
VCC regulator	V_{CC}	V_{IN} = 5V		3.4		V

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [5], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VCC load regulation	REG_{VCC}	I_{CC} = 5mA		3		%
Power Good						
Power good UV rising threshold	$PGUV_{VTH_HI}$		90%	90%	100%	V_{FB}
Power good UV falling threshold	$PGUV_{VTH_LO}$		80%	80%	90%	V_{FB}
Power good OV rising threshold	$PGOV_{VTH_HI}$		120%	120%	130%	V_{FB}
Power good OV falling threshold	$PGOV_{VTH_LO}$		110%	110%	120%	V_{FB}
Power good delay	t_{PGTD}	Both edge		50		µs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 5V			10	µA
Thermal Protection						
Thermal shutdown [6]	T_{SD}			150		°C
Thermal hysteresis [6]	T_{SD-HYS}			20		°C

Notes:

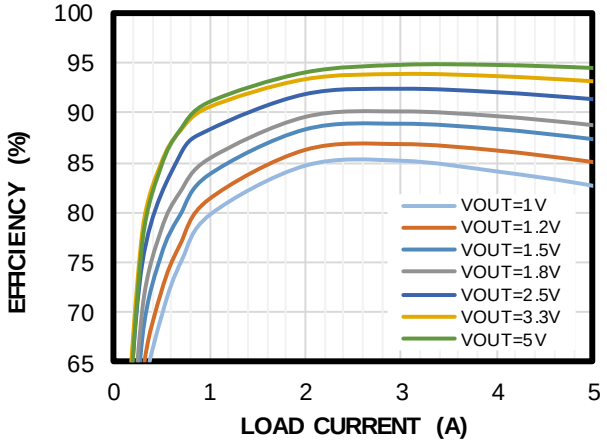
5) Not tested in production. Guaranteed by over-temperature correlation.
6) Guaranteed by design and characterization tests.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

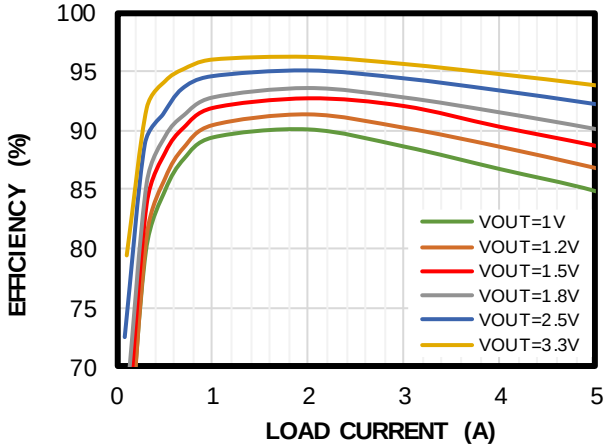
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, $V_{OUT1/2/3/4}$ = 1.5V, f_{SW} = 1000kHz, T_A = 25°C, unless otherwise noted.

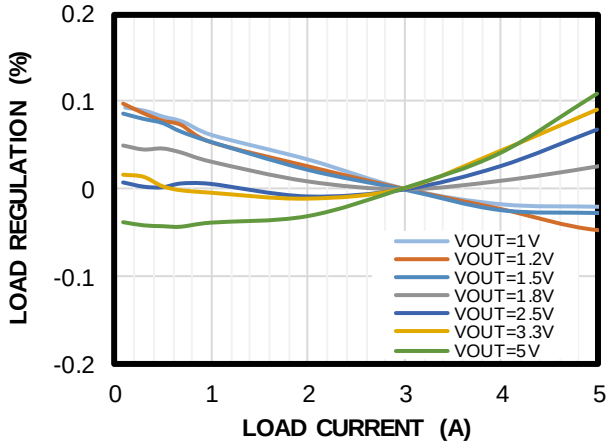
Efficiency vs. Load Current
V_{IN} = 12V



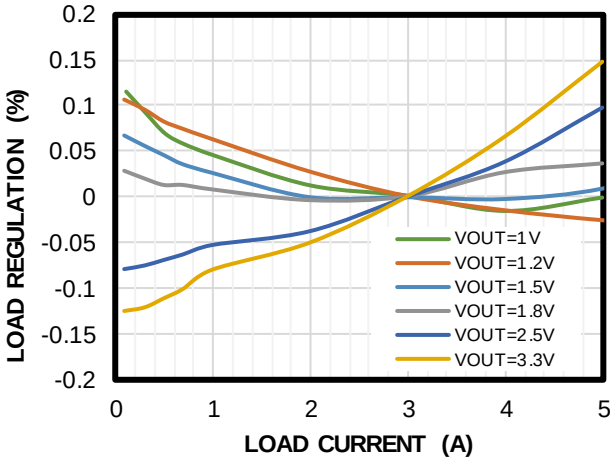
Efficiency vs. Load Current
V_{IN} = 5V



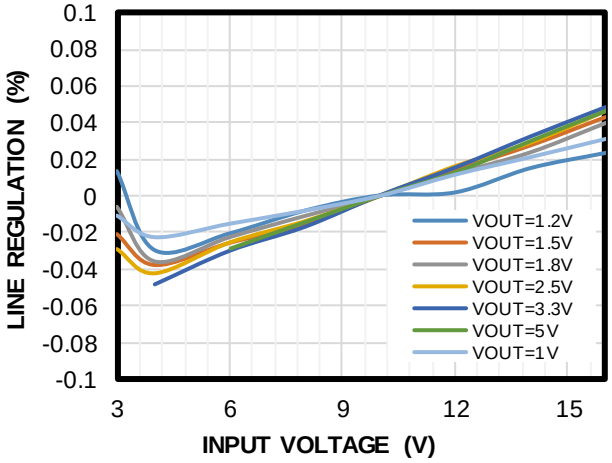
Load Regulation vs. Load Current
V_{IN} = 12V



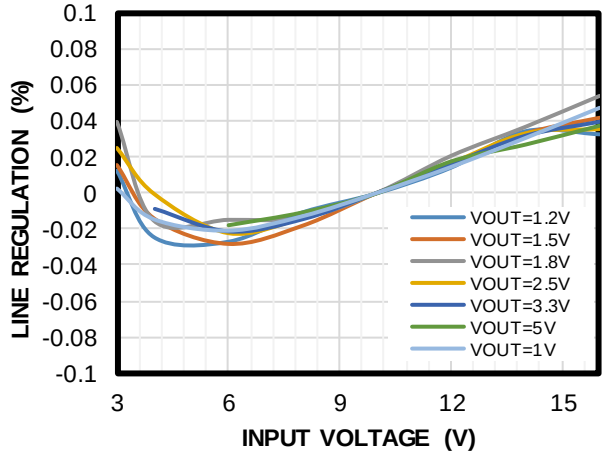
Load Regulation vs. Load Current
V_{IN} = 5V



Line Regulation vs. Input Voltage
I_{OUT} = 0A



Line Regulation vs. Input Voltage
I_{OUT} = 2.5A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

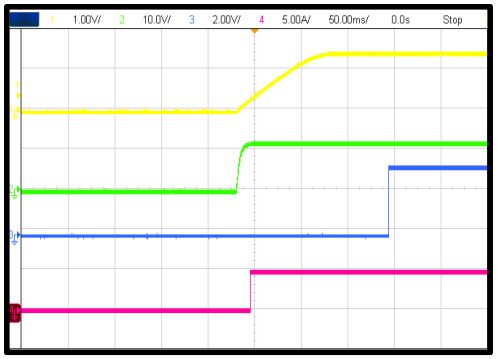
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, $V_{OUT1/2/3/4}$ = 1.5V, f_{SW} = 1000kHz, T_A = 25°C, unless otherwise noted.

VIN On

I_{OUT} = 5A

CH1: V_{OUT} 1V/div.
CH2: V_{IN} 10V/div.
CH3: PG 2V/div.
CH4: I_{OUT} 5A/div.

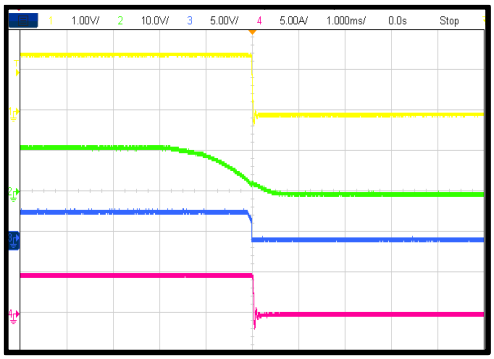


50ms/div.

VIN Off

I_{OUT} = 5A

CH1: V_{OUT} 1V/div.
CH2: V_{IN} 10V/div.
CH3: PG 5V/div.
CH4: I_{OUT} 5A/div.

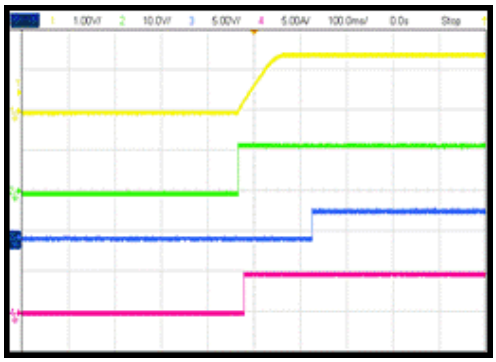


1ms/div.

EN On

I_{OUT} = 5A

CH1: V_{OUT} 1V/div.
CH2: V_{EN} 10V/div.
CH3: PG 5V/div.
CH4: I_{OUT} 5A/div.

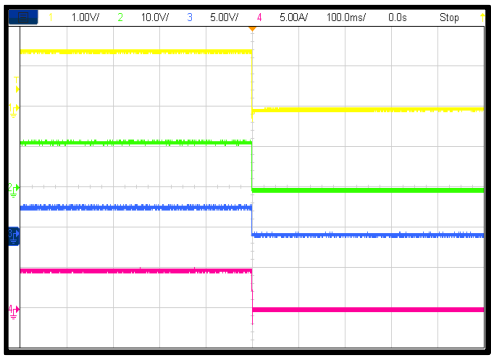


100ms/div.

EN Off

I_{OUT} = 5A

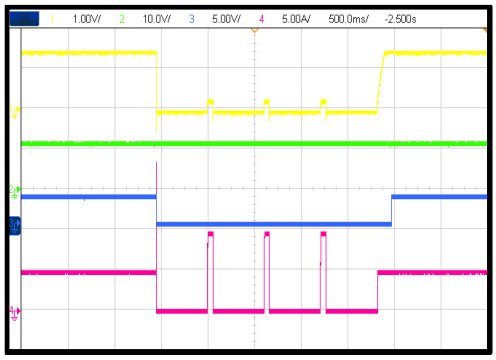
CH1: V_{OUT} 1V/div.
CH2: V_{EN} 10V/div.
CH3: PG 5V/div.
CH4: I_{OUT} 5A/div.



100ms/div.

SCP Entry And Recovery

CH1: V_{OUT} 1V/div.
CH2: V_{IN} 10V/div.
CH3: PG 5V/div.
CH4: I_{OUT} 5A/div.

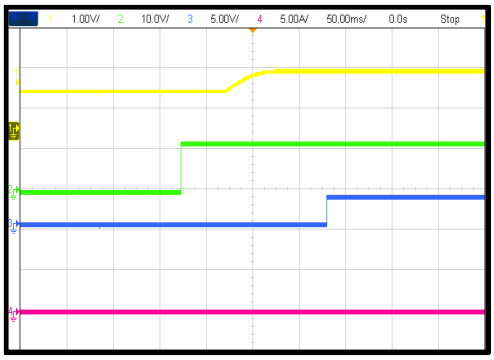


500ms/div.

Pre-Biased Start-Up

V_{BIAS} = 1V

CH1: V_{OUT} 1V/div.
CH2: V_{IN} 10V/div.
CH3: PG 5V/div.
CH4: I_{OUT} 5A/div.



50ms/div.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

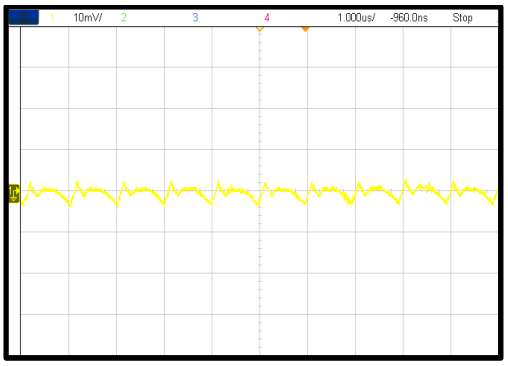
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, $V_{OUT1/2/3/4}$ = 1.5V, f_{SW} = 1000kHz, T_A = 25°C, unless otherwise noted.

Output Voltage Ripple

I_{OUT} = 5A

CH1: $V_{OUT/AC}$ 10mV/div.



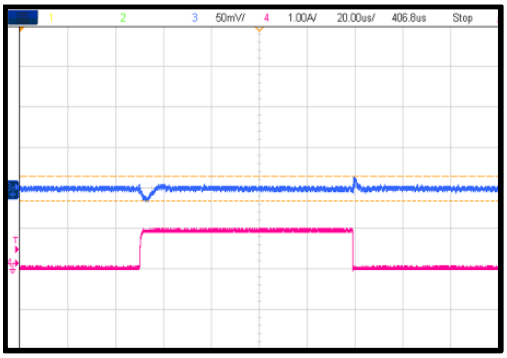
1µs/div.

Load Transient

V_{OUT} = 1V, C_{FF} = 100pF, C_{OUT} = 47µF, slew rate = 1A/µs

CH3: $V_{OUT/AC}$ 50mV/div.

CH4: I_{OUT} 1A/div.



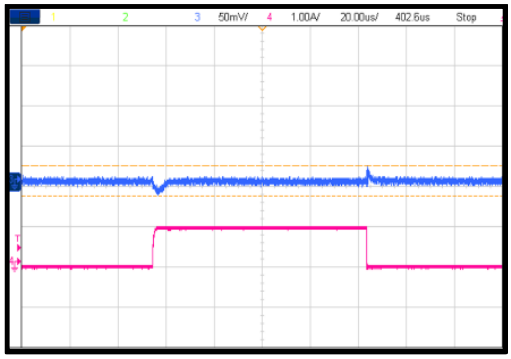
20µs/div.

Load Transient

V_{OUT} = 1.5V, C_{FF} = 100pF, C_{OUT} = 47µF, slew rate = 1A/µs

CH3: $V_{OUT/AC}$ 50mV/div.

CH4: I_{OUT} 1A/div.



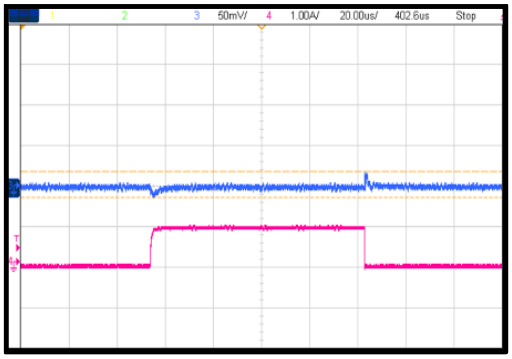
20µs/div.

Load Transient

V_{OUT} = 2.5V, C_{FF} = 100pF, C_{OUT} = 47µF, slew rate = 1A/µs

CH3: $V_{OUT/AC}$ 50mV/div.

CH4: I_{OUT} 1A/div.



20µs/div.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

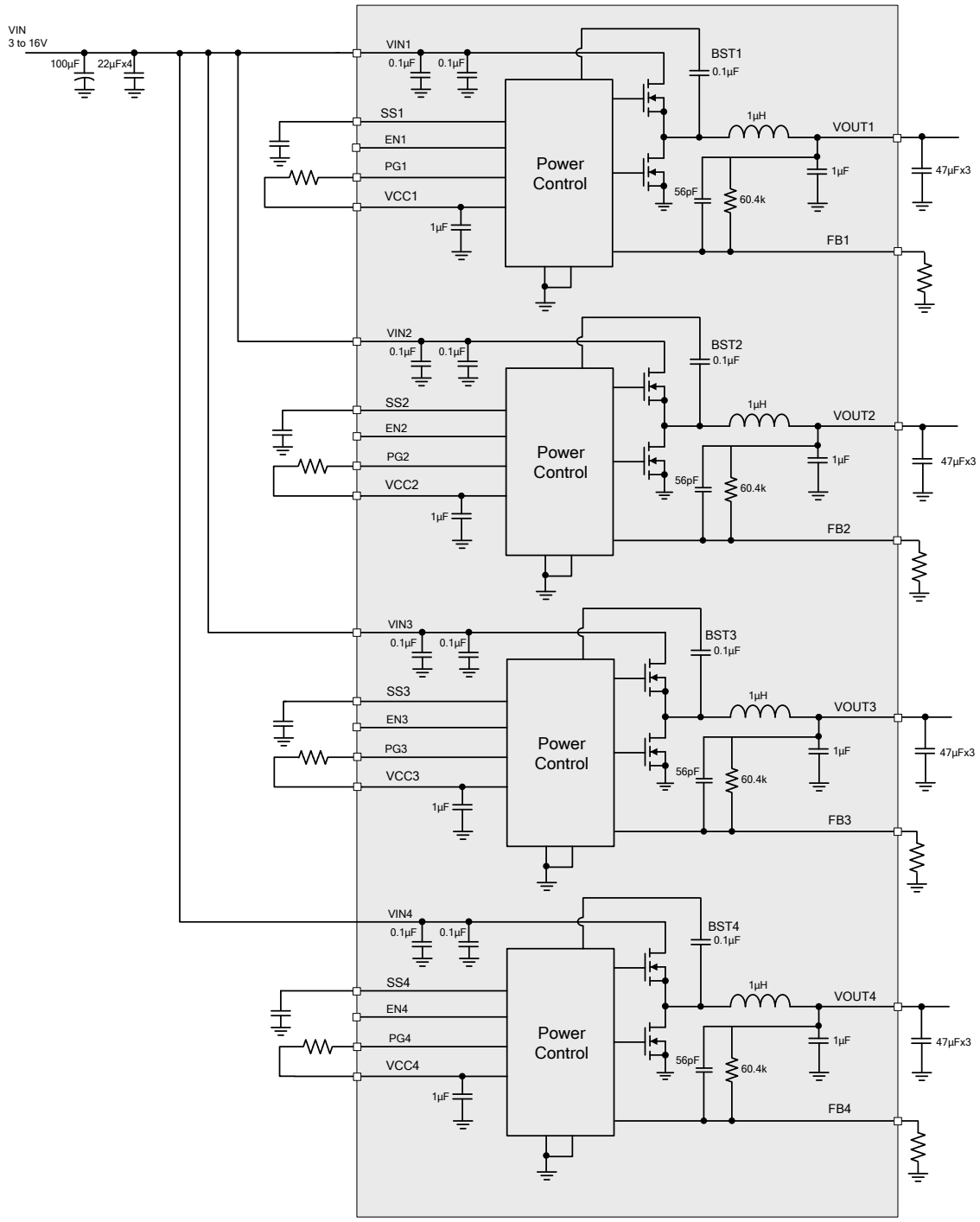


Figure 2: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

OPERATION

The MPM54504 is a quad-output, fully integrated, synchronous, rectified step-down converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. Figure 3 shows the simplified ramp compensation block.

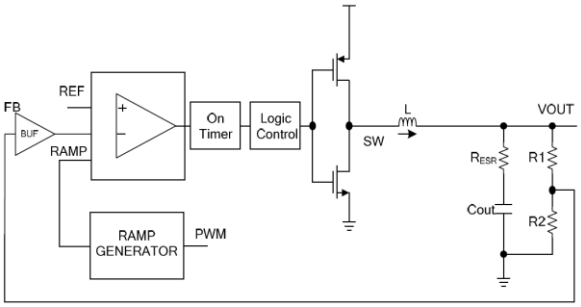


Figure 3: Simplified Ramp Compensation

The high-side MOSFET (HS-FET) turns on at the beginning of each cycle when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}). The on time is determined by the input voltage and output voltage to make the switching frequency nearly constant across the entire input voltage range.

After the on time elapses, the HS-FET turns off. It turns on again when V_{FB} drops below V_{REF}. The output voltage is regulated by repeating this operation. To minimize conduction loss, the integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off. There is a dead short between the input and GND if both the HS-FET and LS-FET turn on at the same time. This is called a shoot-through. To avoid shoot-through, a dead time (DT) is internally generated between the HS-FET off time and LS-FET on time, or vice versa.

Internal compensation is applied for COT control to keep the loop stable, even when ceramic capacitors are used as output capacitors. Internal compensation improves the stability without affecting line or load regulation.

Output Voltage

The feedback reference voltage is 0.6V. A 60.4kΩ resistor is integrated inside the module as the upper feedback resistor. Connect a single resistor between the feedback pin and ground to set the output voltage.

Forced Continuous Conduction Mode (FCCM)

The MPM54504 works in forced continuous conduction mode (FCCM) (see Figure 4). When V_{FB} drops below V_{EAO}, the HS-FET turns on for a fixed interval that is determined by the one-shot on-timer. When the HS-FET turns off, the LS-FET turns on until the next period.

In FCCM, the switching frequency is fairly constant.

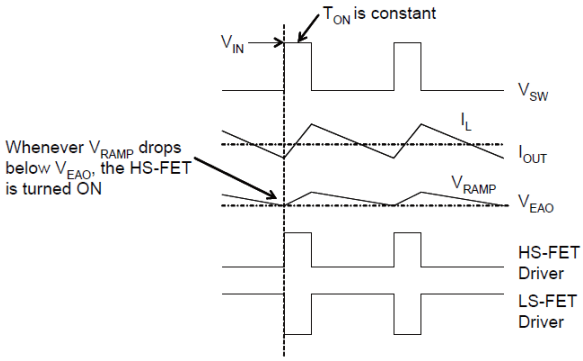


Figure 4: FCCM Operation

VCC Regulator

The 3.4V internal regulator powers most of the internal circuits. This regulator takes the VIN input and can operate in the full V_{IN} range. When V_{IN} exceeds 3.4V, the output of the regulator is in full regulation; when V_{IN} falls below 3.4V, the output decreases following V_{IN}. An internal 1µF decoupling ceramic capacitor is integrated inside the module.

Enable (EN)

EN is a digital control pin that turns the regulator on or off. Drive EN above 1.25V to turn the regulator on; drive EN below 1V to turn it off. Do not leave this pin floating. Connect EN to GND to disable the regulator. EN can be directly connected to VIN. It supports an input voltage up to 16V.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPM54504 UVLO comparator monitors the output voltage of the internal regulator (VCC). The VCC UVLO rising threshold is about 2.8V, and its falling threshold is 2.5V.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

When the input voltage exceeds the UVLO rising threshold voltage, the MPM54504 powers up. The device shuts down when the input voltage drops below the UVLO falling threshold voltage. This is non-latch protection.

Soft Start

The MPM54504 employs a soft start (SS) mechanism to ensure the output ramps smoothly during start-up. When the EN pin goes high, an internal current source (6µA) charges the SS capacitor. During soft start, the soft start voltage works instead of V_{FB}. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage (V_{SS}) rises above V_{REF}, V_{REF} takes over. At this point, soft start is completed, and the device enters steady state operation.

The SS capacitor value (C_{SS}) can be calculated with Equation (1):

$$C_{SS}(nF)=0.83\times\frac{t_{SS}(ms)\times I_{SS}(\mu A)}{V_{REF}(V)} \quad (1)$$

Ensure that the SS time is not too short if the output capacitance is large. A large capacitance can prevent the current limit from being reached during soft start.

Power Good (PG) Indicator

The PG pin is the open drain of a MOSFET that is connected to VCC (or another voltage source) through a resistor (e.g. 100kΩ). The MOSFET turns on when an input voltage is applied, so that the PG pin is pulled to GND before SS is ready. After the FB voltage (V_{FB}) reaches 90% of V_{REF}, the PG pin is pulled high after a 50µs delay. When V_{FB} drops to 80% of V_{REF}, the PG pin is pulled low.

If under-voltage lockout (UVLO) or over-temperature protection (OTP) occurs, the PG pin is pulled low immediately. If an over-current (OC) condition occurs, the PG pin is pulled low when V_{FB} drops below 80% of V_{REF} after a 50µs delay.

If an over-voltage (OV) condition occurs, the PG pin is pulled low when V_{FB} rises above 120% of V_{REF} after a 50µs delay. If V_{FB} drops below 110% of V_{REF}, the PG pin is pulled high after a 50µs delay.

If the input supply fails to power the MPM54504, PG is clamped low, even if PG is tied to an external DC source through a pull-up resistor. Figure 4 shows the relationship between the PG voltage and the pull-up current.

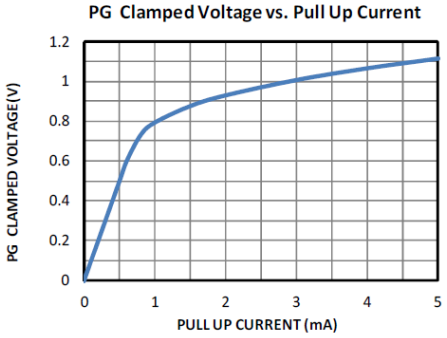


Figure 5: PG Clamped Voltage vs. Pull-Up Current

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MPM54504 has valley current limit control. The LS-FET monitors the current flowing through the LS-FET. The HS-FET does not turn on until the valley current limit disappears. An under-voltage (UV) condition is triggered if V_{FB} drops below the UV threshold (typically below 50% of V_{REF}). Once UVP is triggered, the MPM54504 enters hiccup mode to periodically restart the part.

During over-current protection (OCP), the device tries to recover from the OC fault with hiccup mode. This means that the chip disables the output power stage and soft-start capacitor, then automatically tries to initiate a soft start. If the OC condition remains after soft start ends, the device repeats this operation until the OC condition is removed. Then the output rises back to the regulated voltage. OCP is a non-latch protection.

Pre-Biased Start-Up

The MPM54504 has been designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft-start capacitor is also charged. If the BST voltage exceeds its rising threshold voltage and the soft-start capacitor voltage exceeds the sensed output voltage at the FB pin, the part starts to work normally.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 150°C, the chip shuts down. The chip is enabled again when the temperature falls below its lower threshold (typically 130°C).

Start-Up and Shutdown Circuit

If both VIN and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN going low, VIN going low, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering. The internal supply rail is then pulled down.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider sets the output voltage. There is an internal 60.4kΩ resistor connected between the FB and VOUT pins. Choose R2 to set the output voltage. A 100pF capacitor (C_F) guarantees good performance and a load transient with a 1A/µs step. R2 can be calculated with Equation (2):

$$R2 = \frac{60.4 \times V_{REF}}{V_{OUT} - V_{REF}} \quad (2)$$

Figure 6 shows the feedback circuit.

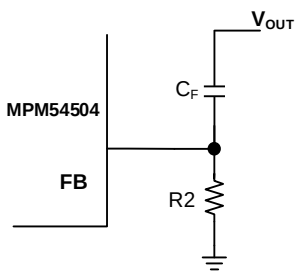


Figure 6: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R2 (kΩ)	C_F (pF)
0.9	120	100
1.0	84.5	100
1.2	60.4	100
1.5	40	100
1.8	30	100
2.5	19	100
3.3	13.3	100
5	8.2	100

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance, and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable amid temperature fluctuations.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. The input ripple current can be estimated with Equation (3):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (4):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the relevant specifications.

The input voltage ripple can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (6):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (6)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. It is recommended to use ceramic or POSCAP capacitors. The output voltage ripple can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (7)$$

If using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (8):

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

If using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

In addition to considering the output ripple, a larger-value output capacitor improves the load transient response. However, the maximum output capacitor limit should be also considered in design applications. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time, and the device fails to regulate. The maximum output capacitor value (C_{O_MAX}) can be calculated using Equation (10):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (10)$$

Where I_{LIM_AVG} is the average start-up current during soft start, and t_{SS} is the soft-start time.

PCB Layout Guidelines

The PCB layout is critical for stable operation. A 6-layer layout is recommended to improve thermal performance. For the best results, refer to Figure 7 and follow the guidelines below:

1. Keep the power loop as small as possible.
2. Use a large ground plane to connect directly to PGND. Add as many vias as possible on the PGND plane, and near the device to improve thermal performance.
3. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
4. Place the ceramic input capacitor, especially capacitors with a small package size (0402), as close to the VIN and PGND pins as possible to minimize high-frequency noise. Keep the input capacitor and VIN pin traces as short and wide as possible.
5. Place the VCC capacitor as close to the VCC pin and GND as possible.
6. Do not place the GND plane under the device.

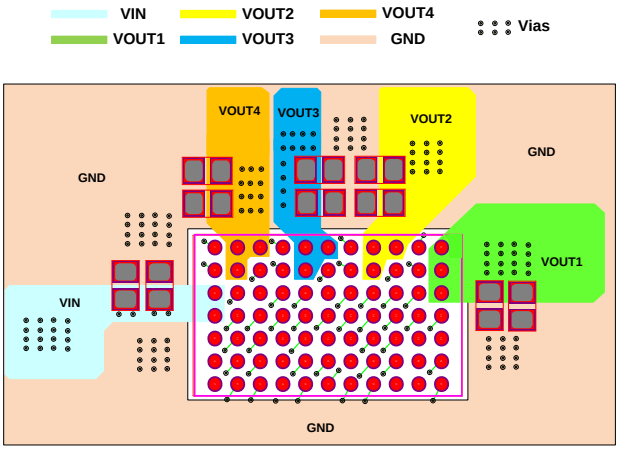


Figure 7: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

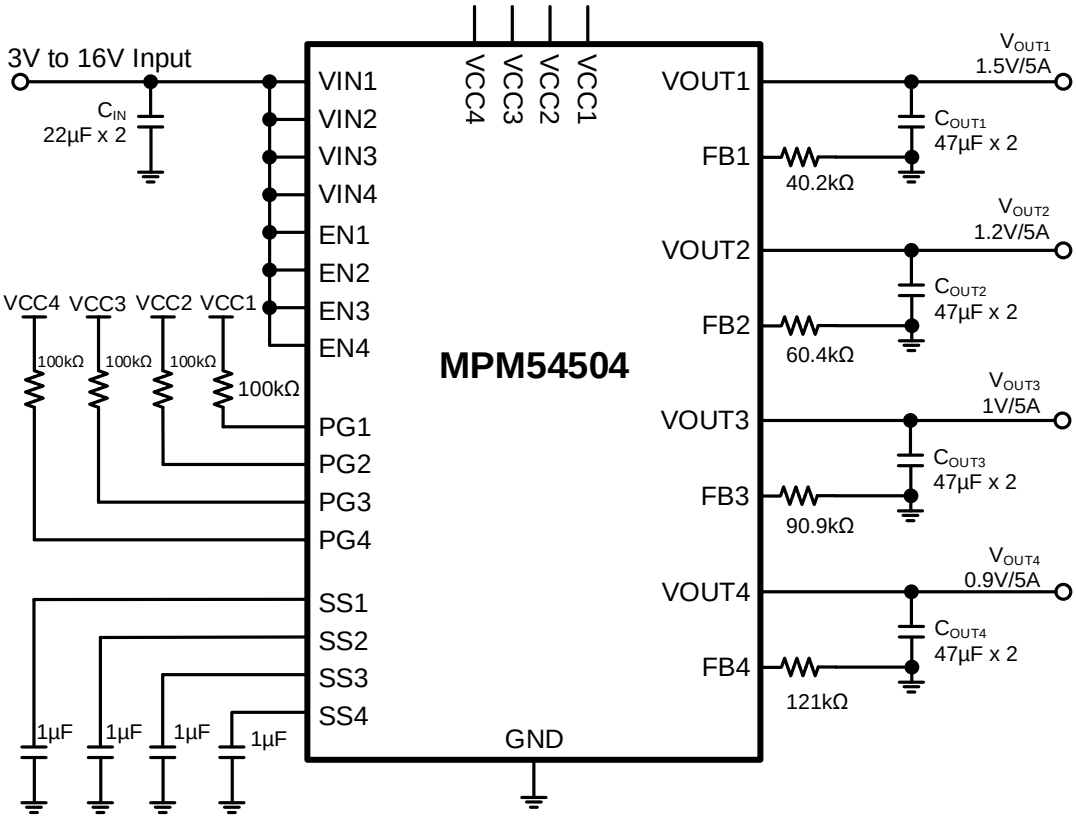
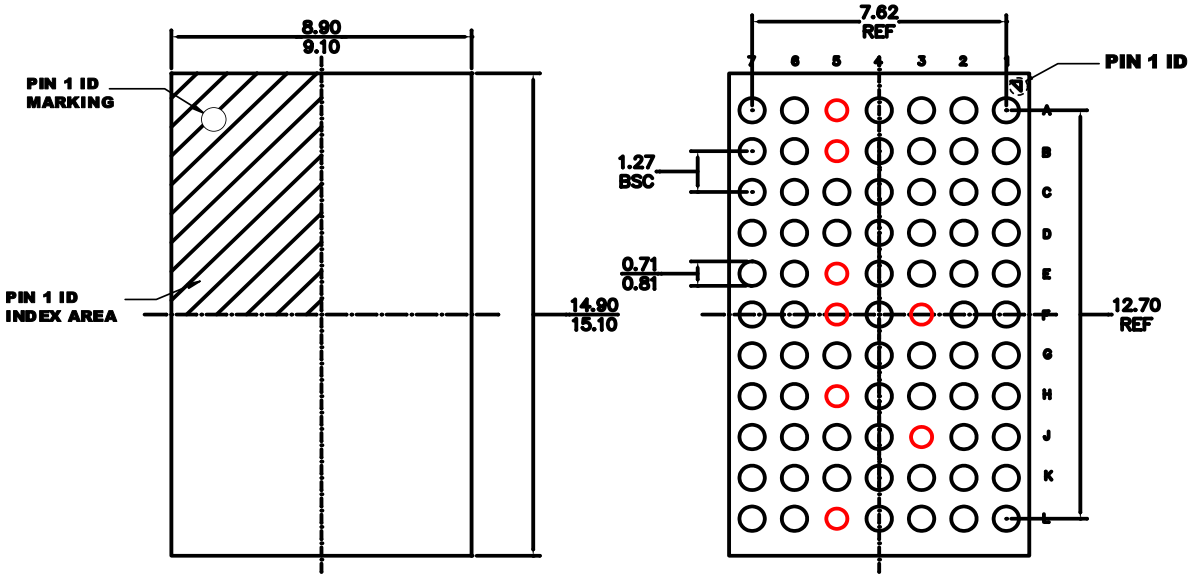


Figure 8: 3V to 16V Input, Quad (1.2V, 1.5V, 0.9V, and 1.0V) Outputs

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

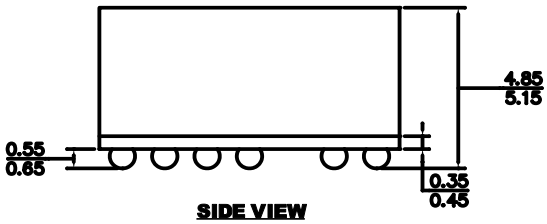
PACKAGE INFORMATION

BGA (9mmx15mmx5mm)

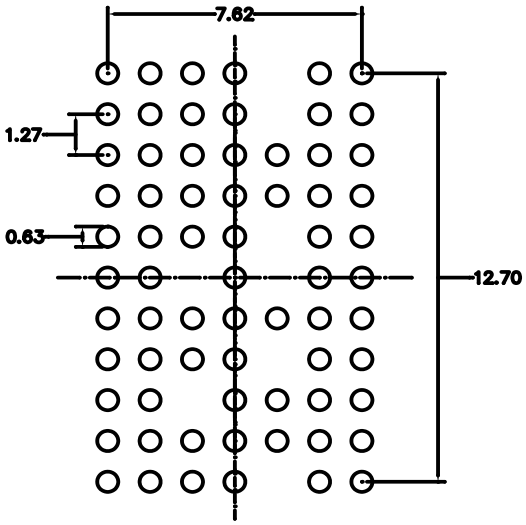


TOP VIEW

BOTTOM VIEW



SIDE VIEW



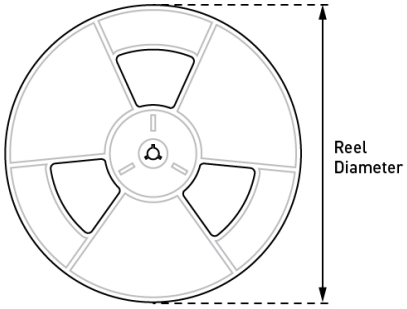
RECOMMENDED LAND PATTERN

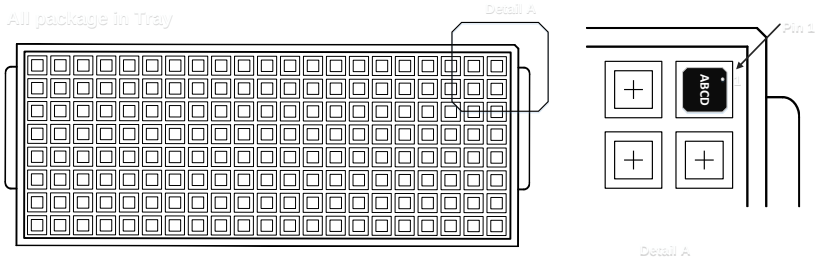
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) RED CIRCLE MEANS TEST PAD,NO BALL ON PAD FOR BOTTOM VIEW.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-275.
5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM54504GBS–T	BGA (9mmx15mmx5mm)	N/A	N/A	170	N/A	N/A	N/A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/19/2021	Initial Release	-

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.