User's Guide

TPS56637 Buck Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS56637 as well as support documentation for the TPS56637EVM-029 evaluation module. Included are the performance specifications, schematic, and the bill of materials of the TPS56637EVM-029.

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1 Introduction

The TPS56637 is an adaptive on-time D-CAP3™ mode synchronous step-down DC/DC converter, being able to deliver 6-A continuous output current. This switch mode power supply (SMPS) IC is optimized for applications requiring very low power consumption, such as printers, DTV and monitor, by providing an Eco-mode™ (pulse-skipping). The TPS56637 integrates 30-V capable MOSFETs which is suitable for applications working from 24-V bus power lines. D-CAP3™ mode provides an easy-to-design, stable regulation with very little external components, and it supports cost-effective ceramic capacitors. To widen more applications, the TPS56637 device provides both FCCM and Eco-mode for selection at light-load operation. In addition, D-CAP3 mode output can support up to 13 V. Table 1-1 shows the rated input voltage and output current ranges for the evaluation module.

The TPS56637EVM-029 evaluation module (EVM) is a single, synchronous buck converter providing 5 V at 6 A from 4.5-V to 28-V input. This user's guide describes the TPS56637EVM-029 performance.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage (V_{IN}) RANGE	OUTPUT CURRENT (I_{OUT}) RANGE
TPS56637EVM-029	4.5 V to 28 V	0 A to 6 A

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2 Performance Specification Summary

A summary of the TPS56637EVM-029 performance specifications is provided in Table 2-1. Specifications are given for an input voltage of V_{IN} = 24 V and an output voltage of 5 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2-1. TPS56637EVM-029 Performance Specifications Summary

SPECIFICATIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range (V_{IN})		4.5	24	28	V
Output voltage			5		V
Operating frequency	V_{IN} = 24 V, I_O = 6A		500		kHz
Output current range		0		6	A
Output ripple voltage	V_{IN} = 24 V, I_O = 6 A		30		mV_{PP}
Maximum efficiency	V_{IN} = 24V, I_O= 3 A		92		%

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3 Modifications

These evaluation modules are designed to provide access to the features of the TPS56637. Some modifications can be made to this module.

3.1 Output Voltage Setpoint

To change the output voltage of the EVMs, it is necessary to change the value of resistor R6. Changing the value of R6 can change the output voltage above 0.6 V. The value of R6 for a specific output voltage can be calculated using Equation 1.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R6}{R7}\right) \quad (1)$$

Table 3-1 lists the R6 values for some common output voltages.

Table 3-1. Recommended Component Values

OUTPUT VOLTAGE(1) (V)	R6(2) (kΩ)	R7 (kΩ)	L1 (µH)	C_{OUT} (3) (µF)			C9 (pF)(4)	R8 (kΩ)(4)
				MIN	TYP	MAX		
1.05	7.5	10.0	1	30	35	100		
1.2	10	10.0	1	30	35	100		
1.8	20	10.0	1.2	30	35	100		
3.3	45.3	10.0	2.2	20	35	100	100 to 220	20
5	73.2	10.0	3.3	20	30	100	100 to 220	20
12	191	10.0	5.6	25	30	100	100 to 220	20

(1) Please use the recommended L1 and C_{OUT} combination of the higher and closest output rail for unlisted output rails.
(2) R6=0Ω for V_{OUT}=0.6V
(3) C_{OUT} is the sum of effective output capacitance. In this datasheet the effective capacitance is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. A careful study of bias and temperature variation of any capacitor bank should be made in order to ensure that the minimum value of effective capacitance is provided. Refer to the information of DC bias and temperature characteristics from manufacturers of ceramic capacitors.
(4) R8 and C9 can be used to improve the load transient response or improve the loop-phase margin. The application report Optimizing Transient Response of Internally Compensated DCDC Converters with Feed-forward Capacitor is helpful when experimenting with a feed-forward capacitor.

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4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS56637EVM-029. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up, and switching frequency.

4.1 Input/Output Connections

Table 4-1 shows the provided input/output connectors and test points on the TPS56637EVM-029. A power supply capable of supplying 6 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 6 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP8 is used to monitor the output voltage with TP9 as the ground reference.

Table 4-1. Connection and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1-1 for V_{IN} range)
J2	V_{OUT}, 5 V at 6-A maximum
J3	EN control. Connect EN to GND to disable
TP1	V_{IN} test point at V_{IN} connector
TP2	GND test point at V_{IN} connector
TP3	GND test point at V_{IN} connector
TP4	Switch node test point
TP5	Power good (PG) test point
TP6	Test point provided to connect external voltage source for PG pullup
TP7	Test point between voltage divider network and output. Used for loop response measurements
TP8	Output voltage test point at V_{OUT} connector
TP9	GND test point near the AGND

4.2 Start-Up Procedure

1. Ensure that the jumper at J3 (Enable control) pins 1 and 2 are covered to shunt EN to GND, disabling the output.
2. Apply appropriate V_{IN} voltage to VIN (J1-1) and GND (J1-2).
3. Move the jumper at J3 (Enable control) away from pins 2 and 1 (EN and GND) to enable the output.

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5 Board Layout

This section provides a description of the TPS56637EVM-029, board layout, and layer illustrations.

5.1 Layout

The board layouts for the TPS56637EVM-029 are shown in Figure 5-3, Figure 5-4 and Figure 5-7. The top layer contains the main power traces for VIN, VOUT, and ground. Also on the top layer are connections for the pins of the TPS56637 and a large area filled with ground. Most of the signal traces are also located on the top side. The input decoupling capacitors, C1, C2, and C3 are located as close to the IC as possible. The input and output connectors, test points, and all of the components are located on the top side. GND layer 1, GND layer 2, and the bottom layer are predominantly power ground planes. Analog ground (AGND) area is provided on GND layer 1, GND layer 2, and the bottom layer. Figure 5-7 shows the analog ground (AGND) and power ground (PGND) are connected at a single point on the bottom layer. The bottom layer contains the output voltage feedback trace as well as a connection to the VIN pin of the EN control.

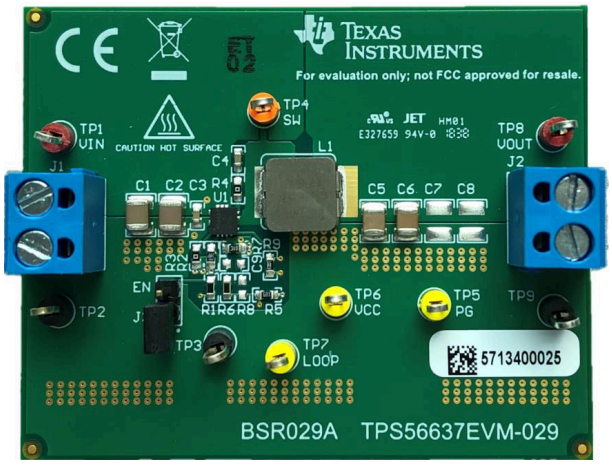


Figure 5-1. TPS56637EVM-029 Front Photo

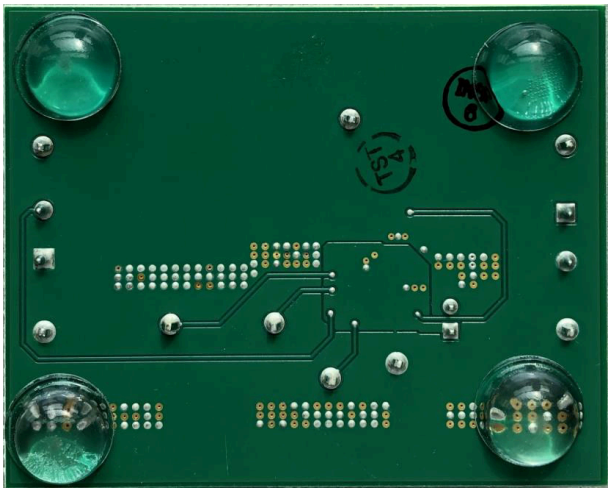


Figure 5-2. TPS56637EVM-029 Back Photo

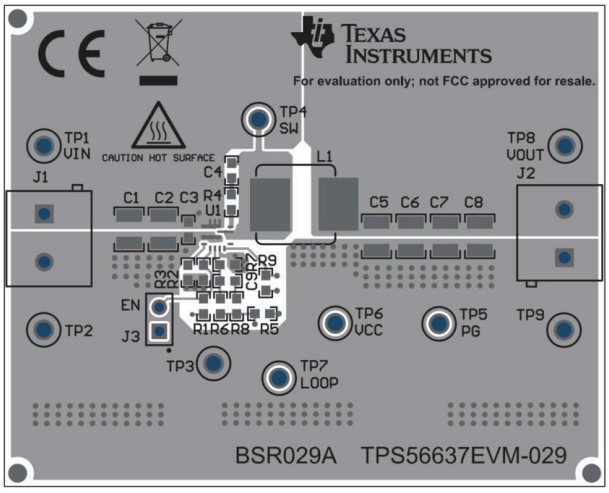


Figure 5-3. Top Assembly

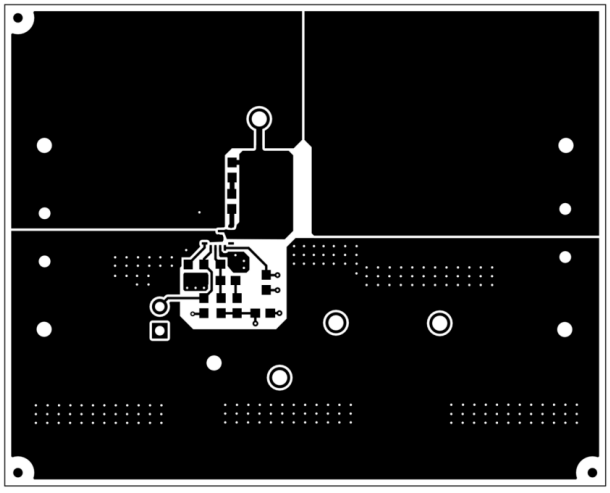


Figure 5-4. Top Layer

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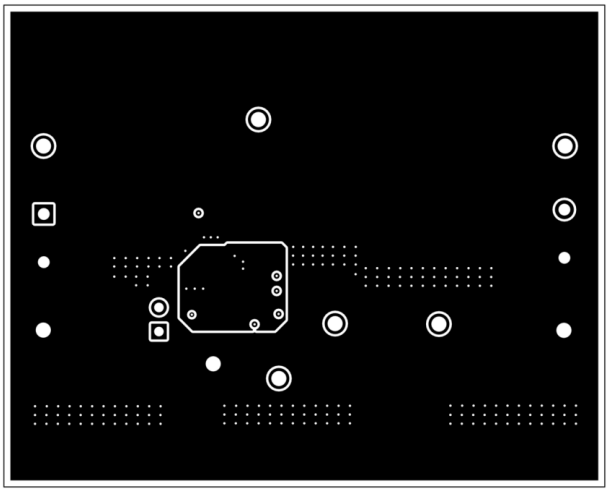


Figure 5-5. GND Layer 1

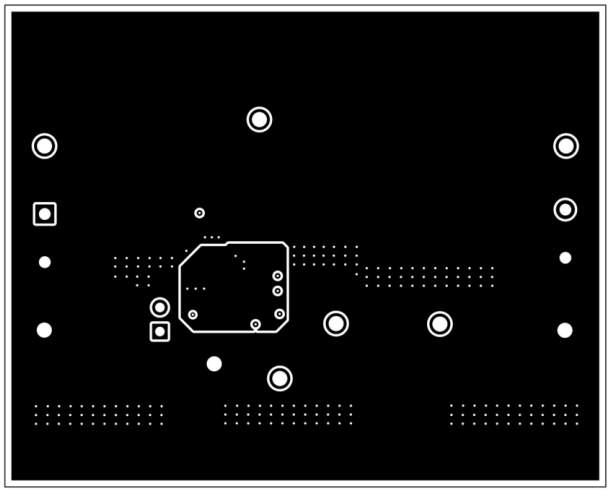


Figure 5-6. GND Layer 2

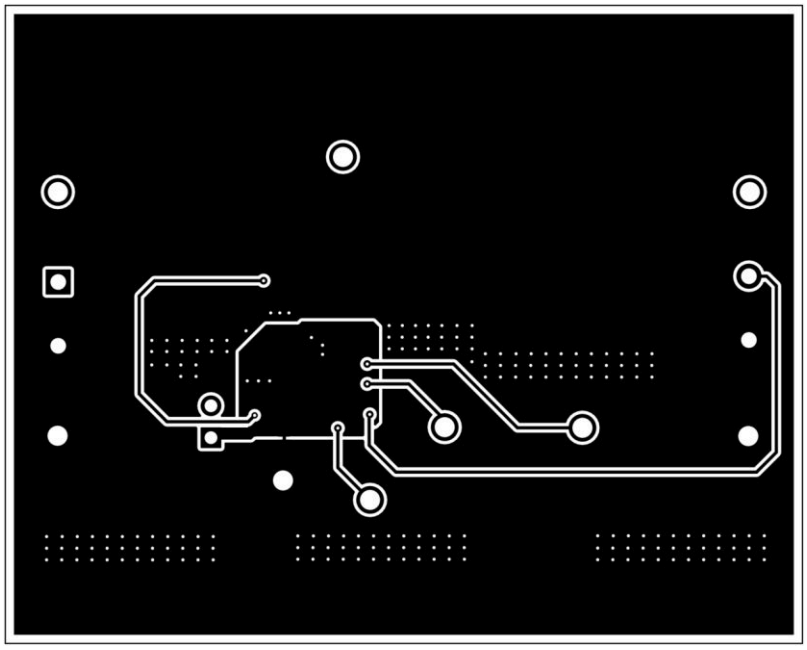


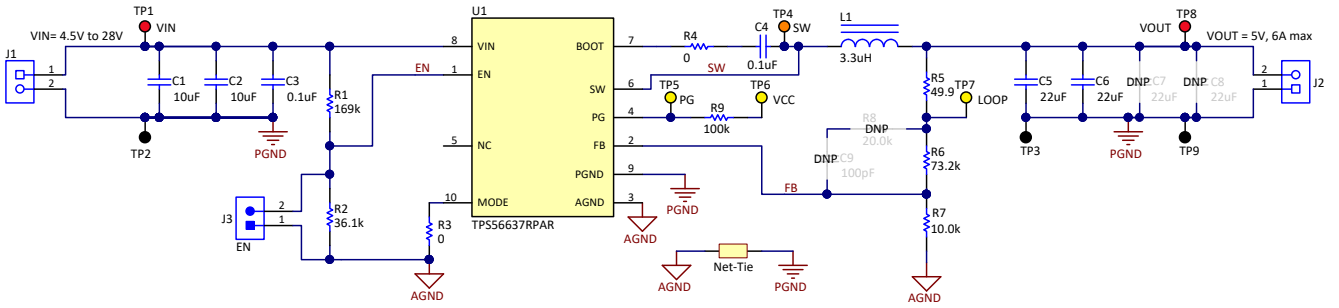
Figure 5-7. Bottom Layer

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6 Schematic, List of Materials, and Reference

6.1 Schematic

Figure 6-1 is the schematic for the TPS56637EVM-029.



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Figure 6-1. TPS56637EVM-029 Schematic Diagram

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6.2 List of Materials

Table 6-1. List of Materials

Designator	QTY	Description	Part Number	Manufacturer
PCB	1	Printed circuit board, 2000 mil x 2500 mil	BSR029	Any
C1, C2	2	Capacitor, ceramic, 10 µF, 35V, +10/%, X7R, 1210	GRM32ER7YA106KA12L	Murata
C3, C4	2	Capacitor, ceramic, 0.1 µF, 50V, +10/%, X7R, 0603	885012206095	Wurth Elektronik
C5, C6	2	Capacitor, ceramic, 22 µF, 25 V, ±10%, X7R, 1210	GRM32ER71E226KE15L	Murata
H9, H10, H11, H12	4	Bumpon, transparent, hemisphere, 0.44 X 0.20, clear	SJ-5303 (CLEAR)	3M
J1, J2	2	Terminal block, 5.08 mm, 2 x 1, brass, TH	ED120/2DS	On-Shore Technology
J3	1	Header, 100 mil, 2 x 1, gold, TH	TSW-102-07-G-S	Samtec
L1	1	Inductor, shielded, powdered iron, 3.3 uH, 9.7 A, 0.0149 Ω, SMD	IHLP3232DZER3R3M11	Vishay-Dale
R1	1	Resistor, 169 kΩ, 0.1%, 0.1 W, 0603	RT0603BRD07169KL	Yageo America
R2	1	Resistor, 36.1 kΩ, 0.1%, 0.1 W, 0603	RT0603BRD0736K1L	Yageo America
R3, R4	2	Resistor, 0 Ω, 5%, 0.1 W, 0603	CRCW06030000Z0EA	Vishay-Dale
R5	1	Resistor, 49.9 Ω, 0.5%, 0.1 W, 0603	RT0603DRE0749R9L	Yageo America
R6	1	Resistor, 73.2 kΩ, 0.1%, 0.1 W, 0603	RG1608P-7322-B-T5	Susumu Co Ltd
R7	1	Resistor, 10.0 kΩ, 0.1%, 0.1 W, 0603	RT0603BRD0710KL	Yageo America
R9	1	Resistor, 100 kΩ, 1%, 0.1 W, 0603	CRCW0603100KFKEA	Vishay-Dale
TP1, TP8	2	Test point, multipurpose, red, TH	5010	Keystone
TP2, TP3, TP9	3	Test point, multipurpose, black, TH	5011	Keystone
TP4	1	Test point, multipurpose, orange, TH	5013	Keystone
TP5, TP6, TP7	3	Test point, multipurpose, yellow, TH	5014	Keystone
U1	1	4.5-V to 28-V Input, 6-A Synchronous Buck Converter with ULQ-mode, RPA0010A (VQFN-HR-10)	TPS56637-RPA	Texas Instruments
C7, C8	0	Capacitor, ceramic, 22 µF, 25 V, ±10%, X7R, 1210	GRM32ER71E226KE15L	Murata
C9	0	Capacitor, ceramic, 100 pF, 25 V, ±10%, X7R, 0603	GCM1885C1H680JA16D	Murata
R8	0	Resistor, 20.0 kΩ, 0.5%, 0.1 W, 0603	RT0603DRE0720KL	Yageo America
FID1, FID2, FID3	0	Fiducial mark. There is nothing to buy or mount.	N/A	N/A

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6.3 Reference

1. Texas Instruments, *TPS56637 4.5-V to 28-V Input, 6-A Synchronous Buck Converter With ULQ-Mode™ Data Sheet*

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2019) to Revision B (June 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated user's guide title	2

Changes from Revision * (May 2018) to Revision A (September 2019)	Page
• Added TPS56637EVM-029 board images	6

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