Quasi-Resonant PWM controller ICE2QS03G

Off-Line SMPS Quasi-Resonant PWM Controller with integrated 500V Startup cell in DSO8

Data Sheet
V2.3 2014-03-06

Power Management & Multimarket

Edition 2014-03-06

Published by Infineon Technologies AG,

81726 Munich, Germany.

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Revision History

Major changes since previous revision

Date	Version	Changed By	Change Description
2014-03-06	2.3		Added $V_{VCCPD,}$ and marking drawing. Removed V_{OUT}. Revised typo, $I_{VCCcharge1}$, $I_{VCCcharge2}$, I_{ZCMAX}, outline dimension drawing and upgrade to -40°C operating temperature

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Off-Line SMPS Quasi-Resonant PWM Controller with integrated 500V startup cell in DSO8

Product Highlights

- **Active burst mode for low standby power**
- **Quasi resonant operation**
- **Digital frequency reduction for better overall system efficiency**
- **Integrated 500V startup cell**
- **Pb-free lead plating, halogen free mold compound, RoHS compliant**

PG-DSO-8

Features

- Quasi resonant operation till very low load
- Active burst mode operation at light/no load for low standby input power (< 100mW)
- Digital frequency reduction with decreasing load
- Startup cell for VCC pre-charging with constant current
- Built-in digital soft-start
- Foldback correction and cycle-by-cycle peak current limitation
- Auto restart mode for VCC Over-voltage protection, VCC Under-voltage protection and open loop/over-load protection
- Latch-off mode for adjustable output over-voltage protection and short-winding protection

Description

ICE2QS03G is a quasi-resonant PWM controller optimized for off-line switch power supply. The digital frequency reduction with decreasing load enables a quasi-resonant operation till very low load. As a result, the overall system efficiency is significantly improved compared to other conventional solutions. The active burst mode operation enables ultra-low power consumption at standby mode with small and controllable output voltage ripple. Based on the BiCMOS technology, the product has a wide operation range (up to 25V) of IC power supply and lower power consumption. The numerous protection functions give a full protection of the power supply system in failure situations. All of these make the ICE2QS03G an outstanding controller for quasi-resonant flyback converter in the market.

Applications

- Adapter/Charger,
- LCD monitor, DVD R/W, DVD Combo, Blue-ray/DVD player, Set-top box,
- Auxiliary power supply for CRT TV, LCD TV, PC, Server, Printer, TV, Home theater/Audio System, etc.

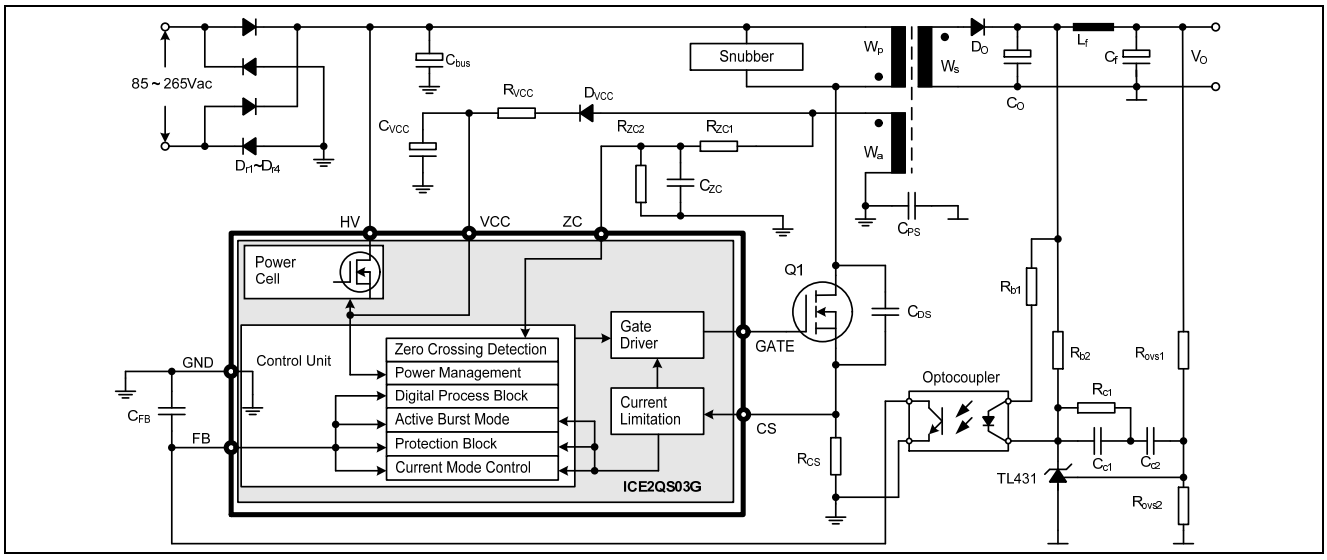


Figure 1 Typical Application

Type	Package	Marking
ICE2QS03G	PG-DSO-8	2QS03G

1 Pin Configuration and Functionality

1.1 Pin Configuration with PG-DSO-8

Table 1 Pin configuration

Pin	Symbol	Function
1	ZC	Zero Crossing
2	FB	Feedback
3	CS	Current Sense
4	GATE	Gate Drive Output
5	HV	High Voltage input
6	N.C.	Not Connected
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

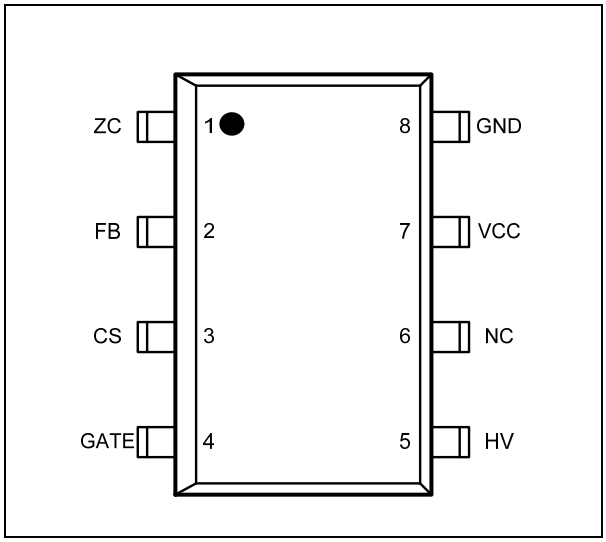


Figure 2 Pin configuration PG-DSO-8 (top view)

1.2 Pin Functionality

ZC (Zero Crossing)

At this pin, the voltage from the auxiliary winding after a time delay circuit is applied. Internally, this pin is connected to the zero-crossing detector for switch-on determination. Additionally, the output overvoltage detection is realized by comparing the voltage Vzc with an internal preset threshold.

FB (Feedback)

Normally an external capacitor is connected to this pin for a smooth voltage V_{FB}. Internally this pin is connected to the PWM signal generator block for switch-off determination (together with the current sensing signal), to the digital signal processing block for the frequency reduction with decreasing load during normal operation, and to the Active Burst Mode controller block for entering Active Burst Mode operation determination and burst ratio control during Active Burst Mode operation. Additionally, the open-loop / over-load protection is implemented by monitoring the voltage at this pin.

CS (Current Sense)

This pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the feedback voltage) internally. Moreover, short-winding protection is realized by monitoring the voltage V_{cs} during on-time of the main power switch.

GATE (Gate Drive Output)

This output signal drives the external main power switch, which is a power MOSFET in most case.

HV (High Voltage)

The pin HV is connected to the bus voltage externally and to the startup cell internally. The current through this pin pre-charges the VCC capacitor with constant current once the supply bus voltage is applied.

VCC (Power supply)

VCC pin is the positive supply of the IC. The operating range is between V_{VCCoff} and V_{VCCOVP}.

GND (Ground)

This is the common ground of the controller.

2 Representative Block Diagram

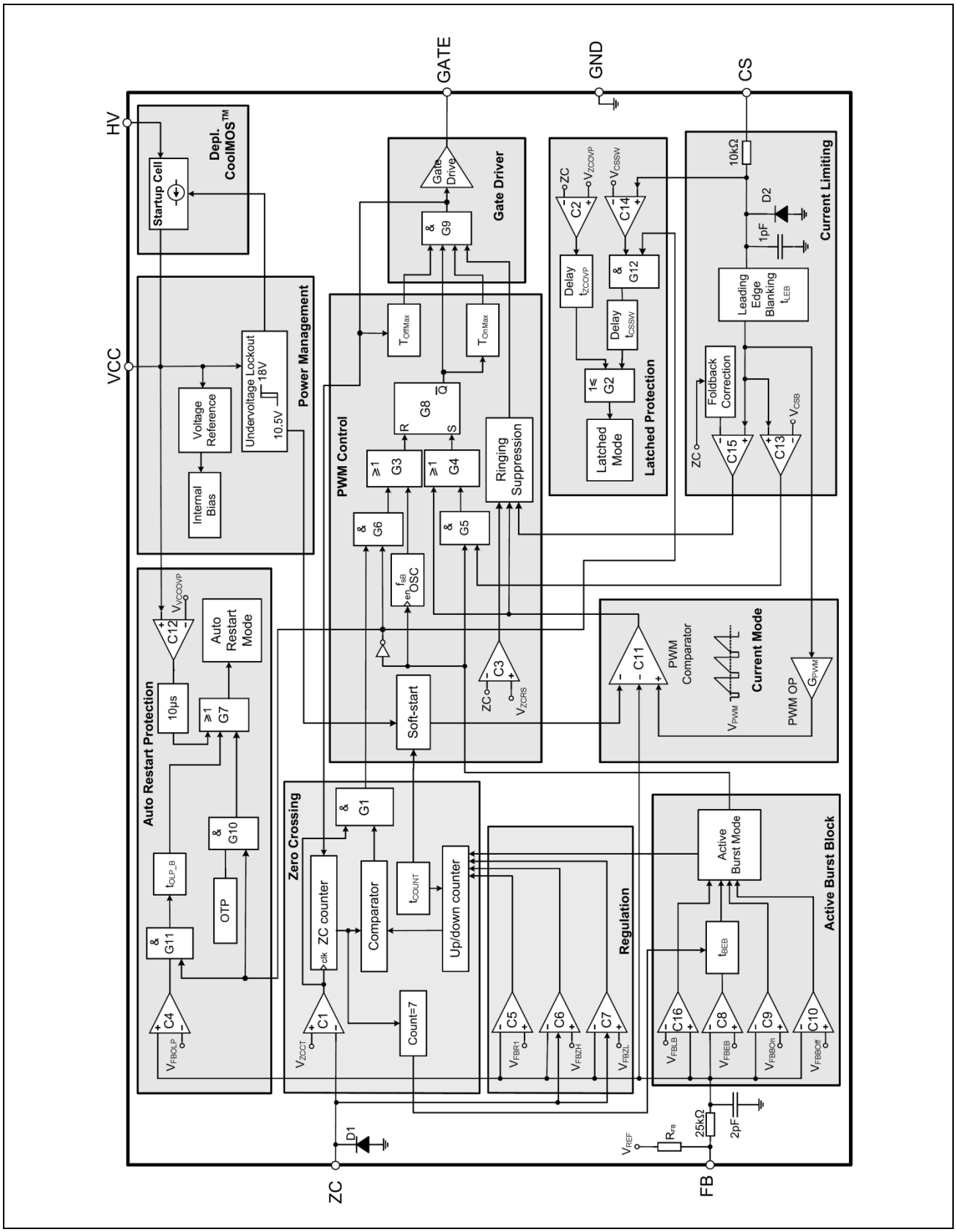


Figure 3 Representative Block Diagram

3 Functional Description

3.1 VCC Pre-Charging and Typical VCC Voltage During Start-up

In ICE2QS03G, a high voltage startup cell is integrated. As shown in Figure 3, the start cell consists of a high voltage device and a controller, whereby the high voltage device is controlled by the controller. The startup cell provides a pre-charging of the VCC capacitor till VCC voltage reaches the VCC turned-on threshold V_{VCCon} and the IC begins to operate.

Once the mains input voltage is applied, a rectified voltage shows across the capacitor C_{bus}. The high voltage device provides a current to charge the VCC capacitor C_{vcc}. Before the VCC voltage reaches a certain value, the amplitude of the current through the high voltage device is only determined by its channel resistance and can be as high as several mA. After the VCC voltage is high enough, the controller controls the high voltage device so that a constant current around 1mA is provided to charge the VCC capacitor further, until the VCC voltage exceeds the turned-on threshold V_{VCCon}. As shown as the time phase I in Figure 4, the VCC voltage increase near linearly and the charging speed is independent of the mains voltage level.

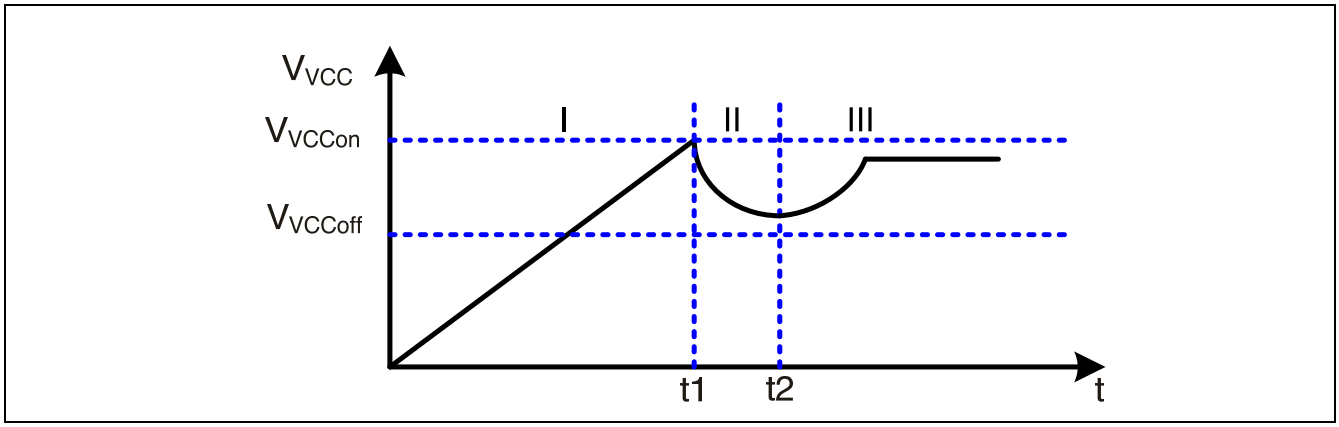


Figure 4 VCC voltage at start up

The time taking for the VCC pre-charging can then be approximately calculated as:

$$t_1 = \frac{V_{VCCon} \cdot C_{VCC}}{I_{VCCcharge2}} \qquad [1]$$

where $I_{VCCcharge2}$ is the charging current from the startup cell which is 1.05mA, typically.

When the VCC voltage exceeds the VCC turned-on threshold V_{VCCon} at time t_1, the startup cell is switched off and the IC begins to operate with soft-start. Due to power consumption of the IC and the fact that there is still no energy from the auxiliary winding to charge the VCC capacitor before the output voltage is built up, the VCC voltage drops (Phase II). Once the output voltage is high enough, the VCC capacitor receives the energy from the auxiliary winding from the time point t_2 onward. The VCC then will reach a constant value depending on output load.

3.2 Soft-start

As shown in Figure 5, at the time t_{on}, the IC begins to operate with a soft-start. By this soft-start the switching stresses for the switch, diode and transformer are minimized. The soft-start implemented in ICE2QS03G is a digital time-based function. The preset soft-start time is t_{SS} (12ms**)** with 4 steps. If not limited by other functions, the peak voltage on CS pin will increase step by step from 0.32V to 1V finally.

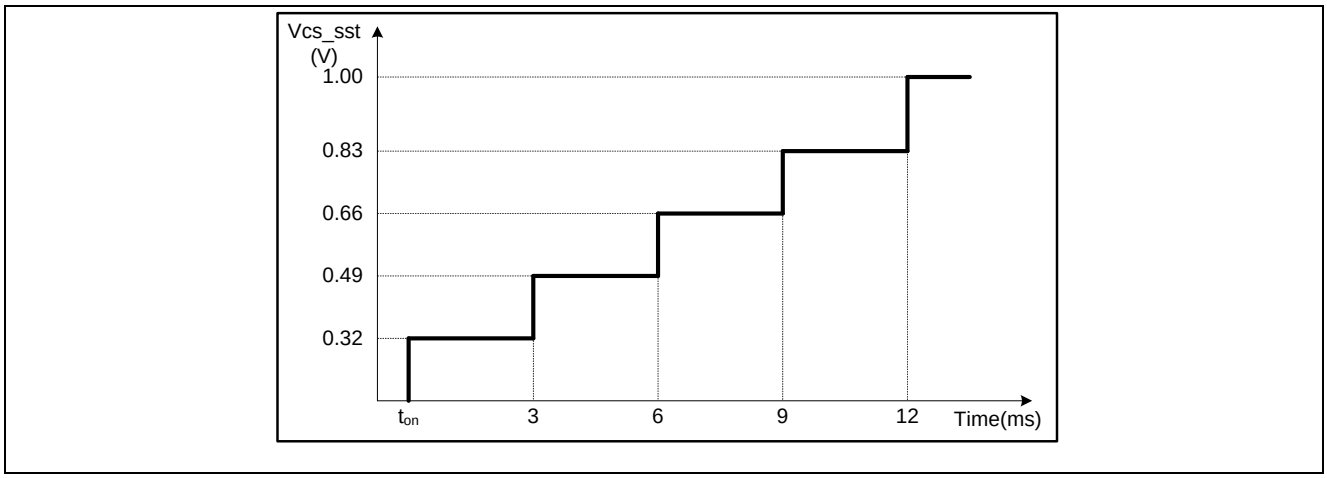


Figure 5 Maximum current sense voltage during soft start

3.3 Normal Operation

The PWM controller during normal operation consists of a digital signal processing circuit including an up/down counter, a zero-crossing counter (ZC counter) and a comparator, and an analog circuit including a current measurement unit and a comparator. The switch-on and -off time points are each determined by the digital circuit and the analog circuit, respectively. As input information for the switch-on determination, the zero-crossing input signal and the value of the up/down counter are needed, while the feedback signal V_{FB} and the current sensing signal V_{CS} are necessary for the switch-off determination. Details about the full operation of the PWM controller in normal operation are illustrated in the following paragraphs.

3.3.1 Digital Frequency Reduction

As mentioned above, the digital signal processing circuit consists of an up/down counter, a ZC counter and a comparator. These three parts are key to implement digital frequency reduction with decreasing load. In addition, a ringing suppression time controller is implemented to avoid mis-triggering by the high frequency oscillation, when the output voltage is very low under conditions such as soft start period or output short circuit. Functionality of these parts is described as in the following.

3.3.1.1 Up/down counter

The up/down counter stores the number of the zero crossing where the main power switch is switched on after demagnetization of the transformer. This value is fixed according to the feedback voltage, V_{FB}, which contains information about the output power. Indeed, in a typical peak current mode control, a high output power results in a high feedback voltage, and a low output power leads to a low regulation voltage. Hence, according to V_{FB}, the value in the up/down counter is changed to vary the power MOSFET off-time according to the output power. In the following, the variation of the up/down counter value according to the feedback voltage is explained.

The feedback voltage V_{FB} is internally compared with three threshold voltages V_{FBZL}, V_{FBZH} and V_{FBR1}, at each clock period of 48ms. The up/down counter counts then upward, keep unchanged or count downward, as shown in Table 2.

Table 2 Operation of the up/down counter

V_{FB}	up/down counter action
Always lower than V_{FBZL}	Count upwards till 7
Once higher than V_{FBZL}, but always lower than V_{FBZH}	Stop counting, no value changing
Once higher than V_{FBZH}, but always lower than V_{FBR1}	Count downwards till 1
Once higher than V_{FBR1}	Set up/down counter to 1

In the ICE2QS03G, the number of zero crossing is limited to 7. Therefore, the counter varies between 1 and 7, and any attempt beyond this range is ignored. When V_{FB} exceeds V_{FBR1} voltage, the up/down counter is reset to 1, in order to allow the system to react rapidly to a sudden load increase. The up/down counter value is also reset to 1 at the start-up time, to ensure an efficient maximum load start up. Figure 6 shows some examples on how up/down counter is changed according to the feedback voltage over time.

The use of two different thresholds V_{FBZL} and V_{FBZH} to count upward or downward is to prevent frequency jittering when the feedback voltage is close to the threshold point. However, for a stable operation, these two thresholds must not be affected by the foldback current limitation (see section 3.4.1), which limits the V_{CS} voltage. Hence, to prevent such situation, the threshold voltages, V_{FBZL} and V_{FBZH}, are changed internally depending on the line voltage levels.

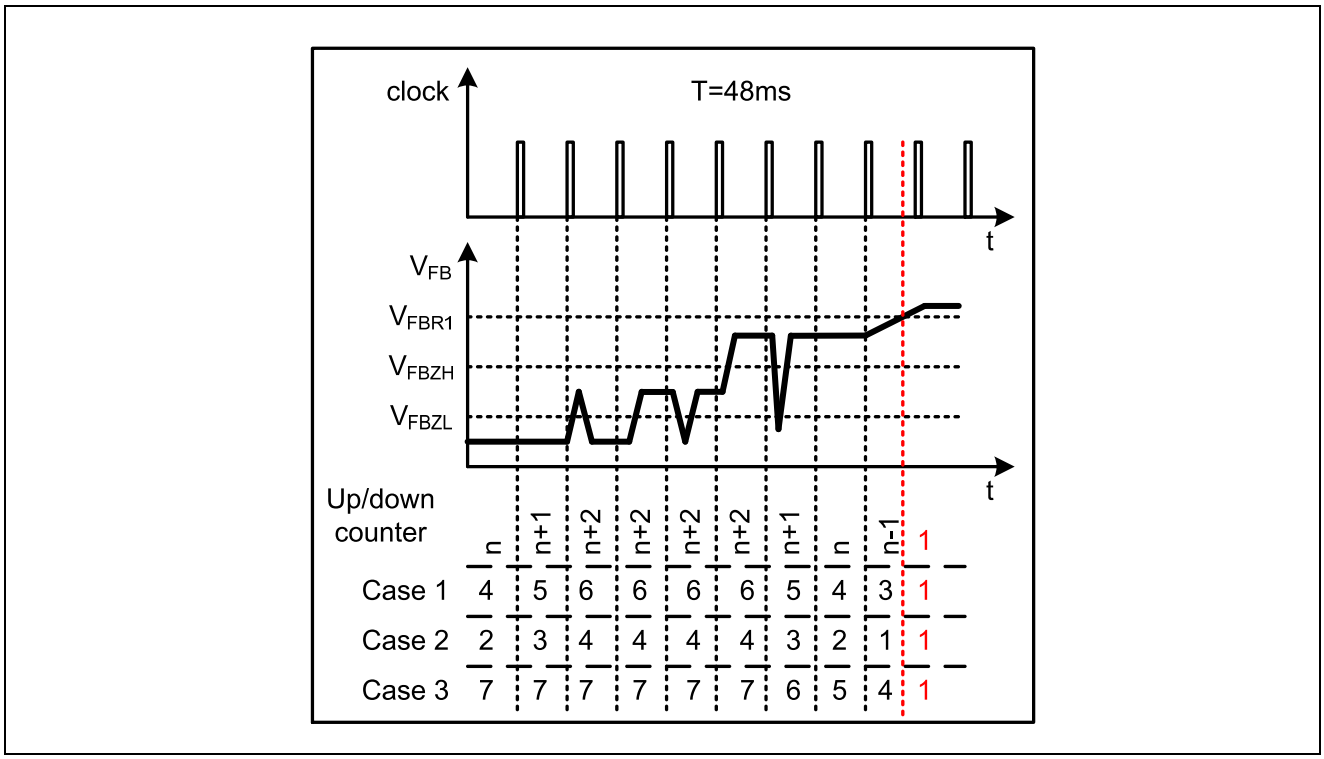


Figure 6 Up/down counter operation

3.3.1.2 Zero crossing (ZC counter)

In the system, the voltage from the auxiliary winding is applied to the zero-crossing pin through a RC network, which provides a time delay to the voltage from the auxiliary winding. Internally this pin is connected to a clamping network, a zero-crossing detector, an output overvoltage detector and a ringing suppression time controller.

During on-state of the power switch a negative voltage applies to the ZC pin. Through the internal clamping network, the voltage at the pin is clamped to certain level.

The ZC counter has a minimum value of 0 and maximum value of 7. After the internal MOSFET is turned off, every time when the falling voltage ramp of on ZC pin crosses the V_{ZCCT} (100mV) threshold, a zero crossing is detected and ZC counter will increase by 1. It is reset every time after the DRIVER output is changed to high.

The voltage V_{ZC} is also used for the output overvoltage protection. Once the voltage at this pin is higher than the threshold V_{ZCOVP} during off-time of the main switch, the IC is latched off after a fixed blanking time.

To achieve the switch-on at voltage valley, the voltage from the auxiliary winding is fed to a time delay network (the RC network consists of D_{zc}, R_{zc1}, R_{zc2} and C_{zc} as shown in Figure 1) before it is applied to the zero-crossing detector through the ZC pin. The needed time delay to the main oscillation signal Δt should be approximately one fourth of the oscillation period, T_{osc} (by transformer primary inductor and drain-source capacitor) minus the propagation delay from the detected zero-crossing to the switch-on of the main switch t_{delay}.

$$\Delta t = \frac{T_{osc}}{4} - t_{delay} \quad [2]$$

This time delay should be matched by adjusting the time constant of the RC network which is calculated as:

$$\tau_{td} = C_{zc} \cdot \frac{R_{zc1} \cdot R_{zc2}}{R_{zc1} + R_{zc2}} \quad [3]$$

3.3.2 Ringing suppression time

After MOSFET is turned off, there will be some oscillation on V_{DS}, which will also appear on the voltage on ZC pin. To avoid mis-triggering by such oscillations to turn on the MOSFET, a ringing suppression timer is implemented. This suppression time is depended on the voltage V_{ZC}. If the voltage V_{ZC} is lower than the threshold V_{ZCRS}, a longer preset time t_{ZCRS2} is applied. However, if the voltage V_{ZC} is higher than the threshold, a shorter time t_{ZCRS1} is set.

3.3.2.1 Switch on determination

After the gate drive goes to low, it cannot be changed to high during ring suppression time.

After ring suppression time, the gate drive can be turned on when the ZC counter value is higher or equal to up/down counter value.

However, it is also possible that the oscillation between primary inductor and drain-source capacitor damps very fast and IC cannot detect enough zero crossings and ZC counter value will not be high enough to turn on the gate drive. In this case, a maximum off time is implemented. After gate drive has been remained off for the period of T_{OffMax}, the gate drive will be turned on again regardless of the counter values and V_{ZC}. This function can effectively prevent the switching frequency from going lower than 20kHz. Otherwise it will cause audible noise during start up.

3.3.3 Switch Off Determination

In the converter system, the primary current is sensed by an external shunt resistor, which is connected between low-side terminal of the main power switch and the common ground. The sensed voltage across the shunt resistor V_{CS} is applied to an internal current measurement unit, and its output voltage V_1 is compared with the regulation voltage V_{FB}. Once the voltage V_1 exceeds the voltage V_{FB}, the output flip-flop is reset. As a result, the main power switch is switched off. The relationship between the V_1 and the V_{CS} is described by:

$$V_1 = G_{PWM} \cdot V_{CS} + V_{PWM} \quad [4]$$

To avoid mis-triggering caused by the voltage spike across the shunt resistor at the turn on of the main power switch, a leading edge blanking time, t_{LEB}, is applied to the output of the comparator. In other words, once the gate drive is turned on, the minimum on time of the gate drive is the leading edge blanking time.

In addition, there is a maximum on time, t_{OnMax}, limitation implemented in the IC. Once the gate drive has been in high state longer than the maximum on time, it will be turned off to prevent the switching frequency from going too low because of long on time.

3.3.4 Modulated gate drive

The drive-stage is optimized for EMI consideration. The switch on speed is slowed down before it reaches the CoolMOS™ turn on threshold. That is a slope control of the rising edge at the output of driver (Figure 7). Thus the leading switch spike during turn on is minimized.

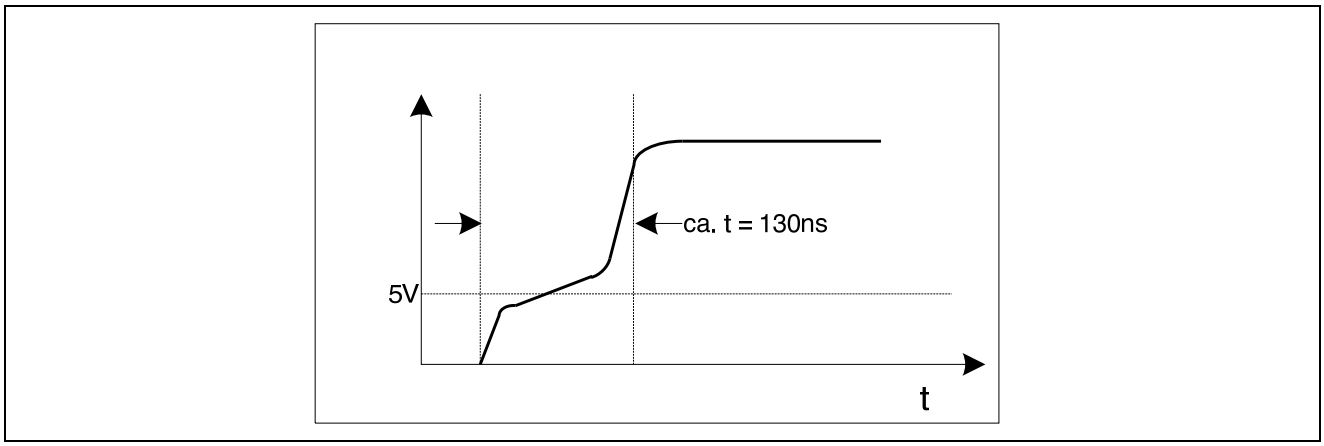


Figure 7 Gate rising waveform

3.4 Current Limitation

There is a cycle by cycle current limitation realized by the current limit comparator to provide an over-current detection. The source current of the MOSFET is sensed via a sense resistor R_{CS}. By means of R_{CS} the source current is transformed to a sense voltage V_{CS} which is fed into the pin CS. If the voltage V_{CS} exceeds an internal voltage limit, adjusted according to the Mains voltage, the comparator immediately turns off the gate drive.

To prevent the Current Limitation process from distortions caused by leading edge spikes, a Leading Edge Blanking time (t_{LEB}) is integrated in the current sensing path.

A further comparator is implemented to detect dangerous current levels (V_{CSSW}) which could occur if one or more transformer windings are shorted or if the secondary diode is shorted. To avoid an accidental latch off, a spike blanking time of t_{CSSW} is integrated in the output path of the comparator.

3.4.1 Foldback Point Correction

When the main bus voltage increases, the switch on time becomes shorter and therefore the operating frequency is also increased. As a result, for a constant primary current limit, the maximum possible output power is increased which is beyond the converter design limit.

To avoid such a situation, the internal foldback point correction circuit varies the V_{CS} voltage limit according to the bus voltage. This means the V_{CS} will be decreased when the bus voltage increases. To keep a constant maximum input power of the converter, the required maximum V_{CS} versus various input bus voltage can be calculated, which is shown in Figure 8.

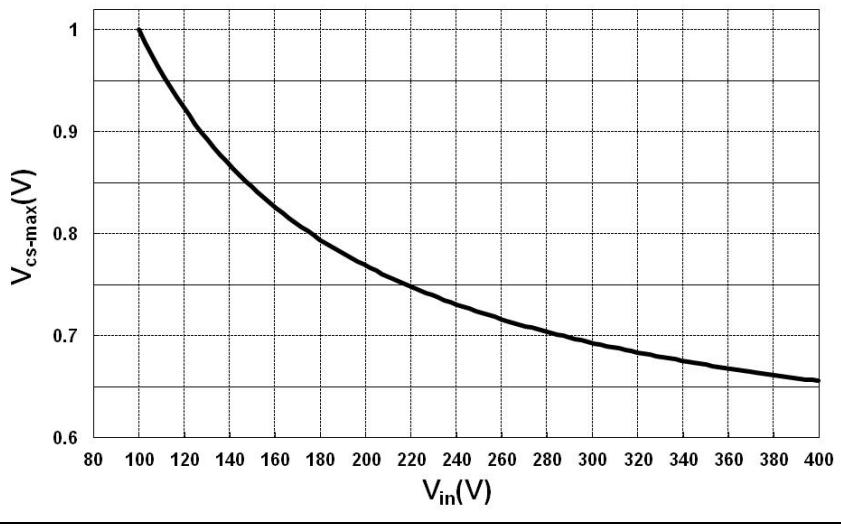


Figure 8 Variation of the V_{CS} limit voltage according to the I_{ZC} current

According to the typical application circuit, when MOSFET is turned on, a negative voltage proportional to bus voltage will be coupled to auxiliary winding. Inside ICE2QS03G, an internal circuit will clamp the voltage on ZC pin to nearly 0V. As a result, the current flowing out from ZC pin can be calculated as

$$I_{ZC} = \frac{V_{BUS} \cdot N_a}{R_{ZC1} \cdot N_p} \quad [5]$$

When this current is higher than I_{ZC_FS}, the amount of current exceeding this threshold is used to generate an offset to decrease the maximum limit on V_{CS}. Since the ideal curve shown in Figure 8 is a nonlinear one, a digital block in ICE2QS03G is implemented to get a better control of maximum output power. Additional advantage to use digital circuit is the production tolerance is smaller compared to analog solutions. The typical maximum limit on V_{CS} versus the ZC current is shown in Figure 9.

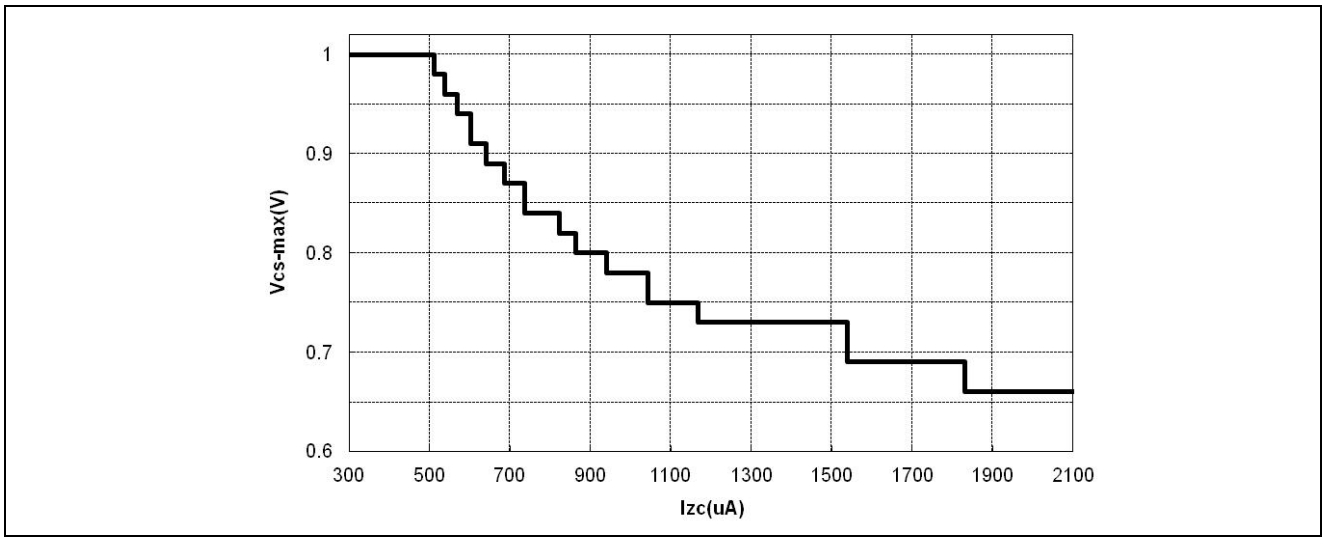


Figure 9 $V_{CS\text{-}max}$ versus I_{ZC}

3.5 Active Burst Mode Operation

At light load condition, the IC enters Active Burst Mode operation to minimize the power consumption. Details about Active Burst Mode operation are explained in the following paragraphs.

3.5.1 Entering Active Burst Mode Operation

For determination of entering Active Burst Mode operation, three conditions apply:

- the feedback voltage is lower than the threshold of V_{FBEB} (1.25V). Accordingly, the peak current sense voltage across the shunt resistor is 0.17V;
- the up/down counter is N_{ZC_ABM} (7) and
- a certain blanking time t_{BEB} (24ms).

Once all of these conditions are fulfilled, the Active Burst Mode flip-flop is set and the controller enters Active Burst Mode operation. This multi-condition determination for entering Active Burst Mode operation prevents mis-triggering of entering Active Burst Mode operation, so that the controller enters Active Burst Mode operation only when the output power is really low during the preset blanking time.

3.5.2 During Active Burst Mode Operation

After entering the Active Burst Mode the feedback voltage rises as V_{OUT} starts to decrease due to the inactive PWM section. One comparator observes the feedback signal if the voltage level V_{FBBOn} (3.6V) is exceeded. In that case the internal circuit is again activated by the internal bias to start with switching.

Turn-on of the power MOSFET is triggered by the timer. The PWM generator for Active Burst Mode operation composes of a timer with a fixed frequency of f_{sB} (52kHz, typical) and an analog comparator. Turn-off is resulted if the voltage across the shunt resistor at CS pin hits the threshold V_{csB} (0.34V). A turn-off can also be triggered if the duty ratio exceeds the maximal duty ratio D_{maxB} (50%). In operation, the output flip-flop will be reset by one of these signals which come first.

If the output load is still low, the feedback signal decreases as the PWM section is operating. When feedback signal reaches the low threshold V_{FBBOff} (3.0V), the internal bias is reset again and the PWM section is disabled until next time regulation signal increases beyond the V_{FBBOn} (3.6V) threshold. If working in Active Burst Mode the feedback signal is changing like a saw tooth between V_{FBBOff} and V_{FBBOn} shown in Figure 10.

3.5.3 Leaving Active Burst Mode Operation

The feedback voltage immediately increases if there is a high load jump. This is observed by a comparator. As the current limit is 34% during Active Burst Mode a certain load is needed so that feedback voltage can exceed V_{FBLB} (4.5V). After leaving active burst mode, maximum current can now be provided to stabilize V_O. In addition, the up/down counter will be set to 1 immediately after leaving Active Burst Mode. This is helpful to decrease the output voltage undershoot.

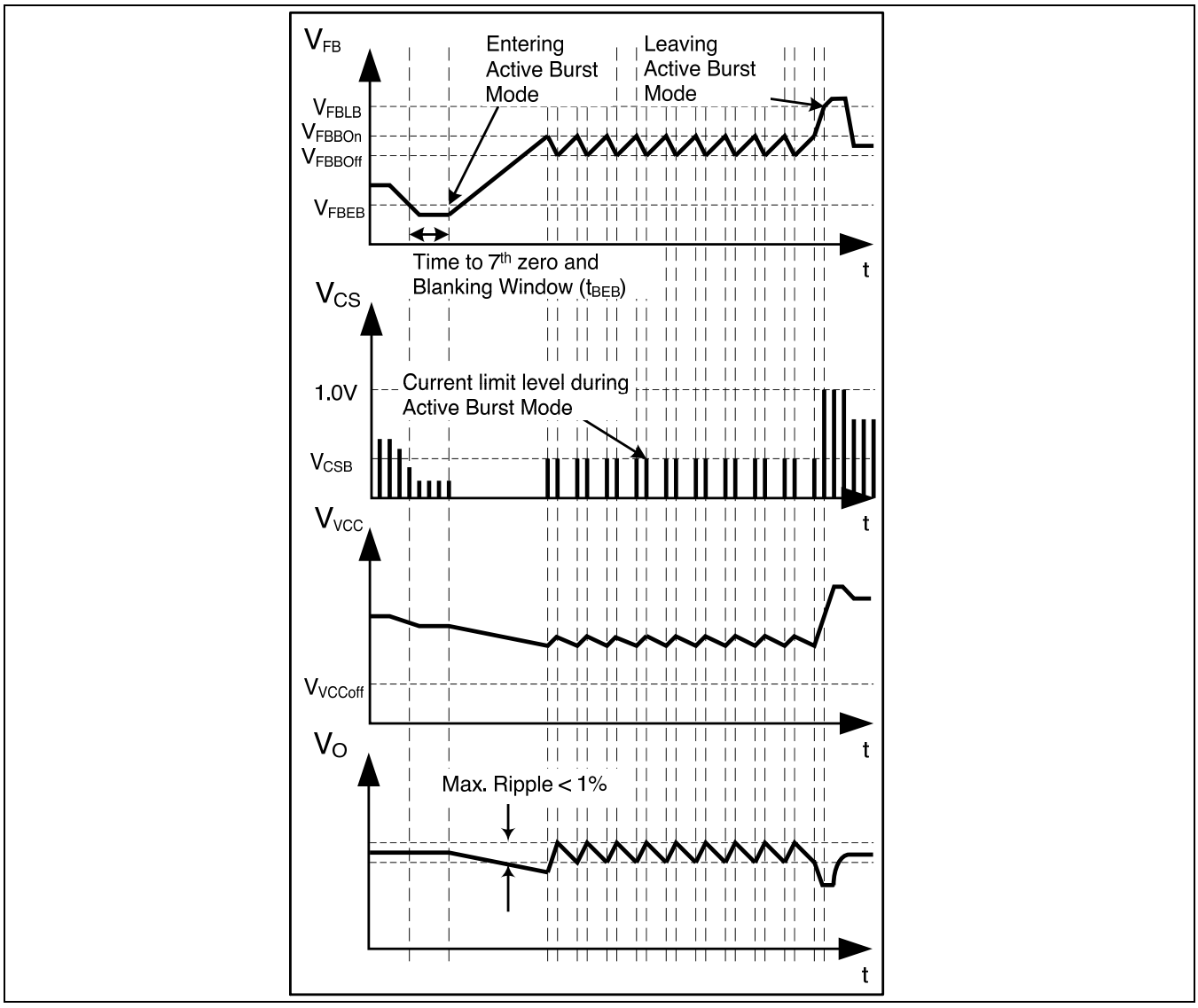


Figure 10 Signals in Active Burst Mode

3.6 Protection Functions

The IC provides full protection functions. The following table summarizes these protection functions.

Table 3 Protection features

VCC Over-voltage	Auto Restart Mode
VCC Under-voltage	Auto Restart Mode
Over-load/Open Loop	Auto Restart Mode
Over-temperature	Auto Restart Mode
Output Over-voltage	Latched Off Mode
Short Winding	Latched Off Mode

During operation, the VCC voltage is continuously monitored. In case of an under-voltage or an over-voltage, the IC is reset and the main power switch is then kept off. After the VCC voltage falls below the threshold V_{VCCoff}, the startup cell is activated. The VCC capacitor is then charged up. Once the voltage exceeds the threshold V_{VCCon}, the IC begins to operate with a new soft-start.

In case of open control loop or output over load, the feedback voltage will be pulled up. After a blanking time of t_{OLP_B} (30ms), the IC enters auto-restart mode. The blanking time here enables the converter to provide a peak power in case the increase in V_{FB} is due to a sudden load increase. This output over load protection is disabled during burst mode.

During off-time of the power switch, the voltage at the zero-crossing pin is monitored for output over-voltage detection. If the voltage is higher than the preset threshold V_{ZCOVP}, the IC is latched off after the preset blanking time t_{ZCOVP}. This latch off mode can only be reset if the Vcc < V_{VCCPD}.

If the junction temperature of IC controller exceeds T_{jCon} (130 °C), the IC enters into OTP auto restart mode. This OTP is disabled during burst mode.

If the voltage at the current sensing pin is higher than the preset threshold V_{CSSW} during on-time of the power switch, the IC is latched off. This is short-winding protection. The short winding protection is disabled during burst mode.

During latch-off protection mode, the VCC voltage drops to V_{VCCoff} (10.5V) and then the startup cell is activated. The VCC voltage is then charged to V_{VCCon} (18V). The startup cell is shut down again. This action repeats again and again.

There is also a maximum on time limitation implemented inside the ICE2QS03G. Once the gate voltage is high and longer than t_{OnMax}, the switch is turned off immediately.

4 Electrical Characteristics

Note : All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Note : Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason it needs to make sure that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
HV Voltage	V_{HV}	-	500	V	
VCC Supply Voltage	V_{VCC}	-0.3	27	V	
FB Voltage	V_{FB}	-0.3	5.5	V	
ZC Voltage	V_{ZC}	-0.3	5.5	V	
CS Voltage	V_{CS}	-0.3	5.5	V	
Current out from ZC pin	I_{ZCMAX}	-	3	mA	
Junction Temperature	T_j	-40	150	°C	
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance Junction -Ambient	R_{thJA}	-	185	K/W	
ESD Capability (incl. Drain Pin)	V_{ESD}	-	2	kV	Human body model[1]

4.2 Operating Range

Note : Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	V_{VCC}	V_{VCCoff}	V_{VCCOVP}	V	
Junction Temperature of Controller	T_{jCon}	-40	130	°C	Limited by over temperature protection

[1] According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kW series resistor)

4.3 Characteristics

4.3.1 Supply Section

Note : The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_j from – 40 °C to 125 °C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 18 V is assumed.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Start Up Current	$I_{VCCstart}$	-	300	550	µA	V_{VCC} =V_{VCCon} -0.2V
VCC Charge Current	$I_{VCCcharge1}$	-	1.22	5.0	mA	V_{VCC} = 0V
	$I_{VCCcharge2}$	0.8	1.1	-	mA	V_{VCC} = 1V
	$I_{VCCcharge3}$	-	1	-	mA	V_{VCC} =V_{VCCon} -0.2V
Maximum Input Current of Startup Cell	$I_{DrainIn}$	-	-	2	mA	V_{VCC} =V_{VCCon} -0.2V
Leakage Current of Startup Cell	$I_{DrainLeak}$	-	0.2	50	µA	V_{Drain} = 500V at T_j=100°C
Supply Current in normal operation	I_{VCCNM}	-	1.5	2.3	mA	I_{FB} = 0A
Supply Current in Auto Restart Mode with Inactive Gate	I_{VCCAR}	-	300	-	µA	I_{FB} = 0A
Supply Current in Latch-off Mode	$I_{VCClatch}$	-	300	-	µA	I_{FB} = 0A
Supply Current in Burst Mode with inactive Gate	$I_{VCCburst}$	-	500	950	µA	V_{FB} = 2.5V, exclude the current flowing out from FB pin
VCC Turn-On Threshold	V_{VCCon}	17.0	18.0	19.0	V	
VCC Turn-Off Threshold	V_{VCCoff}	9.8	10.5	11.2	V	
VCC Turn-On/Off Hysteresis	V_{VCChys}	-	7.5	-	V	

4.3.2 Internal Voltage Reference

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Internal Reference Voltage	V_{REF}	4.80	5.00	5.20	V	Measured at pin FB I_{FB}=0

4.3.3 PWM Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Feedback Pull-Up Resistor	R_{FB}	14	23	33	kΩ	
PWM-OP Gain	G_{PWM}	3.18	3.3	-	-	
Offset for Voltage Ramp	V_{PWM}	0.6	0.7	-	V	
Maximum on time in normal operation	t_{OnMax}	22	30	41	µs	

4.3.4 Current Sense

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Peak current limitation in normal operation	V_{CSth}	0.97	1.03	1.09	V	
Leading Edge Blanking time	t_{LEB}	200	330	460	ns	
Peak Current Limitation in Active Burst Mode	V_{CSB}	0.29	0.34	0.39	V	

4.3.5 Soft Start

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Soft-Start time	t_{SS}	8.5	12	-	ms	
soft-start time step	t_{SS_S}[1]	-	3	-	ms	
Internal regulation voltage at first step	V_{SS1}[1]	-	1.76	-	V	
Internal regulation voltage step at soft start	V_{SS_S}[1]	-	0.56	-	V	

4.3.6 Foldback Point Correction

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
ZC current first step threshold	I_{ZC_FS}	0.35	0.5	0.621	mA	
ZC current last step threshold	I_{ZC_LS}	1.3	1.7	2.2	mA	
CS threshold minimum	V_{CSMF}	-	0.66	-	V	I_{zc}=2.2mA, V_{FB}=3.8V

[1]The parameter is not subjected to production test - verified by design/characterization

4.3.7 Digital Zero Crossing

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Zero crossing threshold voltage	V_{ZCCT}	50	100	170	mV	
Ringing suppression threshold	V_{ZCRS}	-	0.7	-	V	
Minimum ringing suppression time	t_{ZCRS1}	1.62	2.5	4.5	µs	$V_{ZC} > V_{ZCRS}$
Maximum ringing suppression time	t_{ZCRS2}	-	25	-	µs	$V_{ZC} < V_{ZCRS}$
Threshold to set Up/Down Counter to one	V_{FBR1}	-	3.9	-	V	
Threshold for downward counting at low line	V_{FBZHL}	-	3.2	-	V	
Threshold for upward counting at low line	V_{FBZLL}	-	2.5	-	V	
Threshold for downward counting at high line	V_{FBZHH}	-	2.9	-	V	
Threshold for upward counting at high line	V_{FBZLH}	-	2.3	-	V	
ZC current for IC switch threshold to high line	I_{ZCSH}	-	1.3	-	mA	
ZC current for IC switch threshold to low line	I_{ZCSL}	-	0.8	-	mA	
Counter time[1]	t_{COUNT}	-	48	-	ms	
Maximum restart time in normal operation	t_{OffMax}	30	42	57.5	µs	

4.3.8 Active Burst Mode

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Feedback voltage for entering Active Burst Mode	V_{FBEB}	-	1.25	-	V	
Minimum Up/down value for entering Active Burst Mode	N_{ZC_ABM}	-	7	-		
Blanking time for entering Active Burst Mode	t_{BEB}	-	24	-	ms	
Feedback voltage for leaving Active Burst Mode	V_{FBLB}	-	4.5	-	V	
Feedback voltage for burst-on	V_{FBBOn}	-	3.6	-	V	
Feedback voltage for burst-off	V_{FBBOff}	-	3.0	-	V	

[1]The parameter is not subjected to production test - verified by design/characterization

Fixed Switching Frequency in Active Burst Mode	f_{sB}	39	52	65	kHz	
Max. Duty Cycle in Active Burst Mode	D_{maxB}	-	0.5	-		

4.3.9 Protection

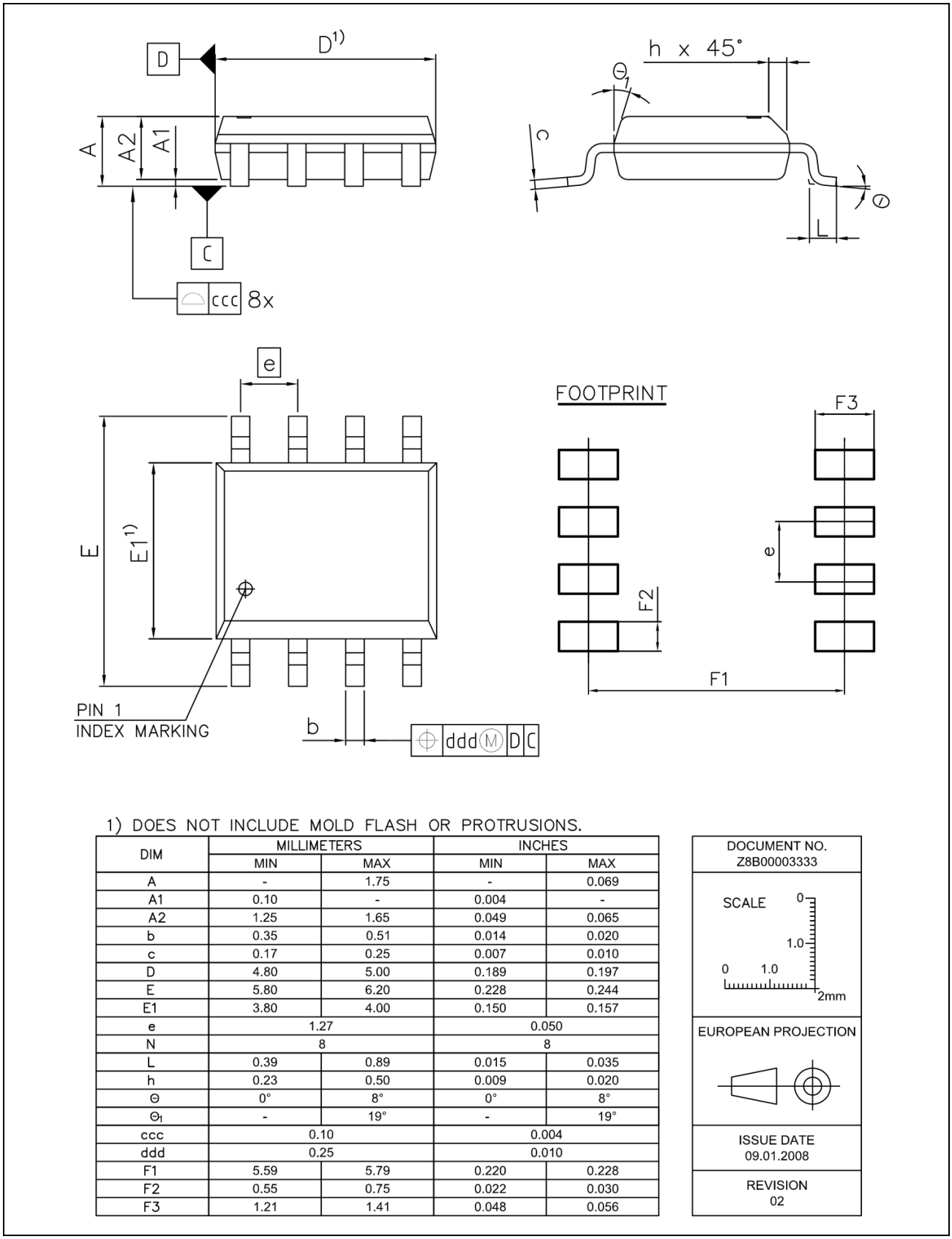
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
VCC overvoltage threshold	V_{VCCOVP}	24.0	25.0	26.0	V	
Over Load or Open Loop Detection threshold for OLP protection at FB pin	V_{FBOLP}	-	4.5	-	V	
Over Load or Open Loop Protection Blanking Time	t_{OLP_B}	20	30	44	ms	
Output Overvoltage detection threshold at the ZC pin	V_{ZCOVP}	3.55	3.7	3.84	V	
Blanking time for Output Overvoltage protection	t_{ZCOVP}	-	100	-	µs	
Threshold for short winding protection	V_{CSSW}	1.63	1.68	1.78	V	
Blanking time for short-winding protection	t_{CSSW}	-	190	-	ns	
Over temperature protection[1]	T_{jCon}	130	140	150	°C	
Power Down Reset threshold for Latched Mode	V_{VCCPD}	5.2	-	7.8	V	After Latched Off Mode is entered

Note : The trend of all the voltage levels in the Control Unit is the same regarding the deviation except V_{VCCOVP} *&* V_{VCCPD}.

4.3.10 Gate Drive

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output voltage at logic low	$V_{GATElow}$	-	-	1.0	V	V_{VCC}=18V I_{OUT} = 10mA
Output voltage at logic high	$V_{GATEhigh}$	9.0	10.0	-	V	V_{VCC}=18V I_{OUT} = -10mA
Output voltage active shut down	$V_{GATEasd}$	-	-	1.0	V	V_{VCC} = 7V I_{OUT} = 10mA
Rise Time	t_{rise}	-	117	-	ns	C_{OUT} = 1.0nF V_{GATE}= 2V ... 8V
Fall Time	t_{fall}	-	27	-	ns	C_{OUT} = 1.0nF V_{GATE}= 8V ... 2V

5 Outline Dimension



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

DOCUMENT NO.
Z8B00003333

SCALE 0 1.0 0 1.0 2mm

EUROPEAN PROJECTION

ISSUE DATE
09.01.2008

REVISION
02

Figure 11 PG-DSO-8 (Pb-free lead plating Plastic Dual Small Outline Package)

6 Marking

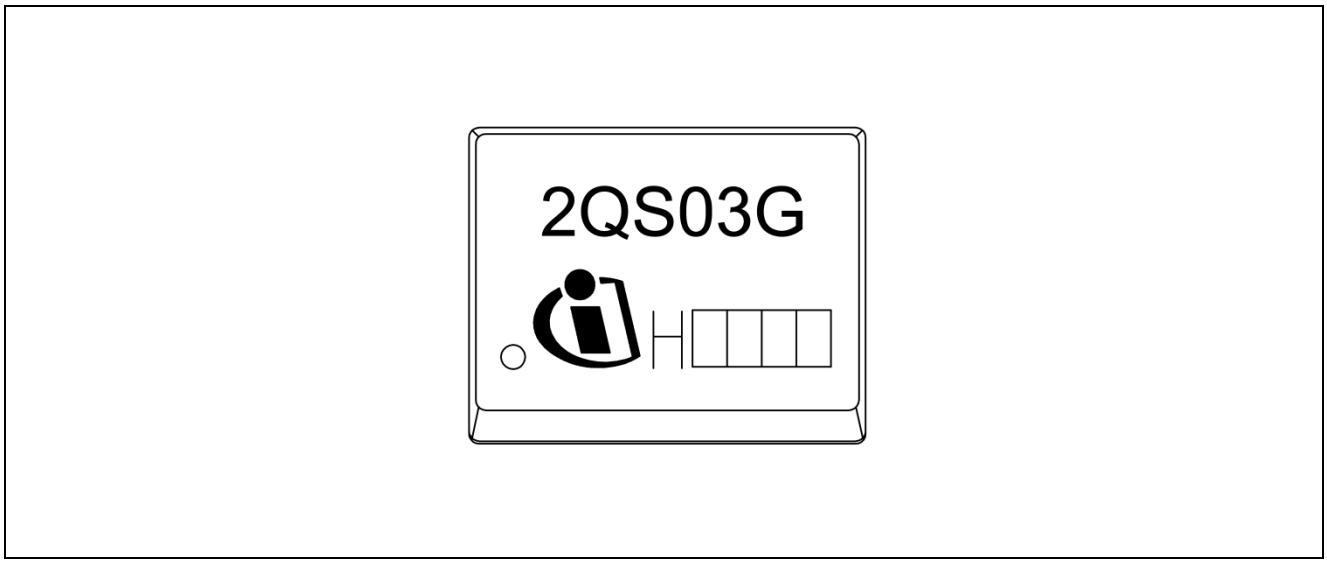


Figure 12 Marking for ICE2QS03G

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