NTQD6866R2

Power MOSFET
6.9 Amps, 20 Volts
N−Channel TSSOP−8

Features

- New Low Profile TSSOP−8 Package
- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperatures
- Pb−Free Package is Available

Applications

- Power Management in Portable and Battery−Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular and Cordless Phones
- Battery Applications
- NoteBook PC

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	20	Vdc
Drain−to−Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	±12	Vdc
Thermal Resistance − Single Die Junction−to−Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ T_A = 25°C Pulsed Drain Current (Note 4)	 $R_{\theta JA}$ P_D I_D I_{DM}	 62.5 2.0 6.9 24	 °C/W W Adc Adc
Thermal Resistance − Single Die Junction−to−Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ T_A = 25°C Continuous Drain Current @ T_A = 70°C Pulsed Drain Current (Note 4)	 $R_{\theta JA}$ P_D I_D I_D I_{DM}	 88 1.42 5.8 4.6 20	 °C/W W Adc Adc Adc
Thermal Resistance − Single Die Junction−to−Ambient (Note 3) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ T_A = 25°C Continuous Drain Current @ T_A = 70°C Pulsed Drain Current (Note 4)	 $R_{\theta JA}$ P_D I_D I_D I_{DM}	 132 0.94 4.7 3.8 14	 °C/W W Adc Adc Adc
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 20 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 5.5 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	150	mJ
Maximum Lead Temperature for Soldering Purposes for 10 seconds	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Mounted onto a 2″ square FR−4 board (1 in sq, 2 oz Cu 0.06″ thick single−sided), t < 10 seconds.
2. Mounted onto a 2″ square FR−4 board (1 in sq, 2 oz Cu 0.06″ thick single−sided), t = ss.
3. Minimum FR−4 or G−10 PCB, t = steady state.
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

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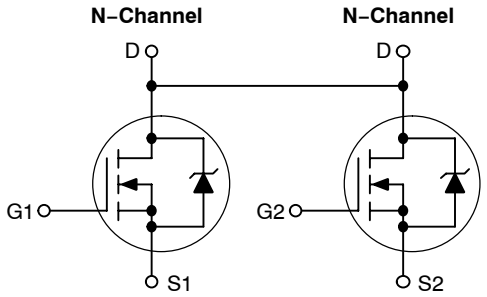
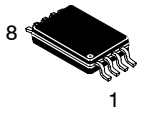
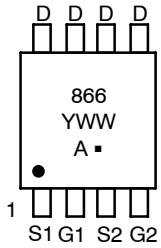
6.9 AMPERES
20 VOLTS
30 mΩ @ V_{GS} = 4.5 V



MARKING DIAGRAM & PIN ASSIGNMENT



TSSOP−8
CASE 948S
PLASTIC



866	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTQD6866R2	TSSOP−8	4000/Tape & Reel
NTQD6866R2G	TSSOP−8 (Pb−Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

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March, 2006 − Rev. 3
Publication Order Number:
NTQD6866R2/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 20 –	 – 18.5	 – –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{GS} = 0 Vdc, V_{DS} = 20 Vdc, T_J = 25°C) (V_{GS} = 0 Vdc, V_{DS} = 20 Vdc, T_J = 100°C)		I_{DSS}	 – –	 – –	 1.0 10	μAdc
Gate−Body Leakage Current (V_{GS} = ±12 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	±100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	 0.6 –	 0.9 −2.7	 1.2 –	Vdc mV/°C
Static Drain−to−Source On−State Resistance (V_{GS} = 4.5 Vdc, I_D = 6.9 Adc) (V_{GS} = 4.5 Vdc, I_D = 5.8 Adc) (V_{GS} = 2.5 Vdc, I_D = 3.5 Adc) (V_{GS} = 2.5 Vdc, I_D = 2.9 Adc)		$R_{DS(on)}$	 – – – –	 0.026 0.025 0.030 0.030	 0.032 0.030 0.038 0.038	Ω
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 5.8 Adc)		g_{FS}	–	14	–	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	875	1400	pF
Output Capacitance		C_{oss}	–	325	550	
Reverse Transfer Capacitance		C_{rss}	–	100	175	
SWITCHING CHARACTERISTICS (Note 5)						
Turn−On Delay Time	(V_{DD} = 16 Vdc, I_D = 5.8 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	–	10	18	ns
Rise Time		t_r	–	45	80	
Turn−Off Delay Time		$t_{d(off)}$	–	40	75	
Fall Time		t_f	–	90	150	
Turn−On Delay Time	(V_{DD} = 16 Vdc, I_D = 5.8 Adc, V_{GS} = 4.5 Vdc, R_G = 3.0 Ω)	$t_{d(on)}$	–	8.0	–	
Rise Time		t_r	–	45	–	
Turn−Off Delay Time		$t_{d(off)}$	–	35	–	
Fall Time		t_f	–	75	–	
Gate Charge	(V_{DS} = 16 Vdc, V_{GS} = 4.5 Vdc, I_D = 5.8 Adc)	Q_{tot}	–	13	22	nC
		Q_{gs}	–	1.8	–	
		Q_{gd}	–	4.5	–	
BODY−DRAIN DIODE RATINGS						
Forward On−Voltage	(I_S = 5.8 Adc, V_{GS} = 0 Vdc) (I_S = 5.8 Adc, V_{GS} = 0 Vdc, T_J = 100°C)	V_{SD}	– –	0.85 0.75	1.0 –	Vdc
Reverse Recovery Time	(I_S = 5.8 Adc, V_{GS} = 0 Vdc, V_{DS} = 20 Vdc dI_S/dt = 100 A/μs)	t_{rr}	–	23	–	ns
		t_b	–	11	–	
		t_a	–	12	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.013	–	μC

5. Switching characteristics are independent of operating junction temperature.

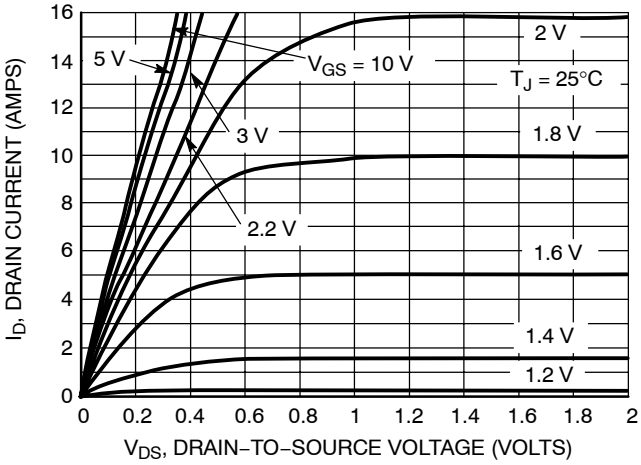


Figure 1. On−Region Characteristics

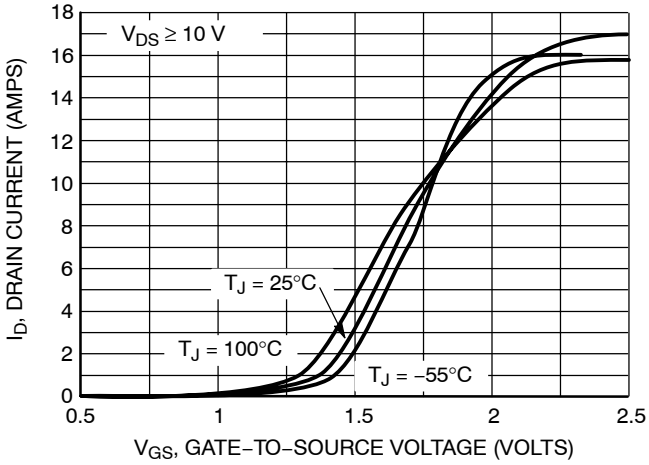


Figure 2. Transfer Characteristics

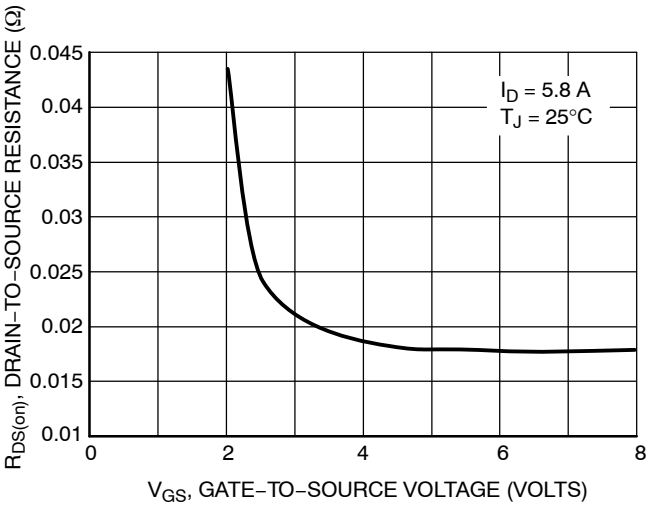


Figure 3. On−Resistance versus Gate−to−Source Voltage

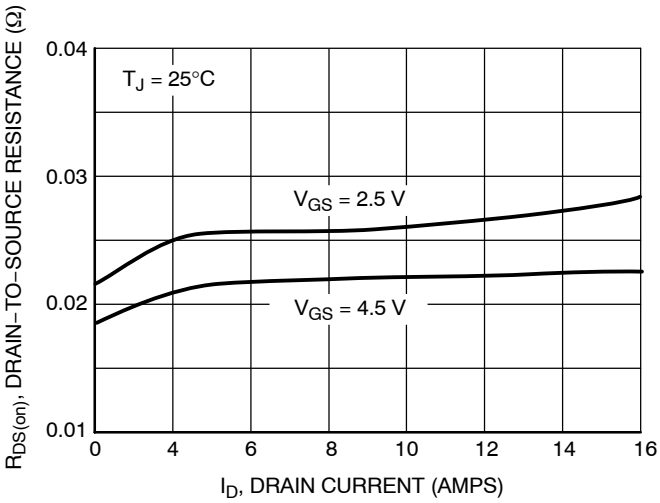


Figure 4. On−Resistance versus Drain Current and Gate Voltage

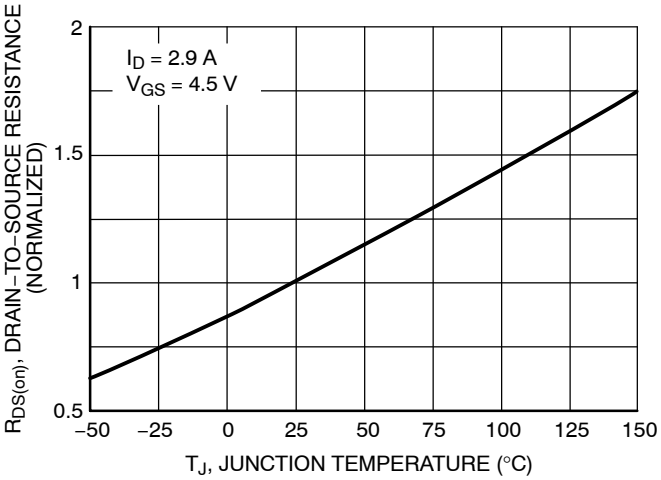


Figure 5. On−Resistance Variation with Temperature

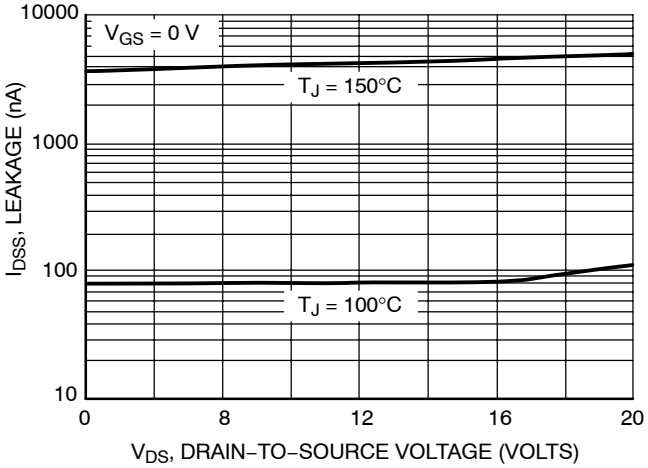


Figure 6. Drain−to−Source Leakage Current versus Voltage

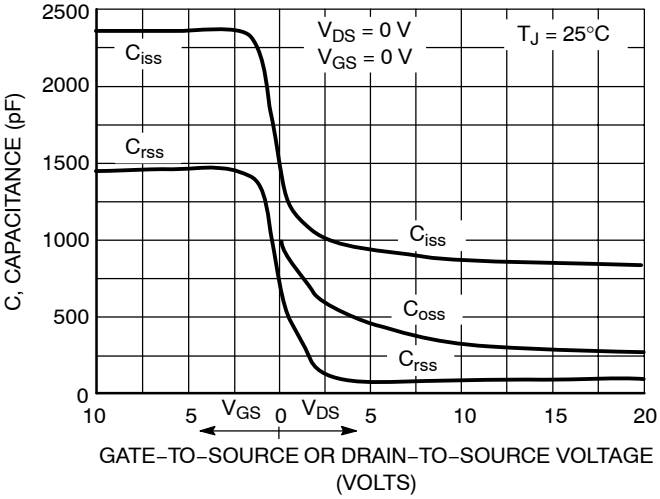


Figure 7. Capacitance Variation

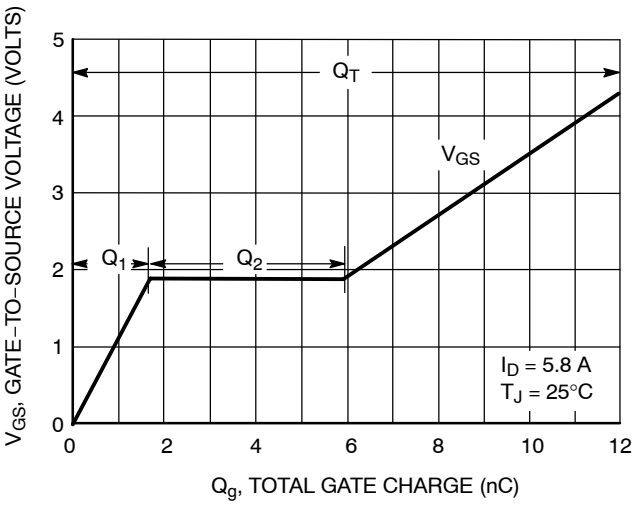


Figure 8. Gate−to−Source Voltage versus Total Charge

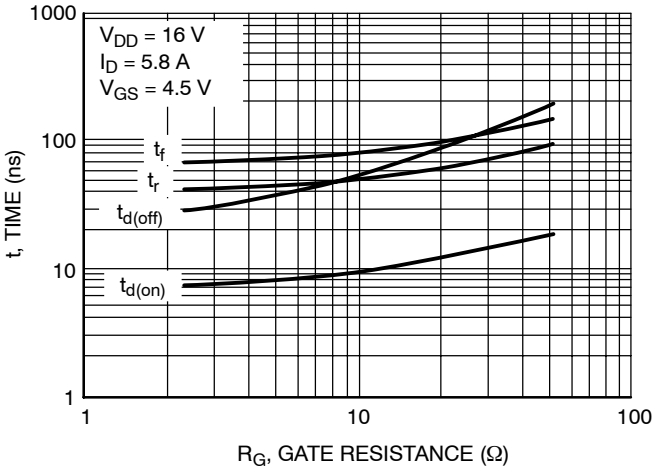


Figure 9. Resistive Switching Time Variation versus Gate Resistance

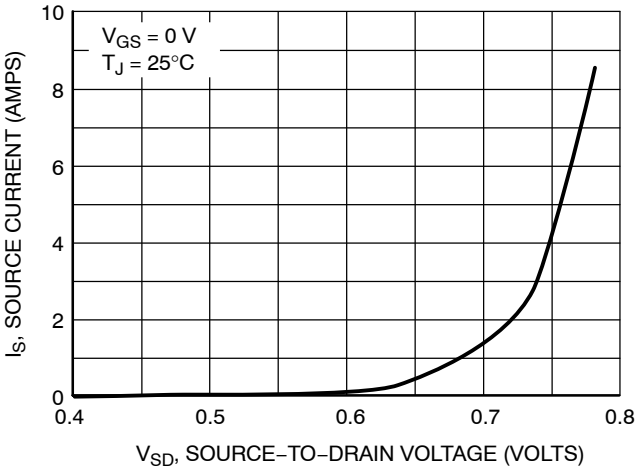


Figure 10. Diode Forward Voltage versus Current

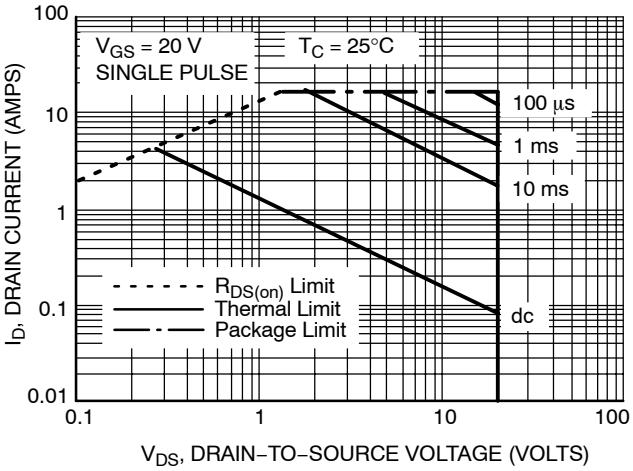


Figure 11. Maximum Rated Forward Biased Safe Operating Area

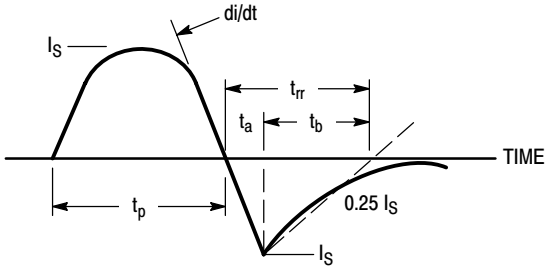


Figure 12. Diode Reverse Recovery Waveform

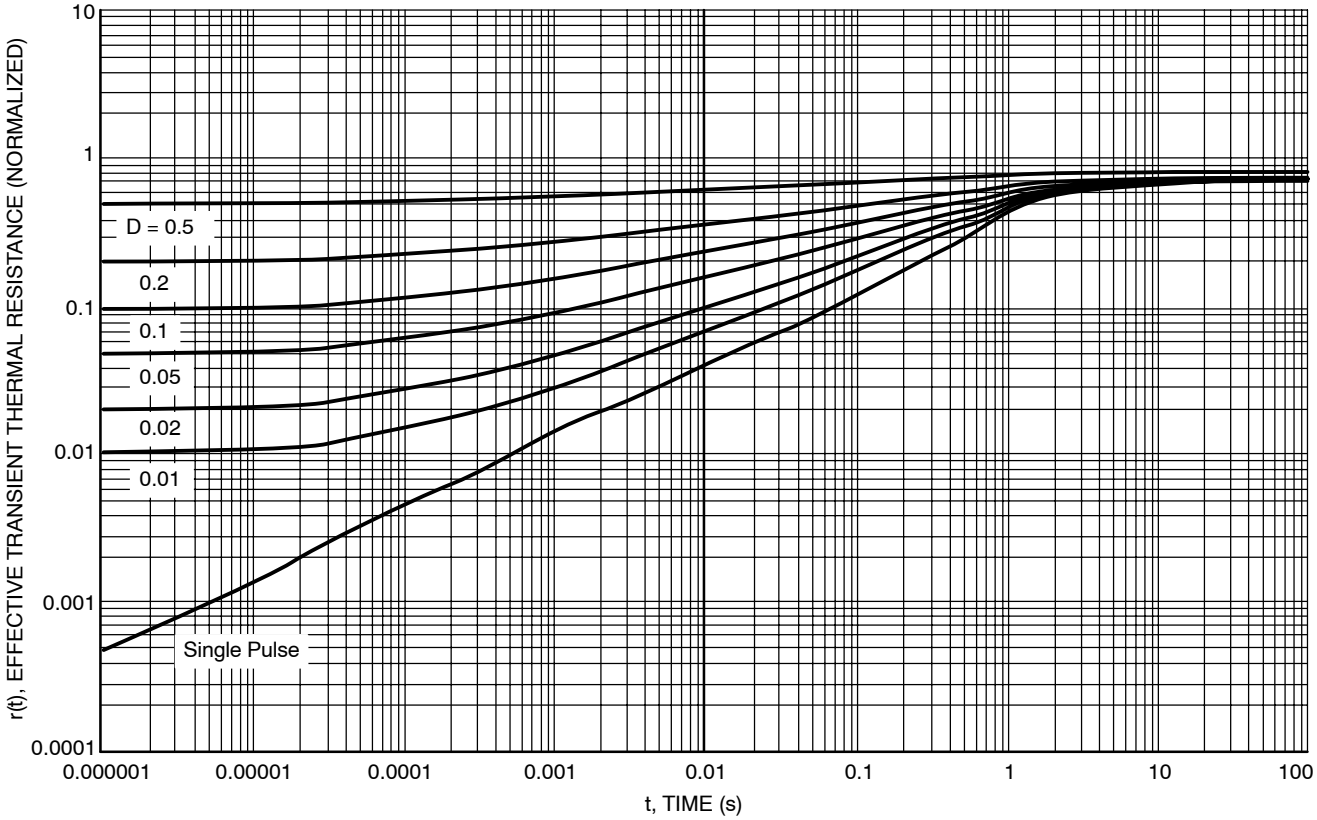
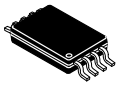


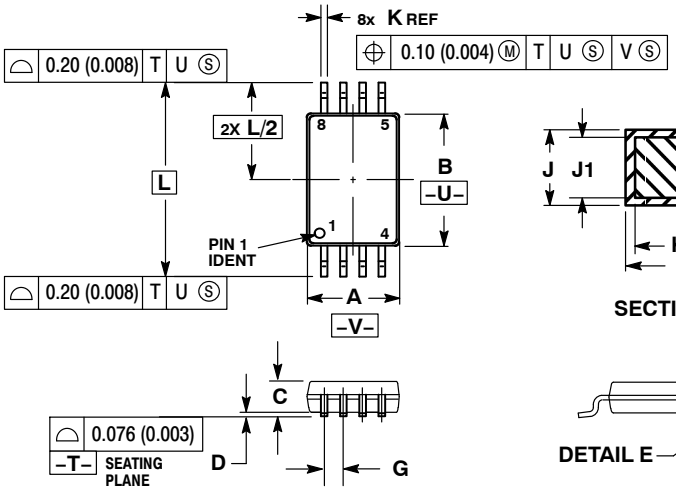
Figure 13. Thermal Response

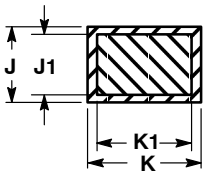
TSSOP−8
CASE 948S−01
ISSUE C

DATE 20 JUN 2008

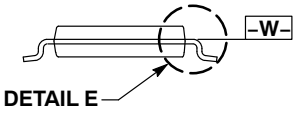


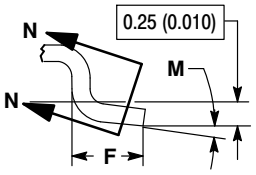
SCALE 2:1





SECTION N−N



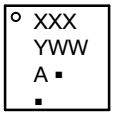


DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION.	18 APR 2000
A	ADDED MARKING DIAGRAM INFORMATION. REQ. BY V. BASS.	13 JAN 2006
B	CORRECTED MARKING DIAGRAM PIN 1 LOCATION AND MARKING. REQ. BY C. REBELLO.	13 MAR 2006
C	REMOVED EXPOSED PAD VIEW AND DIMENSIONS P AND P1. CORRECTED MARKING INFORMATION. REQ. BY C. REBELLO.	20 JUN 2008

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