OptiMOS™-T2 Power-Transistor

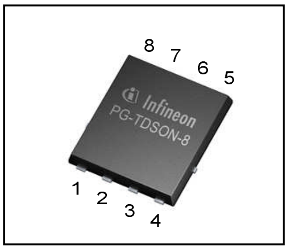
Product Summary

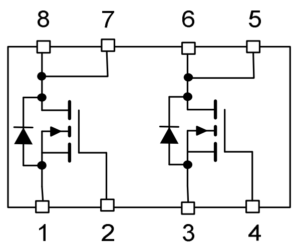
V_{DS}	40	V
$R_{DS(on),max}$ [4]	8.2	mΩ
I_D	20	A

Features

- Dual N-channel Logic Level - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

PG-TDSON-8-4





Type	Package	Marking
IPG20N04S4L-08	PG-TDSON-8-4	4N04L08

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current one channel active	I_D	T_C=25 °C, V_{GS}=10 V[1]	20	A
		T_C=100 °C, V_{GS}=10 V[2]	20	
Pulsed drain current[2] one channel active	$I_{D,pulse}$	-	80	
Avalanche energy, single pulse[2, 4]	E_{AS}	I_D=10A	145	mJ
Avalanche current, single pulse[4]	I_{AS}	-	15	A
Gate source voltage	V_{GS}	-	±16	V
Power dissipation one channel active	P_{tot}	T_C=25 °C	54	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2)]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	2.8	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	100	-	
		6 cm^2 cooling area[3)]	-	60	-	

Electrical characteristics, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D= 1 mA	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D= 22µA	1.2	1.7	2.2	
Zero gate voltage drain current[4)]	I_{DSS}	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C	-	0.01	1	µA
		V_{DS}=18 V, V_{GS}=0 V, T_j=85 °C[2)]	-	1	100	
Gate-source leakage current[4)]	I_{GSS}	V_{GS}=16 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance[4)]	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=10 A	-	9.2	10.9	mΩ
		V_{GS}=10 V, I_D=17A	-	7.2	8.2	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2)]						
Input capacitance[4)]	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	2350	3050	pF
Output capacitance[4)]	C_{oss}		-	440	570	
Reverse transfer capacitance[4)]	C_{rss}		-	20	46	
Turn-on delay time	$t_{d(on)}$	V_{DD}=20 V, V_{GS}=10 V, I_D=20 A, R_G=11 Ω	-	7	-	ns
Rise time	t_r		-	3	-	
Turn-off delay time	$t_{d(off)}$		-	40	-	
Fall time	t_f		-	20	-	
Gate Charge Characteristics[2, 4)]						
Gate to source charge	Q_{gs}	V_{DD}=32 V, I_D=20 A, V_{GS}=0 to 10 V	-	6.5	8.5	nC
Gate to drain charge	Q_{gd}		-	3.2	7.4	
Gate charge total	Q_g		-	30	39	
Gate plateau voltage	$V_{plateau}$		-	2.8	-	V
Reverse Diode						
Diode continous forward current[2)] one channel active	I_S	T_C=25 °C	-	-	20	A
Diode pulse current[2)] one channel active	$I_{S,pulse}$		-	-	80	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=17 A, T_j=25 °C	-	0.9	1.3	V
Reverse recovery time[2)]	t_{rr}	V_R=20 V, I_F=I_S, di_F/dt=100 A/µs	-	34	-	ns
Reverse recovery charge[2, 4)]	Q_{rr}		-	30	-	nC

1) Current is limited by bondwire; with an R_{thJC}=2.8 K/W the chip is able to carry 66A at 25°C.

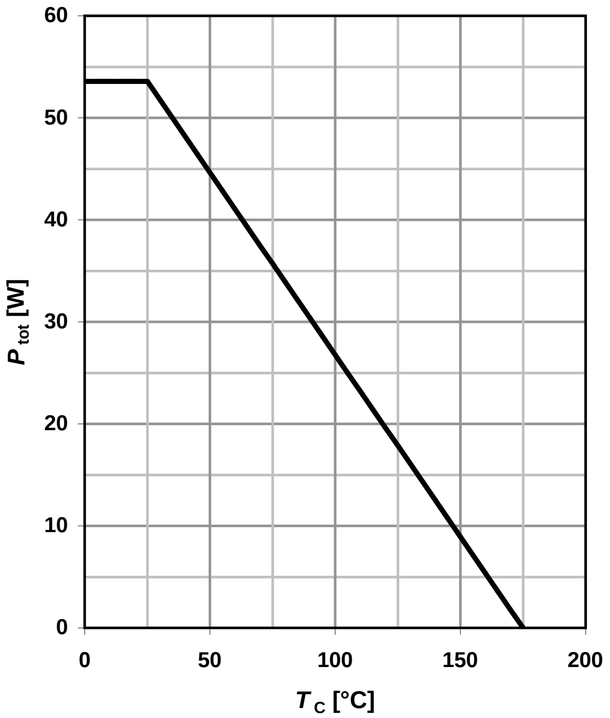
2) Specified by design. Not subject to production test.

3) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

4) Per channel

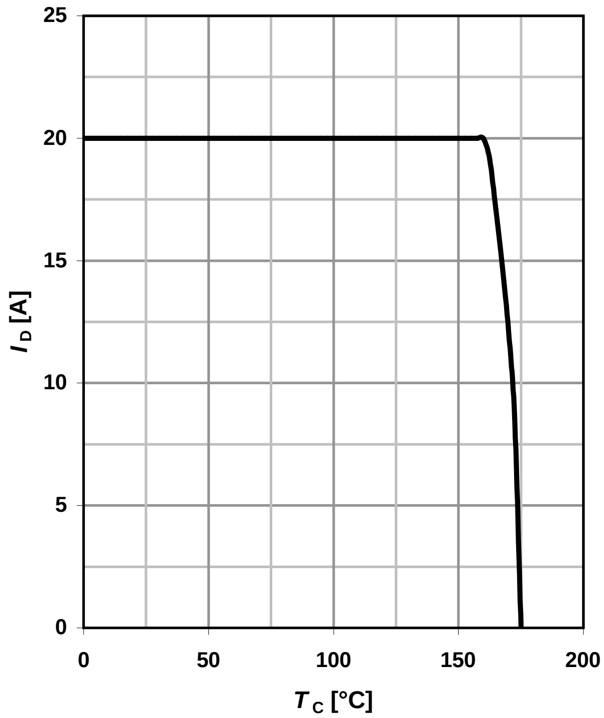
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V; one channel active



2 Drain current

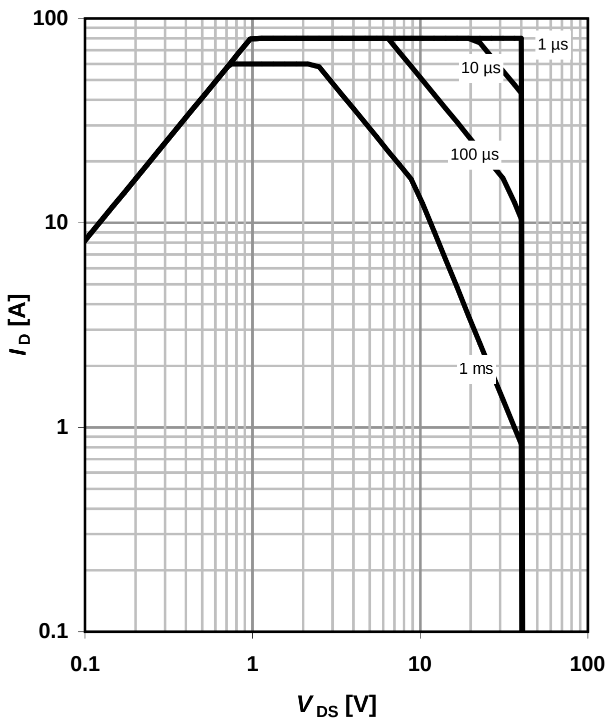
$I_D = f(T_C)$; $V_{GS} \geq 6$ V; one channel active



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25°C$; $D = 0$; one channel active

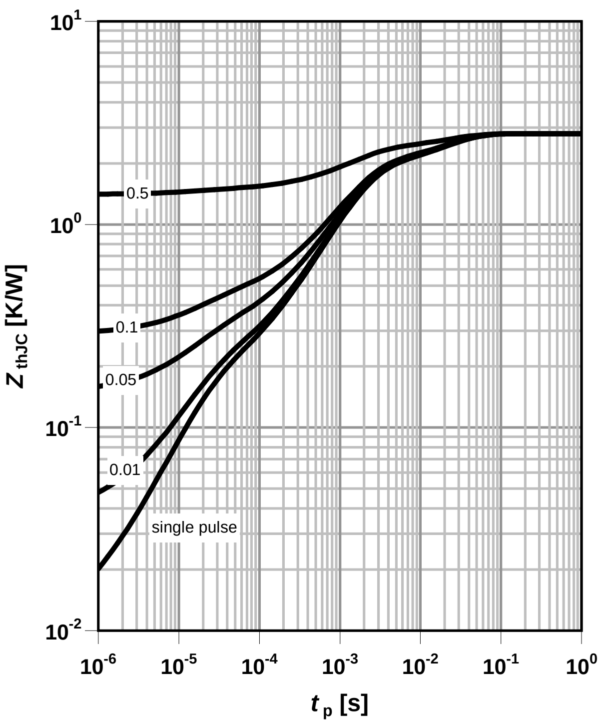
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

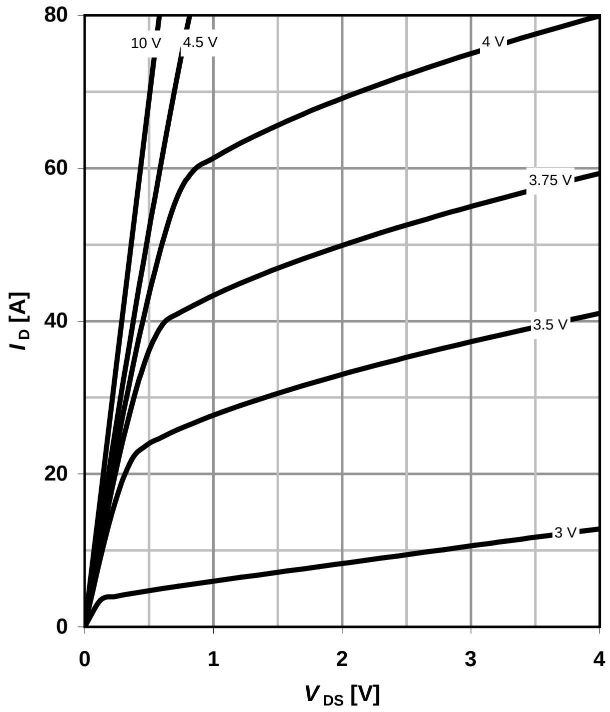
parameter: $D = t_p/T$



5 Typ. output characteristics[4)]

$I_D = f(V_{DS})$; $T_j = 25$ °C

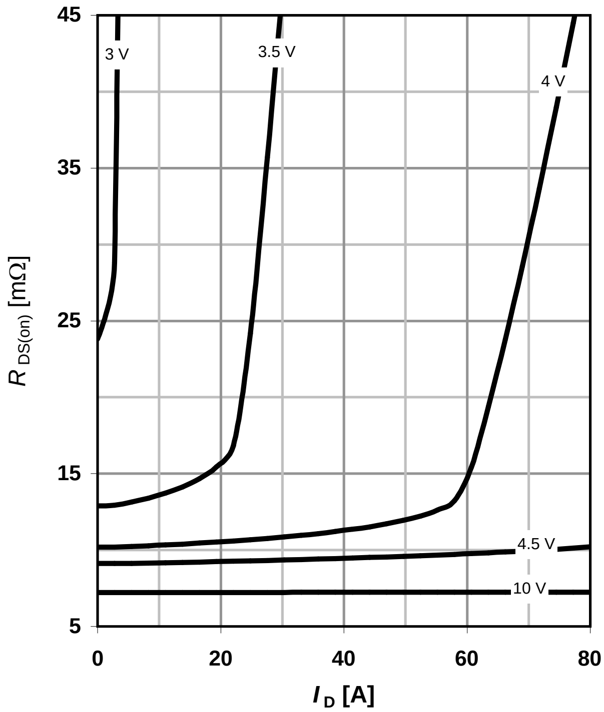
parameter: V_{GS}



6 Typ. drain-source on-state resistance[4)]

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C

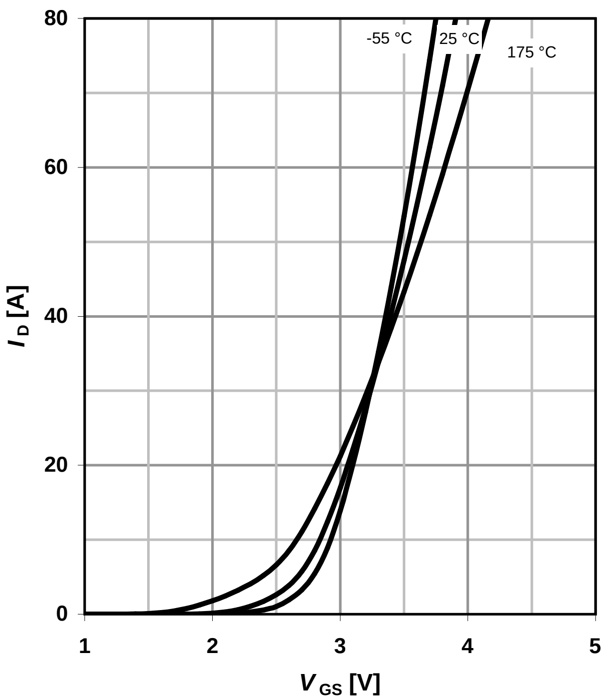
parameter: V_{GS}



7 Typ. transfer characteristics[4)]

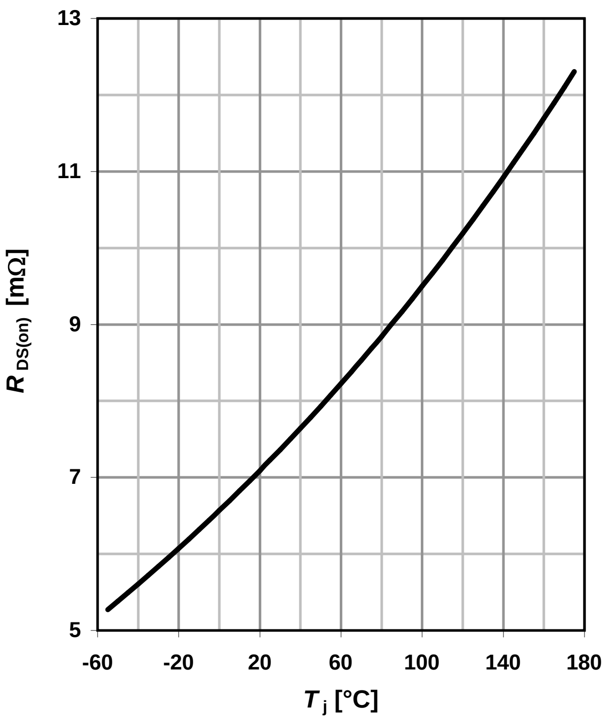
$I_D = f(V_{GS})$; $V_{DS} = 6$V

parameter: T_j



8 Typ. drain-source on-state resistance[4)]

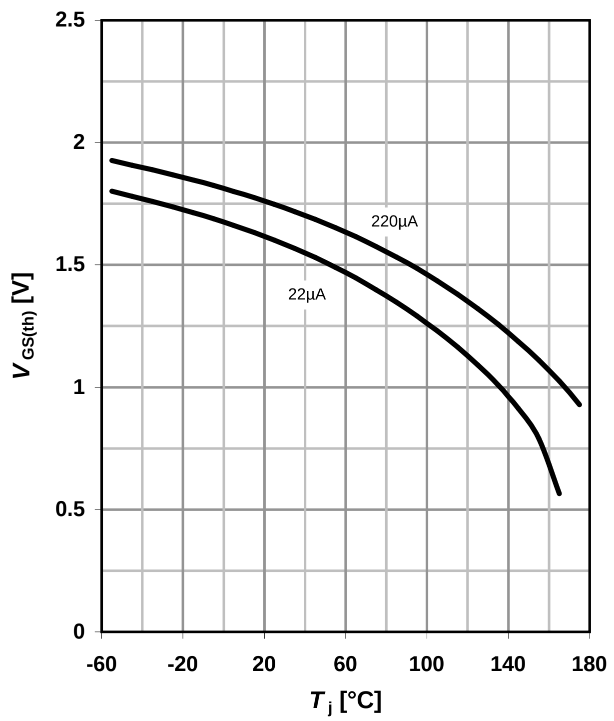
$R_{DS(on)} = f(T_j)$; $I_D = 17$ A; $V_{GS} = 10$ V



9 Typ. gate threshold voltage

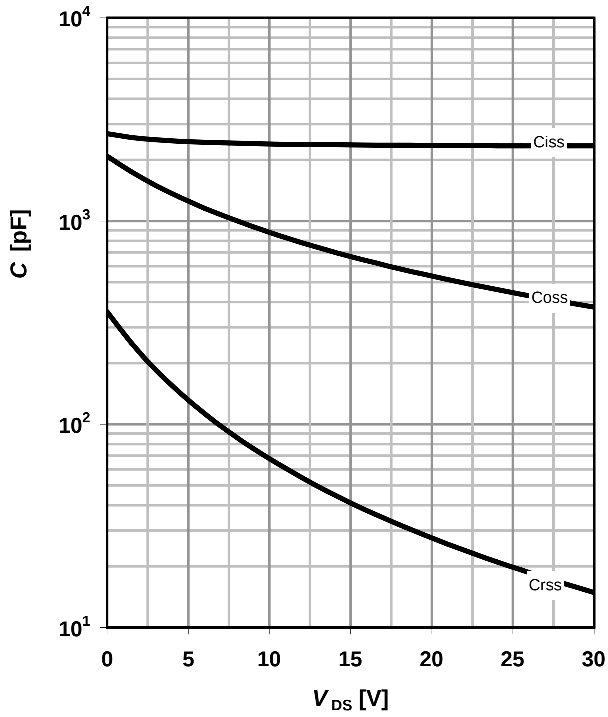
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. Capacitances[4)]

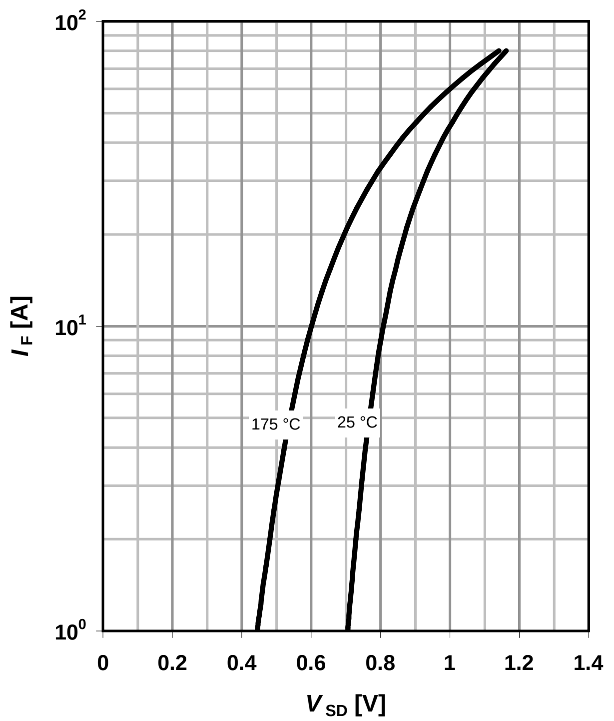
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristicis[4)]

$IF = f(V_{SD})$

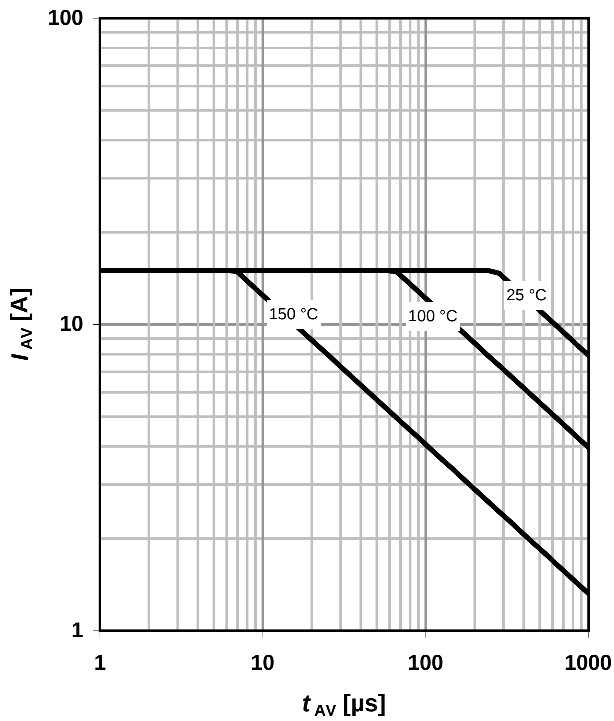
parameter: T_j



12 Avalanche characteristics[4)]

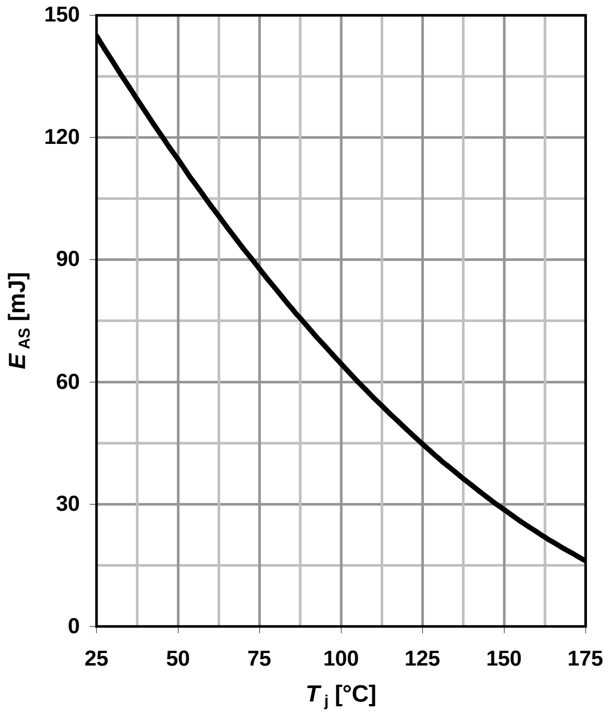
$I_{AS} = f(t_{AV})$

parameter: $T_{j(start)}$



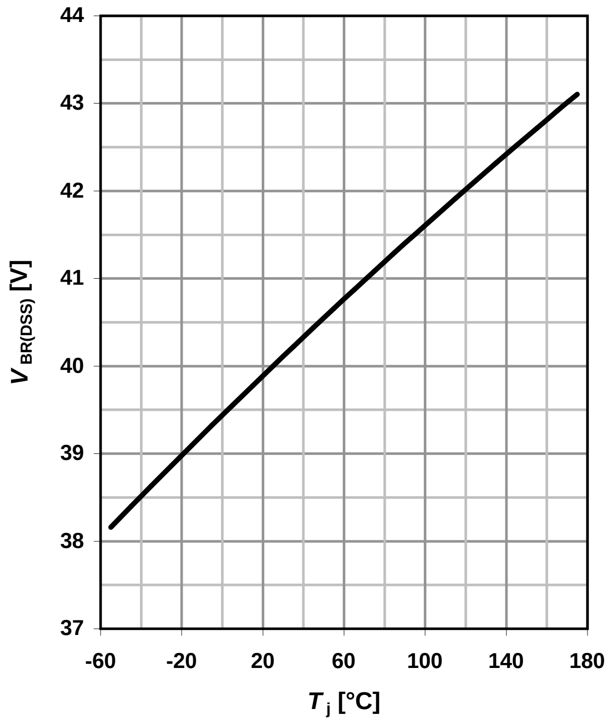
13 Avalanche energy[4)]

$E_{AS} = f(T_j)$, $I_D = 10A$



14 Drain-source breakdown voltage

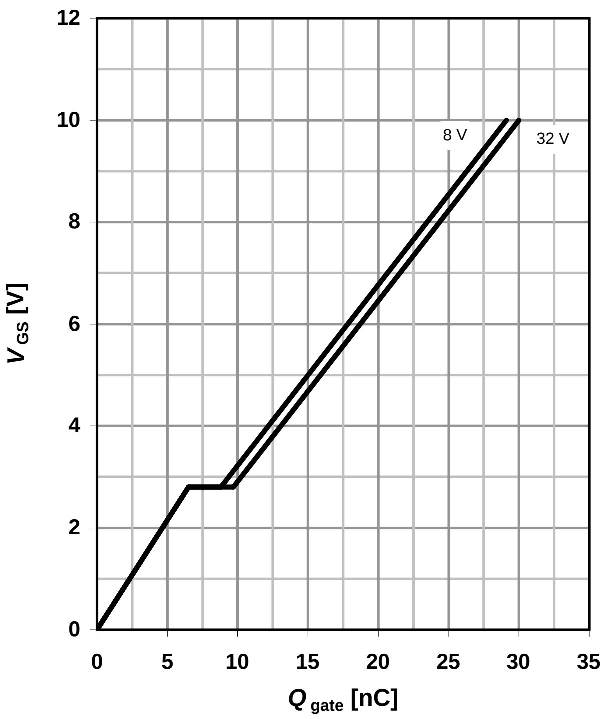
$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA



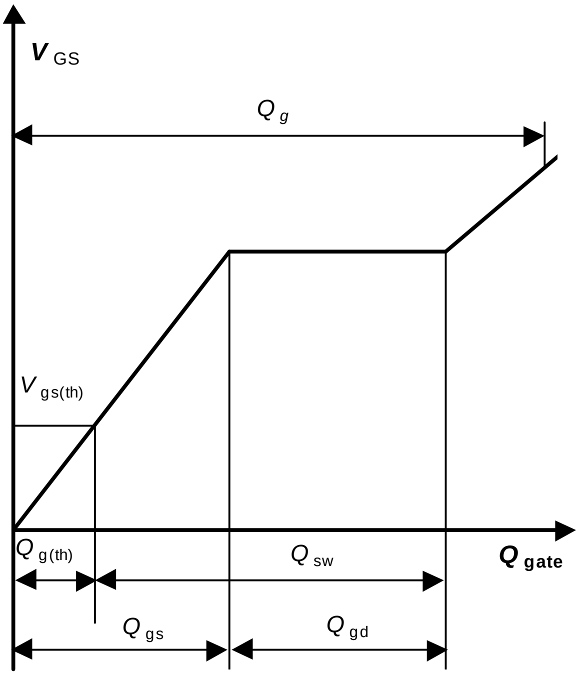
15 Typ. gate charge[4)]

$V_{GS} = f(Q_{gate})$; $I_D = 20$ A pulsed

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Revision 1.0	05.10.2010	Data Sheet revision 1.0