Title	***Reference Design Report for a 60 W Isolated Flyback Power Supply Using InnoSwitch™3-AQ INN3949CQ***
Specification	50 – 1000 VDC Input; 50 VDC: 4 W 100 VDC: 35 W 200 VDC: 48 W 300 VDC – 1000 VDC: 60 W
Application	High Input Voltage for Automotive Application
Author	Applications Engineering Department
Document Number	RDR-919Q
Date	January 17, 2022
Revision	1.0

Summary and Features

- High input voltage: up to 1000 VDC
- Works in extreme hot condition: 85 ºC with continuous 20 W operation at 1000 VDC input
- InnoSwitch™3-AQ – industry first AC/DC ICs with isolated, safety rated integrated feedback
- Built-in synchronous rectification for >82% efficiency
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing

PATENT INFORMATION
The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using a high voltage DC Supply to provide the DC input to the prototype board.

1 Introduction

This engineering report describes a 50 VDC to 1000 VDC input, 24 V output, 60 W power supply utilizing INN3949CQ from Power Integrations. The document contains the power supply specification, schematic, bill-of-materials and basic performance data.

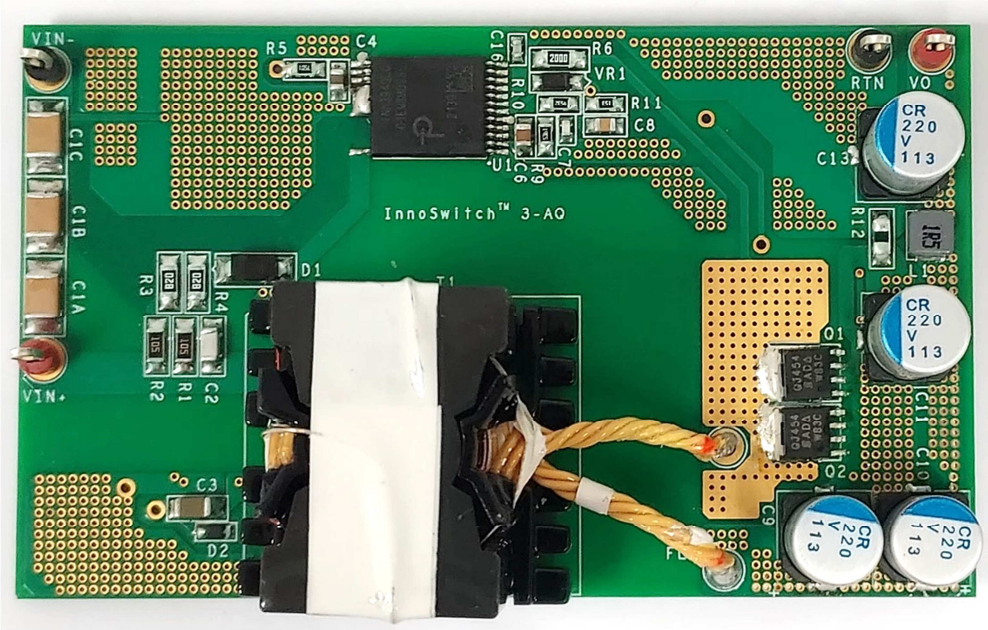


Figure 1 – Populated Circuit Board Photograph, Top.

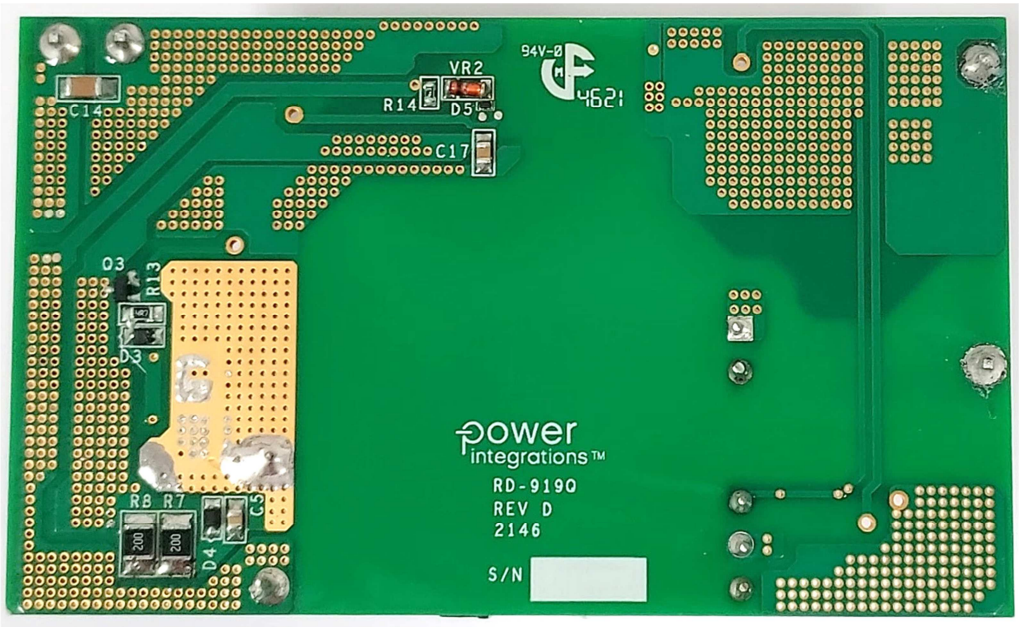


Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	$\mathbf{V_{IN}}$	300	800	1000	VDC	For Electric Vehicle Emergency PSU. For 60 W Output Power.
No-load Input Power				30	mW	
Output						
Output Voltage	$\mathbf{V_{OUT}}$		24		V	±5%
Output Current	$\mathbf{I_{OUT}}$		2.5		A	
Output Ripple Voltage	$\mathbf{V_{RIPPLE}}$			240	mV	On Board. (V_{IN} 300 VDC to 1000 VDC.)
Total Output Power						
Continuous Output Power	$\mathbf{P_{OUT}}$			4	W	V_{IN} of 50 VDC.
Continuous Output Power	$\mathbf{P_{OUT}}$			35	W	V_{IN} of 100 VDC.
Continuous Output Power	$\mathbf{P_{OUT}}$			48	W	V_{IN} of 200 VDC.
Continuous Output Power	$\mathbf{P_{OUT}}$			60	W	V_{IN} 300 VDC to 1000 VDC.
Ambient Temperature	$\mathbf{T_{AMB}}$	-40		85	°C	Inside Inverter.

3 Schematic

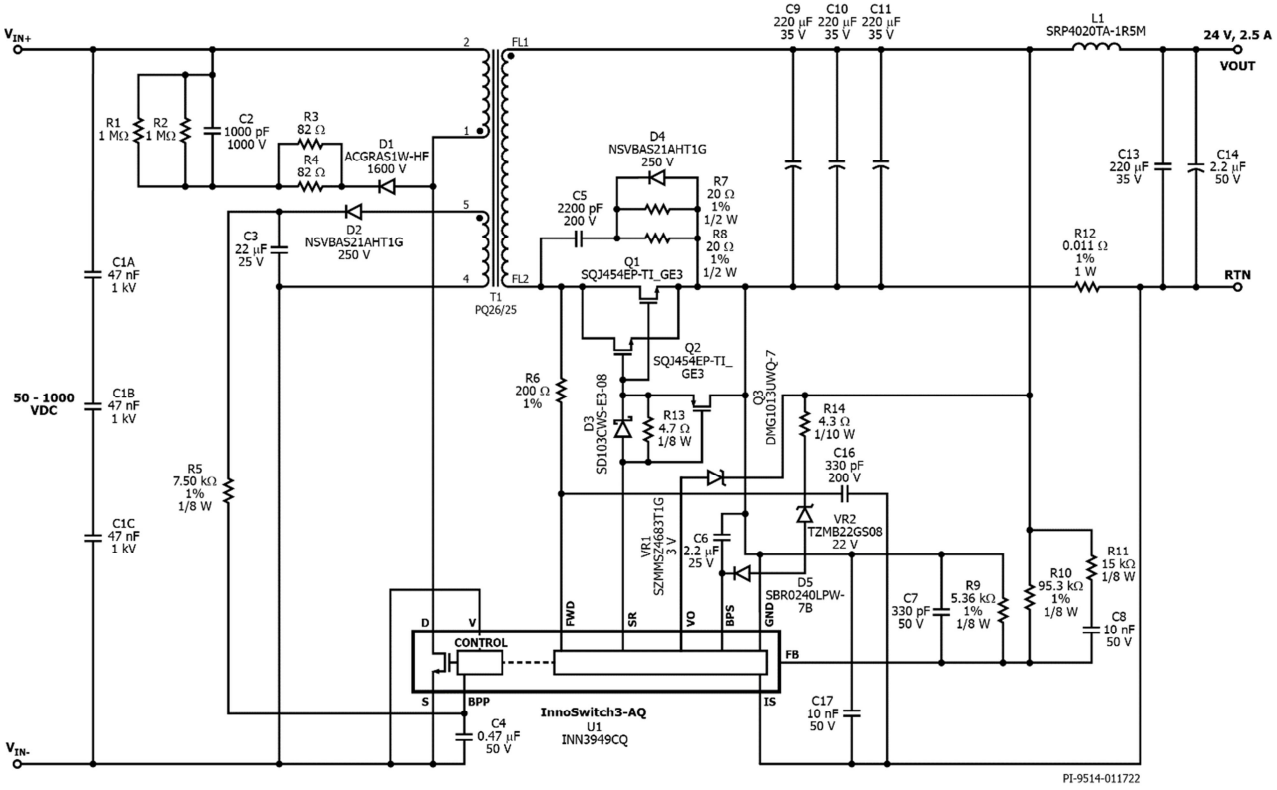


Figure 3 – Schematic.

4 Circuit Description

4.1 *INN3949CQ IC Primary*

One end of the transformer primary is connected to the DC bus, the other is connected to the integrated power MOSFET inside the INN3949CQ IC (U1). High-voltage ceramic capacitors C1A, C1B and C1C are used for the decoupling capacitors for the DC input voltage, and a low-cost RCD clamp formed by D1, R1, R2, R3, R4 and C2 limits the peak Drain voltage due to transformer leakage inductance effect.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C4, when DC input voltage is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer. The output is configured as a flyback winding, which is rectified and filtered using diode D2 and capacitor C3, fed the BPP pin capacitor via a current limiting resistor R5.

In this design the input primary under and overvoltage features were disabled by connecting the V pin to source.

4.2 *INN3949CQ IC Secondary*

The secondary-side of the INN3949CQ IC provides output voltage, output current sensing, and drive a MOSFET providing synchronous rectification.

The 24 V output rectification is provided by SR FETs Q1 and Q2. Low ESR capacitors, C9, C10, C11, C13, C14 and output inductor L1 provide filtering. RC snubber network comprising D4, R7, R8, and C5 for Q1 and Q2 damps high frequency ringing across SR FETs, which results from leakage inductance of the transformer windings and the secondary trace inductances. The gates of Q1 and Q2 are turned on based on the winding voltage sensed via R6 and the FWD pin of the IC. Capacitor C16 is used to suppress high frequency spikes on the FWD pin. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below ground. Secondary-side control of the primary-side MOSFET ensures that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin. A gate enhancement circuit comprising D3, R13 and Q3 prevents Vgs to turn-on during primary turn-ons. The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into Zener VR1 which is connected to the VO pin. Zener VR1 is used to reduce the voltage stress on the VO pin. It will charge the BPS pin capacitor C6 via an internal regulator. The OVP sensing circuit, R14, VR2 and D5, connected to BPS pin provides secondary-side overvoltage protection.

Resistors R9 and R10 form a voltage divider network that senses the output voltage. INN3949CQ IC has an internal reference of 1.265 V. Capacitor C7 provides decoupling from high frequency noise affecting power supply operation, and C8 and R11 is the feedforward network to speed up the response time to lower the output ripple. The output current is sensed by R12 and filtered by C17 with a threshold of approximately 35 mV to reduce losses. Once the current sense threshold across this resistor is exceeded, the device will go into auto-restart.

5 PCB Layout

Layers: 4
Board Thickness: 0.062”
Board Material: FR4
Copper Weight: 2 oz
Surface finish: LF HASL

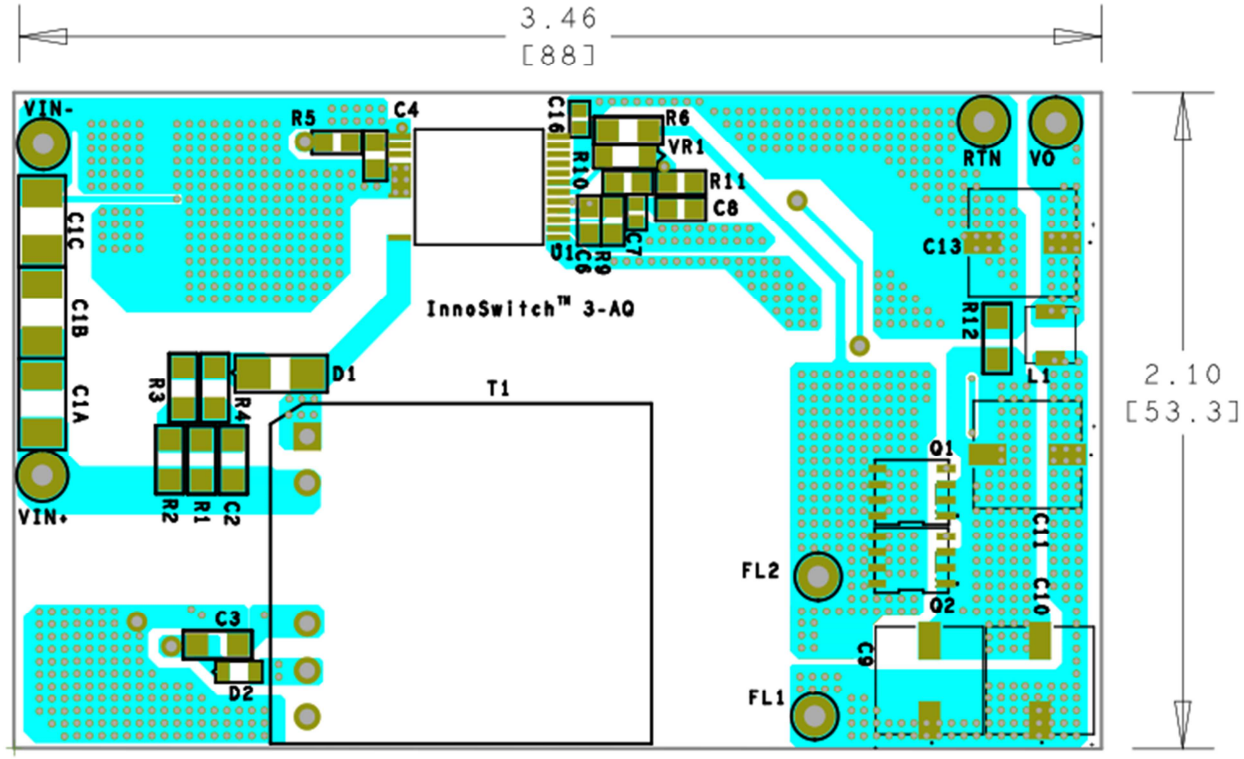


Figure 4 – Printed Circuit Board Layout (Top).

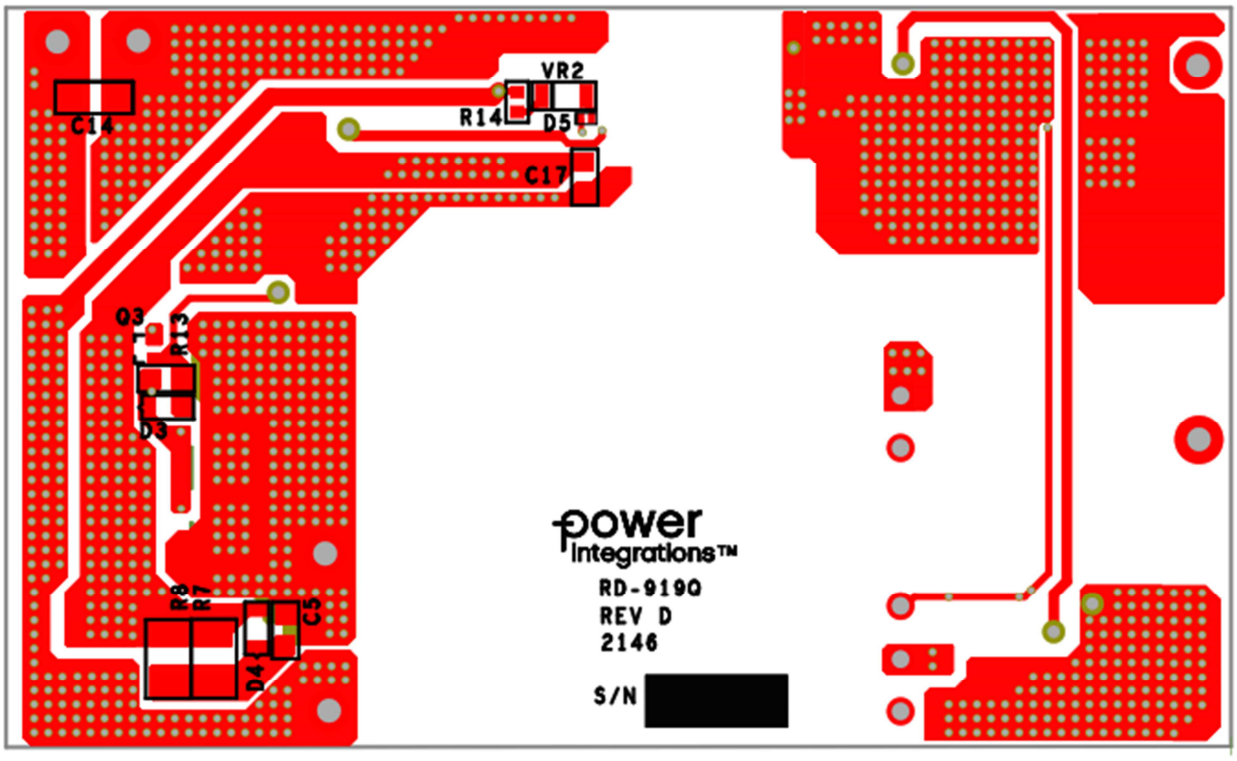


Figure 5 – Printed Circuit Board Layout (Bottom).

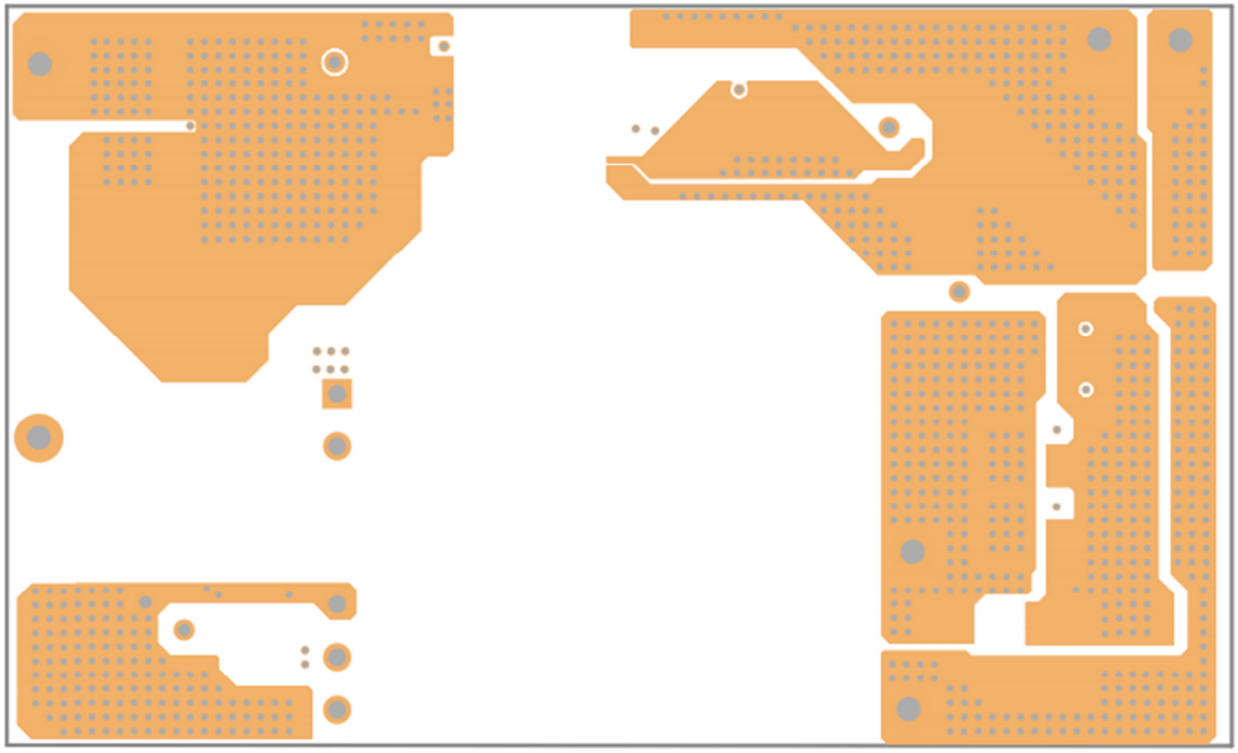


Figure 6 – Printed Circuit Board Layout (Internal layer 1).

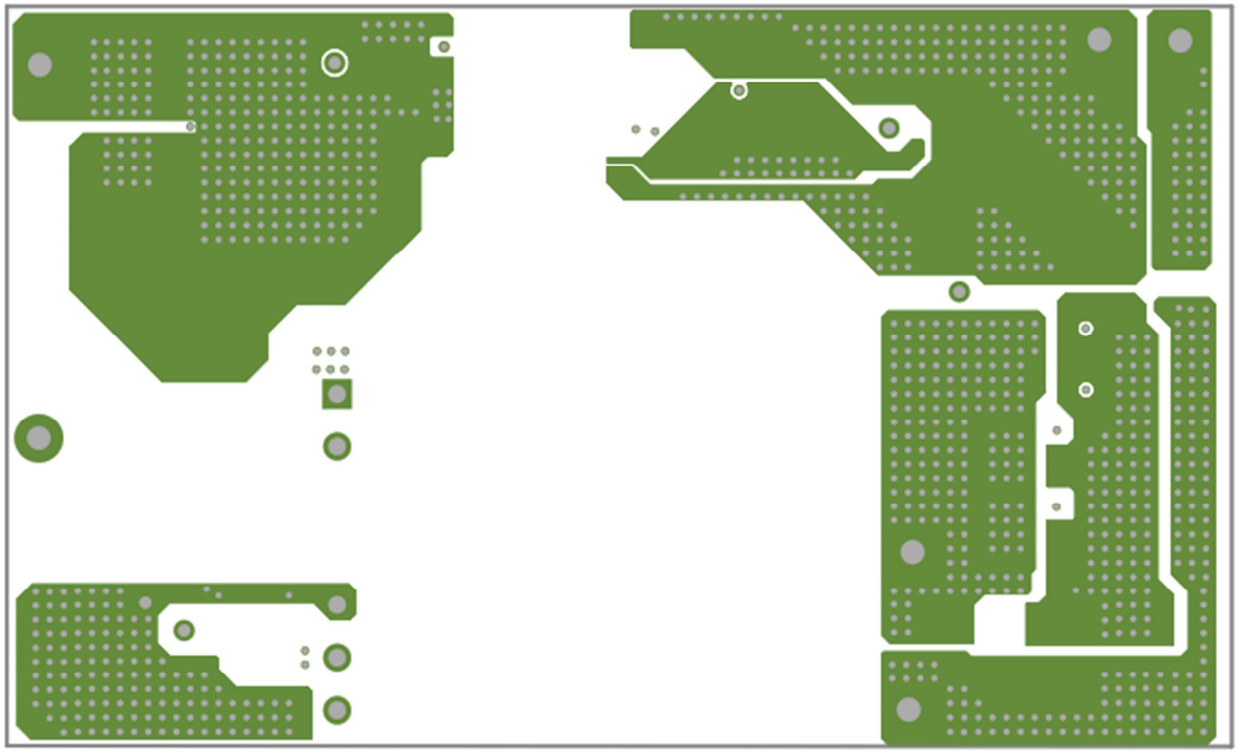


Figure 7 – Printed Circuit Board Layout (Internal layer 2).

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C2	1000 pF, ±10%, 1000 V (1 kV), Ceramic, C0G, NP0 1206 (3216 Metric)	C1206C102KDGACAUTO	Kemet
2	1	C3	22 µF, ±20%, 25 V, Ceramic, X5R, 1206 (3216 Metric)	12063D226MAT2A	AVX
3	1	C4	0.47 µF, ±10% ,50 V, Ceramic, X7R, 0805 (2012 Metric), -55 °C ~ 125 °C	CGA4J3X7R1H474K125AB	TDK
4	1	C5	2200 pF, ±10%, 200 V, Ceramic, X7R, 0805 (2012 Metric)	08052C222K4T2A	AVX
5	1	C6	2.2 µF ±10% 25 V Ceramic X7R 0805 (2012 Metric)	GCM21BR71E225KA73L	Murata
6	1	C7	330 pF, ±5%, 50 V, Ceramic, C0G, NP0, 0603 (1608 Metric)	C0603C331J5GACAUTO	KEMET
7	2	C8 C17	10 nF, 50 V, Ceramic, X7R, 0805	C0805C103K5RACTU	Kemet
8	4	C9 C10 C11 C13	220 µF, 20%, 35 V, Aluminum - Polymer, (8.30 mm x 8.30 mm), Height 0.472" (12.00 mm), SMD	PCR1V221MCL1GS	Nichicon
9	1	C14	2.2 µF, ±10%, 50 V, Ceramic, X7R, Bypass, Decoupling, 1206 (3216 Metric)	C1206C225K5RACAUTO7210	KEMET
10 Alt.	1 1	C16 C16	330 pF ±5%, 200 V, Ceramic, C0G, NP0, 0603 (1608 Metric) 330 pF ±5%, 200 V, Ceramic, C0G, NP0, 0805 (2012 Metric)	CGJ3E3C0G2D331J080AA C0805C331J2GACAUTO	TDK Corp Kemet
11	3	C1A C1B C1C	0.047 µF, ±10%, 1000 V (1 kV), Ceramic, X7R, 1812 (4532 Metric)	1812Y1K00473KST	Knowles Syfer
12	1	D1	Diode Standard 1600 V 1 A Surface Mount DO-214AC (SMA)	ACGRAS1W-HF	Comchip
13 Alt.	2 2	D2 D4 D2 D4	Diode, Standard, 250 V, 200 mA, SC-76, SOD-323 Diode, Standard, 200 V, 200 mA (DC), SOD-323, SC-17	NSVBAS21AHT1G SBAS20HT1G	ON Semi ON Semi
14 Alt.	1 1	D3 D3	Diode, Schottky, 20 V, 350 mA (DC), SMT, SOD-323 SC-76 Diode, Schottky, 40 V, 350 mA (DC), SMT, SOD-323 SC-76	SD103CWS-E3-08 SD103AWS-HE3-08	Vishay Vishay
15	1	D5	Diode Standard 40 V 200 mA Surface Mount X1-DFN1006-2	SBR0240LPW-7B	Diodes Incorporated
16	2	FL1 FL2	Flying Lead, Hole size 70 mils	N/A	N/A
17	1	L1	1.5 µH, ±20%, Shielded, Wirewound, Inductor, 4.5 A, 42 mΩ Max, Automotive, AEC-Q200, 2-SMD	SRP4020TA-1R5M	Bourns
18	2	Q1 Q2	MOSFET, N-Channel, 200 V, 13 A (Tc), 68 W (Tc), Automotive, AEC-Q101, PowerPAK® SO-8	SQJ454EP-T1_GE3	Vishay
19	1	Q3	MOSFET, P-Channel 20 V, 820 mA (Ta), 310 mW (Ta), SMT, SC-70, SOT-323	DMG1013UWQ-7	Diodes Incorporated
20	2	R1 R2	RES, 1 MΩ, ±5%, ¼ W Chip, 1206 (3216 Metric), High Voltage Thick Film	KTR18EZPJ105	Rohm Semi
21	2	R3 R4	RES, 82 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ820V	Panasonic
22	1	R5	RES, 7.50 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF7501V	Panasonic
23	1	R6	RES, 200 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2000V	Panasonic
24	2	R7 R8	RES, 20 Ω ±1% 0.5W, Thick Film1210 (3225 Metric)	CRCW121020R0FKEA	Vishay Dale
25	1	R9	RES, 5.36 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5361V	Panasonic
26	1	R10	RES, 95.3 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF9532V	Panasonic
27	1	R11	RES, 15 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ153V	Panasonic
28	1	R12	0.011 Ω, ±1%, ±75ppm/°C, 1 W, 1206 (3216 Metric), Automotive AEC-Q200, Current Sense, -55 °C ~ 155 °C	ERJ-8CWFR011V	Panasonic
29	1	R13	RES, 4.7 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ4R7V	Panasonic
30	1	R14	RES, 4.3 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ4R3V	Panasonic
31	2	RTN VIN-	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
32	1	T1	Bobbin, PQ26/25, Vertical, 12 pins	PQ26X25	Pin Shine
33	1	U1	InnoSwitch3-AQ, 1700 V, InSOP-24D	INN3949CQ	Power Integrations
34	1	VR1	Diode Zener 3 V 500 mW SOD123	SZMMSZ4683T1G	ON Semi
35	1	VR2	Diode Zener 22 V 500 mW SOD80	TZMB22-GS08	Vishay
36	2	VIN+ VO	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone

7 Transformer Design

7.1 *Electrical Diagram*

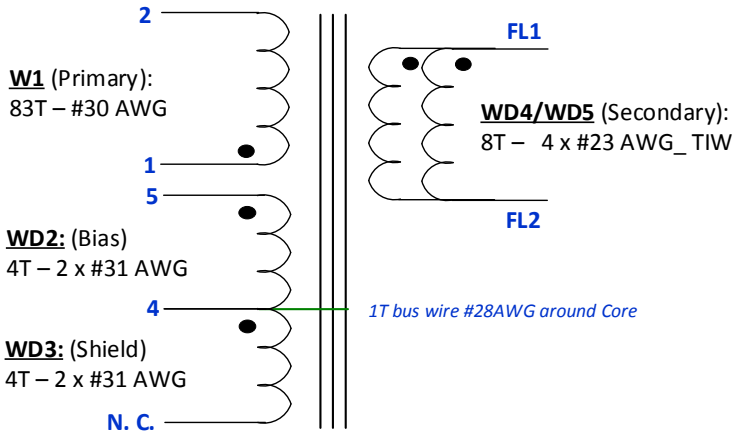


Figure 8 – Electrical Diagram.

7.2 *Electrical Specification*

Parameter	Condition	Spec.
Electrical Strength	60 seconds, 10 mA, from pins 1-6 to FL1 & FL2.	3000 VAC
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and 2, with all other windings open.	1735 µH ±5%
Resonant Frequency	Between pin 1 and 2, other windings open.	550 kHz (Min.)
Primary Leakage Inductance	Between pin 1 and 2, with pins: FL1-FL2 shorted.	30 µH (Max.)

7.3 *Materials List*

Item	Description
[1]	Core: PQ26/25 – TDK PC95.
[2]	Bobbin: PQ26/25 – Vertical – 12 pins (6/6); PI#: 25-00055-00; or Equivalent.
[3]	Magnet Wire: #30 AWG, Double Coated.
[4]	Magnet Wire: #31 AWG, Double Coated.
[5]	Magnet Wire: #23 AWG, Triple Insulated Wire.
[6]	Bus Wire: #28 AWG, Alpha Wire, Tinned Copper.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 13.5 mm Width.
[8]	Varnish: Dolph BC-359.

7.4 *Transformer Build Diagram*

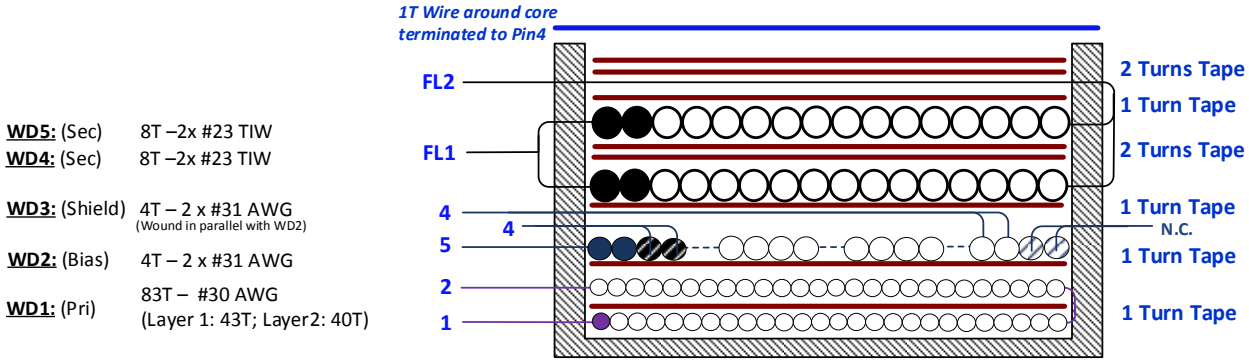
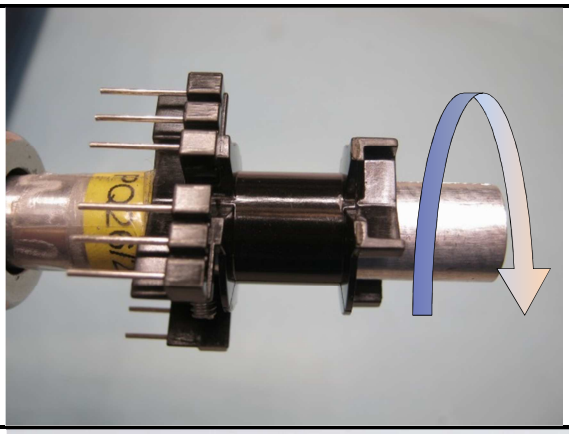
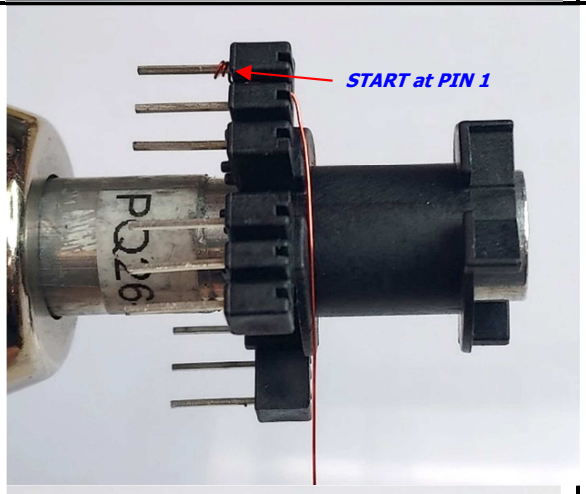
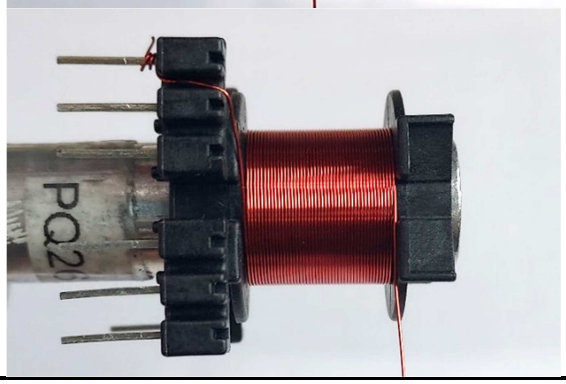


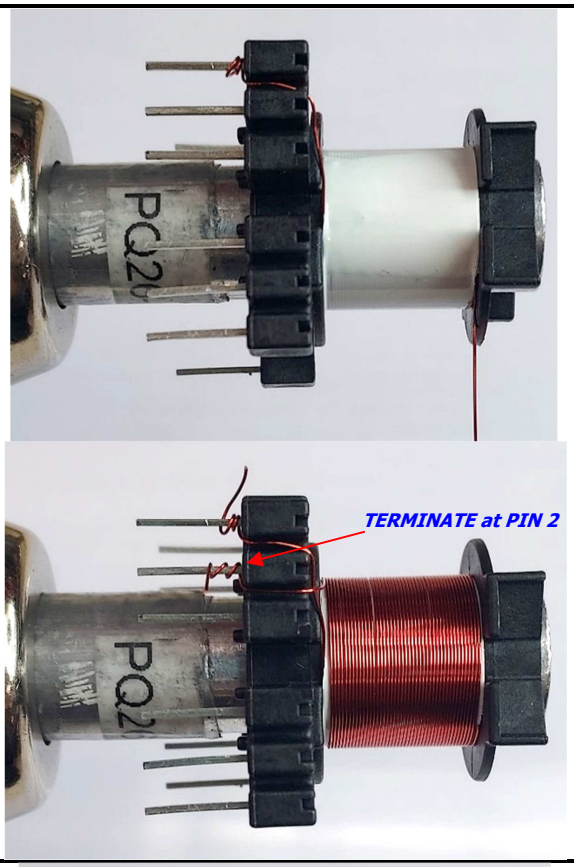
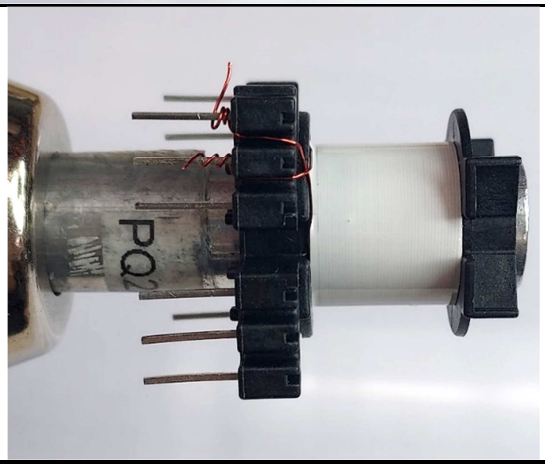
Figure 9 – Transformer Build Diagram.

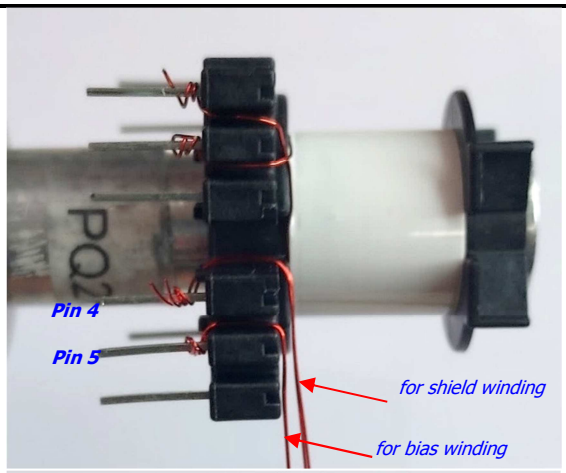
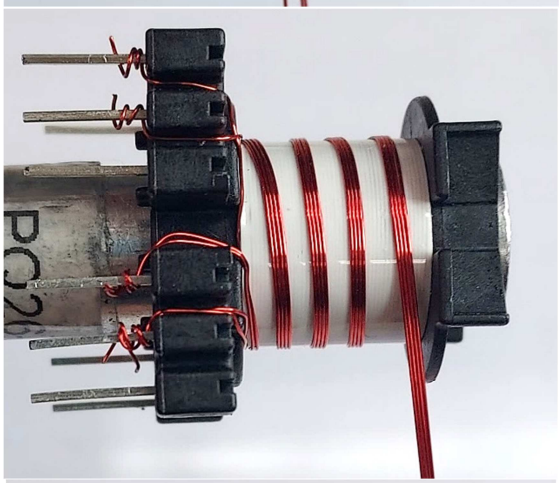
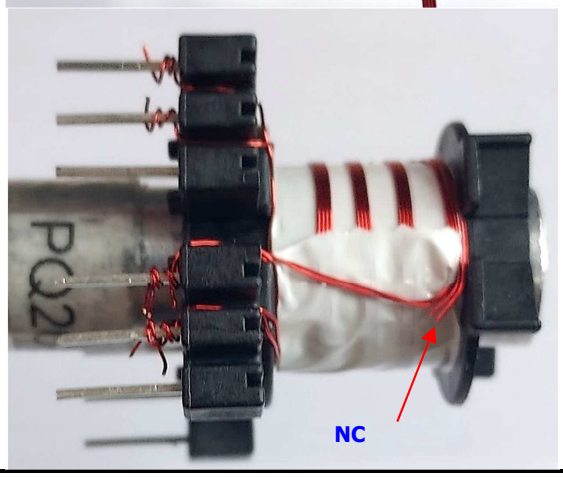
7.5 *Transformer Instruction*

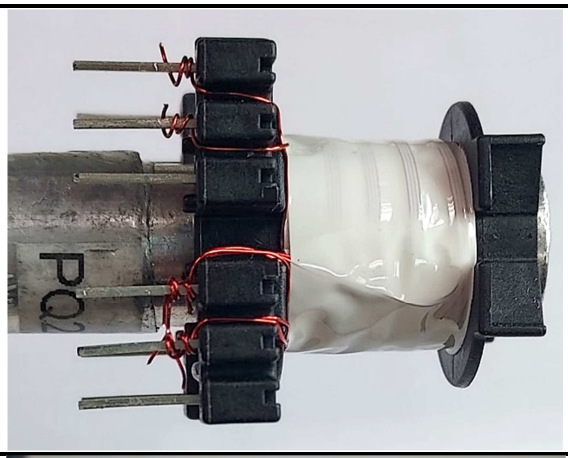
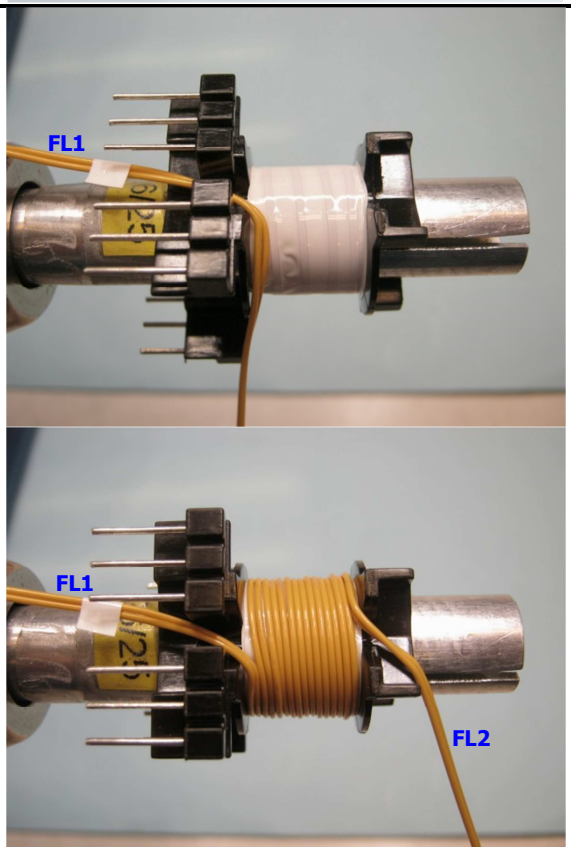
Winding Preparation	Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction.
WD1 1st Primary	Start at pin 1, wind 43 turns of wire Item [3] with tight tension, from left to right, and place 1 layer of tape Item [7]. Continue wind another 40T from right to left, at the last turn, terminate this wire at pin 2.
Insulation	1 layer of tape Item [7].
WD2: Bias & WD3: Shield	Use 2 wires Item [4] start at pin 5 for Bias winding, also use 2 wires same Item [4] start at pin 4 for Shield winding. Wind all 4 wires in parallel and together; spread the wires evenly on the bobbin. At the 4th turn: - bring 2 wires for Bias winding to the left and terminate at pin 4, - cut short 2 wires for Shield Winding as No-Connect.
Insulation	1 layer of tape Item [7].
WD4 Secondary	Start at left slot of secondary side of bobbin, use 2 wires Item [5] leaving ~1", mark as FL1, and wind 8 turns with tight tension. At the last turn, exit the wire at the right slot, also leaving ~ 2" and mark as FL2.
Insulation	Place 2 layers of tape Item [7].
WD5 Secondary	Repeat same winding above and on top, also start as FL1 and end FL2.
Insulation	Place 1 layer of tape Item [7], bring 4 wires floating FL2 from Secondary – WD3 to left slot and continue placing another 2 layers of tape to secure these wires and all the windings.
Finish	Gap core halves to get 1735 µH. Use 2" of bus wire Item [6], solder to pin 4 then lean along core halves and secure with tape. Remove pins 3, 7, 8, 9, 10, 11 & 12. Varnish with Item [8].

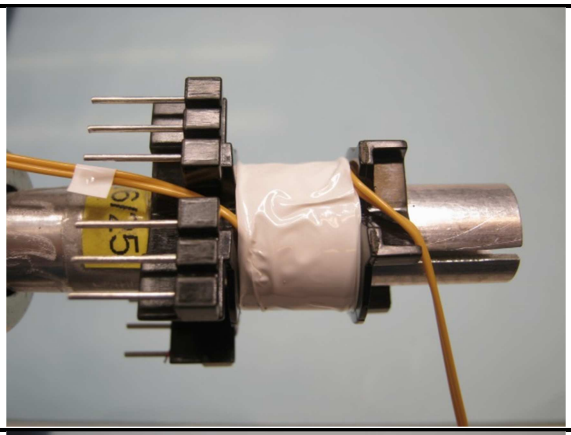
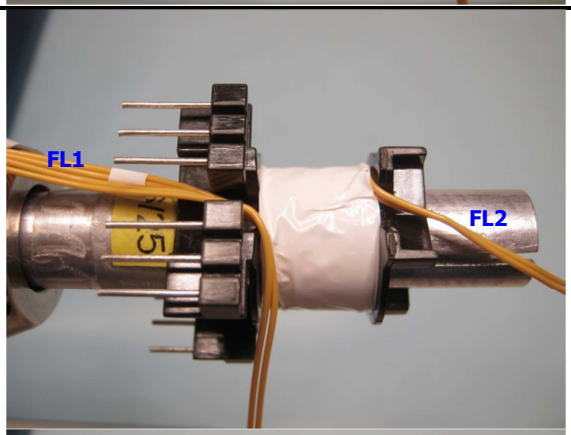
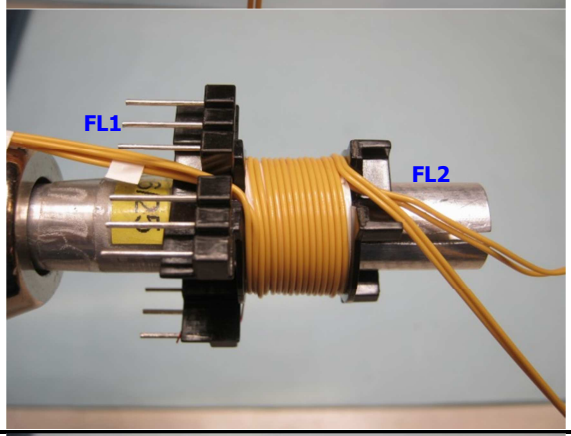
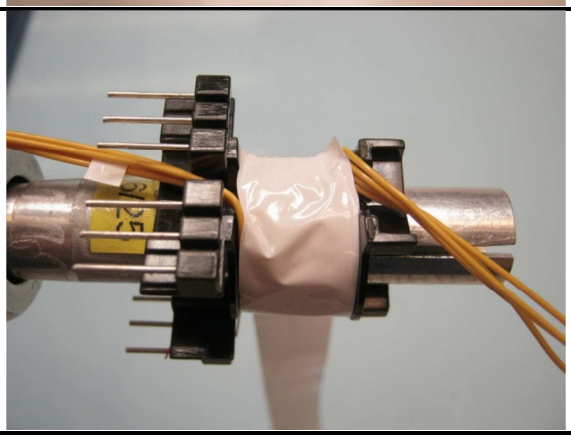
7.6 *Winding Illustrations*

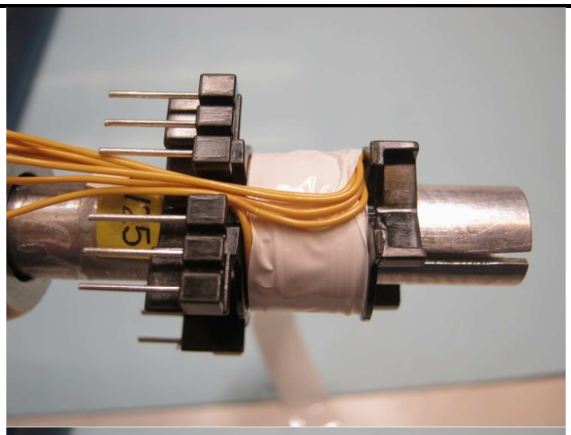
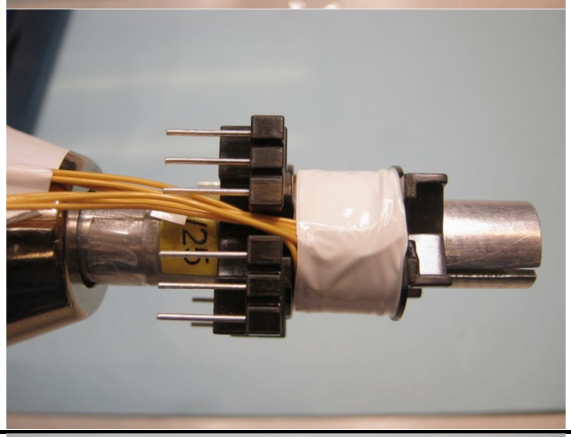
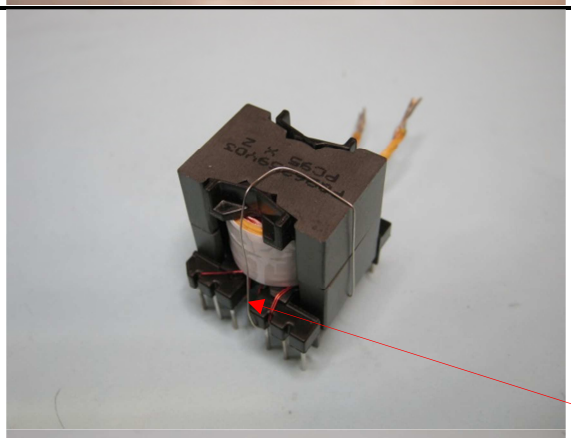
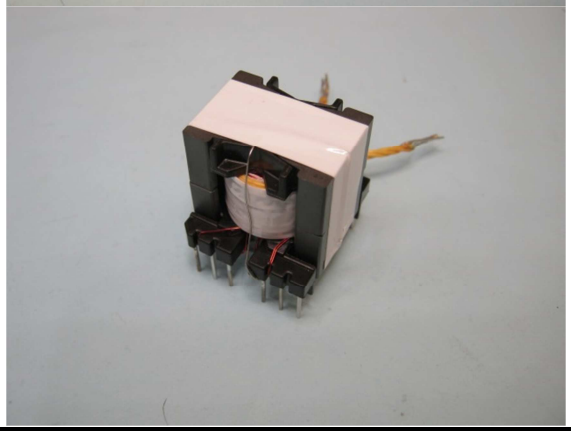
Winding Preparation		Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction.
WD1: Primary	 	Start at pin 1, wind 43 turns of wire Item [3] with tight tension, from left to right, and place 1 layer of tape Item [7]. Continue wind another 40T from right to left, at the last turn, terminate this wire at pin 2.

		
Insulation		1 layer of tape Item [7].

WD2: Bias & WD3: Shield	  	Use 2 wires Item [4] start at pin 5 for Bias winding, also use 2 wires same Item [4] start at pin 4 for Shield winding. Wind all 4 wires in parallel and together; spread the wires evenly on the bobbin. At the 4th turn: - bring 2 wires for Bias winding to the left and terminate at pin 4, - cut short 2 wires for Shield Winding as No-Connect.

Insulation		1 layer of tape Item [7].
WD4 Secondary		Start at left slot of secondary side of bobbin, use 2 wires Item [5] leaving ~1”, mark as FL1, and wind 8 turns with tight tension. At the last turn, exit the wire at the right slot, also leaving ~2” and mark as FL2.

Insulation		Place 2 layers of tape Item [7].
WD5 Secondary	 	Repeat same winding above and on top, also start as FL1 and end FL2.
Insulation		Place 1 layer of tape Item [7], bring 4 wires floating FL2 from Secondary – WD3 to left slot and continue placing another 2 layers of tape to secure these wires and all the windings.

	 	
Finish	 	Gap core halves to get 1735uH. Use 2” of bus wire Item [6], solder to pin 4 then lean along core halves and secure with tape. Remove pins 3, 7, 8, 9, 10, 11 & 12. Varnish with Item [8].

7.7 *Transformer Design Spreadsheet*

1	DCDC_InnoSwitch3AQ1700V _Flyback_120821; Rev.2.2; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ1700V Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VOUT	24.00		24.00	V	Output Voltage
4	**OPERATING CONDITION 1**					
5	VINDC1	1000.00		1000.00	V	Input DC voltage 1
6	IOUT1	2.500		2.500	A	Output current 1
7	POUT1			60.00	W	Output power 1
8	EFFICIENCY1			0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
11	**OPERATING CONDITION 2**					
12	VINDC2	300.00		300.00	V	Input DC voltage 2
13	IOUT2	2.500		2.500	A	Output current 2
14	POUT2			60.00	W	Output power 2
15	EFFICIENCY2			0.85		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
69	**PRIMARY CONTROLLER SELECTION**					
70	ENCLOSURE			ADAPTER		Power supply enclosure
71	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
72	VDRAIN_BREAKDOWN			1700	V	Device breakdown voltage
73	DEVICE_CODE	INN3949CQ		INN3949CQ		Device code
74	PDEVICE_MAX			70	W	Device maximum power capability
75	RDSON_25DEG			0.62	Ω	Primary switch on-time resistance at 25°C
76	RDSON_100DEG			0.98	Ω	Primary switch on-time resistance at 100°C
77	ILIMIT_MIN			1.767	A	Primary switch minimum current limit
78	ILIMIT_TYP			1.900	A	Primary switch typical current limit
79	ILIMIT_MAX			2.033	A	Primary switch maximum current limit
80	VDRAIN_ON_PRSW			0.21	V	Primary switch on-time voltage drop
81	VDRAIN_OFF_PRSW			1290	V	Peak drain voltage on the primary switch during turn-off
85	**WORST CASE ELECTRICAL PARAMETERS**					
86	FSWITCHING_MAX	36500		36500	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
87	VOR	250.0		250.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
88	KP			1.932		Measure of continuous/discontinuous mode of operation
89	MODE_OPERATION			DCM		Mode of operation
90	DUTYCYCLE			0.302		Primary switch duty cycle
91	TIME_ON_MIN			2.43	us	Minimum primary switch on-time
92	TIME_ON_MAX			9.50	us	Maximum Primary switch on-time
93	TIME_OFF			19.30	us	Primary switch off-time

94	LPRIMARY_MIN			1647.9	uH	Minimum primary magnetizing inductance
95	LPRIMARY_TYP			1734.6	uH	Typical primary magnetizing inductance
96	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
97	LPRIMARY_MAX			1821.3	uH	Maximum primary magnetizing inductance
99	**PRIMARY CURRENT**					
100	IAVG_PRIMARY			1.600	A	Primary switch average current
101	IPEAK_PRIMARY			1.600	A	Primary switch peak current
102	IPEDESTAL_PRIMARY			0.218	A	Primary switch current pedestal
103	IRIPPLE_PRIMARY			1.600	A	Primary switch ripple current
104	IRMS_PRIMARY			0.482	A	Primary switch RMS current
106	**SECONDARY CURRENT**					
107	IPEAK_SECONDARY			16.599	A	Secondary winding peak current
108	IPEDESTAL_SECONDARY			0.000	A	Secondary winding pedestal current
109	IRMS_SECONDARY			5.476	A	Secondary winding RMS current
110	IRIPPLE_CAP_OUT			4.872	A	Output capacitor ripple current
113	**TRANSFORMER CONSTRUCTION PARAMETERS**					
114	**CORE SELECTION**					
115	CORE	PQ26/25		PQ26/25		Core selection
116	CORE NAME			B65877A0000R095		Core code
117	AE			122.0	mm^2	Core cross sectional area
118	LE			53.6	mm	Core magnetic path length
119	AL			5700	nH	Ungapped core effective inductance per turns squared
120	VE			6530	mm^3	Core volume
121	BOBBIN NAME			B65878E1012D001		Bobbin name
122	AW			47.0	mm^2	Bobbin window area
123	BW			12.70	mm	Bobbin width
124	MARGIN			0.0	mm	Bobbin safety margin
126	**PRIMARY WINDING**					
127	NPRIMARY			83		Primary winding number of turns
128	BPEAK			3743	Gauss	Peak flux density
129	BMAX			2814	Gauss	Maximum flux density
130	BAC			1407	Gauss	AC flux density (0.5 x Peak to Peak)
131	ALG			252	nH	Typical gapped core effective inductance per turns squared
132	LG			0.582	mm	Core gap length
133	LAYERS_PRIMARY			2		Primary winding number of layers
134	AWG_PRIMARY	30		30		Primary wire gauge
135	OD_PRIMARY_INSULATED			0.303	mm	Primary wire insulated outer diameter
136	OD_PRIMARY_BARE			0.255	mm	Primary wire bare outer diameter
137	CMA_PRIMARY			208.5	Cmils/A	Primary winding wire CMA
139	**SECONDARY WINDING**					

140	NSECONDARY	8		8		Secondary winding number of turns
141	AWG_SECONDARY			19		Secondary wire gauge
142	OD_SECONDARY_INSULATED			1.217	mm	Secondary wire insulated outer diameter
143	OD_SECONDARY_BARE			0.912	mm	Secondary wire bare outer diameter
144	CMA_SECONDARY			235.2	Cmils/A	Secondary winding wire CMA
146	**BIAS WINDING**					
147	NBIAS			4		Bias winding number of turns
151	**PRIMARY COMPONENTS SELECTION**					
152	**BIAS WINDING**					
153	VBIAS			9.00	V	Rectified bias voltage
154	VF_BIAS			0.70	V	Bias winding diode forward drop
155	VREVERSE_BIASDIODE			57.19	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
156	CBIAS			22	uF	Bias winding rectification capacitor
157	CBPP			0.47	uF	BPP pin capacitor
161	**SECONDARY COMPONENTS SELECTION**					
162	**RECTIFIER**					
163	VDRAIN_OFF_SRFET			144.46	V	Secondary rectifier reverse voltage (accounting for a 20% parasitic voltage ring)
164	SRFET	SQJ454EP		SQJ454EP		Secondary rectifier (Logic MOSFET)
165	VBREAKDOWN_SRFET			200	V	Secondary rectifier breakdown voltage
166	RDSON_SRFET			150.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
168	**FEEDBACK COMPONENTS**					
169	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
170	RFB_LOWER			5.62	kΩ	Lower feedback resistor
171	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
175	**INPUT VOLTAGE SET-POINTS ANALYSIS**					
176	**TOLERANCE CORNER**					
177	USER_VINDC			1000	V	Input DC voltage corner to be evaluated
178	USER_ILIMIT	MAX		2.033	A	Current limit corner to be evaluated
179	USER_LPRIMARY	MAX		1821.3	uH	Primary inductance corner to be evaluated
181	**OPERATING CONDITION SELECTION**					
182	IOUT			2.500	A	Output current to be evaluated
183	EFFICIENCY			0.85		Converter efficiency to be evaluated
184	Z FACTOR			0.50		Z-factor to be evaluated
185	FSWITCHING			29299	Hz	Maximum switching frequency at full load
186	KP			2.745		Measure of continuous/discontinuous mode of operation
187	MODE_OPERATION			DCM		Mode of operation
188	DUTYCYCLE			0.083		Primary switch duty cycle

189	TIME_ON			2.85	us	Primary switch on-time
190	TIME_OFF			31.28	us	Primary switch off-time
192	**PRIMARY CURRENT**					
193	IAVG_PRIMARY			0.065	A	Primary switch average current
194	IPEAK_PRIMARY			1.564	A	Primary switch peak current
195	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
196	IRIPPLE_PRIMARY			1.564	A	Primary switch ripple current
197	IRMS_PRIMARY			0.261	A	Primary switch RMS current
199	**SECONDARY CURRENT**					
200	IPEAK_SECONDARY			16.230	A	Secondary winding peak current
201	IPEDESTAL_SECONDARY			0.000	A	Secondary winding pedestal current
202	IRMS_SECONDARY			5.415	A	Secondary winding RMS current
203	IRIPPLE_CAP_OUT			4.803	A	Output capacitor ripple current
205	**MAGNETIC FLUX DENSITY**					
206	BPEAK			3743	Gauss	Peak flux density
207	BMAX			2814	Gauss	Maximum flux density
208	BAC			1407	Gauss	AC flux density (0.5 x Peak to Peak)

8 Performance Data

Measured at PCB output terminal.

8.1 *Efficiency vs. Load and Input Voltage*

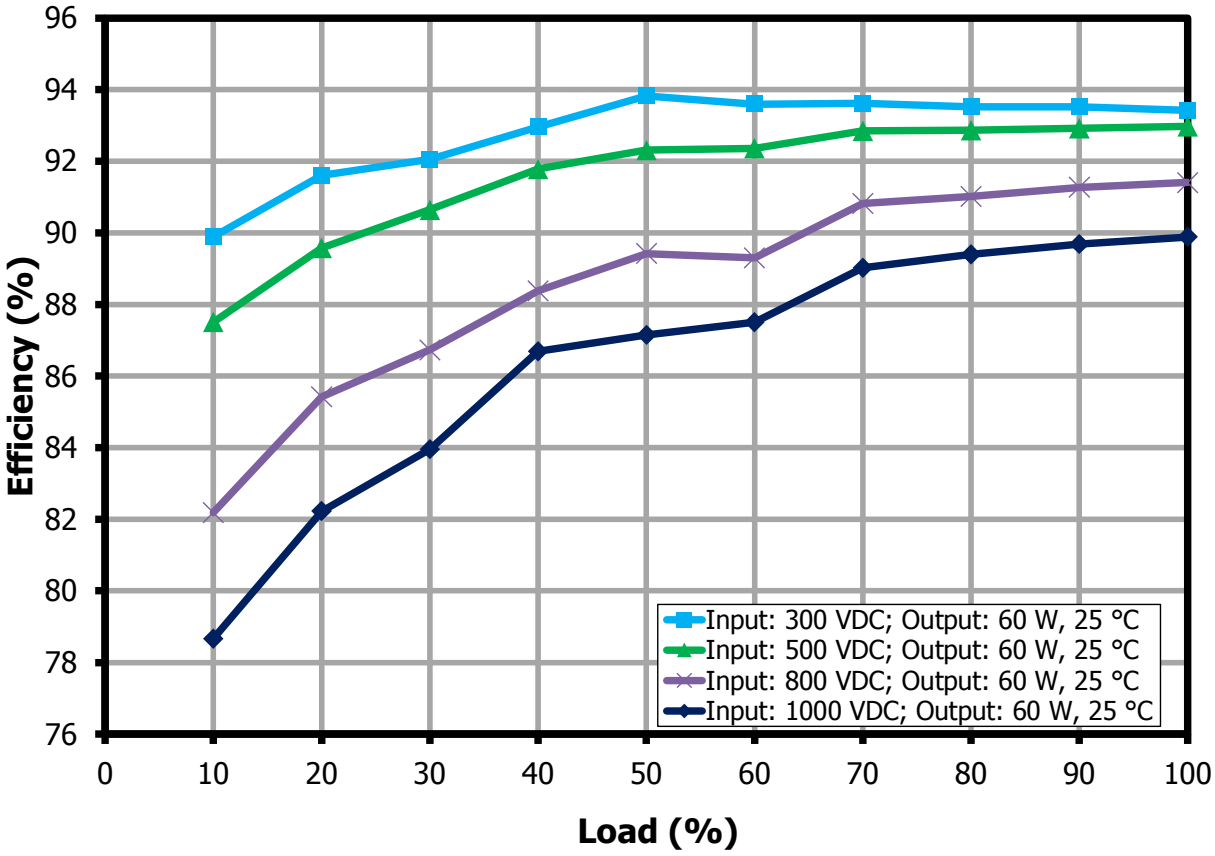


Figure 10 – Efficiency vs. Load and Input Voltage, 25 ºC Ambient Temperature.

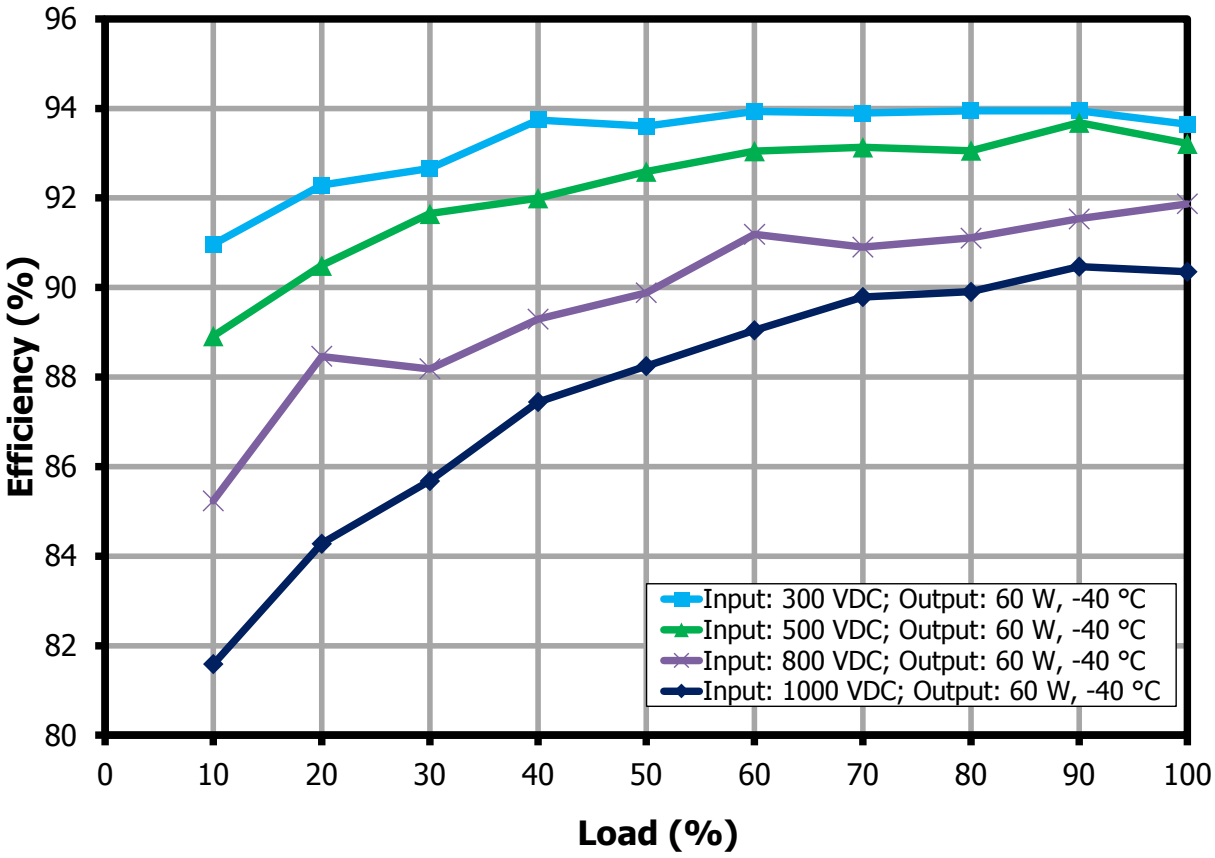


Figure 11 – Efficiency vs. Load and Input Voltage, -40 ºC Ambient Temperature.

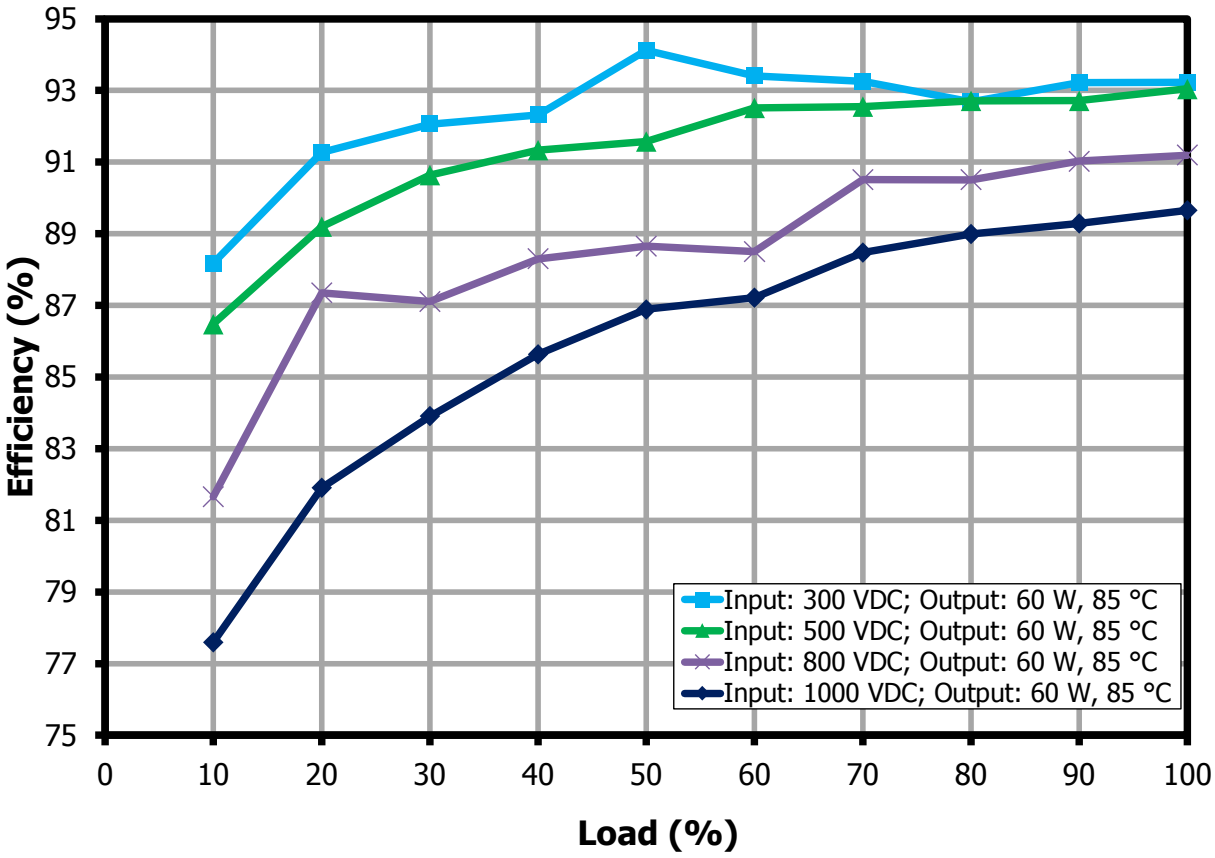


Figure 12 – Efficiency vs. Load and Input Voltage, 85 ºC Ambient Temperature.

8.2 *Full Load Efficiency vs. Line*

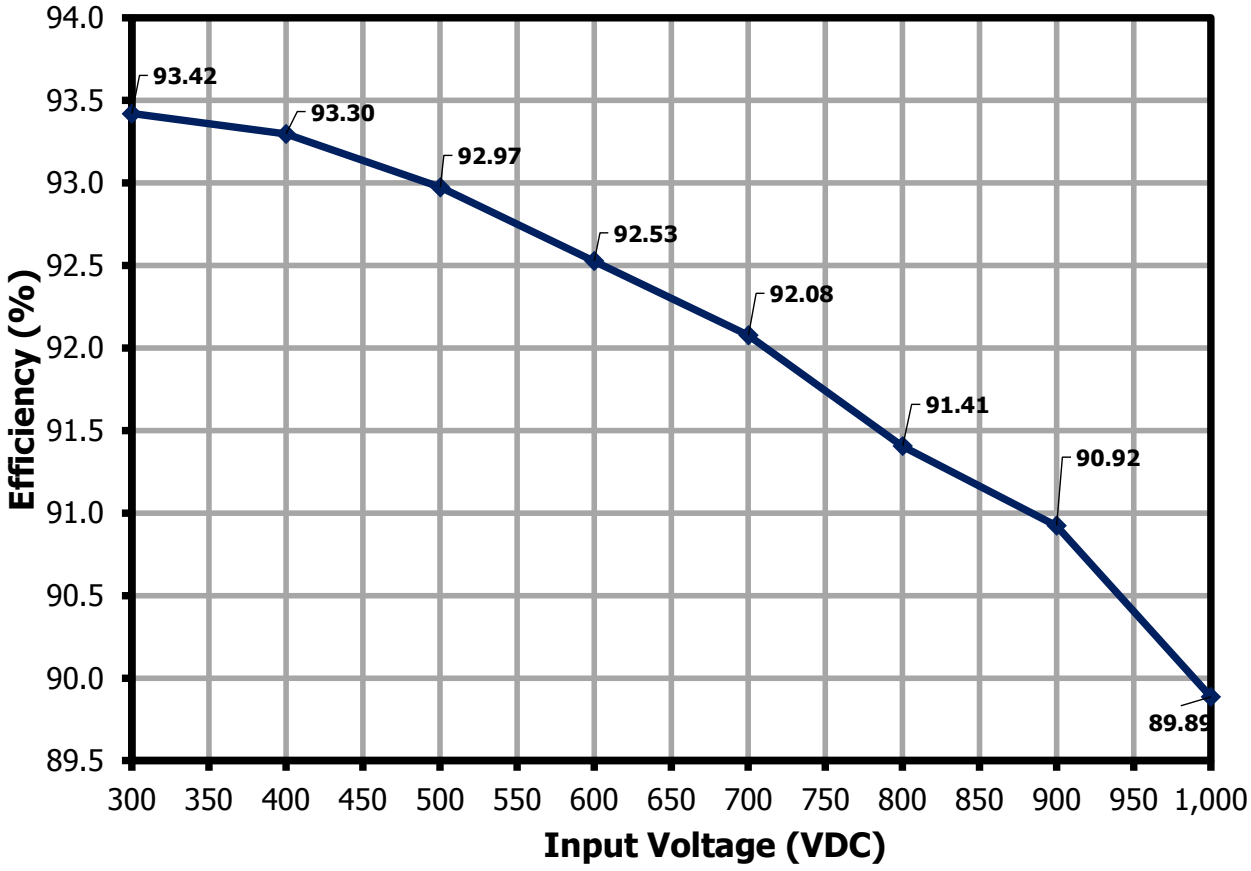


Figure 13 – Efficiency vs. Line (VDC), Room Temperature.

8.3 *Maximum Power at Low Input Voltage*

V_{IN} (VDC)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
50	4.73	23.41	0.18	4.20	88.68
60	9.02	23.04	0.36	8.25	91.48
70	27.74	23.10	1.10	25.29	91.18
80	31.06	23.18	1.23	28.51	91.79
90	34.01	23.25	1.35	31.39	92.29
100	36.97	23.30	1.47	34.25	92.64
200	50.1	23.53	2.00	47.06	93.92

8.4 *No-Load Input Power*

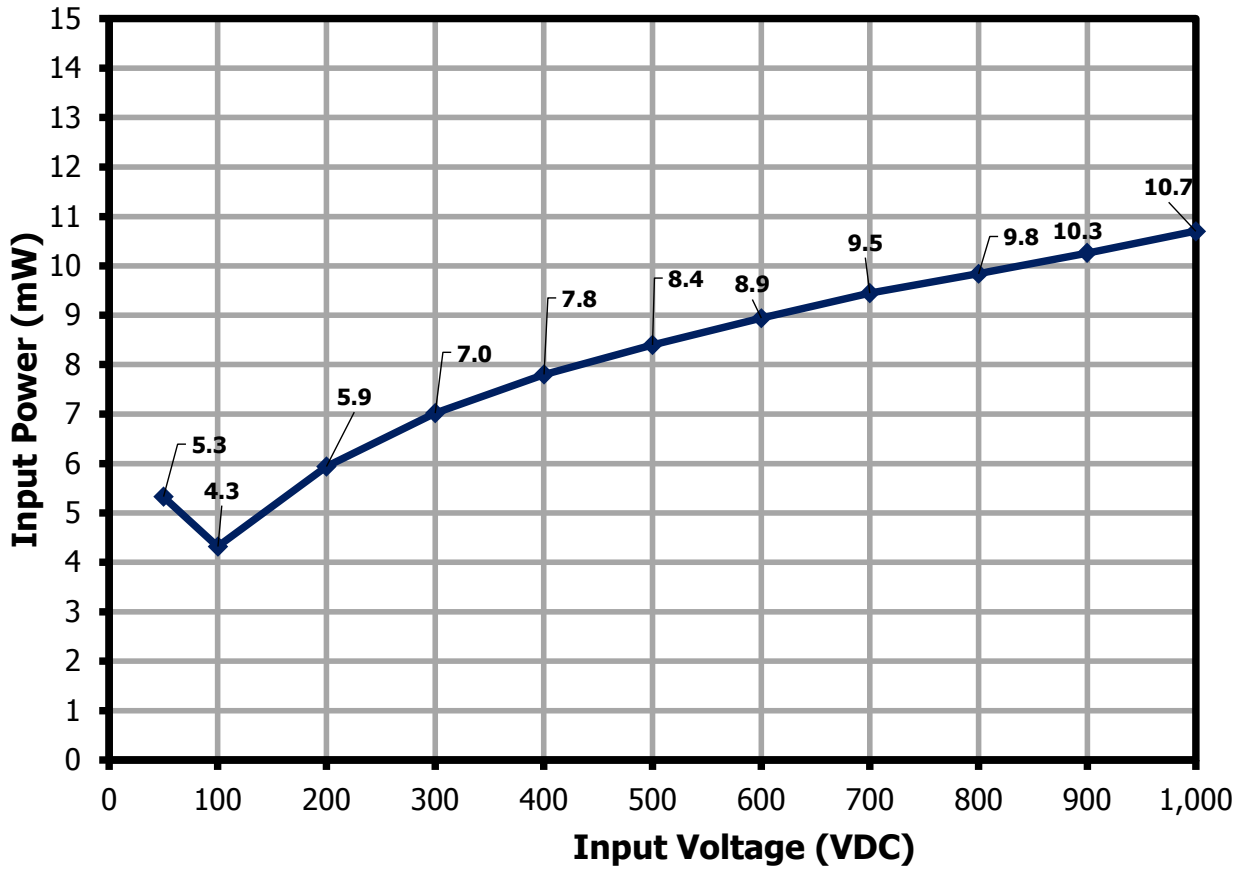


Figure 14 – No-Load Input Power, Room Temperature.

8.5 *Load and Line Regulation*

Measurements taken at 0% to 100% of rated load

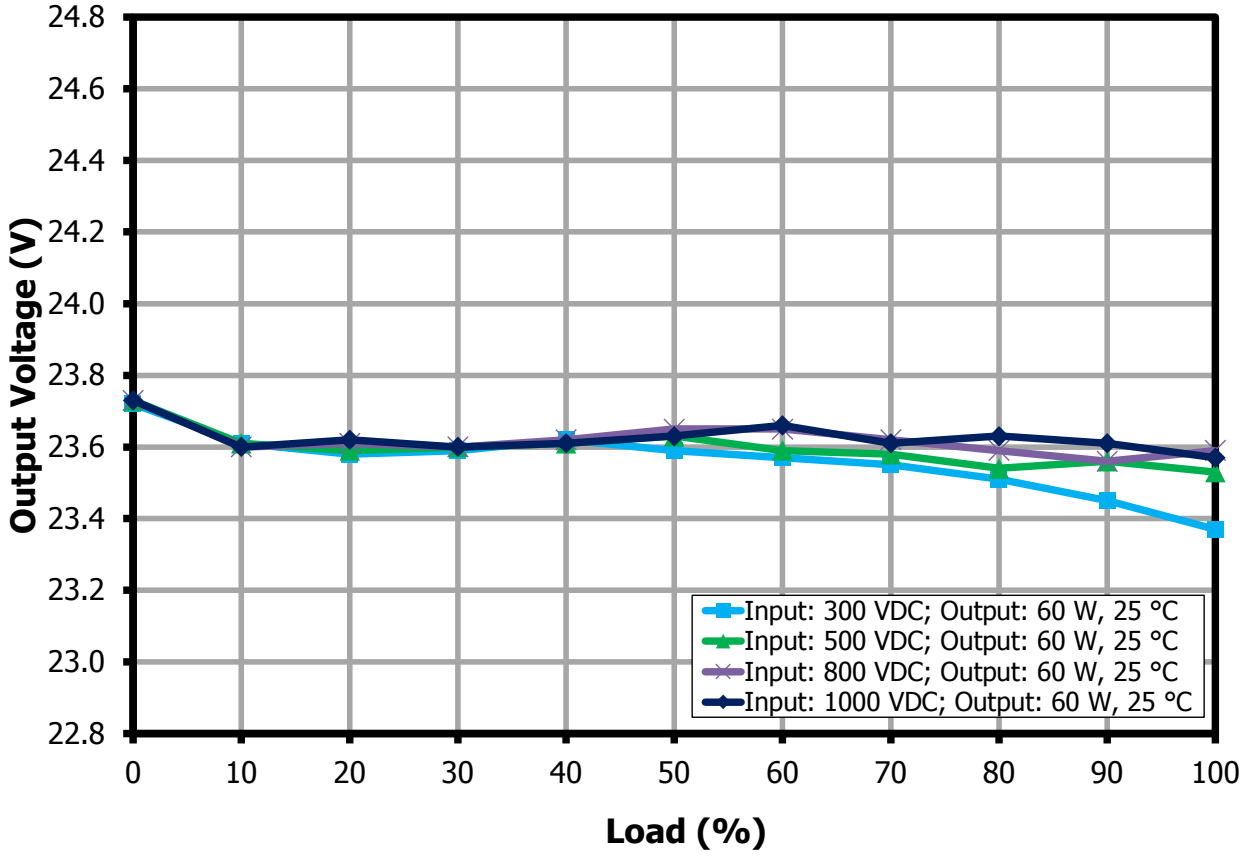


Figure 15 – Output Voltage vs. Output Current and Input Voltage (VDC), 25 °C Ambient Temperature.

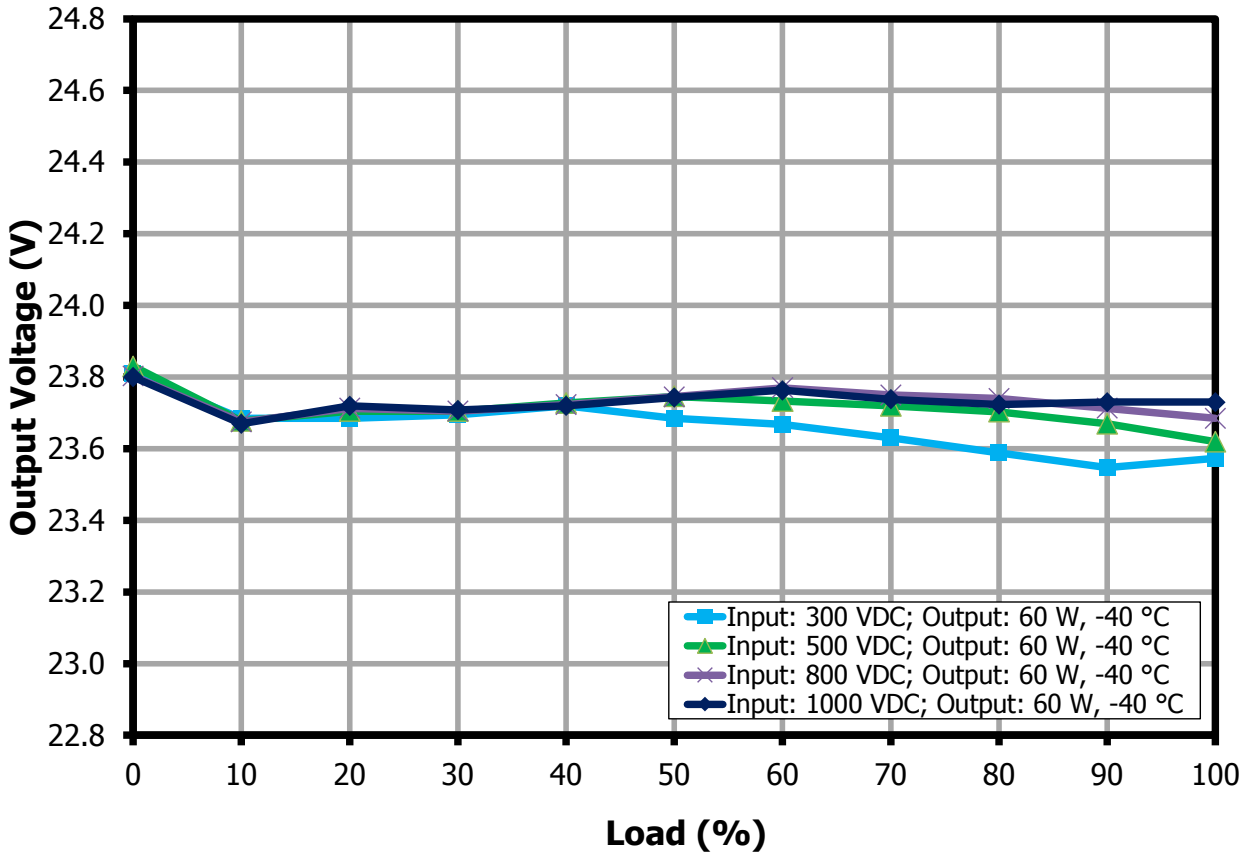


Figure 16 – Output Voltage vs. Output Current and Input Voltage (VDC), -40 °C Ambient Temperature.

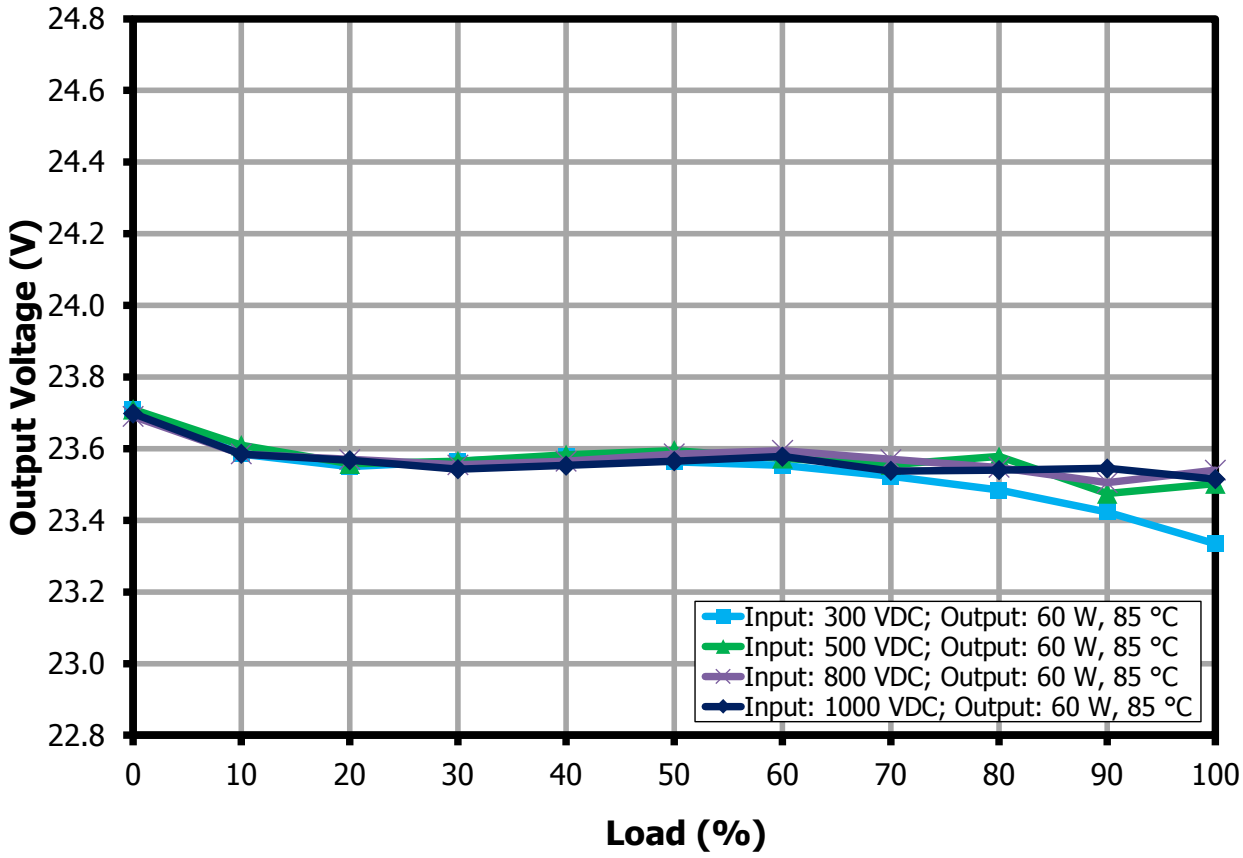


Figure 17 – Output Voltage vs. Output Current and Input Voltage (VDC), 85 °C Ambient Temperature.

9 Waveforms

9.1 *INN3949CQ Drain Voltage and Current, Steady-State*

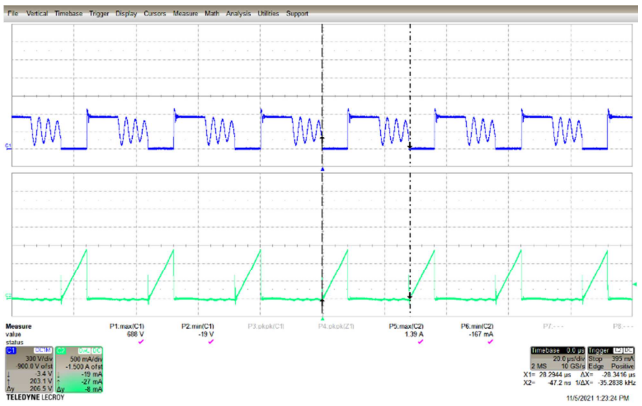


Figure 18 – Drain Voltage and Current Waveforms.
V_{IN} = 300 VDC, I_{OUT} = 2.5 A.
$V_{DS(MAX)}$ = 688 V.
$I_{DS(MAX)}$ = 1.39 A.
Upper: V_{DRAIN}, 300 V, 20 µs / div.
Lower: I_{DRAIN}, 500 mA, 20 µs / div.

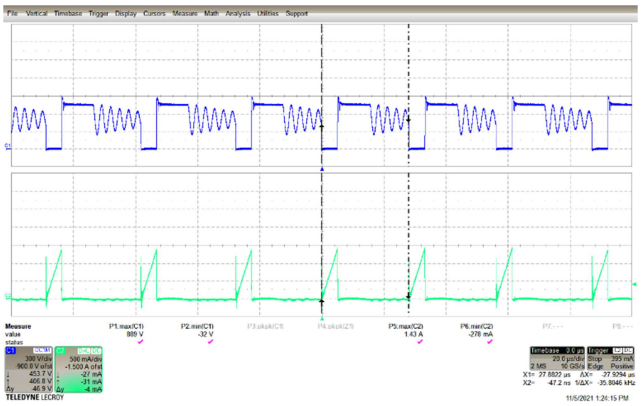


Figure 19 – Drain Voltage and Current Waveforms.
V_{IN} = 500 VDC, I_{OUT} = 2.5 A.
$V_{DS(MAX)}$ = 889 V.
$I_{DS(MAX)}$ = 1.43 A.
Upper: V_{DRAIN}, 300 V, 20 µs / div.
Lower: I_{DRAIN}, 500 mA, 20 µs / div.

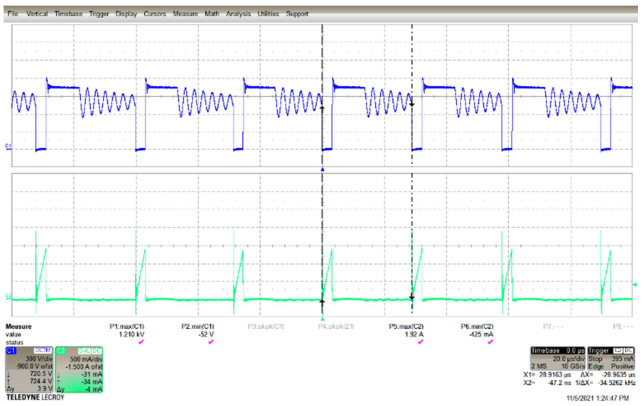


Figure 20 – Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 2.5 A.
$V_{DS(MAX)}$ = 1210 V.
$I_{DS(MAX)}$ = 1.92 A.
Upper: V_{DRAIN}, 300 V, 20 µs / div.
Lower: I_{DRAIN}, 500 mA, 20 µs / div.

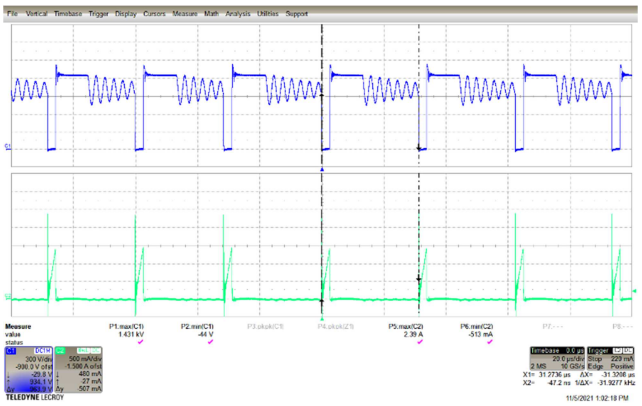


Figure 21 – Drain Voltage and Current Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 2.5 A.
$V_{DS(MAX)}$ = 1431 V.
$I_{DS(MAX)}$ = 2.39 A.
Upper: V_{DRAIN}, 300 V, 20 µs / div.
Lower: I_{DRAIN}, 500 mA, 20 µs / div.

9.2 *INN3949CQ Drain Voltage and Current, Start-up*

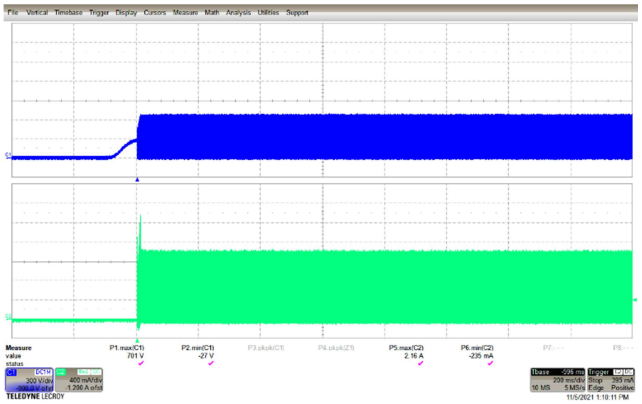


Figure 22 – Drain Voltage and Current Waveforms.
V_{IN} = 300 VDC, I_{OUT} = 2.5 A.
$V_{DS(MAX)}$ = 701 V.
$I_{DS(MAX)}$ = 2.16 A.
Upper: V_{DRAIN}, 300 V, 200 ms / div.
Lower: I_{DRAIN}, 400 mA, 200 ms / div.

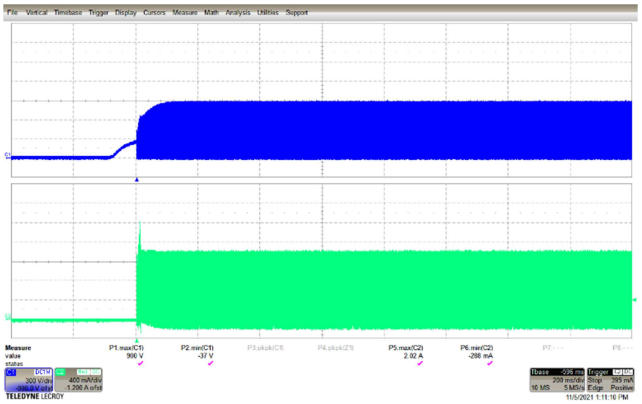


Figure 23 – Drain Voltage and Current Waveforms.
V_{IN} = 500 VDC, I_{OUT} = 2.5 A.
$V_{DS(MAX)}$ = 900 V.
$I_{DS(MAX)}$ = 2.02 A.
Upper: V_{DRAIN}, 300 V, 200 ms / div.
Lower: I_{DRAIN}, 400 mA, 200 ms / div.

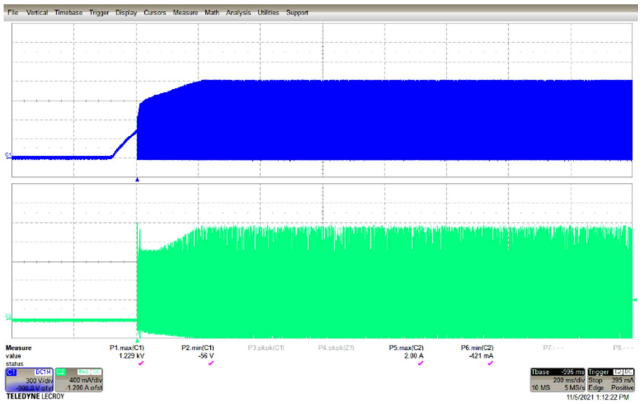


Figure 24 – Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 2.5 A.
$V_{DS(MAX)}$ = 1229 V.
$I_{DS(MAX)}$ = 2.00 A.
Upper: V_{DRAIN}, 300 V, 200 ms / div.
Lower: I_{DRAIN}, 400 mA, 200 ms / div.

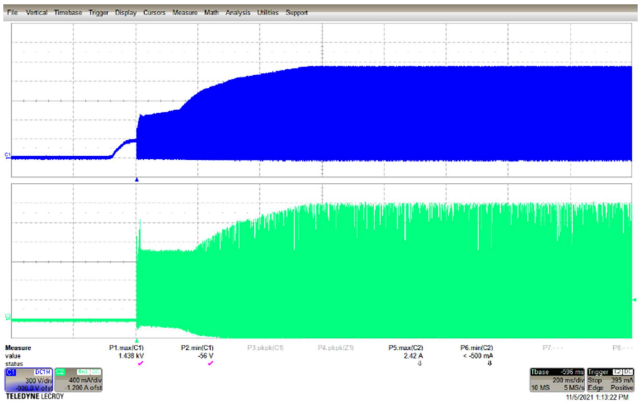


Figure 25 – Drain Voltage and Current Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 2.5 A.
$V_{DS(MAX)}$ = 1438 V.
$I_{DS(MAX)}$ = 2.42 A.
Upper: V_{DRAIN}, 300 V, 200 ms / div.
Lower: I_{DRAIN}, 400 mA, 200 ms / div.

9.3 *INN3949CQ Drain Voltage and Current, Output Shorted*

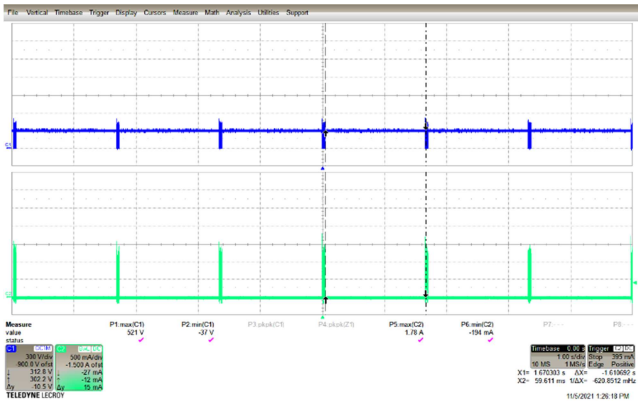


Figure 26 – Drain Voltage and Current Waveforms.
V_{IN} = 300 VDC, I_{OUT} = Output Shorted.
$V_{DS(MAX)}$ = 521 V.
$I_{DS(MAX)}$ = 1.78 A.
Upper: V_{DRAIN}, 300 V, 1 s / div.
Lower: I_{DRAIN}, 500 mA, 1 s / div.

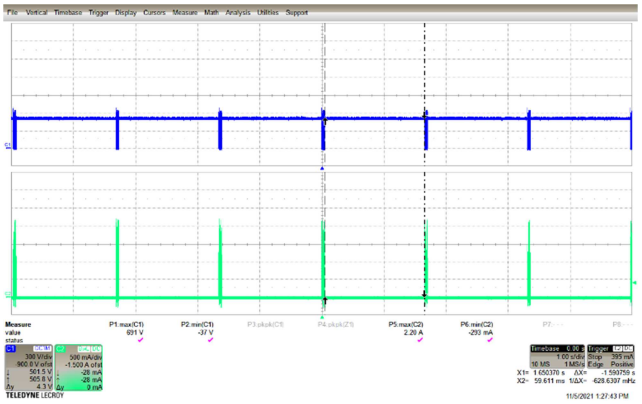


Figure 27 – Drain Voltage and Current Waveforms.
V_{IN} = 500 VDC, I_{OUT} = Output Shorted.
$V_{DS(MAX)}$ = 691 V.
$I_{DS(MAX)}$ = 2.20 A.
Upper: V_{DRAIN}, 300 V, 1 s / div.
Lower: I_{DRAIN}, 500 mA, 1 s / div.

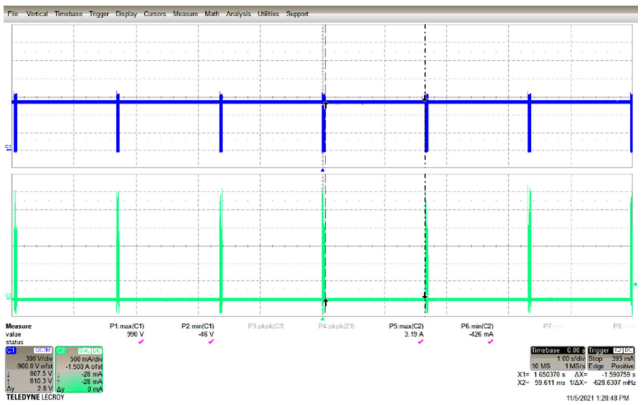


Figure 28 – Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = Output Shorted.
$V_{DS(MAX)}$ = 990 V.
$I_{DS(MAX)}$ = 3.19 A.
Upper: V_{DRAIN}, 300 V, 1 s / div.
Lower: I_{DRAIN}, 500 mA, 1 s / div.

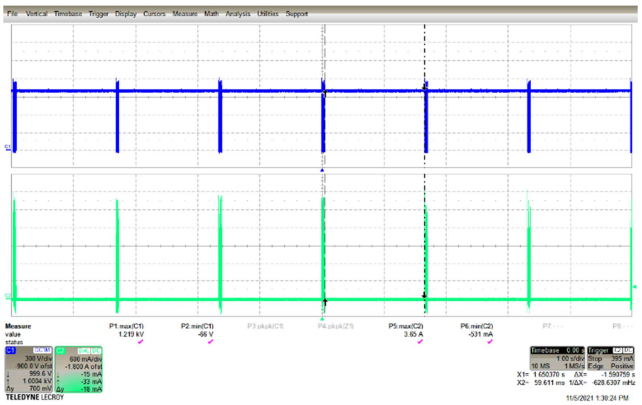


Figure 29 – Drain Voltage and Current Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = Output Shorted.
$V_{DS(MAX)}$ = 1219 V.
$I_{DS(MAX)}$ = 3.65 A.
Upper: V_{DRAIN}, 300 V, 1 s / div.
Lower: I_{DRAIN}, 500 mA, 1 s / div.

9.4 *SR FET Waveforms, Steady-State*

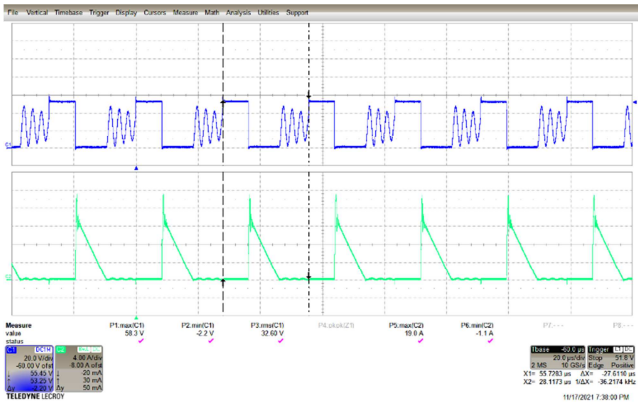


Figure 30 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 300 VDC, I_{OUT} = 2.5 A.
SRFET $V_{DS(MAX)}$ = 58.3 V.
SRFET $I_{DS(MAX)}$ = 19.0 A.
Upper: SRFET V_{DS}, 20 V, 20 µs / div.
Lower: SRFET I_{DS}, 4 A, 20 µs / div.

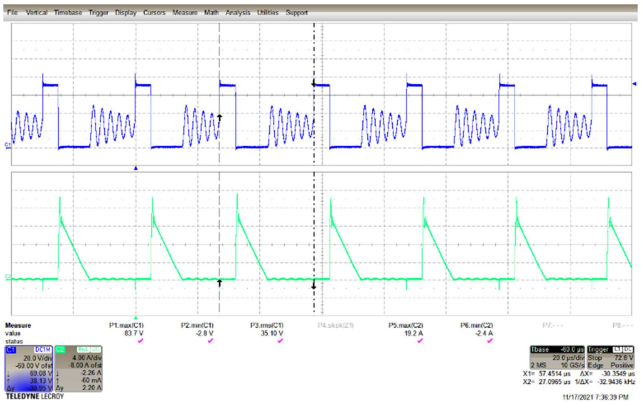


Figure 31 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 500 VDC, I_{OUT} = 2.5 A.
SRFET $V_{DS(MAX)}$ = 83.7 V.
SRFET $I_{DS(MAX)}$ = 19.2 A.
Upper: SRFET V_{DS}, 20 V, 20 µs / div.
Lower: SRFET I_{DS}, 4 A, 20 µs / div.

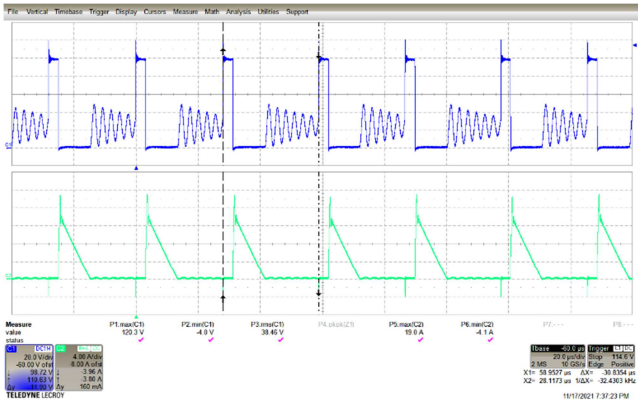


Figure 32 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 2.5 A.
SRFET $V_{DS(MAX)}$ = 120.3 V.
SRFET $I_{DS(MAX)}$ = 19.0 A.
Upper: SRFET V_{DS}, 20 V, 20 µs / div.
Lower: SRFET I_{DS}, 4 A, 20 µs / div.

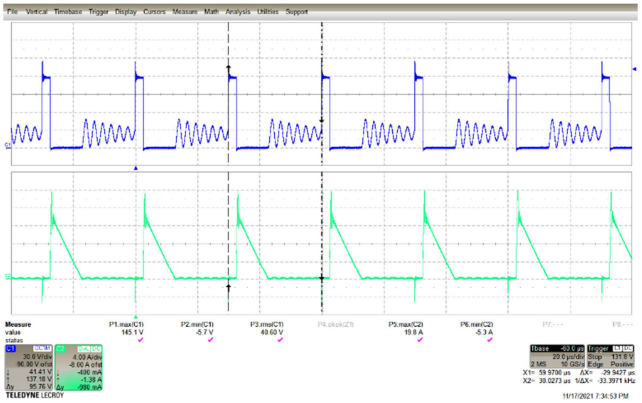


Figure 33 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 2.5 A.
SRFET $V_{DS(MAX)}$ = 145.1 V.
SRFET $I_{DS(MAX)}$ = 19.8 A.
Upper: SRFET V_{DS}, 30 V, 20 µs / div.
Lower: SRFET I_{DS}, 4 A, 20 µs / div.

9.5 *SR FET Waveforms, Start-up*

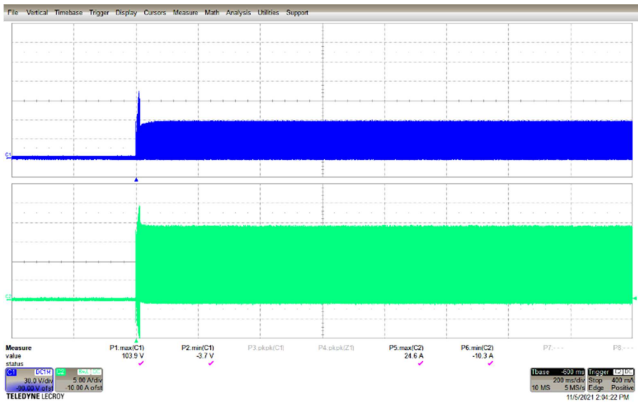


Figure 34 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 300 VDC, I_{OUT} = 2.5 A.
SRFET $V_{DS(MAX)}$ = 103.9 V.
SRFET $I_{DS(MAX)}$ = 24.6 A.
Upper: SRFET V_{DS}, 30 V, 200 ms / div.
Lower: SRFET I_{DS}, 5 A, 200 ms / div.

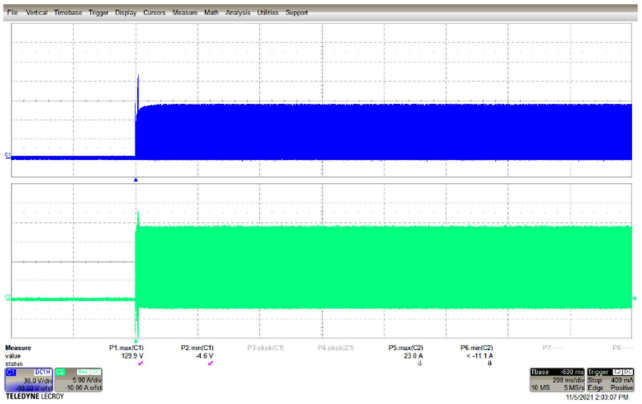


Figure 35 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 500 VDC, I_{OUT} = 2.5 A.
SRFET $V_{DS(MAX)}$ = 129.9 V.
SRFET $I_{DS(MAX)}$ = 23.0 A.
Upper: SRFET V_{DS}, 30 V, 200 ms / div.
Lower: SRFET I_{DS}, 5 A, 200 ms / div.

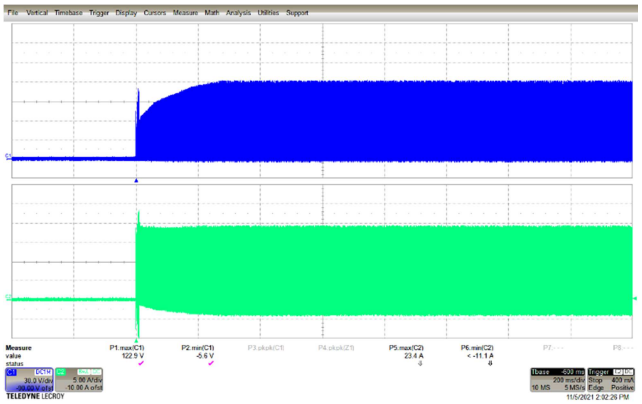


Figure 36 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 2.5 A.
SRFET $V_{DS(MAX)}$ = 122.9 V.
SRFET $I_{DS(MAX)}$ = 23.4 A.
Upper: SRFET V_{DS}, 30 V, 200 ms / div.
Lower: SRFET I_{DS}, 5 A, 200 ms / div.

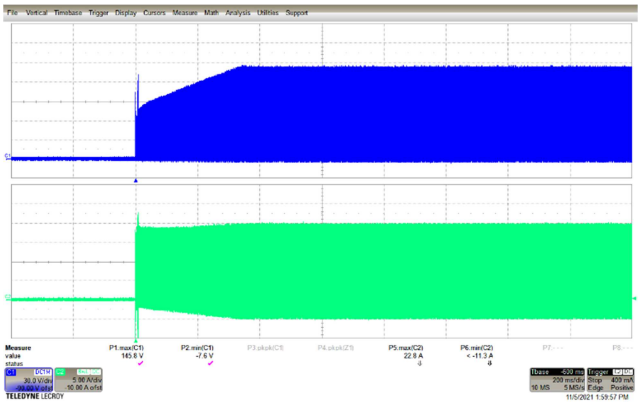


Figure 37 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 2.5 A.
SRFET $V_{DS(MAX)}$ = 145.8 V.
SRFET $I_{DS(MAX)}$ = 22.8 A.
Upper: SRFET V_{DS}, 30 V, 200 ms / div.
Lower: SRFET I_{DS}, 5 A, 200 ms / div.

9.6 *SR FET Waveforms, Output Shorted*

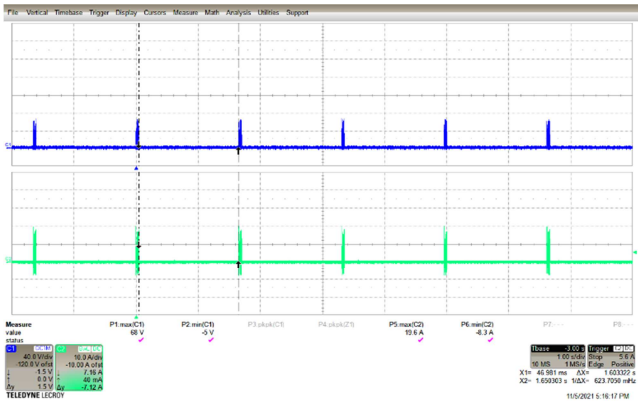


Figure 38 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 300 VDC, I_{OUT} = 2.5 A.
SRFET $V_{DS(MAX)}$ = 68 V.
SRFET $I_{DS(MAX)}$ = 19.6 A.
Upper: SRFET V_{DS}, 40 V, 1 s / div.
Lower: SRFET I_{DS}, 10 A, 1 s / div.

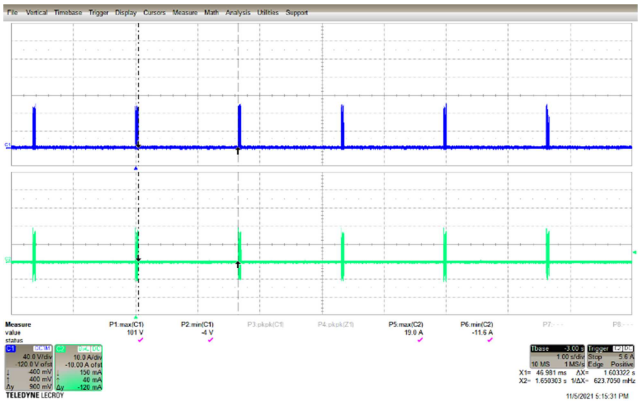


Figure 39 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 500 VDC, I_{OUT} = 2.5 A.
SRFET $V_{DS(MAX)}$ = 101 V.
SRFET $I_{DS(MAX)}$ = 19.0 A.
Upper: SRFET V_{DS}, 40 V, 1 s / div.
Lower: SRFET I_{DS}, 10 A, 1 s / div.

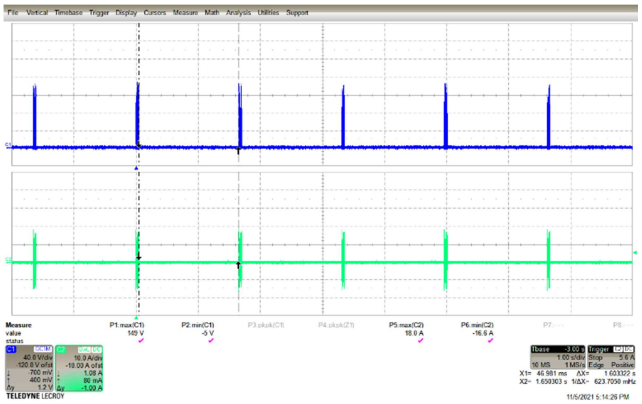


Figure 40 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 2.5 A.
SRFET $V_{DS(MAX)}$ = 149 V.
SRFET $I_{DS(MAX)}$ = 18.0 A.
Upper: SRFET V_{DS}, 40 V, 1 s / div.
Lower: SRFET I_{DS}, 10 A, 1 s / div.

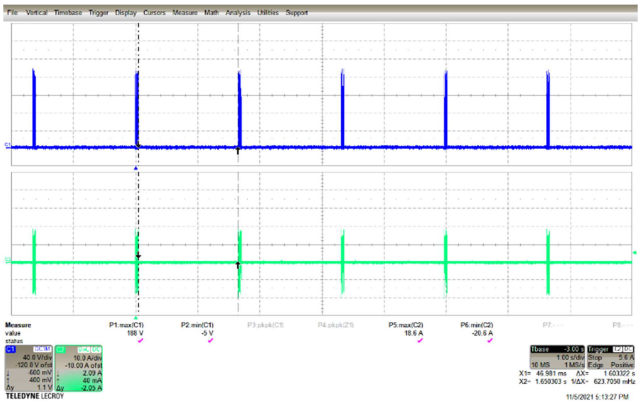


Figure 41 – SRFET Drain Voltage and Current Waveforms.
V_{IN} = 1000 VDC, I_{OUT} = 2.5 A.
SRFET $V_{DS(MAX)}$ = 188 V.
SRFET $I_{DS(MAX)}$ = 18.6 A.
Upper: SRFET V_{DS}, 40 V, 1 s / div.
Lower: SRFET I_{DS}, 10 A, 1 s / div.

9.7 *Output Ripple Measurements*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with once capacitor tied in parallel across the probe tip. The capacitor includes one (1) 1 µF/50 V ceramic type.

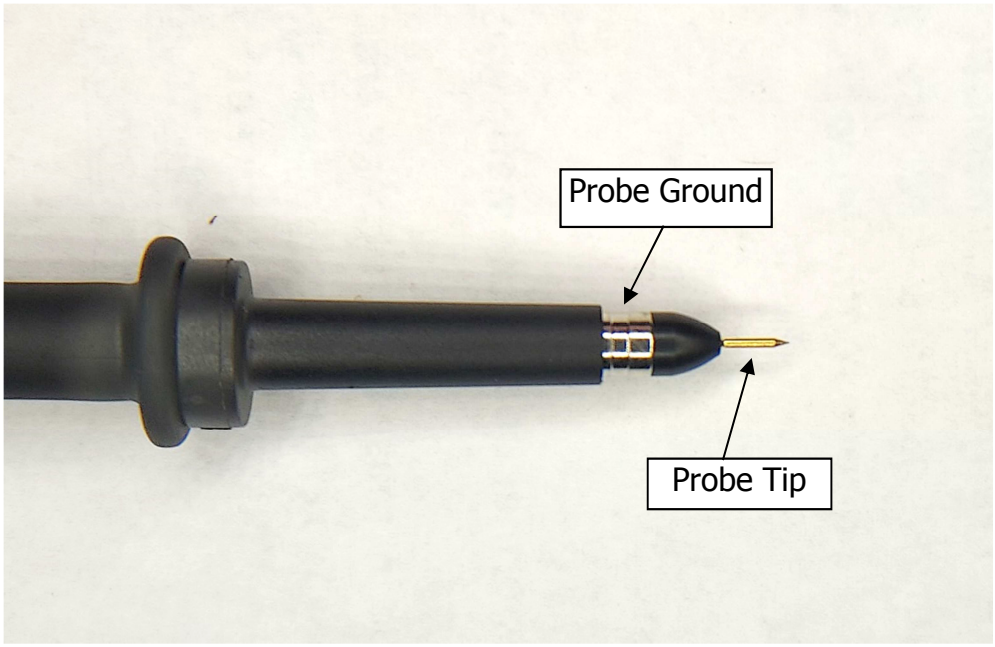


Figure 42 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)



Figure 43 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and one parallel decoupling capacitor added)

9.7.1 100% Loading Condition

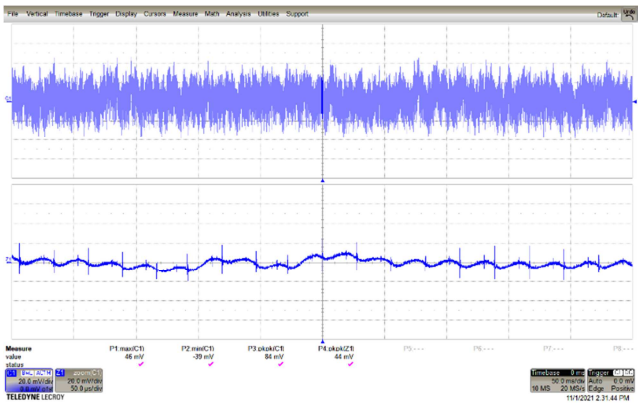


Figure 44 – Output Voltage Ripple.
V_{IN} = 300 VDC, I_{OUT} = 2.5 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 84 mV_{P-P}.

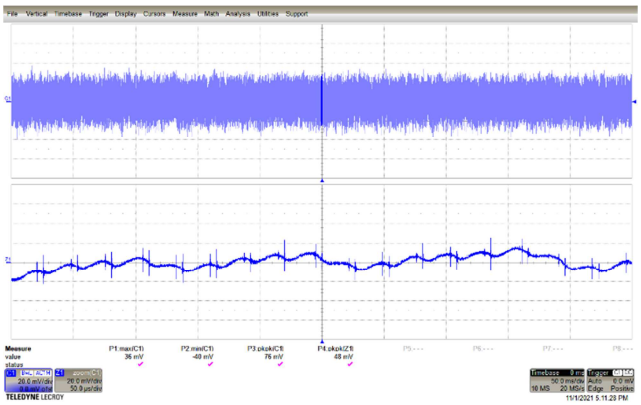


Figure 45 – Output Voltage Ripple.
V_{IN} = 500 VDC, I_{OUT} = 2.5 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 76 mV_{P-P}.

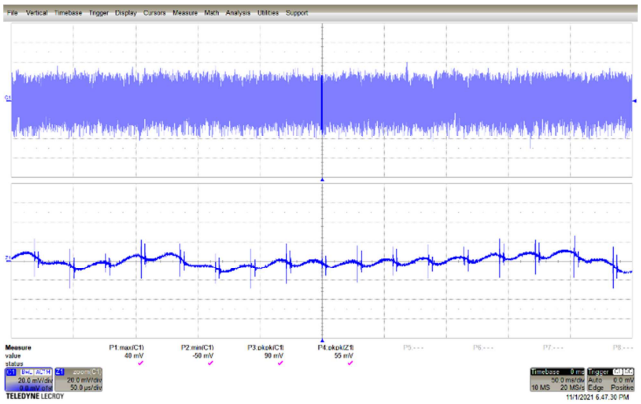


Figure 46 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 2.5 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 90 mV_{P-P}.

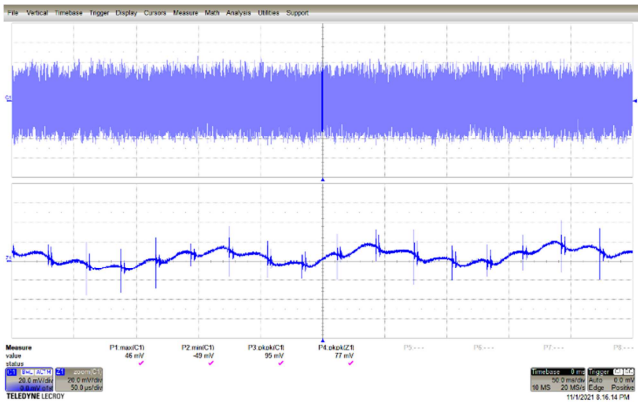


Figure 47 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 2.5 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 95 mV_{P-P}.

9.7.2 75% Loading Condition

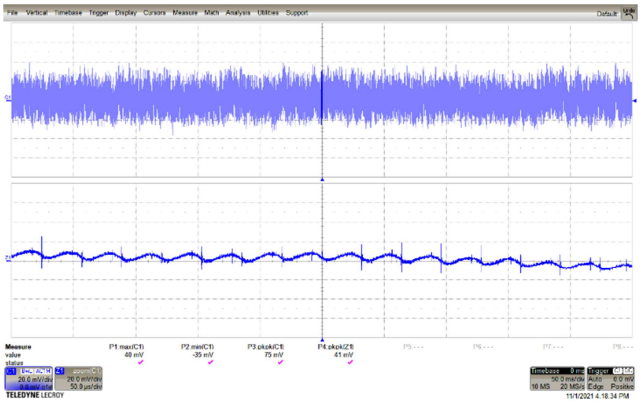


Figure 48 – Output Voltage Ripple.
V_{IN} = 300 VDC, I_{OUT} = 1.875 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} =75 mV_{P-P}.

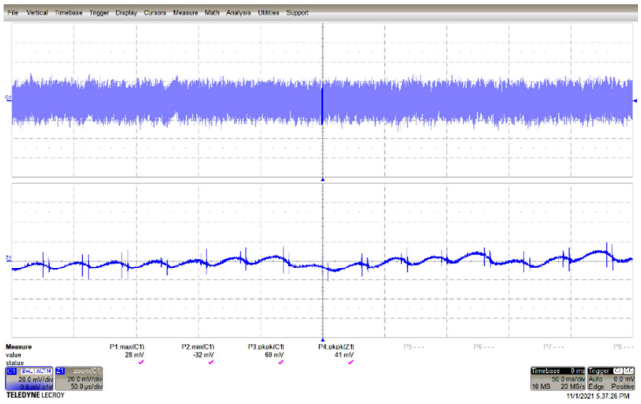


Figure 49 – Output Voltage Ripple.
V_{IN} = 500 VDC, I_{OUT} = 1.875 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 60 mV_{P-P}.

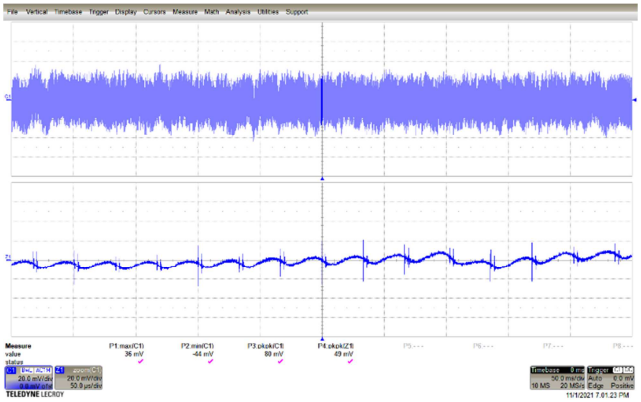


Figure 50 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 1.875 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 80 mV_{P-P}.

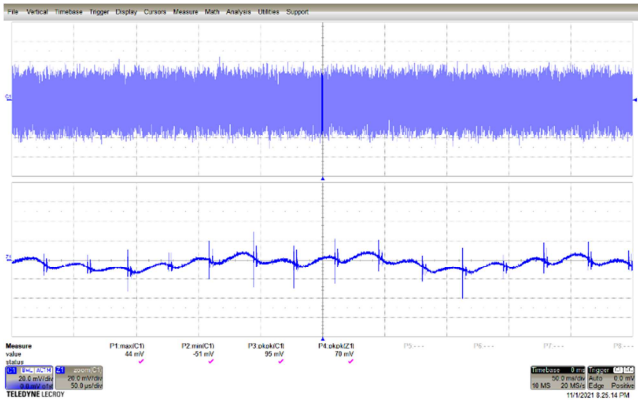


Figure 51 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 1.875 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 95 mV_{P-P}.

9.7.3 50% Loading Condition

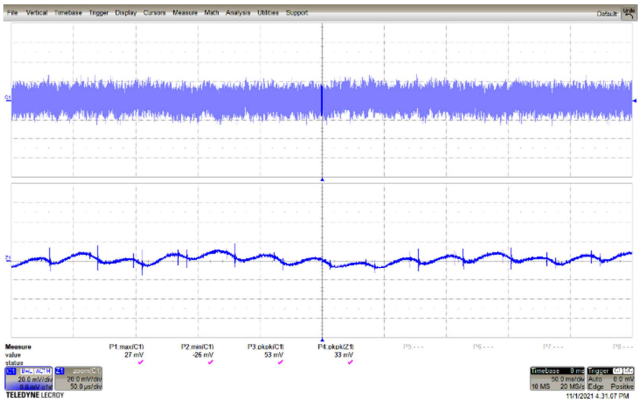


Figure 52 – Output Voltage Ripple.
V_{IN} = 300 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 53 mV_{P-P}.

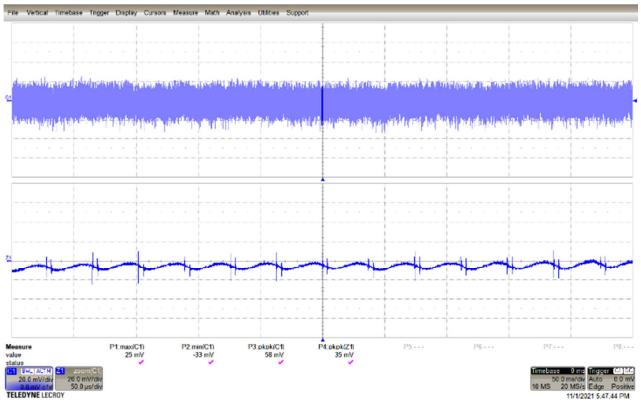


Figure 53 – Output Voltage Ripple.
V_{IN} = 500 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 58 mV_{P-P}.

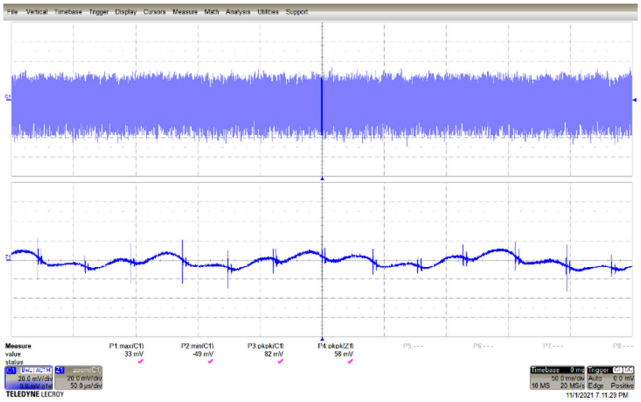


Figure 54 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 82 mV_{P-P}.

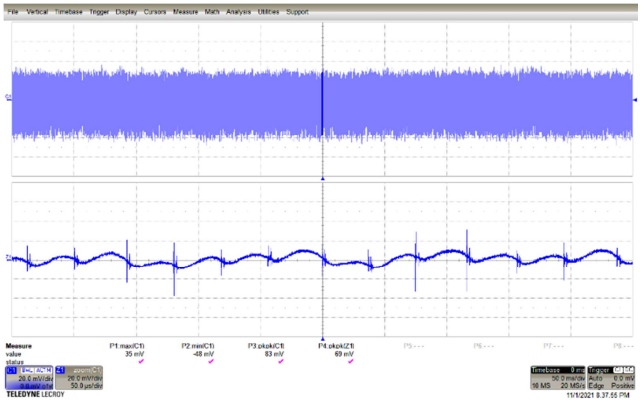


Figure 55 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 1.25 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 83 mV_{P-P}.

9.7.4 25% Loading Condition



Figure 56 – Output Voltage Ripple.
V_{IN} = 300 VDC, I_{OUT} = 0.625 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 34 mV_{P-P}.

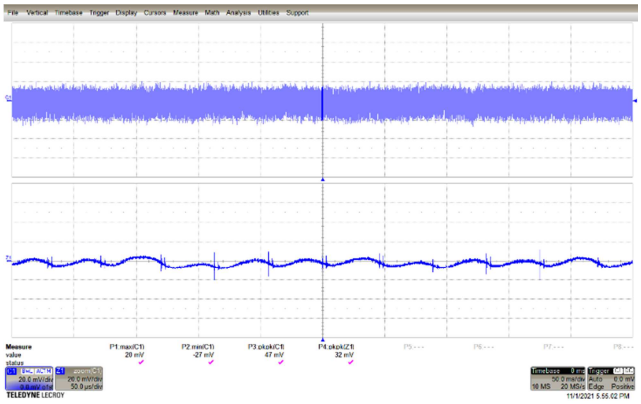


Figure 57 – Output Voltage Ripple.
V_{IN} = 500 VDC, I_{OUT} = 0.625 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 47 mV_{P-P}.

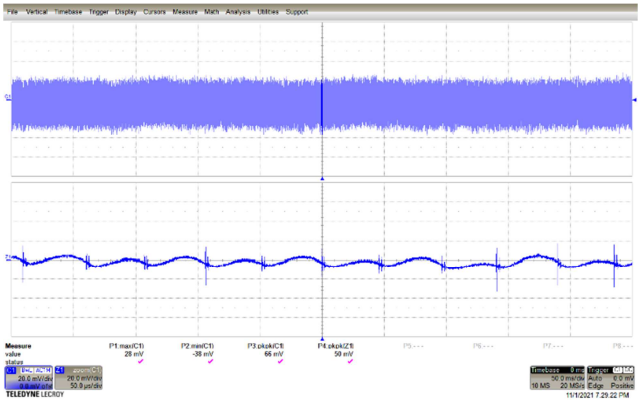


Figure 58 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 0.625 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 66 mV_{P-P}.

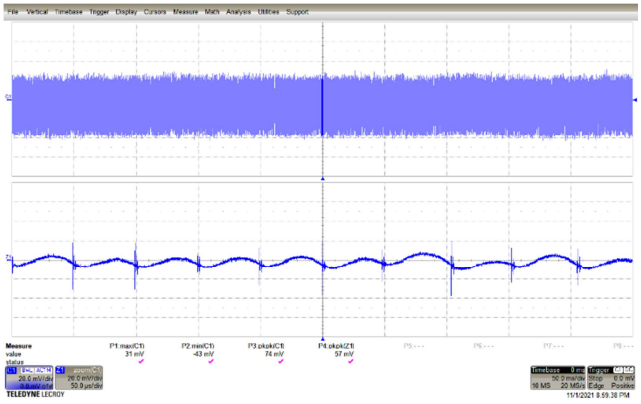


Figure 59 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 0.625 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 74 mV_{P-P}.

9.7.5 0% Loading Condition

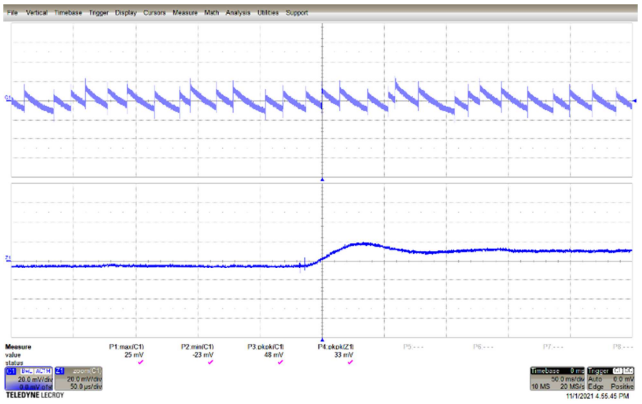


Figure 60 – Output Voltage Ripple.
V_{IN} = 300 VDC, I_{OUT} = 0 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 48 mV_{P-P}.

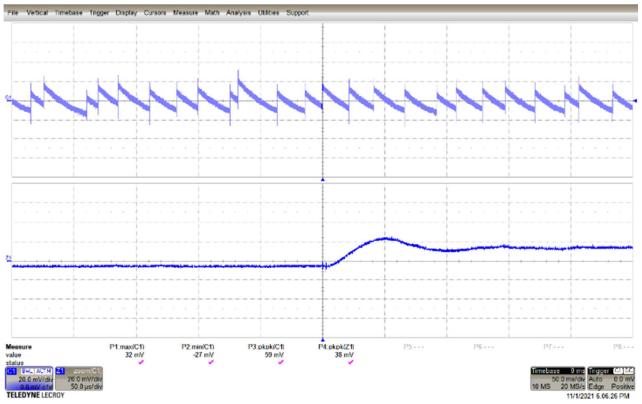


Figure 61 – Output Voltage Ripple.
V_{IN} = 500 VDC, I_{OUT} = 0 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 59 mV_{P-P}.

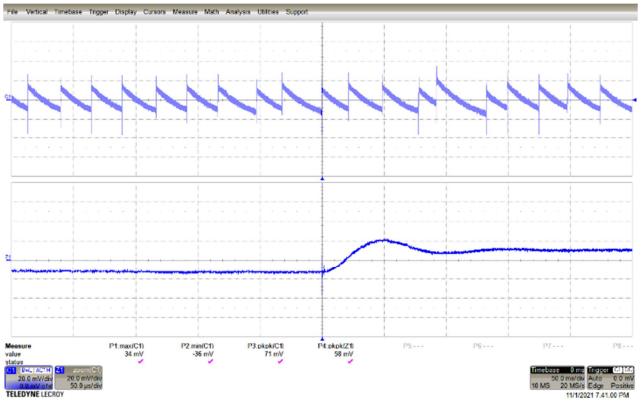


Figure 62 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 0 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 71 mV_{P-P}.

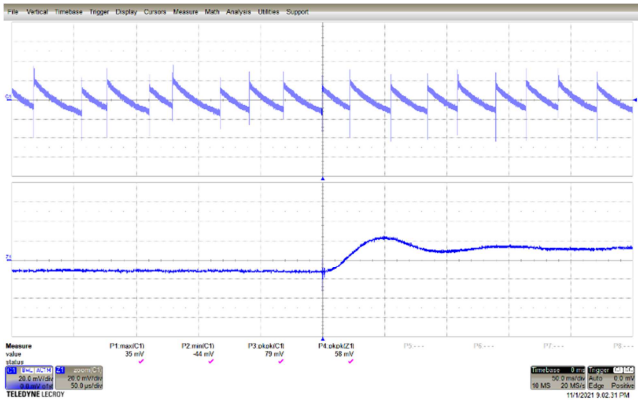


Figure 63 – Output Voltage Ripple.
V_{IN} = 1000 VDC, I_{OUT} = 0 A.
Upper: V_{OUT}, 20 mV, 50 ms / div.
Lower: Zoom @ 50 µs / div.
V_{RIPPLE} = 79 mV_{P-P}.

9.8 *Output Voltage Ripple (ATE)*

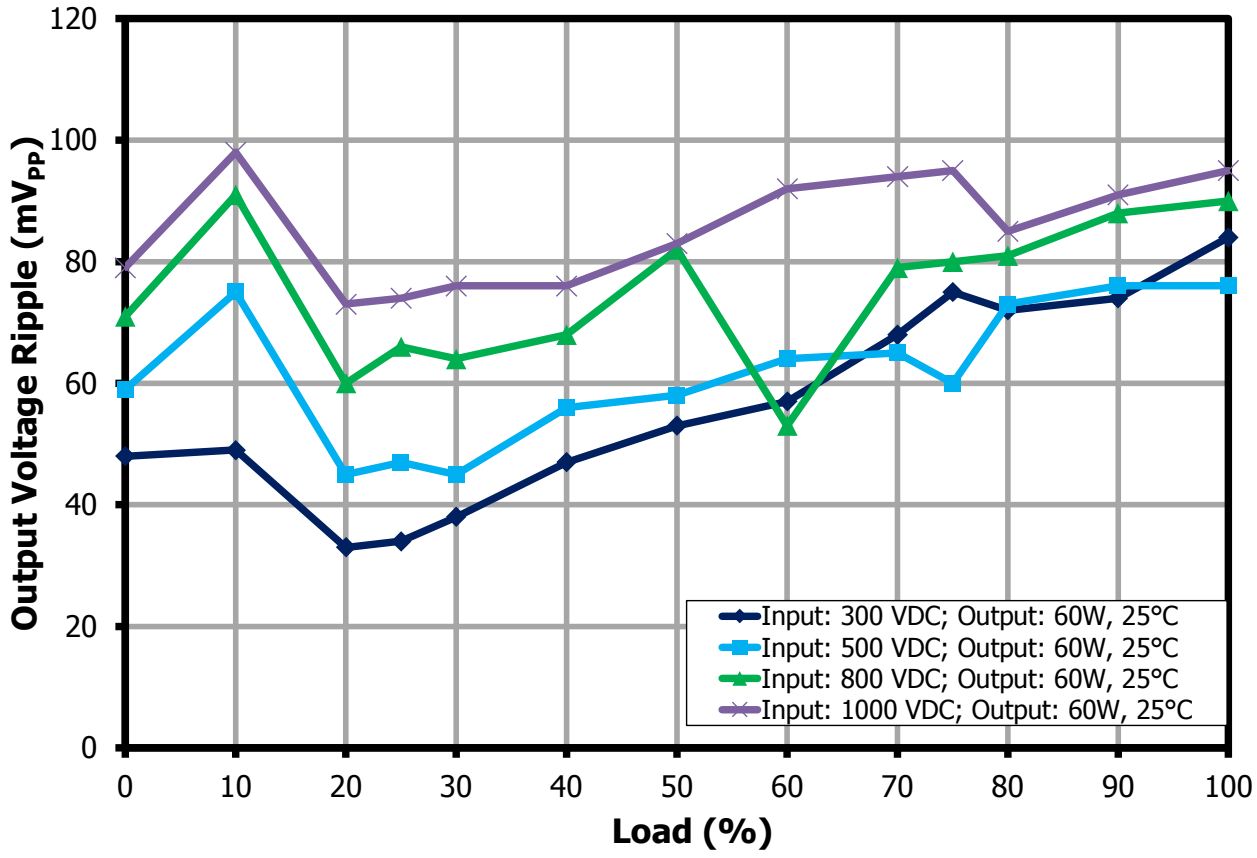


Figure 64 – Output Voltage Ripple, 25 °C Ambient Temperature.

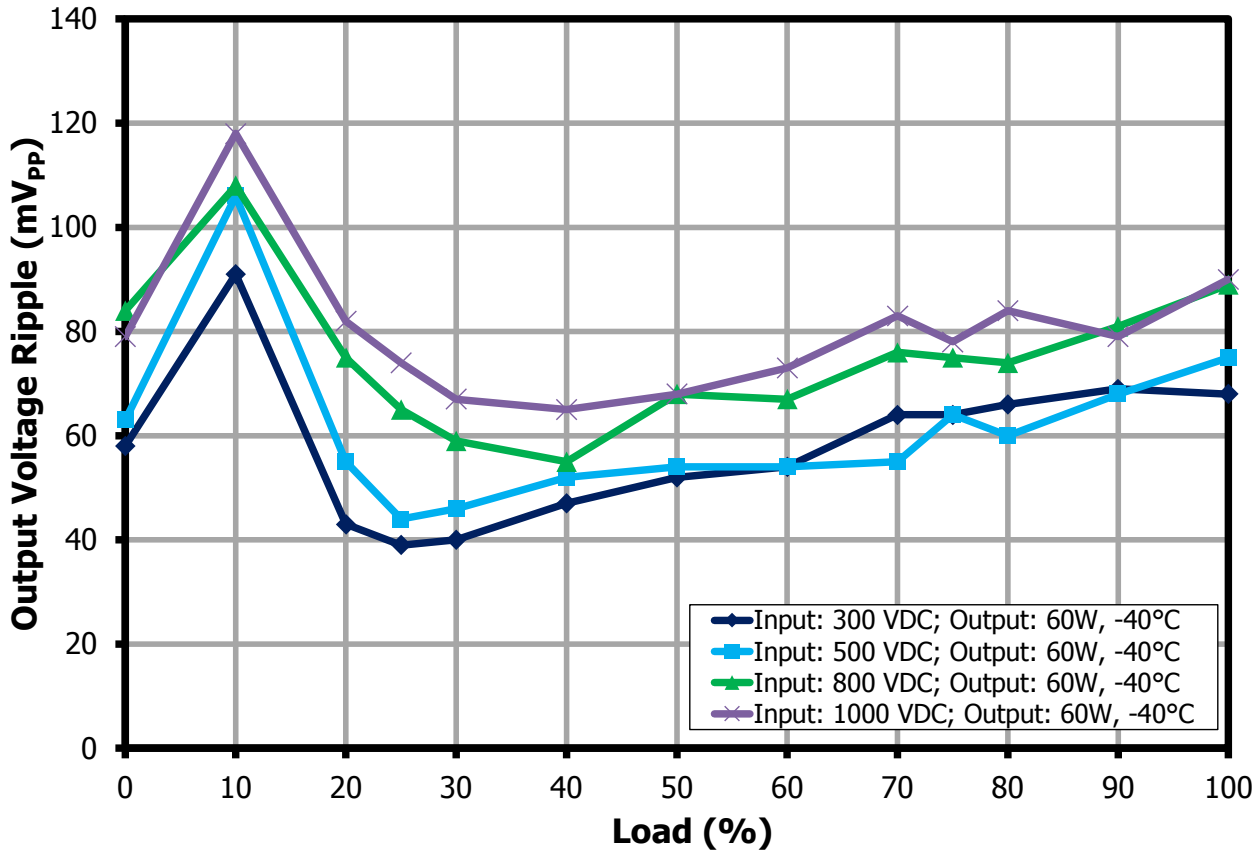


Figure 65 – Output Voltage Ripple, -40 °C Ambient Temperature.

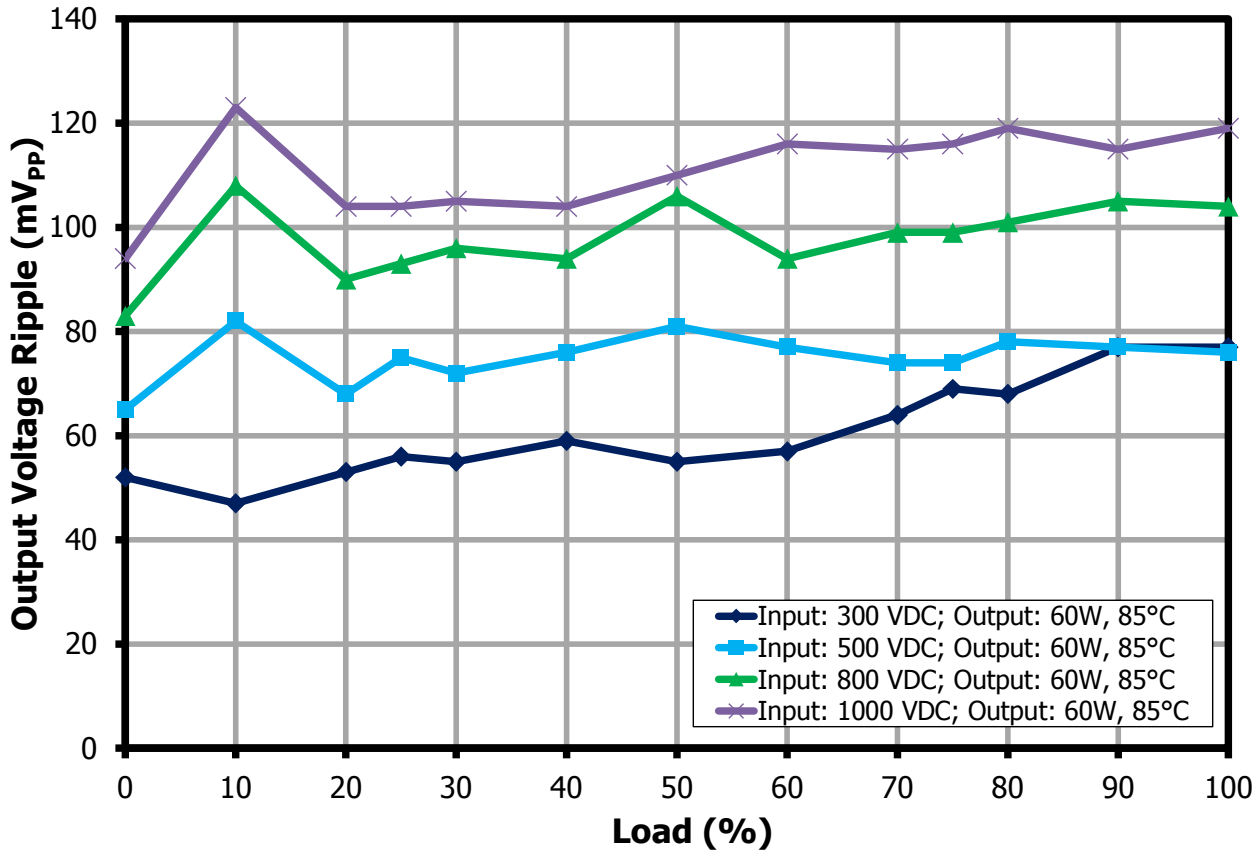


Figure 66 – Output Voltage Ripple, 85 °C Ambient Temperature.

9.9 *Output Load Transient*

9.9.1 Output Load Transient, 100% to 50% Load

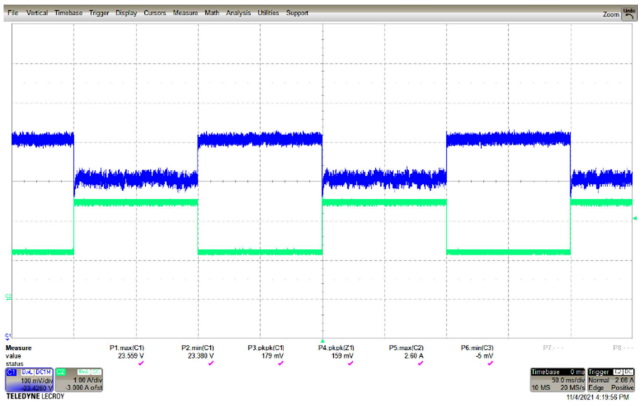


Figure 67 – Output Load Transient, 100-50% Load.
V_{IN} = 300 VDC, I_{OUT} = 2.5 A to 1.25 A.
$V_{OUT(MAX)}$ = 23.56 V, $V_{OUT(MIN)}$ = 23.38 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

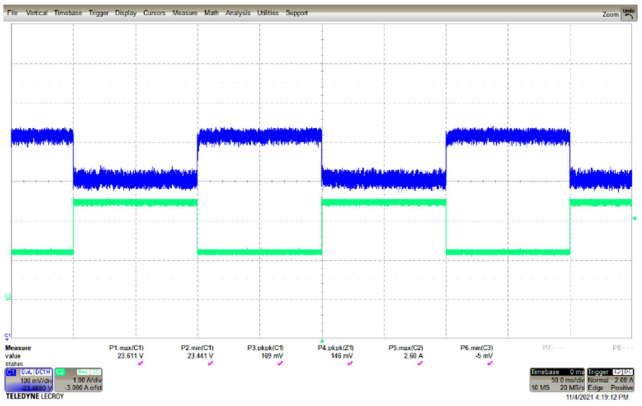


Figure 68 – Output Load Transient, 100-50% Load.
V_{IN} = 500 VDC, I_{OUT} = 2.5 A to 1.25 A.
$V_{OUT(MAX)}$ = 23.61 V, $V_{OUT(MIN)}$ = 23.44 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

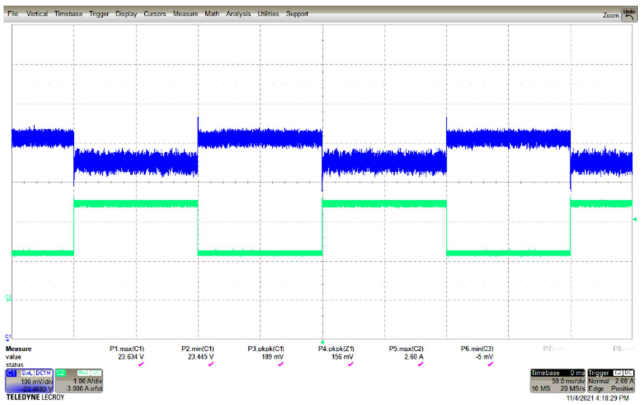


Figure 69 – Output Load Transient, 100-50% Load.
V_{IN} = 800 VDC, I_{OUT} = 2.5 A to 1.25 A.
$V_{OUT(MAX)}$ = 23.63 V, $V_{OUT(MIN)}$ = 23.45 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

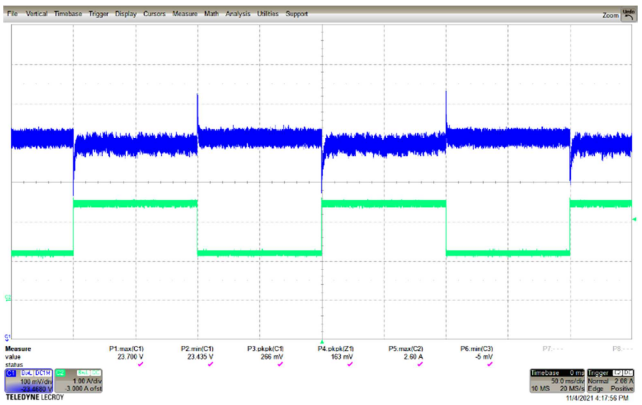


Figure 70 – Output Load Transient, 100-50% Load.
V_{IN} = 1000 VDC, I_{OUT} = 2.5 A to 1.25 A.
$V_{OUT(MAX)}$ = 23.70 V, $V_{OUT(MIN)}$ = 23.44 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

9.9.2 Output Load Transient, 100% to 0% Load

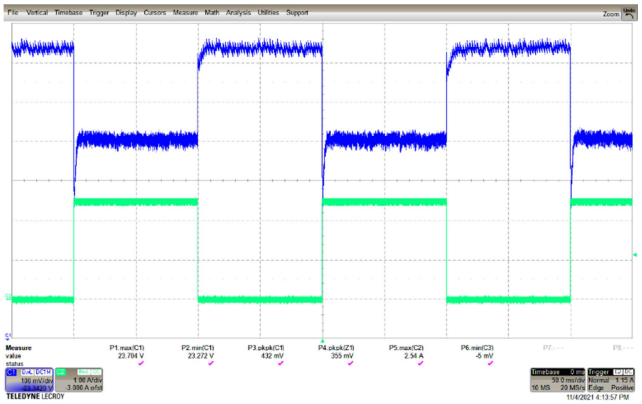


Figure 71 – Output Load Transient, 100-0% Load.
V_{IN} = 300 VDC, I_{OUT} = 2.5 A to 0 A.
$V_{OUT(MAX)}$ = 23.70 V, $V_{OUT(MIN)}$ = 23.27 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

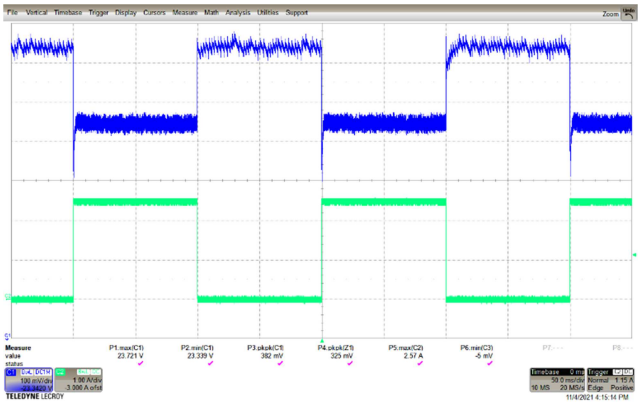


Figure 72 – Output Load Transient, 100-0% Load.
V_{IN} = 500 VDC, I_{OUT} = 2.5 A to 0 A.
$V_{OUT(MAX)}$ = 23.72 V, $V_{OUT(MIN)}$ = 23.34 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

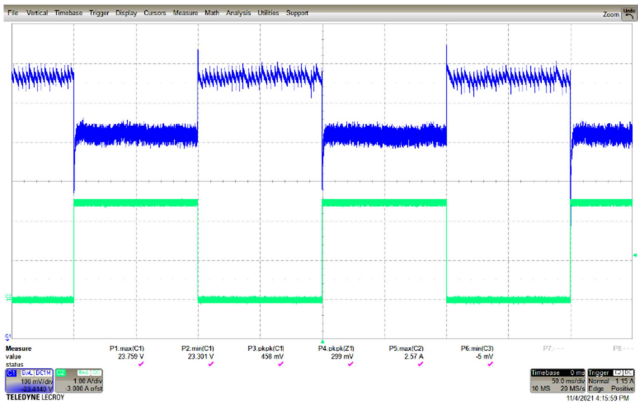


Figure 73 – Output Load Transient, 100-0% Load.
V_{IN} = 800 VDC, I_{OUT} = 2.5 A to 0 A.
$V_{OUT(MAX)}$ = 23.76 V, $V_{OUT(MIN)}$ = 23.0 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

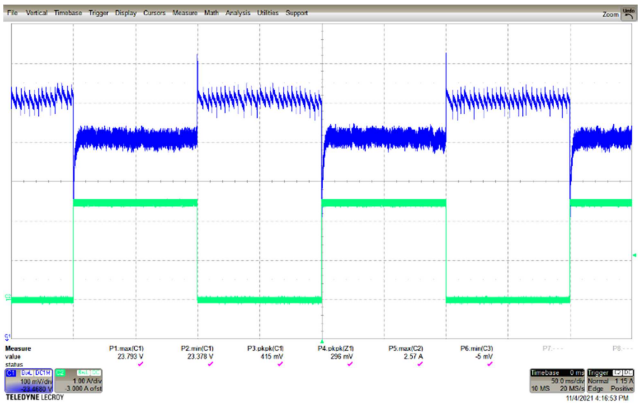


Figure 74 – Output Load Transient, 100-0% Load.
V_{IN} = 1000 VDC, I_{OUT} = 2.5 A to 0 A.
$V_{OUT(MAX)}$ = 23.79 V, $V_{OUT(MIN)}$ = 23.38 V.
Upper: V_{OUT}, 100 mV, 50 ms / div.
Lower: $I_{OUT,}$ 1 A, 50 ms / div.

9.10 *FWD Waveforms, Steady-State*

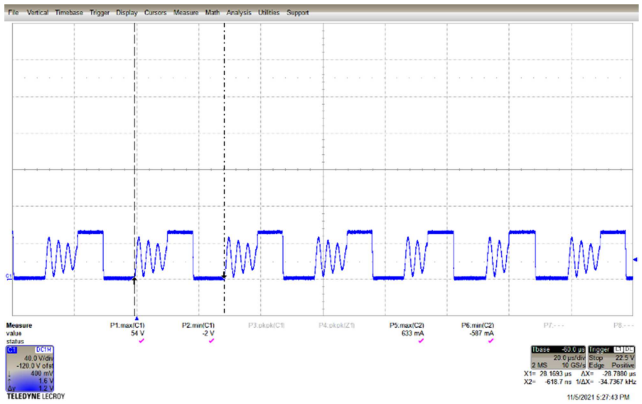


Figure 75 – FWD Voltage During Steady State.
V_{IN} = 300 VDC $V_{FWD(MAX)}$ = 54 V.
CH1: V_{FWD}, 40 V, 20 µs / div.

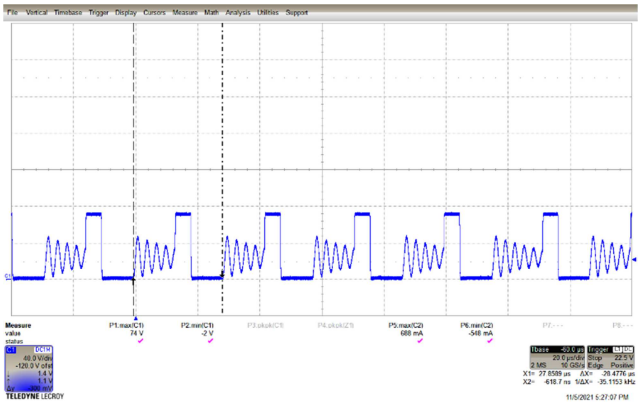


Figure 76 – FWD Voltage During Steady State.
V_{IN} = 500 VDC $V_{FWD(MAX)}$ = 74 V.
CH1: V_{FWD}, 40 V, 20 µs / div.

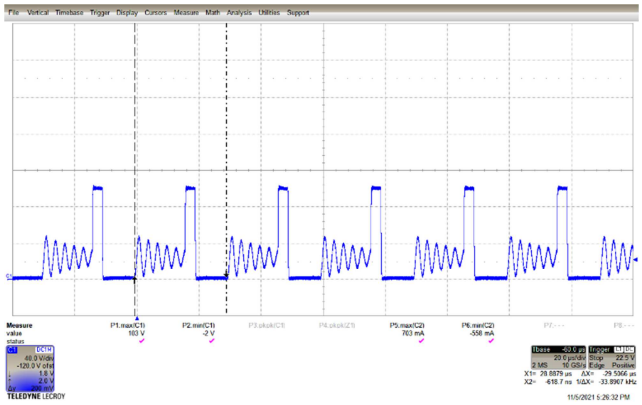


Figure 77 – FWD Voltage During Steady State.
V_{IN} = 800 VDC $V_{FWD(MAX)}$ = 103 V.
CH1: V_{FWD}, 40 V, 20 µs / div.

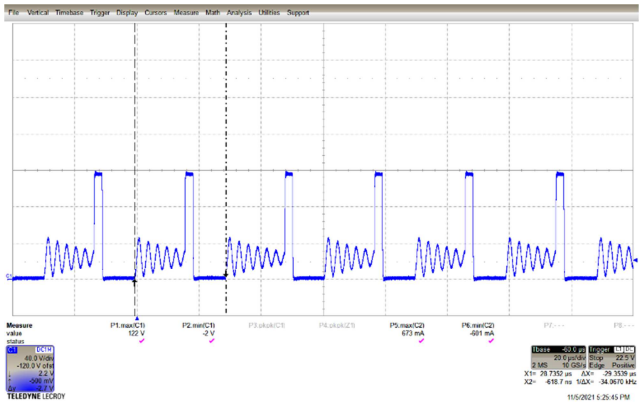


Figure 78 – FWD Voltage During Steady State.
V_{IN} = 1000 VDC $V_{FWD(MAX)}$ = 122 V.
CH1: V_{FWD}, 30 V, 20 µs / div.

9.11 *FWD Waveforms, Start-up*

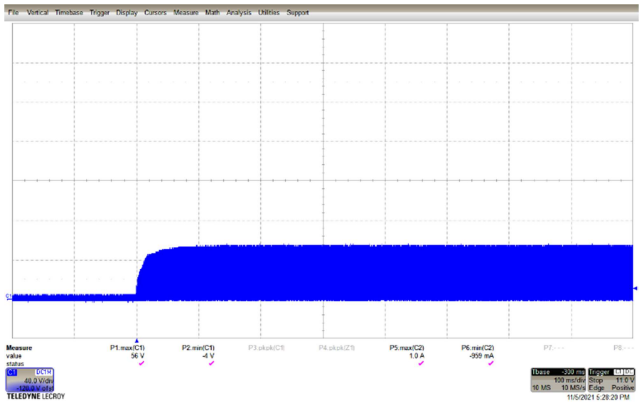


Figure 79 – FWD Voltage During Startup.
V_{IN} = 300 VDC $V_{FWD(MAX)}$ = 56 V.
CH1: V_{FWD}, 40 V, 100 ms / div.

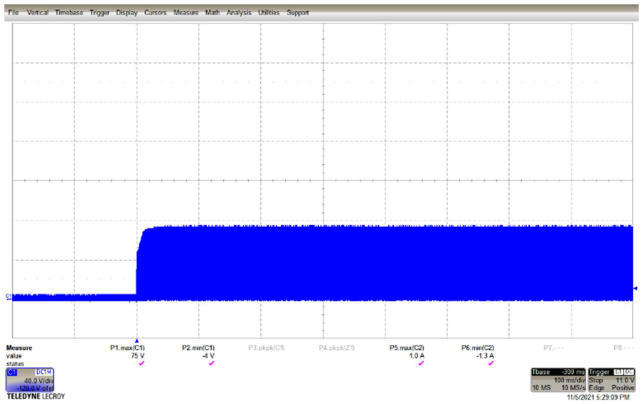


Figure 80 – FWD Voltage During Startup.
V_{IN} = 500 VDC $V_{FWD(MAX)}$ = 75 V.
CH1: V_{FWD}, 40 V, 100 ms / div.

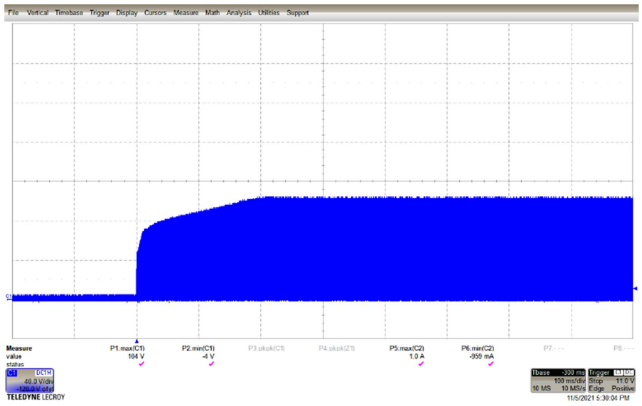


Figure 81 – FWD Voltage During Startup.
V_{IN} = 800 VDC $V_{FWD(MAX)}$ = 104 V.
CH1: V_{FWD}, 40 V, 100 ms / div.

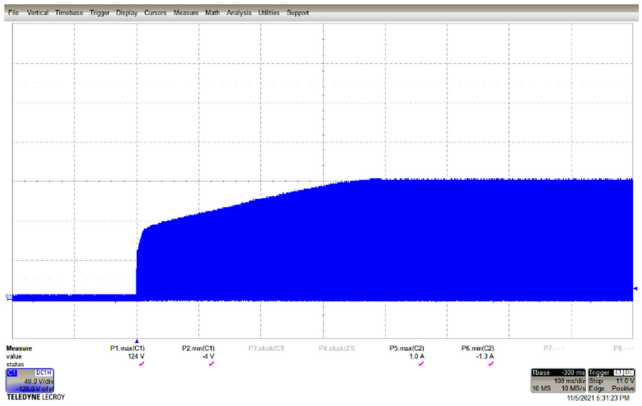


Figure 82 – FWD Voltage During Startup.
V_{IN} = 1000 VDC $V_{FWD(MAX)}$ = 124 V.
CH1: V_{FWD}, 40 V, 100 ms / div.

9.12 *FWD Waveforms, Output Shorted*

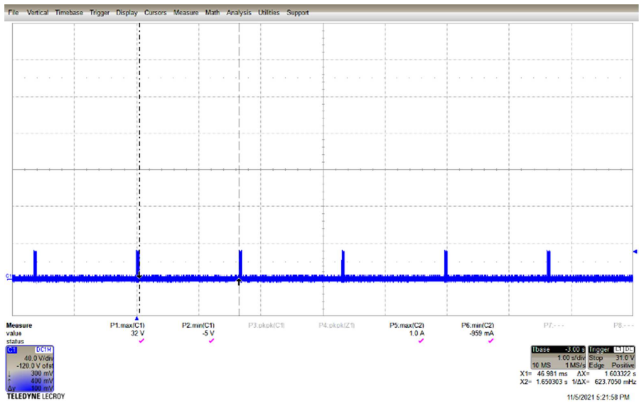


Figure 83 – FWD Voltage During Output Short.
V_{IN} = 300 VDC $V_{FWD(MAX)}$ = 32 V.
CH1: V_{FWD}, 40 V, 1 s / div.

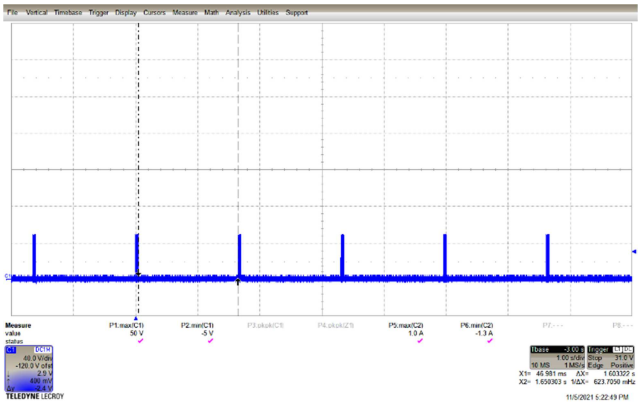


Figure 84 – FWD Voltage During Output Short.
V_{IN} = 500 VDC $V_{FWD(MAX)}$ = 50 V.
CH1: V_{FWD}, 40 V, 1 s / div.

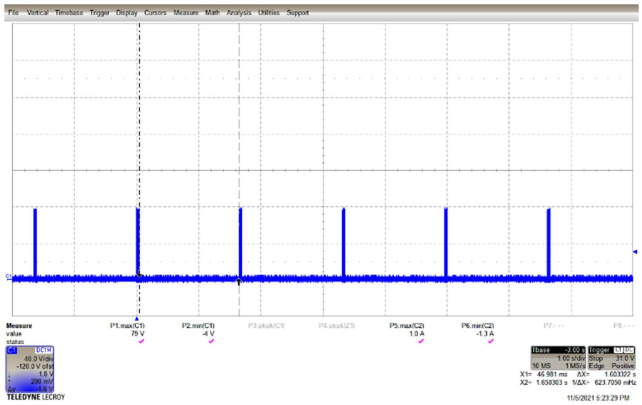


Figure 85 – FWD Voltage During Output Short.
V_{IN} = 800 VDC $V_{FWD(MAX)}$ = 79 V.
CH1: V_{FWD}, 40 V, 1 s / div.

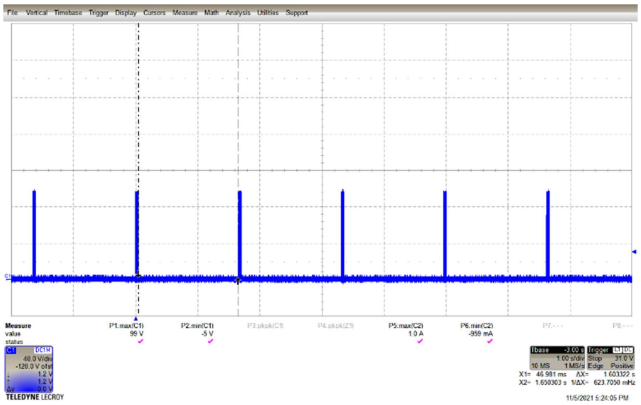


Figure 86 – FWD Voltage During Output Short
V_{IN} = 1000 VDC $V_{FWD(MAX)}$ = 99 V.
CH1: V_{FWD}, 40 V, 1 s / div.

10 Thermal Performance

All measurements have been done at room ambient temperature after 1 hour of continuous operation.

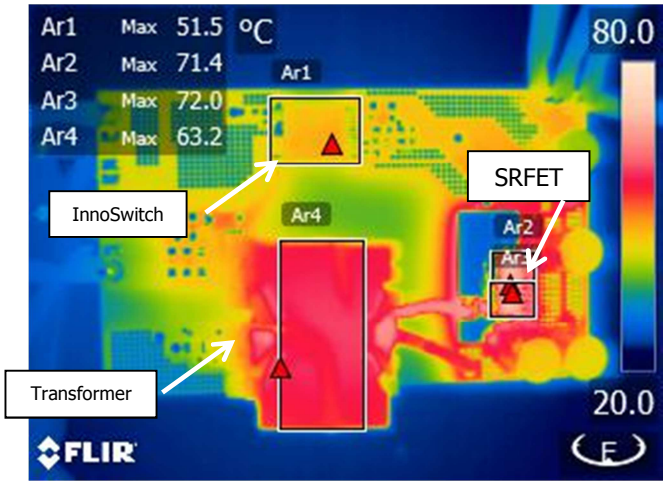


Figure 87 – 300 VDC 2.5 A Full Load.
Temperature of INN3949CQ: 51.5 ºC.
Temperature of SR FET1 (Q2): 71.4 ºC.
Temperature of SR FET2 (Q3): 72.0 ºC.
Temperature of Transformer: 63.2 ºC.
Ambient Temperature: 24.9 ºC.

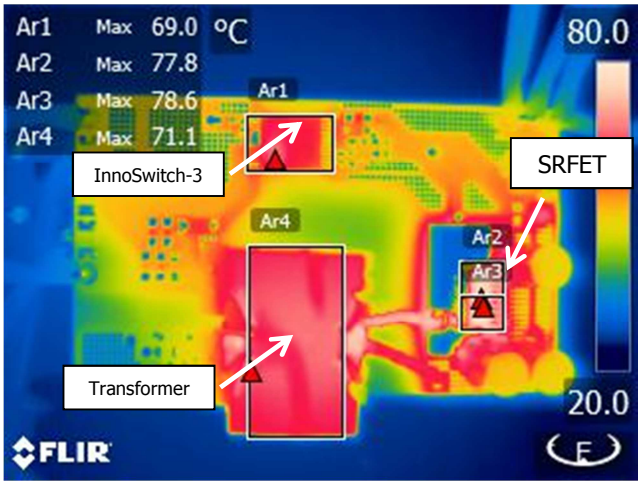


Figure 88 – 800 VDC 2.5 A Full Load.
Temperature of INN3949CQ: 69.0 ºC.
Temperature of SR FET1 (Q2): 77.8 ºC.
Temperature of SR FET2 (Q3): 78.6 ºC.
Temperature of Transformer: 71.1 ºC.
Ambient Temperature: 25.7 ºC.

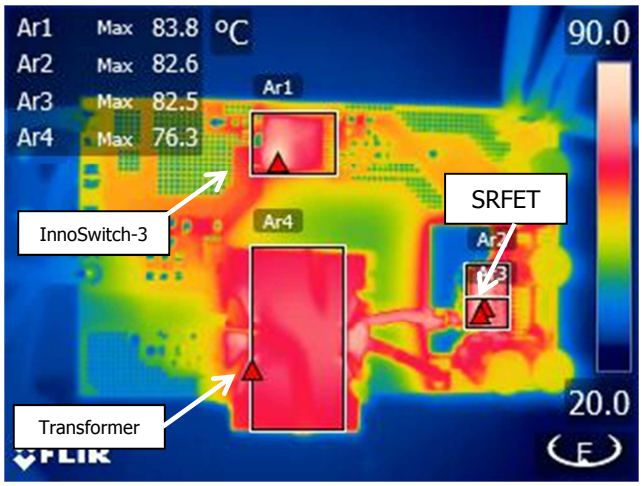


Figure 89 – 1000 VDC 2.5 A Full Load.
Temperature of INN3947CQ: 83.8 ºC.
Temperature of SR FET1 (Q2): 82.6 ºC.
Temperature of SR FET2 (Q3): 82.5 ºC.
Temperature of Transformer: 76.3 ºC.
Ambient Temperature: 26.4 ºC.

10.1 *Temperature vs. Output Power*

Data below is taken with no additional thermal mitigation.

Available output power at elevated ambient can be increased by providing a thermal path from the PCB area connected to the SOURCE pin of the InnoSwitch3-AQ to a surface that is lower in temperature. This is typically the outer wall of the inverter or internally above the water channel cooling the power modules. A very simple approach is a compliant thermal pad (e.g. TGP 1500 from Berquist) placed between the PCB and bottom or top surface of the enclosure.

In the design of the cast enclosure features may be added at no cost to provide a location to place the pad for manufacturing simplicity and reduce the thickness of pad needed to reduce cost of pad needed.

300 VDC								
P_{IN} (W)	**V_{OUT} (V)**	**I_{OUT} (A)**	**P_{OUT} (W)**	**Efficiency (%)**	**INN3949CQ (ºC)**	**AMB (ºC)**	**INN3949CQ Trise (ºC)**	**Projected Max AMB Operating Temp (125 ºC - Trise)**
10.90	23.68	0.42	9.91	90.9	35.8	24.2	11.6	113.4
21.42	23.67	0.84	19.84	92.6	39.7	24.5	15.2	109.8
31.94	23.68	1.26	29.79	93.3	42.5	24.7	17.8	107.2
42.08	23.65	1.66	39.32	93.5	45.2	25.0	20.2	104.8
52.56	23.58	2.08	49.08	93.4	46.6	25.1	21.5	103.5
63.26	23.59	2.5	59.04	93.3	51.5	26.4	25.1	99.9

300 VDC								
P_{IN} (W)	**V_{OUT} (V)**	**I_{OUT} (A)**	**P_{OUT} (W)**	**Efficiency (%)**	**INN3949CQ (ºC)**	**AMB (ºC)**	**INN3949CQ Trise (ºC)**	**Projected Max AMB Operating Temp (125 ºC - Trise)**
11.03	23.69	0.42	9.91	89.8	38.0	24.5	13.5	111.5
21.57	23.69	0.84	19.85	92.0	41.6	25.1	16.5	108.5
32.14	23.72	1.26	29.84	92.8	44.5	25.1	19.4	105.6
42.30	23.68	1.66	39.39	93.1	45.0	24.3	20.7	104.3
52.81	23.63	2.08	49.17	93.1	49.2	24.4	24.8	100.2
63.47	23.62	2.50	59.11	93.1	50.8	24.5	26.3	98.7

500 VDC								
P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	INN3949CQ (ºC)	AMB (ºC)	INN3949CQ Trise (ºC)	Projected Max AMB Operating Temp (125ºC - Trise)
11.19	23.70	0.42	9.91	88.6	38.8	24.2	14.6	110.4
21.77	23.70	0.84	19.86	91.2	41.5	24	17.5	107.5
32.44	23.73	1.26	29.85	92.0	46.4	24.5	21.9	103.1
42.54	23.70	1.66	39.41	92.6	49.2	25.5	23.7	101.3
53.18	23.69	2.08	49.31	92.7	52.0	25.7	26.3	98.7
63.83	23.68	2.50	59.27	92.9	54.4	24.5	29.9	95.1

600 VDC								
P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	INN3949CQ (ºC)	AMB (ºC)	INN3949CQ Trise (ºC)	Projected Max AMB Operating Temp (125 ºC - Trise)
11.38	23.71	0.42	9.92	87.2	41.4	23.8	17.6	107.4
22.02	23.71	0.84	19.87	90.2	47.1	24.0	23.1	101.9
32.70	23.75	1.26	29.88	91.4	51.2	24.0	27.2	97.8
43.22	23.73	1.66	39.46	91.3	52.1	23.8	28.3	96.7
53.45	23.69	2.08	49.30	92.2	54.6	24.3	30.3	94.7
64.15	23.68	2.50	59.27	92.4	56.0	24.2	31.8	93.2

700 VDC								
P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	INN3949CQ (ºC)	AMB (ºC)	INN3949CQ Trise (ºC)	Projected Max AMB Operating Temp (125 ºC - Trise)
11.56	23.72	0.42	9.92	85.8	42.8	23.3	19.5	105.5
22.31	23.72	0.84	19.88	89.1	49.1	23.3	25.8	99.2
32.97	23.75	1.26	29.88	90.6	52.9	23.3	29.6	95.4
43.59	23.74	1.66	39.48	90.6	58.4	25.8	32.6	92.4
53.93	23.76	2.08	49.44	91.7	60.7	25.9	34.8	90.2
64.56	23.69	2.50	59.31	91.9	63.1	25.6	37.5	87.5

800 VDC								
P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	INN3949CQ (ºC)	AMB (ºC)	INN3949CQ Trise (ºC)	Projected Max AMB Operating Temp (125 ºC - Trise)
11.75	23.74	0.42	9.93	84.5	46.9	24.9	22	103
22.63	23.74	0.84	19.90	87.9	56.3	25.2	31.1	93.9
33.37	23.77	1.26	29.91	89.6	61.7	25.7	36	89
44.01	23.77	1.66	39.54	89.8	63.2	25.8	37.4	87.6
54.43	23.76	2.08	49.45	90.8	65.6	25.8	39.8	85.2
65.31	23.78	2.50	59.52	91.1	69.0	25.7	43.3	81.7

900 VDC								
P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	INN3949CQ (ºC)	AMB (ºC)	INN3949CQ Trise (ºC)	Projected Max AMB Operating Temp (125 ºC - Trise)
12.01	23.76	0.42	9.94	82.7	50.3	25.3	25	100
22.93	23.75	0.84	19.90	86.8	61.2	25.6	35.6	89.4
33.82	23.78	1.26	29.92	88.5	67.2	25.9	41.3	83.7
44.55	23.81	1.66	39.60	88.9	71.2	25.9	45.3	79.7
54.83	23.76	2.08	49.46	90.2	72.8	26.2	46.6	78.4
65.76	23.77	2.50	59.49	90.5	75.6	26.3	49.3	75.7

1000 VDC								
P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	INN3949CQ (ºC)	AMB (ºC)	INN3949CQ Trise (ºC)	Projected Max AMB Operating Temp (125 ºC - Trise)
12.26	23.77	0.42	9.94	81.1	52.5	25.3	27.2	97.8
23.18	23.76	0.84	19.92	85.9	65.3	25.7	39.6	85.4
34.21	23.79	1.26	29.93	87.5	72.0	25.8	46.2	78.8
44.90	23.84	1.66	39.64	88.3	77.9	26.5	51.4	73.7
55.38	23.78	2.08	49.49	89.4	80.1	26.7	53.4	71.6
66.24	23.79	2.50	59.54	89.9	83.8	27.6	56.2	68.8

10.2 *Maximum Output Power vs. Ambient Temperature*

(Based on 125 ºC junction temperature of INN3949CQ)

Data below is taken with no additional thermal mitigation

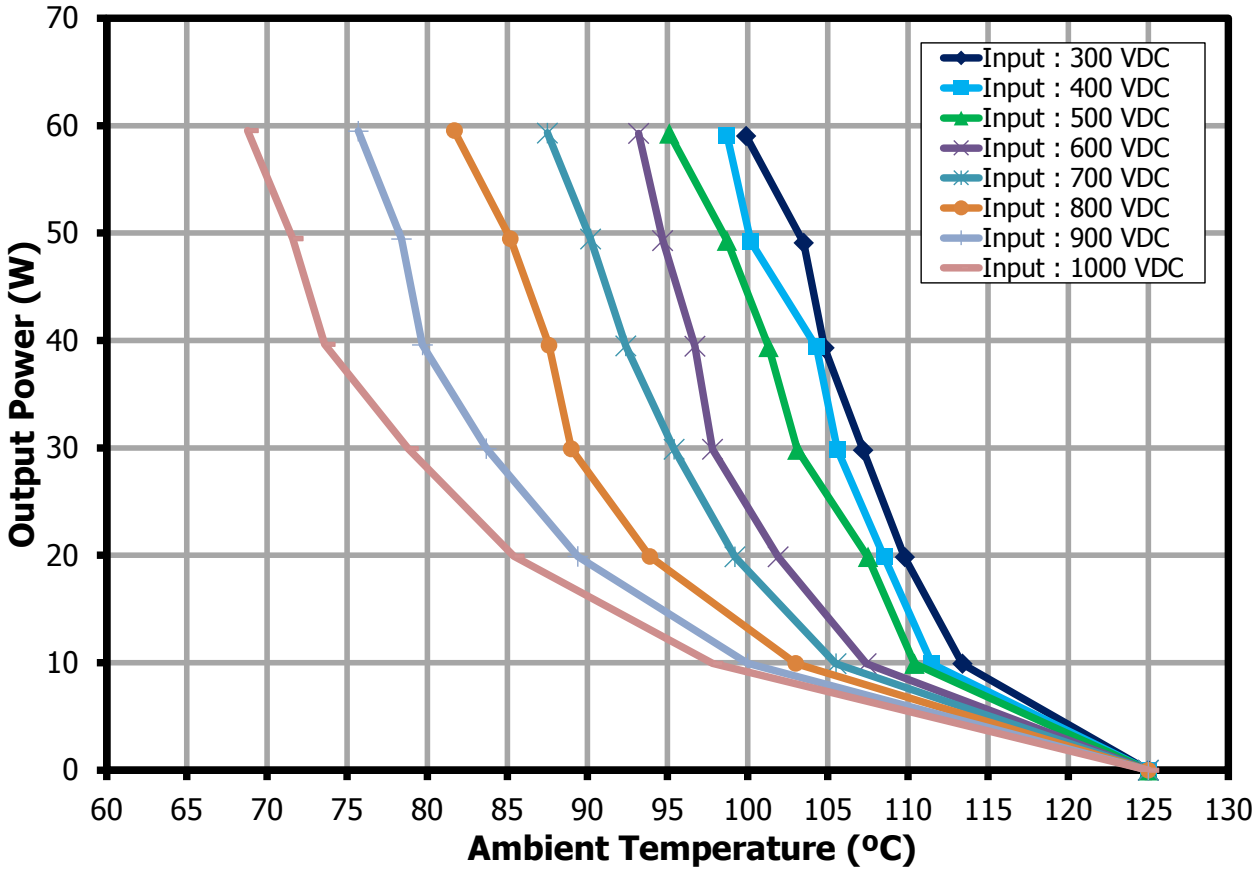


Figure 90 – Maximum Output Power vs. Ambient Temperature.

11 Revision History

Date	Author	Revision	Description & Changes	Reviewed
17-Jan-22	JMR/MA	1.0	Initial Release	Mktg & Apps

For the latest updates, visit our website: www.power.com

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