## Description

The F0443 is a highly integrated 0.6GHz to 2.7GHz dual channel RF digital variable gain amplifier designed for use in diversity/MIMO receivers. The F0443 provides two independent receiver paths each with 29.5dB typical maximum gain and 3.2dB NF at 2.5GHz.

For each path, gain control is split into four separate digital step attenuators: DSA0 provides 6dB of attenuation in a single step using SPI/I3C control. Its counterpart, DSA1, also provides 6dB of attenuation in a single step but it is programmed instead using an external direct control pin. DSA2 yields 29dB of SPI/I3C-controlled attenuation in 1dB steps, while its counterpart, DSA3, includes 18dB attenuation in 6dB steps programmed via two external control pins. The device offers +39dBm nominal output IP3 at 2.5GHz using 372mA total $I_{CC}$ for two active paths with a +5V supply voltage.

The F0443 is packaged in a 7 × 7 mm, 48-LGA with 50Ω single-ended RF input and RF output impedances for ease of integration into the signal path.

## Competitive Advantage

- High Linearity via Renesas' patented *Zero-Distortion*™ Technology
- Exceptionally Low Gain Overshoot/Undershoot via Renesas' patented *Glitch-Free*™ Technology
- Low Noise Figure
- Low DC Current
- High Integration
- High Reliability

## Typical Applications

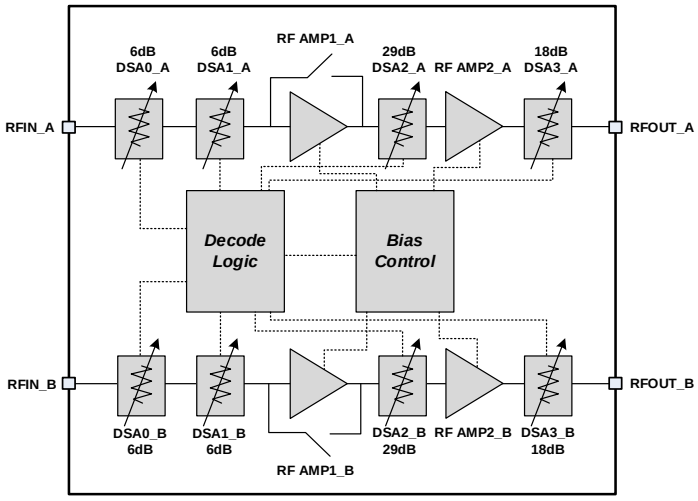
- Multi-mode, Multi-carrier Receivers
- Distributed Antenna Systems
- Digital Radios

## Features

- RF Frequency Range: 0.6GHz to 2.7GHz
- Gain at 2.5GHz:
  - 29.5dB typical max gain in non-bypass mode
  - 10.9dB typical max gain in bypass mode
- DSA Control
  - DSA0: Single 6dB step via SPI/I3C control
  - DSA1: Single 6dB step via 1-bit external pin control
  - DSA2: 29dB range in 1dB steps via SPI/I3C control
  - DSA3: 18dB range in 6dB steps via 2-bit external pin control
- +39dBm OIP3 at 2.5GHz
- NF at 2.5GHz
  - 3.2dB typical in non-bypass mode
  - 8.9dB typical in bypass mode
- +19.7dBm OP1dB at 2.5GHz
- $I_{CC}$ = 372mA
- Standby Mode for power savings with 9mA standby current
- 50Ω single-ended input/output impedances
- 1.8V logic support
- Operating temperature ($T_{EPAD}$) range: -40°C to +105°C
- 7 × 7 mm 48-LGA package

## Block Diagram

Figure 1. Block Diagram



# Contents

Pin Assignments....7
Pin Descriptions....8
Absolute Maximum Ratings....10
Recommended Operating Conditions....11
Electrical Characteristics....12
Thermal Characteristics....26
Typical Operating Conditions (TOC)....26
Functional Description....44
Parallel Programming....44
Standby (STBY) Mode Programming....44
Parallel Programming of DSA1....44
Parallel Programming of DSA3....45
Multi-IC Addressing Scheme....45
Serial Communication....46
Serial Programming....46
Truth Tables....46
SPI Programming....48
SPI Programming - Default....51
I3C Programming....51
Application Information....55
Power Supplies....55
Startup Condition....55
Digital Pin Voltage and Resistance Values....55
Signal Integrity....56
Evaluation Kit Picture....57
Evaluation Kit / Applications Circuit....58
Evaluation Kit BOM....59
Evaluation Kit Operation....60
Power Supply Setup....60
Parallel Logic Control Setup....60
Serial Logic Control Setup....61
Power-On Procedure....61
Power-Off Procedure....61
Package Outline Drawings....62
Ordering Information....62

# List of Figures

Figure 1. Block Diagram ....1
Figure 2. Pin Assignments for 7 × 7 × 0.75 mm 48-LGA Package – Top View ....7
Figure 3. Gain, All DSA = 0dB, Bypass OFF ....27
Figure 4. Gain, All DSA = 0dB, Bypass ON ....27
Figure 5. Gain, DSA0 = 6dB, Bypass OFF ....27
Figure 6. Gain, DSA0 = 6dB, Bypass ON ....27
Figure 7. Gain, DSA1 = 6dB, Bypass OFF ....27
Figure 8. Gain, DSA1 = 6dB, Bypass ON ....27
Figure 9. Gain, DSA2 = 5dB, Bypass OFF ....28
Figure 10. Gain, DSA2 = 5dB, Bypass ON ....28
Figure 11. Gain, DSA2 = 10dB, Bypass OFF ....28
Figure 12. Gain, DSA2 = 10dB, Bypass ON ....28
Figure 13. Gain, DSA2 = 15dB, Bypass OFF ....28
Figure 14. Gain, DSA2 = 15dB, Bypass ON ....28
Figure 15. Gain, DSA2 = 25dB, Bypass OFF ....29
Figure 16. Gain, DSA2 = 25dB, Bypass ON ....29
Figure 17. Gain, DSA3 = 6dB, Bypass OFF ....29
Figure 18. Gain, DSA3 = 6dB, Bypass ON ....29
Figure 19. Gain, DSA3 = 12dB, Bypass OFF ....29
Figure 20. Gain, DSA3 = 12dB, Bypass ON ....29
Figure 21. Gain, DSA3 = 18dB, Bypass OFF ....30
Figure 22. Gain, DSA3 = 18dB, Bypass ON ....30
Figure 23. Relative Gain Error, DSA0 = 6dB, Bypass OFF ....30
Figure 24. Relative Gain Error, DSA1 = 6dB, Bypass OFF ....30
Figure 25. Relative Gain Error, DSA2 = 5dB, Bypass OFF ....30
Figure 26. Relative Gain Error, DSA2 = 10dB, Bypass OFF ....30
Figure 27. Relative Gain Error, DSA2 = 15dB, Bypass OFF ....31
Figure 28. Relative Gain Error, DSA2 = 25dB, Bypass OFF ....31
Figure 29. Relative Gain Error, DSA3 = 6dB, Bypass OFF ....31
Figure 30. Relative Gain Error, DSA3 = 12dB, Bypass OFF ....31
Figure 31. Relative Gain Error, DSA3 = 18dB, Bypass OFF ....31
Figure 32. Gain, All DSA2 Attenuation Settings, Bypass OFF, 25°C ....31
Figure 33. Gain, All DSA2 Attenuation Settings, Bypass ON, 25°C ....32
Figure 34. DSA2 INL (Absolute Attenuation Error) Bypass OFF ....32
Figure 35. DSA2 DNL (Step Attenuation Error) Bypass OFF ....32
Figure 36. DSA2 INL (Absolute Attenuation Error) Bypass ON ....32
Figure 37. DSA2 DNL (Step Attenuation Error) Bypass ON ....32
Figure 38. Gain, All DSA3 Attenuation Settings, Bypass OFF, 25°C ....32

Figure 39. Gain, All DSA3 Attenuation Settings, Bypass ON, 25°C ....33
Figure 40. DSA3 INL (Absolute Attenuation Error) Bypass OFF ....33
Figure 41. DSA3 DNL (Step Attenuation Error) Bypass OFF ....33
Figure 42. DSA3 INL (Absolute Attenuation Error) Bypass ON ....33
Figure 43. DSA3 DNL (Step Attenuation Error) Bypass ON ....33
Figure 44. S11, All DSA = 0dB, Bypass OFF ....33
Figure 45. S11, All DSA = 0dB, Bypass ON ....34
Figure 46. S11, DSA0 = 6dB, Bypass OFF ....34
Figure 47. S11, DSA0 = 6dB, Bypass ON ....34
Figure 48. S11, DSA1 = 6dB, Bypass OFF ....34
Figure 49. S11, DSA1 = 6dB, Bypass ON ....34
Figure 50. S11, DSA2 = 5dB, Bypass OFF ....34
Figure 51. S11, DSA2 = 5dB, Bypass ON ....35
Figure 52. S11, DSA2 = 10dB, Bypass OFF ....35
Figure 53. S11, DSA2 = 10dB, Bypass ON ....35
Figure 54. S11, DSA2 = 15dB, Bypass OFF ....35
Figure 55. S11, DSA2 = 15dB, Bypass ON ....35
Figure 56. S11, DSA2 = 25dB, Bypass OFF ....35
Figure 57. S11, DSA2 = 25dB, Bypass ON ....36
Figure 58. S11, DSA3 = 6dB, Bypass OFF ....36
Figure 59. S11, DSA3 = 6dB, Bypass ON ....36
Figure 60. S11, DSA3 = 12dB, Bypass OFF ....36
Figure 61. S11, DSA3 = 12dB, Bypass ON ....36
Figure 62. S11, DSA3 = 18dB, Bypass OFF ....36
Figure 63. S11, DSA3 = 18dB, Bypass ON ....37
Figure 64. S22, All DSAs = 0dB, Bypass OFF ....37
Figure 65. S22, All DSAs = 0dB, Bypass ON ....37
Figure 66. S22, DSA0 = 6dB, Bypass OFF ....37
Figure 67. S22, DSA0 = 6dB, Bypass ON ....37
Figure 68. S22, DSA1 = 6dB, Bypass OFF ....37
Figure 69. S22, DSA1 = 6dB, Bypass ON ....38
Figure 70. S22, DSA2 = 5dB, Bypass OFF ....38
Figure 71. S22, DSA2 = 5dB, Bypass ON ....38
Figure 72. S22, DSA2 = 10dB, Bypass OFF ....38
Figure 73. S22, DSA2 = 10dB, Bypass ON ....38
Figure 74. S22, DSA2 = 15dB, Bypass OFF ....38
Figure 75. S22, DSA2 = 15dB, Bypass ON ....39
Figure 76. S22, DSA2 = 25dB, Bypass OFF ....39
Figure 77. S22, DSA2 = 25dB, Bypass ON ....39
Figure 78. S22, DSA3 = 6dB, Bypass OFF ....39

Figure 79. S22, DSA3 = 6dB, Bypass ON ....39
Figure 80. S22, DSA3 = 12dB, Bypass OFF ....39
Figure 81. S22, DSA3 = 12dB, Bypass ON ....40
Figure 82. S22, DSA3 = 18dB, Bypass OFF ....40
Figure 83. S22, DSA3 = 18dB, Bypass ON ....40
Figure 84. S12, Max Gain, Bypass OFF ....40
Figure 85. S12, Max Gain, Bypass ON ....40
Figure 86. Noise figure, Max Gain, Bypass OFF ....40
Figure 87. Noise Figure, DSA2 = 5dB, Bypass OFF ....41
Figure 88. Noise Figure, DSA2 = 10dB, Bypass OFF ....41
Figure 89. Noise Figure, DSA2 = 15dB, Bypass OFF ....41
Figure 90. Noise Figure, DSA2 = 25dB, Bypass OFF ....41
Figure 91. Noise figure, Max Gain, Bypass ON ....41
Figure 92. OP1dB at Max Gain, Bypass OFF ....41
Figure 93. OP1dB at Max Gain, Bypass ON ....42
Figure 94. OP1dB at DSA2 = 5dB, Bypass OFF ....42
Figure 95. OP1dB at DSA2 = 10dB, Bypass OFF ....42
Figure 96. OP1dB at DSA2 = 15dB, Bypass OFF ....42
Figure 97. OP1dB at DSA2 = 25dB, Bypass OFF ....42
Figure 98. OIP3 at Max Gain, Bypass OFF ....42
Figure 99. OIP3 at Max Gain, Bypass ON ....43
Figure 100. OIP3 at DSA2 = 5dB, Bypass OFF ....43
Figure 101. OIP3 at DSA2 = 10dB, Bypass OFF ....43
Figure 102. OIP3 at DSA2 = 15dB, Bypass OFF ....43
Figure 103. OIP3 at DSA2 = 25dB, Bypass OFF ....43
Figure 104. SPI Word ....46
Figure 105. I3C Word ....46
Figure 106. Multi-IC Addressing Scheme Using SPI ....48
Figure 107. SPI Timing Diagram ....49
Figure 108. SPI Serial Register Timing Diagram ....50
Figure 109. SPI Programming – Default Register Settings ....51
Figure 110. I3C Static Addressing Scheme ....52
Figure 111. I3C Timing Diagram – Initialization ....53
Figure 112. I3C Timing Diagram ....53
Figure 113. I3C Programming – Default Register Settings for Byte1 (Programming Word) ....54
Figure 114. I3C Timing Intervals (Pictorial View) ....54
Figure 115. Internal Pull-up Configuration for STBY_A, STBY_B, DSA1 and DSA3 Control Pins ....55
Figure 116. Internal Pull-down Configuration for the SPI_I3C_SEL, ID_0, and ID_1 Control Pins ....55
Figure 117. Control Pin Interface for Signal Integrity ....56
Figure 118. Top View ....57

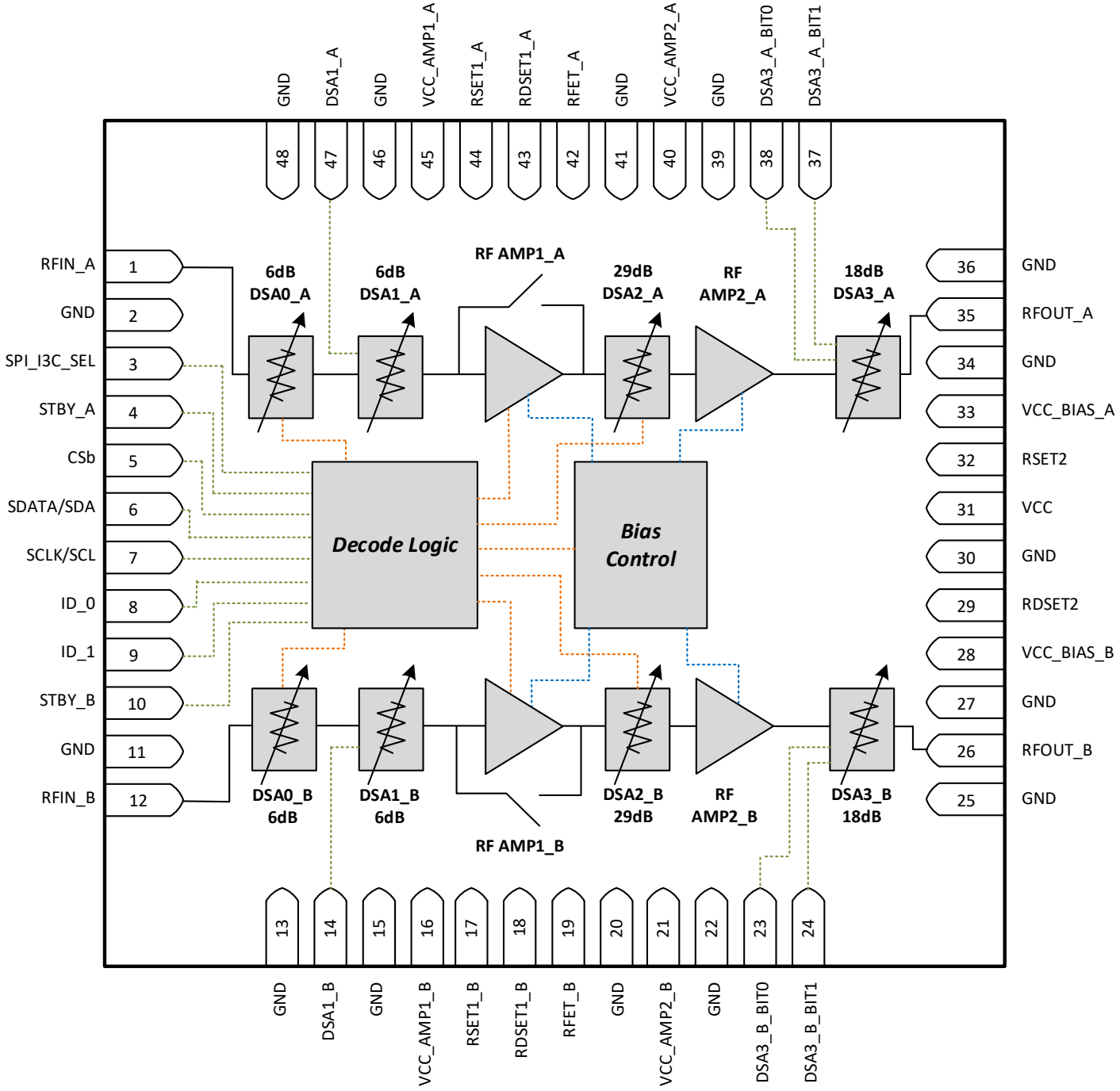
Figure 119. Bottom View ....57
Figure 120. Electrical Schematic ....58
Figure 121. Power Supply and Logic Voltage Connections....60
Figure 122. Power Supply and Logic Voltage Connections....60
Figure 123. Serial Logic Connections....61

## List of Tables

Table 1. Pin Descriptions....8
Table 2. Absolute Maximum Ratings....10
Table 3. Recommended Operating Conditions ....11
Table 4. General Electrical Characteristics ....12
Table 5. Electrical Characteristics – Low Band (0.6GHz to 1.1GHz) Performance ....14
Table 6. Electrical Characteristics – Mid Band (1.5GHz to 2GHz) Performance....18
Table 7. Electrical Characteristics – High Band (2.3GHz to 2.7GHz) Performance ....22
Table 8. Package Thermal Characteristics....26
Table 9. STBY Mode Truth Table....44
Table 10. DSA1 Truth Table....44
Table 11. DSA3 Truth Table....45
Table 12. Static Address Truth Table....45
Table 13. Serial Communication Mode Truth Table ....46
Table 14. Path Select (Path A/Path B) Truth Table....46
Table 15. Bypass Mode (Amp1_A/Amp1_B) Truth Table....47
Table 16. DSA0 Truth Table....47
Table 17. DSA2 Abbreviated Truth Table....47
Table 18. SPI Timing Diagram Values Intervals....50
Table 19. I3C Slave Addressing ....51
Table 20. I3C Timing Intervals (Tabulated Figures) ....54
Table 21. Bill of Materials (BOM)....59

# Pin Assignments

Figure 2. Pin Assignments for 7 × 7 × 0.75 mm 48-LGA Package – Top View



# Pin Descriptions

Table 1. Pin Descriptions

| Pin Number | Name | Description |
|---|---|---|
| 1 | RFIN_A | Channel A RF input internally matched to 50Ω. Must use external DC block. |
| 2, 11, 13, 15, 20, 22, 25, 27, 30, 34, 36, 39, 41, 46, 48 | GND | Internally grounded. This pin must be grounded with a via as close to the pin as possible. |
| 3 | SPI_I3C_SEL | Logic control to select between SPI or I3C mode. Logic HIGH = I3C slave mode using a 'Slave-Lite' version of the MIPI I3C communication protocol. Logic LOW/Open = SPI slave mode. An internal pull-down resistor of 100kΩ connects between this pin and GND. |
| 4 | STBY_A | Standby control for Channel A. HIGH/Open = device power OFF with SPI/I3C still powered ON, LOW = device power ON. An internal pull-up resistor network connects between this pin and 1.67V. |
| 5 | CSb | Chip Select bar input. Used only for SPI mode. Logic LOW allows data to be shifted in. Logic HIGH updates the programming register. |
| 6 | DATA/SDA | SPI slave data in or I3C data in/out. |
| 7 | CLK/SCL | SPI/I3C clock input. |
| 8 | ID_0 | Bit 0 for the I3C static address or used for adding static addressing capability in SPI mode. See the Programming section for details. An internal pull-down resistor of 100kΩ connects between this pin and GND. |
| 9 | ID_1 | Bit 1 for the I3C static address or used for adding static addressing capability in SPI mode. See the Programming section for details. An internal pull-down resistor of 100kΩ connects between this pin and GND. |
| 10 | STBY_B | Standby control for Channel B. HIGH/Open = device power OFF with SPI/I3C still powered ON, LOW = device power ON. An internal pull-up resistor network connects between this pin and 1.67V. |
| 12 | RFIN_B | Channel B RF input internally matched to 50Ω. Must use external DC block. |
| 14 | DSA1_B | Logic control for channel B DSA1. Logic HIGH/Open = 6dB attenuation, logic LOW = 0dB attenuation. An internal pull-up resistor network connects between this pin and 1.67V. |
| 16 | $V_{CC}$_AMP1_B | Channel B amplifier 1 DC supply voltage. Connect bypass capacitor(s) as close to the pin as possible. |
| 17 | RSET1_B | Connect 2.67kΩ external resistor to GND to optimize amplifier bias. Used with RDSET1_B pin 18. |
| 18 | RDSET1_B | Connect 9.1kΩ external resistor to GND to optimize amplifier bias. Used with RSET1_B pin 17. |
| 19 | RFET_B | Connect 4.7kΩ external resistor to GND to optimize amplifier gain variation over temperature. |
| 21 | $V_{CC}$_AMP2_B | Channel B amplifier 2 DC supply voltage. Connect bypass capacitor(s) as close to the pin as possible. |
| 23 | DSA3_B_BIT0 | Logic control bit 0 for channel B DSA3. An internal pull-up resistor network connects between this pin and 1.67V. |
| 24 | DSA3_B_BIT1 | Logic control bit 1 for channel B DSA3. An internal pull-up resistor network connects between this pin and 1.67V. |
| 26 | RFOUT_B | Channel B RF output internally matched to 50Ω. Must use external DC block. |
| 28 | $V_{CC}$_BIAS_B | Channel B bias circuitry DC supply voltage. Connect bypass capacitor(s) as close to the pin as possible. |

| Pin Number | Name | Description |
|---|---|---|
| 29 | RDSET2 | Connect 13kΩ external resistor to GND to optimize amplifier bias. Used with RSET2 pin 32. |
| 31 | VCC | DC supply voltage. Connect bypass capacitor(s) as close to the pin as possible. |
| 32 | RSET2 | Connect 2.94kΩ external resistor to GND to optimize amplifier bias. Used with RDSET2 pin 29. |
| 33 | $V_{CC}$_BIAS_A | Channel A bias circuitry DC supply voltage. Connect bypass capacitor(s) as close to the pin as possible. |
| 35 | RFOUT_A | Channel A RF output internally matched to 50Ω. Must use external DC block. |
| 37 | DSA3_A_BIT1 | Logic control bit 1 for channel B DSA3. An internal pull-up resistor network connects between this pin and 1.67V. |
| 38 | DSA3_A_BIT0 | Logic control bit 0 for channel B DSA3. An internal pull-up resistor network connects between this pin and 1.67V. |
| 40 | $V_{CC}$_AMP2_A | Channel A amplifier 2 DC supply voltage. Connect bypass capacitor(s) as close to the pin as possible. |
| 42 | RFET_A | Connect 4.7kΩ external resistor to GND to optimize amplifier gain variation over temperature. |
| 43 | RDSET1_A | Connect 9.1kΩ external resistor to GND to optimize amplifier bias. Used with RSET1_A pin 44. |
| 44 | RSET1_A | Connect 2.67kΩ external resistor to GND to optimize amplifier bias. Used with RDSET1_A pin 43. |
| 45 | $V_{CC}$_AMP1_A | Channel A Amplifier 1 DC supply voltage. Connect bypass capacitor(s) as close to the pin as possible. |
| 47 | DSA1_A | Logic control for channel A DSA1. Logic HIGH/Open = 6dB attenuation, logic LOW = 0dB attenuation. An internal pull-up resistor network connects between this pin and 1.67V. |
| | – EPAD | Exposed paddle. Internally connected to ground. Solder this exposed paddle to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance. |

# Absolute Maximum Ratings

Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

| Parameter | Symbol | Minimum | Maximum | Units |
|---|---|---|---|---|
| $V_{CC}$ to GND | $V_{CC}$ | -0.3 | +5.5 | V |
| SDATA/SDA, SCLK/SCL, CSb | $V_{SPI_I3C}$ | -0.3 | 2.2[c] | V |
| STBY_A, STBY_B, DSA1_A, DSA1_B, DSA3_A_BIT0, DSA3_A_BIT1, DSA3_B_BIT0, DSA3_B_BIT1, SPI_I3C_SEL, ID_0, ID_1 | $V_{LOGIC}$ | -0.3 | $V_{CC}$ + 0.25[c] | V |
| RFIN_A, RFIN_B externally applied DC voltage | $V_{RFIN}$ | +1.4 | +3.6 | V |
| RFOUT_A, RFOUT_B, externally applied DC voltage | $V_{RFOUT}$ | +1.4 | +3.6 | V |
| RF Input CW Power (RFIN_A or RFIN_B) applied for 24 hours maximum [a]<br>Input/Output VSWR < 2:1 in a 50Ω system<br>$V_{CC}$ = +5.0V, $T_{EPAD}$ = 105°C [b]<br>Under the Max Gain Condition (Bypass OFF) | $P_{RFMAX24_1}$ | | 20 | dBm |
| RF Input CW Power (RFIN_A or RFIN_B) applied for 24 hours maximum [a]<br>Input/Output VSWR < 2:1 in a 50Ω system<br>$V_{CC}$ = +5.0V, $T_{EPAD}$ = 105°C [b]<br>Under the Max Gain Condition (Bypass OFF) with DSA0/DSA1 = 6dB Atten | $P_{RFMAX24_2}$ | | 23 | dBm |
| RF Input CW Power (RFIN_A or RFIN_B) applied for 24 hours maximum [a]<br>Input/Output VSWR < 2:1 in a 50Ω system<br>$V_{CC}$ = +5.0V, $T_{EPAD}$ = 105°C [b]<br>Under the Max Gain Condition (Bypass ON) | $P_{RFMAX24_3}$ | | 21 | dBm |
| RF Input CW Power (RFIN_A or RFIN_B) applied for 24 hours maximum [a]<br>Input/Output VSWR < 2:1 in a 50Ω system<br>$V_{CC}$ = +5.0V, $T_{EPAD}$ = 105°C [b]<br>Under the Max Gain Condition (Bypass ON) with DSA0/DSA1 = 6dB Atten | $P_{RFMAX24_4}$ | | 23 | dBm |
| Storage Temperature Range | $T_{STOR}$ | -65 | +150 | °C |
| Lead Temperature (soldering, 10s) | $T_{LEAD}$ | | +260 | °C |
| Electrostatic Discharge – HBM<br>(JEDEC/ESDA JS-001-2012) | $V_{ESDHBM}$ | | 2000 | V |
| Electrostatic Discharge – CDM<br>(JEDEC 22-C101F) | $V_{ESDCDM}$ | | 500 | V |

[a] Exposure to these maximum RF levels can result in significant $V_{CC}$ current draw due to overdriving the amplifier stage.

[b] $T_{EPAD}$ = Temperature of the exposed paddle.

[c] Control pins should remain at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

# Recommended Operating Conditions

Table 3. Recommended Operating Conditions

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| Power Supply Voltage [a] | $V_{CC}$ | All $V_{CC}$ pins. | 4.75 | | 5.25 | V |
| Operating Temperature Range | $T_{EPAD}$ | Exposed paddle. | -40 | | +105 | °C |
| RF Frequency Range [b] | $f_{RF}$ | Tuning Set 1. | 0.6 | | 1.1 | GHz |
| | | Tuning Set 2. | 1.5 | | 2 | |
| | | Tuning Set 3. | 2.3 | | 2.7 | |
| RF Input CW Power [c] | $P_{RF1}$ | (RFIN_A or RFIN_B) Input/Output VSWR < 2:1 in a 50Ω system $T_{EPAD}$ = 105°C $V_{CC}$ = +5.0V Max Gain Mode, Bypass OFF | | | -23 | dBm |
| | | (RFIN_A or RFIN_B) Input/Output VSWR < 2:1 in a 50Ω system $T_{EPAD}$ = 105°C $V_{CC}$ = +5.0V Max Gain Mode, Bypass ON | | | -4 | dBm |
| Port Impedance (RFIN_A, RFIN_B, RFOUT_A, RFOUT_B) | $Z_{RF}$ | Single-ended. | | 50 | | Ω |
| Junction Temperature | $T_J$ | | | | +125 | °C |

[a] Power-on resets will only occur for $V_{CC}$ < 3.75V. Device is designed to function with any supply voltage ≥ 3.75V, although performance may be degraded when operated outside the recommended voltage range.

[b] To optimize RF performance, different matching components may be used as described in the BOM. The design will strive for one common match that covers the entire 0.6GHz to 2.7GHz band.

[c] Recommended maximum conditions are defined as a guidance towards obtaining the datasheet specified linearity performance.

# Electrical Characteristics

See the F0443 Typical Application Circuit. Specifications apply when operated as a Dual DVGA with $V_{CC}$ = +5.0V, $f_{RF}$ = 1.75GHz, $T_{EPAD}$ = +25°C, STBY_A = STBY_B = logic LOW, $Z_S = Z_L = 50\Omega$, maximum gain setting (all DSAs set to 0dB attenuation), Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Table 4. General Electrical Characteristics

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| GPIO Logic Input Threshold | $V_{IH-GPIO}$ | All GPIO logic input pins. | *1.07* [a] [c] | | 3.6[c] | V |
| | $V_{IL-GPIO}$ | All GPIO logic input pins. | 0 | | *0.68*[c] | V |
| Serial Digital Interface Logic Input Threshold | $V_{IH-SDI}$ | All Serial Interface logic input pins. | *1.07* [a] [c] | | 1.95[c] | V |
| | $V_{IL-SDI}$ | All Serial Interface logic input pins. | 0 | | *0.68*[c] | V |
| Logic Current (per GPIO pin) – DSA1_X, DSA3_X_BIT0, DSA3_X_BIT1, SPI_I3C_SEL, ID_0, ID_1, STBY_X | $I_{IH-GPIO}$ | 3.3V logic. | | | *60*[c] | µA |
| | $I_{IL-GPIO}$ | 1.8V logic. | | | 50[c] | µA |
| Logic Current (per SDI pin) - DATA/SDA, CLK/SCL, CSb | $I_{IL-SDI}$ | 1.8V logic. | | | 20[c] | µA |
| DC Current | $I_{CC_2CH}$ | Both channels on. | | 372 | *400*[c] | mA |
| | $I_{CC_1CH}$ | One channel on. | | 192 | *210*[c] | |
| | $I_{CC_STBY}$ | Standby Mode [b]. | | 9 | *11.5*[c] | |
| Startup Time | $T_{START}$ | 50% of STBY going low to the state where the gain is within ±1dB of its final value with no attenuation. | | 62 | | ns |
| DSA0 Adjustment Range | $G_{ADJ0}$ | 6dB step size. | | 6 | | dB |
| DSA1 Adjustment Range | $G_{ADJ1}$ | 6dB step size. | | 6 | | dB |
| DSA2 Adjustment Range | $G_{ADJ2}$ | 1dB step size. | | 29 | | dB |
| DSA3 Adjustment Range | $G_{ADJ3}$ | 6dB step size. | | 18 | | dB |
| Maximum Attenuation Glitch | $ATTN_G$ | Any DSA state change. | | 1.6 | | dB |
| DSA0 Gain Settling Time | $DSA0_{GST}$ | 50% of CSb (SPI) or STOP command (I3C) to within 0.1dB of final value. | | 35 | | ns |
| DSA1 Gain Settling Time | $DSA1_{GST}$ | 50% CTL to within 0.1dB of the final value, 0dB state to 6dB state. | | 20 | 35[c] | ns |
| | | 50% CTL to within 0.1dB of the final value, 6dB state to 0dB state. | | 20 | 35[c] | |
| DSA2 Gain Settling Time | $DSA2_{GST}$ | 50% of CSb (SPI) or STOP command (I3C) to within 0.1dB of the final value. | | 70 | | ns |

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| DSA3 Gain Settling Time | $DSA3_{GST}$ | 50% CTL to within 0.1dB of the final value, 0dB state to 18dB state. | | 20 | 35[c] | ns |
| | | 50% CTL to within 0.1dB of the final value, 18dB state to 0dB state. | | 20 | 35[c] | |
| Stability K Factor | $K_{FACT}$ | Over entire temperature range. | 1 | | | unit |
| Serial Clock Speed | $f_{SPI_CLK}$ | SPI interface clock. | | | *12.5*[c] | MHz |
| | $f_{I3C_CLK}$ | I3C interface clock. | | | *12.5*[c] | |
| CSb to First Serial Clock Rising Edge | $t_{LS}$ | SPI 3 wire bus. 50% of CSb falling edge to 50% of CLK rising edge. | 10[c] | | | ns |
| Serial Data Hold Time | $t_H$ | SPI 3 wire bus. 50% of CLK rising edge to 50% of Data falling edge. | 10[c] | | | ns |
| Final Serial Clock Rising Edge to CSb | $t_{CLS}$ | SPI 3 wire bus. 50% of CLK rising edge to 50% of CSb rising edge. | 10[c] | | | ns |

[a] Specifications in the minimum/maximum columns that are shown in bold italics are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] During standby mode, SPI is to be left ON and previous state shall be maintained when device is powered up.

[c] The attenuators can be assumed to be purely resistive elements when performing cascaded analysis calculations. Ensure to take into account any relevant INL/DNL effects.

## Table 5. Electrical Characteristics – Low Band (0.6GHz to 1.1GHz) Performance

See the F0443 Typical Application Circuit. Specifications apply when operated as a Dual DVGA. Typical data is with $V_{CC}$ = +5.0V, $f_{RF}$ = 0.9GHz, $T_{EPAD}$ = +25°C, minimum and maximum data is over $f_{RF}$ = 0.6GHz to 1.1GHz and $T_{EPAD}$ = -40°C to +105°C, STBY_A = STBY_B = logic LOW, $Z_S = Z_L = 50\Omega$, maximum gain setting (all DSAs set to 0dB attenuation), Tone Spacing = 1MHz, Pout = 0dBm/Tone, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

| Parameter | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| RF Input Return Loss | $RL_{IN}$ | Worst case typical, $T_{EPAD}$ = 25°C, $f_{RF}$ = 0.6GHz to 1.1GHz. | | | 12.2 | | dB |
| | | Worst case typical, $T_{EPAD}$ = 105°C, $f_{RF}$ = 0.6GHz to 1.1GHz. | | | 10.2 | | |
| RF Output Return Loss | $RL_{OUT}$ | Worst case typical, $T_{EPAD}$ = 25°C, $f_{RF}$ = 0.6GHz to 1.1GHz. | | | 13.7 | | dB |
| | | Worst case typical, $T_{EPAD}$ = 105°C, $f_{RF}$ = 0.6GHz to 1.1GHz. | | | 12.4 | | |
| Gain Non-Bypass Mode | $G_{MAX}$ | Minimum and maximum values are valid over: $f_{RF}$ = 0.6GHz to 1.1GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 0.9GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | *27.6* [a, f] | 30.4 | *32* | dB |
| | $G_1$ | | DSA0, = 0dB, DSA1 = 0dB, DSA2 = 5dB, DSA3 = 0dB | 21.4 | 24.9 | 26 | |
| | $G_2$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 10dB, DSA3 = 0dB | 16.4 | 19.9 | 21.9 | |
| | $G_3$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 15dB, DSA3 = 0dB | 11.1 | 15 | 17.5 | |
| | $G_4$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 25dB, DSA3 = 0dB | 1.4 | 4.9 | 7 | |
| Gain Non-Bypass Mode Variation Over Temperature | $G_{TEMP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | +0.9/ -1.4 | | dB |
| Gain Non-Bypass Mode Flatness | $G_{FLAT}$ | Gain Flatness. Any fixed temperature. Any 200MHz bandwidth within $f_{RF}$ = 0.6GHz to 1.1GHz. | | | 0.6 | | dB |
| Gain Bypass Mode | $G_{BYP}$ | Minimum and maximum values are valid over: $f_{RF}$ = 0.6GHz to 1.1GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 0.9GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | *9* | 11.4 | *13* | dB |
| Gain Bypass Mode Variation Over Temperature | $G_{TEMP_BYP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | +0.7/ -1 | | dB |
| Gain Bypass Mode Flatness | $G_{FLAT_BYP}$ | Gain Flatness. Any fixed temperature. Any 200MHz bandwidth within $f_{RF}$ = 0.6GHz to 1.1GHz. | | | 0.3 | | dB |
| Noise Figure Non-Bypass Mode | $NF_{MAX}$ | Minimum and maximum values are valid over: $f_{RF}$ = 0.6GHz to 1.1GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 0.9GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | | 2.8 | 3.8 | dB |
| | $NF_1$ | | DSA0, = 0dB, DSA1 = 0dB, DSA2 = 5dB, DSA3 = 0dB | | 3.3 | 4.6 | |
| | $NF_2$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 10dB, DSA3 = 0dB | | 4.4 | 6.1 | |
| | $NF_3$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 15dB, DSA3 = 0dB | | 6.7 | 8.9 | |
| | $NF_4$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 25dB, DSA3 = 0dB | | 15 | 17.8 | |

| Parameter | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| NF Non-Bypass Mode Variation Over Temperature | $NF_{TEMP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | -0.5/ +0.7 | | dB |
| Noise Figure Bypass Mode | $NF_{BYP}$ | Minimum and maximum values are valid over: $f_{RF}$ = 0.6GHz to 1.1GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 0.9GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | | 7.5 | 10.2 | dB |
| NF Bypass Mode Variation Over Temperature | $NF_{TEMP_BYP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | -1.1/ +1.4 | | dB |
| Output Third Order Intercept Point | $OIP3_1$ | Tone Spacing = 1MHz Pout = 0dBm/Tone, Pout = -10dBm/Tone at DSA2 = 25dB Attenuation Minimum and maximum values are valid over: $f_{RF}$ = 0.6GHz to 1.1GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 0.9GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum gain | 35.7 | 39.1 | | dBm |
| | $OIP3_2$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 5dB, DSA3 = 0dB | 35.2 | 38 | | |
| | $OIP3_3$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 10dB, DSA3 = 0dB | 33.7 | 36.5 | | |
| | $OIP3_4$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 15dB, DSA3 = 0dB | 30.8 | 34.1 | | |
| | $OIP3_5$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 25dB, DSA3 = 0dB | 22.5 | 25 | | |
| OIP3 Variation Over Temperature | $OIP3_{TEMP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | -0.2/ +0.9 | | dB |
| Output Third Order Intercept Point Bypass Mode | $OIP3_{BYP}$ | Minimum and maximum values are valid over: $f_{RF}$ = 0.6GHz to 1.1GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 0.9GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | 36.3 | 38.7 | | dB |
| OIP3 Bypass Mode Variation Over Temperature | $OIP3_{TEMP_BYP}$ | $T_{EPAD}$ = -40ºC to 105ºC. | | | -0.2/ 0.2 | | dB |
| Output 1dB Compression Non-Bypass Mode[b] | $OP1dB_1$ | Minimum and maximum values are valid over: $f_{RF}$ = 0.6GHz to 1.1GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 0.9GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum gain | *17.8* | 19.1 | | dBm |
| | $OP1dB_2$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 5dB, DSA3 = 0dB | 17.6 | 18.9 | | |
| | $OP1dB_3$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 10dB, DSA3 = 0dB | 17.6 | 18.8 | | |
| | $OP1dB_4$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 15dB, DSA3 = 0dB | 14.9 | 18.4 | | |
| | $OP1dB_5$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 25dB, DSA3 = 0dB | 5.5 | 9.1 | | |
| OP1dB Variation Over Temperature | $OP1dB_{TEMP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | +0.1/ -0.2 | | dB |

| Parameter | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Output 1dB Compression Bypass Mode | $OP1dB_{BYP}$ | Minimum and maximum values are valid over: $f_{RF}$ = 0.6GHz to 1.1GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 0.9GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | 18 | 19.1 | | dBm |
| OP1dB Bypass Mode Variation Over Temperature | $OP1dB_{TEMP_BYP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | +0.2/ -0.3 | | dB |
| Reverse Isolation | $ISO_{REV1}$ | Maximum gain, Non-Bypass mode. | | 42.4 | 44 | | dB |
| | $ISO_{REV2}$ | Maximum gain, Bypass mode. | | 24 | 25.8 | | |
| | $ISO_{REV3}$ | Minimum gain, Non-Bypass mode. | | 82.3 | 83.6 | | |
| | $ISO_{REV4}$ | Minimum gain, Bypass mode. | | 88 | 91 | | |
| Channel-to-Channel Isolation [c] | $ISO_{CH-CH1}$ | Maximum gain on both channels. | | 49 | 57 | | dB |
| | $ISO_{CH-CH2}$ | Minimum gain on both channels, Bypass OFF. | | | 55 | | |
| | $ISO_{CH-CH3}$ | Ch A: Max Gain<br>Ch B: Note [d] | | | 41 | | |
| | $ISO_{CH-CH4}$ | Ch A: Note [d]<br>Ch B: Max Gain | | | 41 | | |
| | $ISO_{CH-CH5}$ | Ch A: Min Gain<br>Ch B: Note [e] | | | 43 | | |
| | $ISO_{CH-CH6}$ | Ch A: Note [e]<br>Ch B: Min Gain | | | 43 | | |
| DSA Attenuation Error (INL)[f] | $ERR_{DSA0ABS}$ | Minimum and maximum values are valid over: $f_{RF}$ = 0.6GHz to 1.1GHz, $T_{EPAD}$ = -40°C to +105°C $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 0.9GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | DSA1, DSA2, DSA3 = 0dB DSA0 = 6dB | | ±0.3 | | dB |
| | $ERR_{DSA1ABS}$ | | DSA0, DSA2, DSA3 = 0dB DSA1 = 6dB | | ±0.3 | | |
| | $ERR_{DSA2ABS}$ | | DSA0, DSA1, DSA3 = 0dB DSA2 = 5dB | | +0.6 | | |
| | | | DSA0, DSA1, DSA3 = 0dB DSA2 = 10dB | | +0.6 | | |
| | | | DSA0, DSA1, DSA3 = 0dB DSA2 = 15dB | | +0.6 | | |
| | | | DSA0, DSA1, DSA3 = 0dB DSA2 = 20dB | | +0.6 | | |
| | | | DSA0, DSA1, DSA3 = 0dB DSA2 = 25dB | | +0.6 | | |
| | $ERR_{DSA3ABS}$ | | DSA0, DSA1, DSA2 = 0dB DSA3 = 6dB | | +0.1 | | |
| | | | DSA0, DSA1, DSA2 = 0dB DSA3 = 12dB | | +0.1 | | |
| | | | DSA0, DSA1, DSA2 = 0dB DSA3 = 18dB | | +0.15 | | |

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| DSA2 Step Error (DNL)[f] | $ERR_{DSA2SE}$ | Between adjacent states. | | ±0.2 | | dB |
| DSA3 Step Error (DNL)[f] | $ERR_{DSA3SE}$ | Between adjacent states. | | ±0.2 | | |
| Relative Phase DSA0 | $\Phi_{DSA0REL}$ | Any state, relative to 0dB attenuation state. | | 3 | | deg |
| Relative Phase DSA1 | $\Phi_{DSA1REL}$ | Any state, relative to 0dB attenuation state. | | 3 | | |
| Phase Deviation DSA2 | $\Phi_{DSA2ADJ}$ | Between adjacent states. | | 1.5 | | |
| Relative Phase DSA2 | $\Phi_{DSA2RELMAX}$ | DSA set to 29dB, relative to 0dB attenuation state. | | 5 | | |
| | $\Phi_{DSA2RELMID}$ | DSA set to 14dB, relative to 0dB attenuation state. | | 3 | | |
| Relative Phase DSA3 | $\Phi_{DSA3REL}$ | Any state, relative to 0dB attenuation state. | | 2 | | |

[a] Specifications in the minimum/maximum columns that are shown in bold italics are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] 1dB compression point is a linearity figure of merit. Refer to Abs Max Ratings table for maximum RF input power.

[c] Signal applied to RFIN_A (RFIN_B) and measure desired signal at RFOUT_B (RFOUT_A) and compare to signal level at RFOUT_A (RFOUT_B).

[d] Channel A or Channel B DSA combinations which yield 24dB in total attenuation. DSA2_A or DSA2_B settings limited to the following: 0dB, 6dB, 12dB, 18dB, and 24dB.

[e] Channel A or Channel B DSA combinations yielding 35dB in total attenuation. DSA2_A or DSA2_B settings limited to the following: 5dB, 11dB, 17dB, 23dB, and 29dB. Since the maximum attenuation state totals 59dB, this will yield a 24dB difference between the two channels.

[f] The attenuators can be assumed to be purely resistive elements when performing cascaded analysis calculations. Be sure to take into account any relevant INL/DNL effects

## Table 6. Electrical Characteristics – Mid Band (1.5GHz to 2GHz) Performance

See the F0443 Typical Application Circuit. Specifications apply when operated as a Dual DVGA. Typical data is with $V_{CC}$ = +5.0V, $f_{RF}$ = 1.75GHz, $T_{EPAD}$ = +25°C, minimum and maximum data is over $f_{RF}$ = 1.5GHz to 2GHz and $T_{EPAD}$ = -40°C to +105°C, STBY_A = STBY_B = logic LOW, $Z_S = Z_L = 50\Omega$, maximum gain setting (all DSAs set to 0dB attenuation), Tone Spacing = 1MHz, Pout = 0dBm/Tone, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

| Parameter | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| RF Input Return Loss | $RL_{IN}$ | Worst case typical, $T_{EPAD}$ = 25°C, $f_{RF}$ = 1.5GHz to 2GHz. | | | 12.5 | | dB |
| | | Worst case typical, $T_{EPAD}$ = 105°C, $f_{RF}$ = 1.5GHz to 2GHz. | | | 10.3 | | |
| RF Output Return Loss | $RL_{OUT}$ | Worst case typical, $T_{EPAD}$ = 25°C, $f_{RF}$ = 1.5GHz to 2GHz. | | | 11 | | dB |
| | | Worst case typical, $T_{EPAD}$ = 105°C, $f_{RF}$ = 1.5GHz to 2GHz. | | | 10.4 | | |
| Gain Non-Bypass Mode | $G_{MAX}$ | Minimum and maximum values are valid over: $f_{RF}$ = 1.5GHz to 2GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 1.75GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | *26.8* [a, f] | 29.5 | *31.5* | dB |
| | $G_1$ | | DSA0, = 0dB, DSA1 = 0dB, DSA2 = 5dB, DSA3 = 0dB | 22 | 24.7 | 27 | |
| | $G_2$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 10dB, DSA3 = 0dB | 17.1 | 19.8 | 22.2 | |
| | $G_3$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 15dB, DSA3 = 0dB | 12 | 14.9 | 17.2 | |
| | $G_4$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 25dB, DSA3 = 0dB | 2.1 | 5.1 | 7.5 | |
| Gain Non-Bypass Mode Variation Over Temperature | $G_{TEMP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | +0.9/ -1.3 | | dB |
| Gain Non-Bypass Mode Flatness | $G_{FLAT}$ | Gain Flatness. Any fixed temperature. Any 200MHz bandwidth within $f_{RF}$ = 1.5GHz to 2GHz. | | | 0.2 | | dB |
| Gain Bypass Mode | $G_{BYP}$ | Minimum and maximum values are valid over: $f_{RF}$ = 1.5GHz to 2GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 1.75GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | *7.8* | 10.9 | *12.4* | dB |
| Gain Bypass Mode Variation Over Temperature | $G_{TEMP_BYP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | +0.8/ -1.0 | | dB |
| Gain Bypass Mode Flatness | $G_{FLAT_BYP}$ | Gain Flatness. Any fixed temperature. Any 200MHz bandwidth within $f_{RF}$ = 1.5GHz to 2GHz. | | | 0.4 | | dB |
| Noise Figure Non-Bypass Mode | $NF_{MAX}$ | Minimum and maximum values are valid over: $f_{RF}$ = 1.5GHz to 2GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 1.75GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | | 3.2 | 4.5 | dB |
| | $NF_1$ | | DSA0, = 0dB, DSA1 = 0dB, DSA2 = 5dB, DSA3 = 0dB | | 3.7 | 5.2 | |
| | $NF_2$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 10dB, DSA3 = 0dB | | 4.8 | 6.7 | |
| | $NF_3$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 15dB, DSA3 = 0dB | | 7.1 | 9.6 | |
| | $NF_4$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 25dB, DSA3 = 0dB | | 15.2 | 18.2 | |

| Parameter | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| NF Non-Bypass Mode Variation Over Temperature | $NF_{TEMP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | -0.6/ +0.9 | | dB |
| Noise Figure Bypass Mode | $NF_{BYP}$ | Minimum and maximum values are valid over: $f_{RF}$ = 1.5GHz to 2GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 1.75GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | | 8.9 | 12 | dB |
| NF Bypass Mode Variation Over Temperature | $NF_{TEMP_BYP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | -1.2/ +1.6 | | dB |
| Output Third Order Intercept Point | $OIP3_1$ | Tone Spacing = 1MHz Pout = 0dBm/Tone, Pout = -10dBm/Tone at DSA2 = 25dB Attenuation | Maximum gain | 34.5 | 41.7 | | dBm |
| | $OIP3_2$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 5dB, DSA3 = 0dB | 33.7 | 40.1 | | |
| | $OIP3_3$ | Minimum and maximum values are valid over: $f_{RF}$ = 1.5GHz to 2GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 1.75GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 10dB, DSA3 = 0dB | 32 | 38.7 | | |
| | $OIP3_4$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 15dB, DSA3 = 0dB | 29 | 36.1 | | |
| | $OIP3_5$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 25dB, DSA3 = 0dB | 22.7 | 27 | | |
| OIP3 Variation Over Temperature | $OIP3_{TEMP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | -1.8/ +0.3 | | dB |
| Output Third Order Intercept Point Bypass Mode | $OIP3_{BYP}$ | Minimum and maximum values are valid over: $f_{RF}$ = 1.5GHz to 2GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 1.75GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | 34.3 | 39 | | dB |
| OIP3 Bypass Mode Variation Over Temperature | $OIP3_{TEMP_BYP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | -1.8/ +1.0 | | dB |
| Output 1dB Compression Non-Bypass Mode[b] | $OP1dB_1$ | Minimum and maximum values are valid over: $f_{RF}$ = 1.5GHz to 2GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 1.75GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum gain | *18.3* | 19.7 | | dBm |
| | $OP1dB_2$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 5dB, DSA3 = 0dB | 17.8 | 19.5 | | |
| | $OP1dB_3$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 10dB, DSA3 = 0dB | 17.8 | 19.6 | | |
| | $OP1dB_4$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 15dB, DSA3 = 0dB | 15.6 | 18.3 | | |
| | $OP1dB_5$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 25dB, DSA3 = 0dB | 7 | 9.1 | | |
| OP1dB Variation Over Temperature | $OP1dB_{TEMP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | +0.4/ -0.7 | | dB |

| Parameter | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Output 1dB Compression Bypass Mode | $OP1dB_{BYP}$ | Minimum and maximum values are valid over: $f_{RF}$ = 1.5GHz to 2GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 1.75GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | 18.8 | 19.9 | | dBm |
| OP1dB Bypass Mode Variation Over Temperature | $OP1dB_{TEMP_BYP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | +0.3/ -0.6 | | dB |
| Reverse Isolation | $ISO_{REV1}$ | Maximum gain, Non-Bypass mode. | | 43 | 45 | | dB |
| | $ISO_{REV2}$ | Maximum gain, Bypass mode. | | 24 | 26.4 | | |
| | $ISO_{REV3}$ | Minimum gain, Non-Bypass mode. | | 74.9 | 77.6 | | |
| | $ISO_{REV4}$ | Minimum gain, Bypass mode. | | 70.7 | 77 | | |
| Channel-to-Channel Isolation [c] | $ISO_{CH-CH1}$ | Maximum gain on both channels. | | 44 | 51 | | dB |
| | $ISO_{CH-CH2}$ | Minimum gain on both channels, Bypass OFF. | | | 50 | | |
| | $ISO_{CH-CH3}$ | Ch A: Max Gain<br>Ch B: Note [d] | | | 38 | | |
| | $ISO_{CH-CH4}$ | Ch A: Note [d]<br>Ch B: Max Gain | | | 38 | | |
| | $ISO_{CH-CH5}$ | Ch A: Min Gain<br>Ch B: Note [e] | | | 38 | | |
| | $ISO_{CH-CH6}$ | Ch A: Note [e]<br>Ch B: Min Gain | | | 38 | | |
| DSA Attenuation Error (INL)[f] | $ERR_{DSA0ABS}$ | Minimum and maximum values are valid over: $f_{RF}$ = 1.5GHz to 2GHz, $T_{EPAD}$ = -40°C to +105°C $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 1.75GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | DSA1, DSA2, DSA3 = 0dB DSA0 = 6dB | | ±0.3 | | dB |
| | $ERR_{DSA1ABS}$ | | DSA0, DSA2, DSA3 = 0dB DSA1 = 6dB | | ±0.3 | | |
| | $ERR_{DSA2ABS}$ | | DSA0, DSA1, DSA3 = 0dB DSA2 = 5dB | | -0.4 | | |
| | | | DSA0, DSA1, DSA3 = 0dB DSA2 = 10dB | | -0.5 | | |
| | | | DSA0, DSA1, DSA3 = 0dB DSA2 = 15dB | | -0.4 | | |
| | | | DSA0, DSA1, DSA3 = 0dB DSA2 = 20dB | | -0.6 | | |
| | | | DSA0, DSA1, DSA3 = 0dB DSA2 = 25dB | | -0.7 | | |
| | $ERR_{DSA3ABS}$ | | DSA0, DSA1, DSA2 = 0dB DSA3 = 6dB | | 0.1 | | |
| | | | DSA0, DSA1, DSA2 = 0dB DSA3 = 12dB | | 0.1 | | |
| | | | DSA0, DSA1, DSA2 = 0dB DSA3 = 18dB | | 0.1 | | |

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| DSA2 Step Error (DNL)[f] | $ERR_{DSA2SE}$ | Between adjacent states. | | ±0.3 | | dB |
| DSA3 Step Error (DNL)[f] | $ERR_{DSA3SE}$ | Between adjacent states. | | ±0.3 | | |
| Relative Phase DSA0 | $\Phi_{DSA0REL}$ | Any state, relative to 0dB attenuation state. | | 3 | | deg |
| Relative Phase DSA1 | $\Phi_{DSA1REL}$ | Any state, relative to 0dB attenuation state. | | 3 | | |
| Phase Deviation DSA2 | $\Phi_{DSA2ADJ}$ | Between adjacent states. | | 2.5 | | |
| Relative Phase DSA2 | $\Phi_{DSA2RELMAX}$ | DSA set to 29dB, relative to 0dB attenuation state. | | 16 | | |
| | $\Phi_{DSA2RELMID}$ | DSA set to 14dB, relative to 0dB attenuation state. | | 6.5 | | |
| Relative Phase DSA3 | $\Phi_{DSA3REL}$ | Any state, relative to 0dB attenuation state. | | 13 | | |

[a] Specifications in the minimum/maximum columns that are shown in bold italics are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] 1dB compression point is a linearity figure of merit. Refer to Abs Max Ratings table for maximum RF input power.

[c] Signal applied to RFIN_A (RFIN_B) and measure desired signal at RFOUT_B (RFOUT_A) and compare to signal level at RFOUT_A (RFOUT_B).

[d] Channel A or Channel B DSA combinations which yield 24dB in total attenuation. DSA2_A or DSA2_B settings limited to the following: 0dB, 6dB, 12dB, 18dB, and 24dB.

[e] Channel A or Channel B DSA combinations yielding 35dB in total attenuation. DSA2_A or DSA2_B settings limited to the following: 5dB, 11dB, 17dB, 23dB, and 29dB. Since the maximum attenuation state totals 59dB, this will yield a 24dB difference between the two channels.

[f] The attenuators can be assumed to be purely resistive elements when performing cascaded analysis calculations. Be sure to take into account any relevant INL/DNL effects.

## Table 7. Electrical Characteristics – High Band (2.3GHz to 2.7GHz) Performance

See the F0443 Typical Application Circuit. Specifications apply when operated as a Dual DVGA. Typical data is with $V_{CC}$ = +5.0V, $f_{RF}$ = 2.5GHz, $T_{EPAD}$ = +25°C, minimum and maximum data is over $f_{RF}$ = 2.3GHz to 2.7GHz and $T_{EPAD}$ = -40°C to +105°C, STBY_A = STBY_B = logic LOW, $Z_S = Z_L = 50\Omega$, maximum gain setting (all DSAs set to 0dB attenuation), Tone Spacing = 1MHz, Pout = 0dBm/Tone, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

| Parameter | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| RF Input Return Loss | $RL_{IN}$ | Worst case typical, $T_{EPAD}$ = 25°C, $f_{RF}$ = 2.3GHz to 2.7GHz. | | | 13.7 | | dB |
| | | Worst case typical, $T_{EPAD}$ = 105°C, $f_{RF}$ = 2.3GHz to 2.7GHz. | | | 12 | | |
| RF Output Return Loss | $RL_{OUT}$ | Worst case typical, $T_{EPAD}$ = 25°C, $f_{RF}$ = 2.3GHz to 2.7GHz. | | | 12 | | dB |
| | | Worst case typical, $T_{EPAD}$ = 105°C, $f_{RF}$ = 2.3GHz to 2.7GHz. | | | 12 | | |
| Gain Non-Bypass Mode | $G_{MAX}$ | Minimum and maximum values are valid over: $f_{RF}$ = 2.3GHz to 2.7GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 2.5GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | *26.4* [a, f] | 30.1 | *33* | dB |
| | $G_1$ | | DSA0, = 0dB, DSA1 = 0dB, DSA2 = 5dB, DSA3 = 0dB | 21.6 | 25 | 28 | |
| | $G_2$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 10dB, DSA3 = 0dB | 16.6 | 20 | 23 | |
| | $G_3$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 15dB, DSA3 = 0dB | 11.5 | 14.5 | 17 | |
| | $G_4$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 25dB, DSA3 = 0dB | 1.6 | 5 | 8.5 | |
| Gain Non-Bypass Mode Variation Over Temperature | $G_{TEMP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | +1.0/ -1.5 | | dB |
| Gain Non-Bypass Mode Flatness | $G_{FLAT}$ | Gain Flatness. Any fixed temperature. Any 200MHz bandwidth within $f_{RF}$ = 2.3GHz to 2.7GHz. | | | 0.3 | | dB |
| Gain Bypass Mode | $G_{BYP}$ | Minimum and maximum values are valid over: $f_{RF}$ = 2.3GHz to 2.7GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 2.5GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | *6.4* | 9.2 | *12* | dB |
| Gain Bypass Mode Variation Over Temperature | $G_{TEMP_BYP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | +0.8/ -1.0 | | dB |
| Gain Bypass Mode Flatness | $G_{FLAT_BYP}$ | Gain Flatness. Any fixed temperature. Any 200MHz bandwidth within $f_{RF}$ = 2.3GHz to 2.7GHz. | | | 0.6 | | dB |
| Noise Figure Non-Bypass Mode | $NF_{MAX}$ | Minimum and maximum values are valid over: $f_{RF}$ = 2.3GHz to 2.7GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at: $f_{RF}$ = 2.5GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | | 3.6 | 5.1 | dB |
| | $NF_1$ | | DSA0, = 0dB, DSA1 = 0dB, DSA2 = 5dB, DSA3 = 0dB | | 4 | 5.8 | |
| | $NF_2$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 10dB, DSA3 = 0dB | | 5.1 | 7.3 | |
| | $NF_3$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 15dB, DSA3 = 0dB | | 7.5 | 10.4 | |
| | $NF_4$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 25dB, DSA3 = 0dB | | 15.4 | 19.2 | |

| Parameter | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| NF Non-Bypass Mode Variation Over Temperature | $NF_{TEMP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | -0.7/ +0.9 | | dB |
| Noise Figure Bypass Mode | $NF_{BYP}$ | Minimum and maximum values are valid over $f_{RF}$ = 2.3GHz to 2.7GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at $f_{RF}$ = 2.5GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | | 10 | 13.3 | dB |
| NF Bypass Mode Variation Over Temperature | $NF_{TEMP_BYP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | -1.3/ +1.8 | | dB |
| Output Third Order Intercept Point | $OIP3_1$ | Tone Spacing = 1MHz Pout = 0dBm/Tone, Pout = -10dBm/Tone at DSA2 = 25dB Attenuation | Maximum gain | 33.4 | 40 | | dBm |
| | $OIP3_2$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 5dB, DSA3 = 0dB | 32 | 40 | | |
| | $OIP3_3$ | Minimum and maximum values are valid over $f_{RF}$ = 2.3GHz to 2.7GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at $f_{RF}$ = 2.5GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 10dB, DSA3 = 0dB | 31.2 | 39.6 | | |
| | $OIP3_4$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 15dB, DSA3 = 0dB | 28.7 | 37.9 | | |
| | $OIP3_5$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 25dB, DSA3 = 0dB | 19 | 27 | | |
| OIP3 Variation Over Temperature | $OIP3_{TEMP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | -1.9/ +0.2 | | dB |
| Output Third Order Intercept Point Bypass Mode | $OIP3_{BYP}$ | Minimum and maximum values are valid over $f_{RF}$ = 2.3GHz to 2.7GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at $f_{RF}$ = 2.5GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | 33.6 | 39 | | dB |
| OIP3 Bypass Mode Variation Over Temperature | $OIP3_{TEMP_BYP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | -2.2/ +2.0 | | dB |
| Output 1dB Compression Non-Bypass Mode[b] | $OP1dB_1$ | Minimum and maximum values are valid over $f_{RF}$ = 2.3GHz to 2.7GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at $f_{RF}$ = 2.5GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum gain | *17.6* | 19.2 | | dBm |
| | $OP1dB_2$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 5dB, DSA3 = 0dB | 17.6 | 19.2 | | |
| | $OP1dB_3$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 10dB, DSA3 = 0dB | 17.4 | 19.2 | | |
| | $OP1dB_4$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 15dB, DSA3 = 0dB | 15.5 | 17.8 | | |
| | $OP1dB_5$ | | DSA0 = 0dB, DSA1 = 0dB, DSA2 = 25dB, DSA3 = 0dB | 4 | 7.7 | | |
| OP1dB Variation Over Temperature | $OP1dB_{TEMP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | +0.5/ -0.8 | | dB |

| Parameter | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Output 1dB Compression Bypass Mode | $OP1dB_{BYP}$ | Minimum and maximum values are valid over $f_{RF}$ = 2.3GHz to 2.7GHz, $T_{EPAD}$ = -40°C to +105°C, $V_{CC}$ = 4.75V to 5.25V Typical values valid at $f_{RF}$ = 2.5GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | Maximum Gain | 16.8 | 19.5 | | dBm |
| OP1dB Bypass Mode Variation Over Temperature | $OP1dB_{TEMP_BYP}$ | $T_{EPAD}$ = -40ºC to +105ºC. | | | +0.4/ -0.8 | | dB |
| Reverse Isolation | $ISO_{REV1}$ | Maximum gain, Non-Bypass mode. | | 42 | 44.3 | | dB |
| | $ISO_{REV2}$ | Maximum gain, Bypass mode. | | 24 | 27.7 | | |
| | $ISO_{REV3}$ | Minimum gain, Non-Bypass mode. | | 69.5 | 72.4 | | |
| | $ISO_{REV4}$ | Minimum gain, Bypass mode. | | 65.4 | 71.4 | | |
| Channel-to-Channel Isolation [c] | $ISO_{CH-CH1}$ | Maximum gain on both channels. | | 46 | 53 | | dB |
| | $ISO_{CH-CH2}$ | Minimum gain on both channels, Bypass OFF. | | | 54 | | |
| | $ISO_{CH-CH3}$ | Ch A: Max Gain<br>Ch B: Note [d] | | | 38 | | |
| | $ISO_{CH-CH4}$ | Ch A: Note [d]<br>Ch B: Max Gain | | | 39 | | |
| | $ISO_{CH-CH5}$ | Ch A: Min Gain<br>Ch B: Note [e] | | | 37 | | |
| | $ISO_{CH-CH6}$ | Ch A: Note [e]<br>Ch B: Min Gain | | | 37 | | |
| DSA Attenuation Error (INL)[f] | $ERR_{DSA0ABS}$ | Minimum and maximum values are valid over $f_{RF}$ = 2.3GHz to 2.7GHz, $T_{EPAD}$ = -40°C to +105°C $V_{CC}$ = 4.75V to 5.25V Typical values valid at $f_{RF}$ = 2.5GHz, $T_{EPAD}$ = +25°C, $V_{CC}$ = 5V | DSA1, DSA2, DSA3 = 0dB DSA0 = 6dB | | ±0.3 | | dB |
| | $ERR_{DSA1ABS}$ | | DSA0, DSA2, DSA3 = 0dB DSA1 = 6dB | | ±0.3 | | |
| | $ERR_{DSA2ABS}$ | | DSA0, DSA1, DSA3 = 0dB DSA2 = 5dB | | -0.2 | | |
| | | | DSA0, DSA1, DSA3 = 0dB DSA2 = 10dB | | +0.1 | | |
| | | | DSA0, DSA1, DSA3 = 0dB DSA2 = 15dB | | +0.1 | | |
| | | | DSA0, DSA1, DSA3 = 0dB DSA2 = 20dB | | +0.2 | | |
| | | | DSA0, DSA1, DSA3 = 0dB DSA2 = 25dB | | -0.2 | | |
| | $ERR_{DSA3ABS}$ | | DSA0, DSA1, DSA2 = 0dB DSA3 = 6dB | | -0.1 | | |
| | | | DSA0, DSA1, DSA2 = 0dB DSA3 = 12dB | | -0.1 | | |
| | | | DSA0, DSA1, DSA2 = 0dB DSA3 = 18dB | | -0.1 | | |

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| DSA2 Step Error (DNL)[f] | $ERR_{DSA2SE}$ | Between adjacent states. | | ±0.3 | | dB |
| DSA3 Step Error (DNL)[f] | $ERR_{DSA3SE}$ | Between adjacent states. | | ±0.2 | | dB |
| Relative Phase DSA0 | $\Phi_{DSA0REL}$ | Any state, relative to 0dB attenuation state. | | 4 | | deg |
| Relative Phase DSA1 | $\Phi_{DSA1REL}$ | Any state, relative to 0dB attenuation state. | | 5 | | deg |
| Phase Deviation DSA2 | $\Phi_{DSA2ADJ}$ | Between adjacent states. | | 3 | | deg |
| Relative Phase DSA2 | $\Phi_{DSA2RELMAX}$ | DSA set to 29dB, relative to 0dB attenuation state. | | 16 | | deg |
| | $\Phi_{DSA2RELMID}$ | DSA set to 14dB, relative to 0dB attenuation state. | | 6 | | deg |
| Relative Phase DSA3 | $\Phi_{DSA3REL}$ | Any state, relative to 0dB attenuation state. | | 15 | | deg |

[a] Specifications in the minimum/maximum columns that are shown in bold italics are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] 1dB compression point is a linearity figure of merit. Refer to Abs Max Ratings table for maximum RF input power.

[c] Signal applied to RFIN_A (RFIN_B) and measure desired signal at RFOUT_B (RFOUT_A) and compare to signal level at RFOUT_A (RFOUT_B).

[d] Channel A or Channel B DSA combinations which yield 24dB in total attenuation. DSA2_A or DSA2_B settings limited to the following: 0dB, 6dB, 12dB, 18dB, and 24dB.

[e] Channel A or Channel B DSA combinations yielding 35dB in total attenuation. DSA2_A or DSA2_B settings limited to the following: 5dB, 11dB, 17dB, 23dB, and 29dB. Since the maximum attenuation state totals 59dB, this will yield a 24dB difference between the two channels.

[f] The attenuators can be assumed to be purely resistive elements when performing cascaded analysis calculations. Be sure to take into account any relevant INL/DNL effects.

# Thermal Characteristics

Table 8. Package Thermal Characteristics

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Junction to Ambient Thermal Resistance. | $\theta_{JA}$ | 16 | °C/W |
| Junction to Case Thermal Resistance.<br>(Case is defined as the exposed paddle) | $\theta_{JC\text{-}BOT}$ | 6 | °C/W |
| Moisture Sensitivity Rating (Per J-STD-020) | | MSL 3 | |

# Typical Operating Conditions (TOC)

Unless otherwise noted, for the TOC graphs on the following pages, the following conditions apply:

- $V_{CC}$ = +5V
- $T_{EPAD}$ = 25°C
- $Z_L = Z_S = 50\Omega$
- Small signal parameters measured with $P_{IN}$ = -35dBm
- ATTN setting = 0dB (Maximum Gain; DSA0 = DSA1 = DSA2 = DSA3 = 0dB)
- $P_{OUT}$ = 0dBm/tone
- All temperatures are referenced to the exposed paddle
- Evaluation Kit traces and connector losses are de-embedded

# Typical Performance Characteristics

Figure 3. Gain, All DSA = 0dB, Bypass OFF

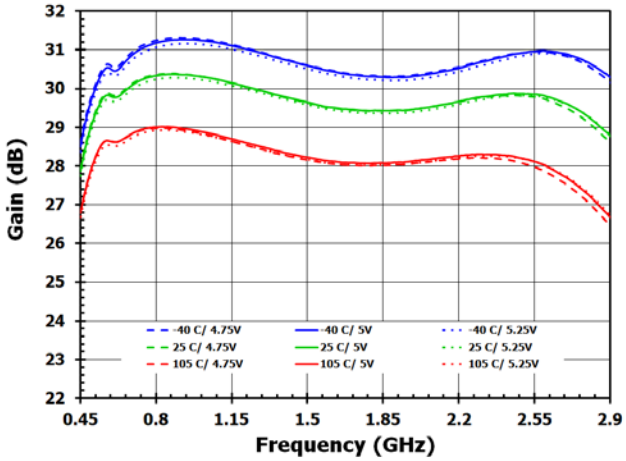



Figure 4. Gain, All DSA = 0dB, Bypass ON

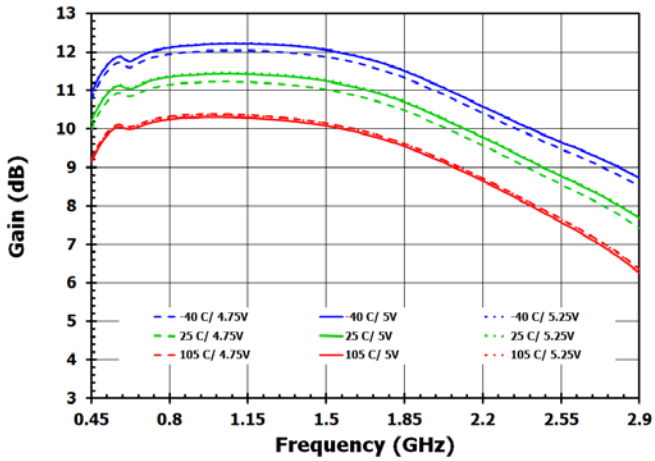



Figure 5. Gain, DSA0 = 6dB, Bypass OFF

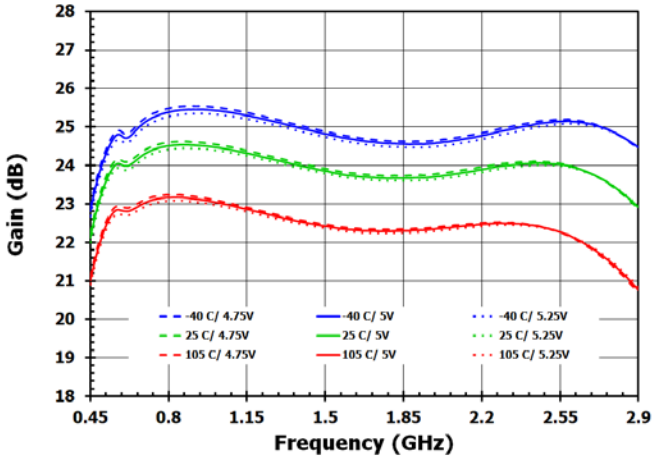



Figure 6. Gain, DSA0 = 6dB, Bypass ON

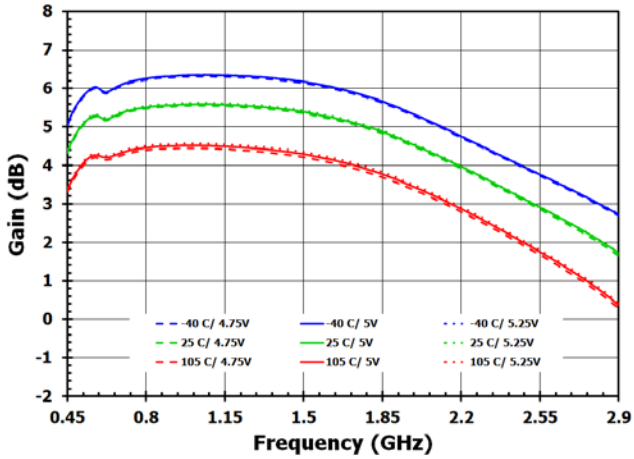



Figure 7. Gain, DSA1 = 6dB, Bypass OFF

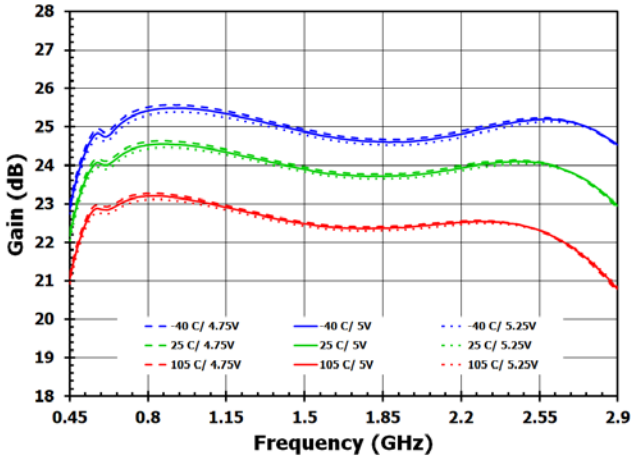



Figure 8. Gain, DSA1 = 6dB, Bypass ON

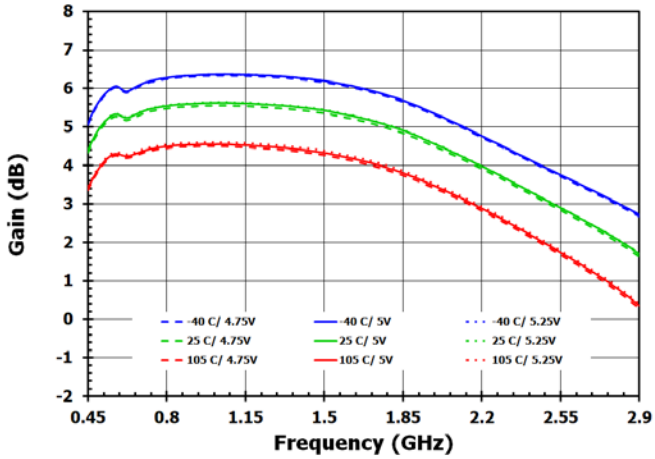


Figure 9. Gain, DSA2 = 5dB, Bypass OFF

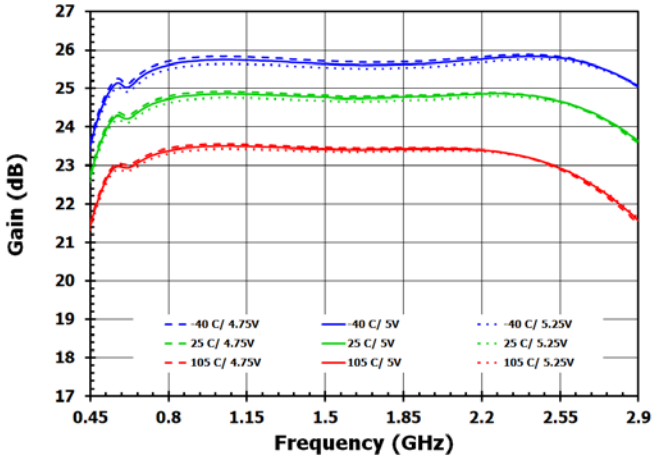



Figure 10. Gain, DSA2 = 5dB, Bypass ON

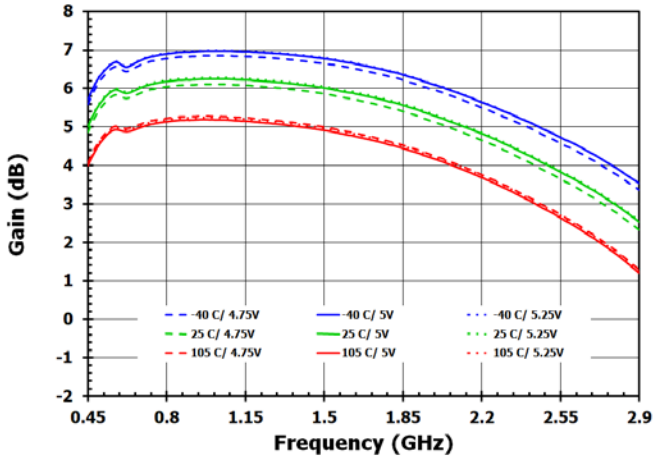



Figure 11. Gain, DSA2 = 10dB, Bypass OFF

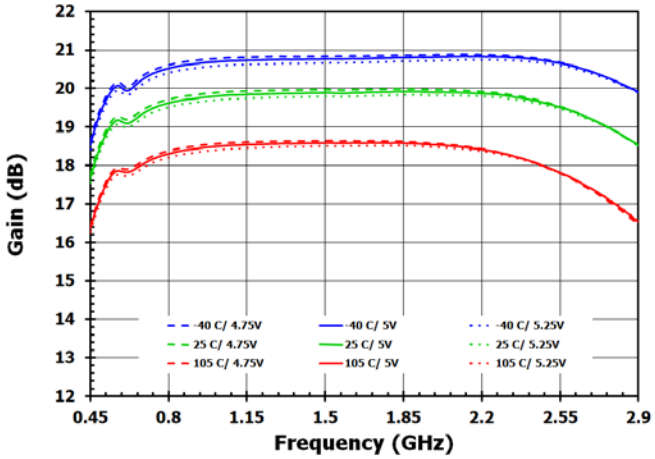



Figure 12. Gain, DSA2 = 10dB, Bypass ON

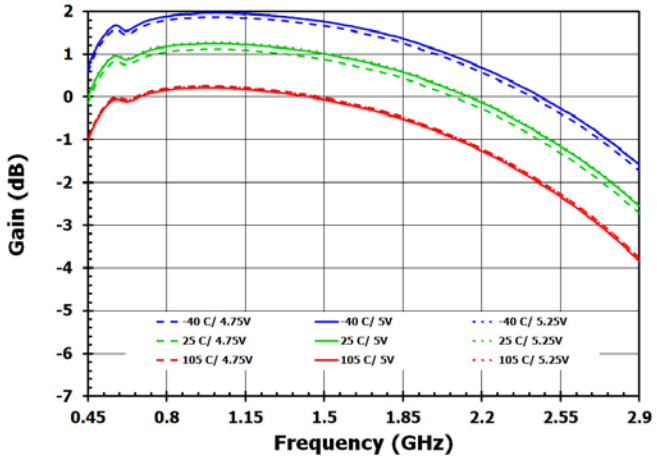



Figure 13. Gain, DSA2 = 15dB, Bypass OFF

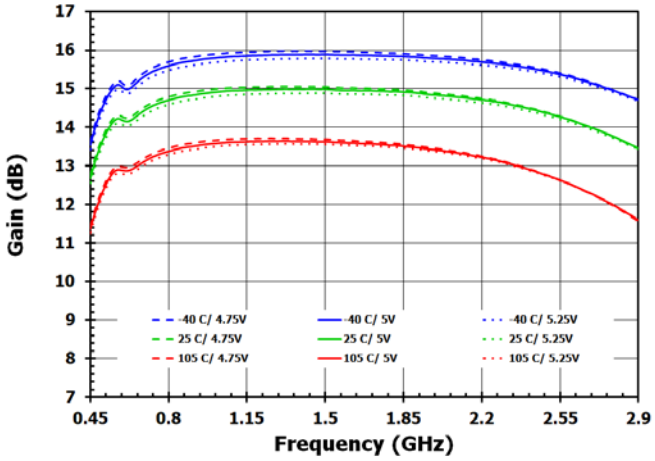



Figure 14. Gain, DSA2 = 15dB, Bypass ON

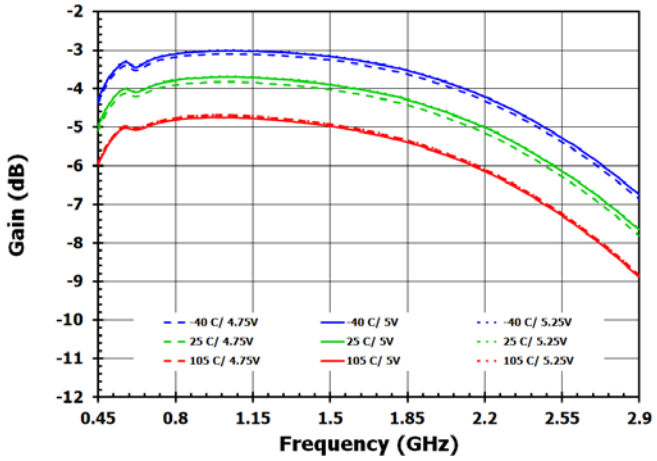


Figure 15. Gain, DSA2 = 25dB, Bypass OFF

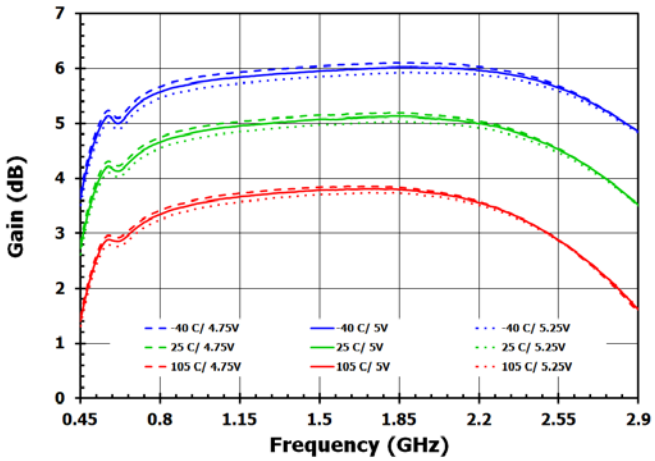



Figure 16. Gain, DSA2 = 25dB, Bypass ON

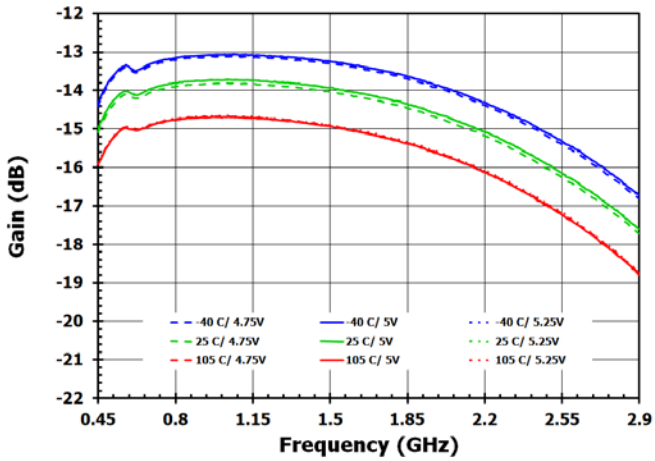



Figure 17. Gain, DSA3 = 6dB, Bypass OFF

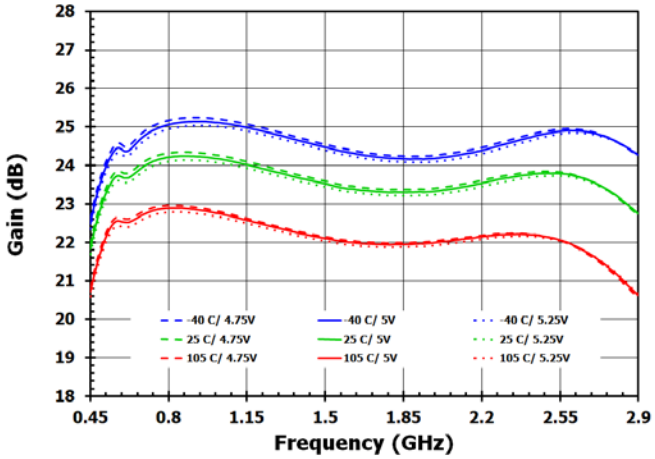



Figure 18. Gain, DSA3 = 6dB, Bypass ON

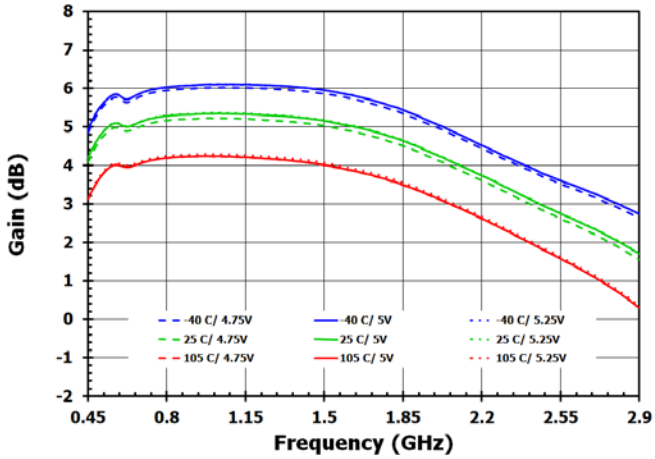



Figure 19. Gain, DSA3 = 12dB, Bypass OFF

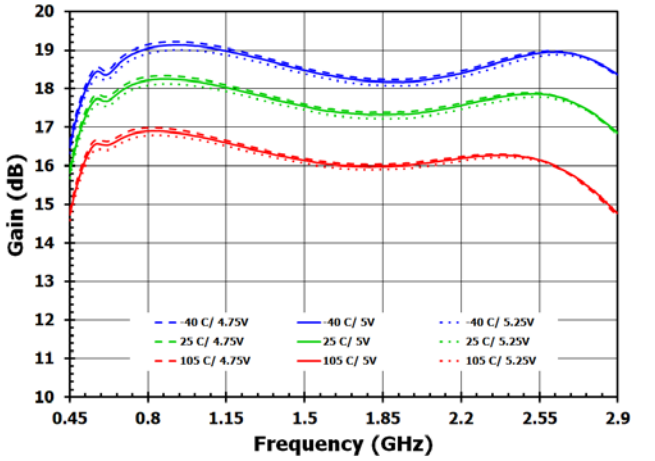



Figure 20. Gain, DSA3 = 12dB, Bypass ON

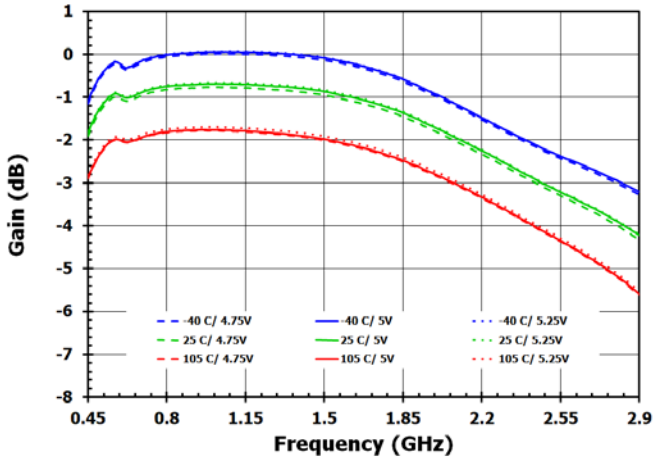


Figure 21. Gain, DSA3 = 18dB, Bypass OFF

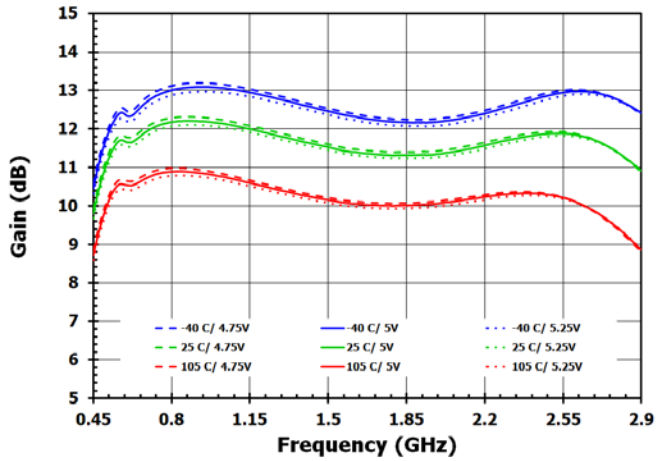



Figure 22. Gain, DSA3 = 18dB, Bypass ON

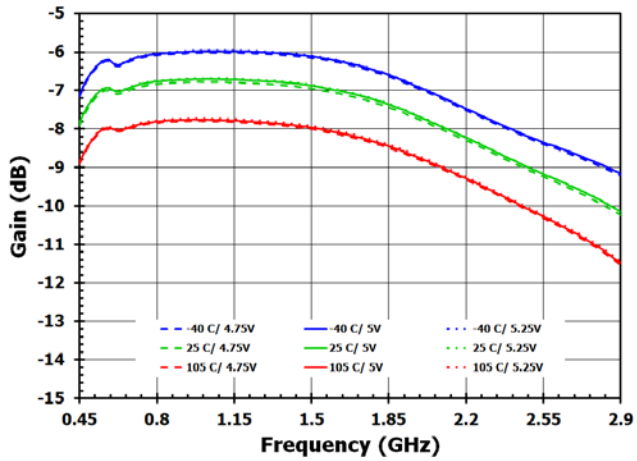



Figure 23. Relative Gain Error, DSA0 = 6dB, Bypass OFF

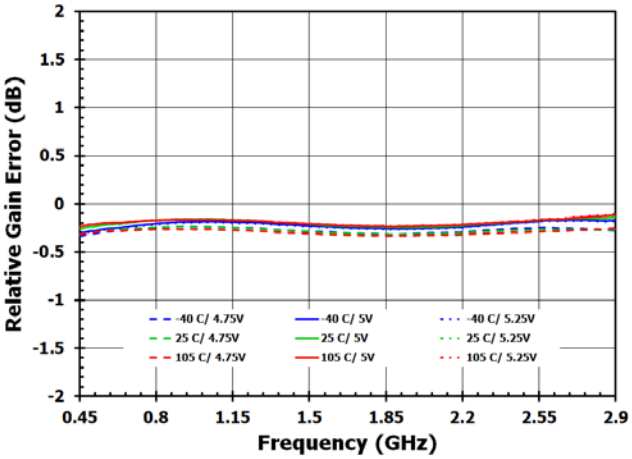



Figure 24. Relative Gain Error, DSA1 = 6dB, Bypass OFF

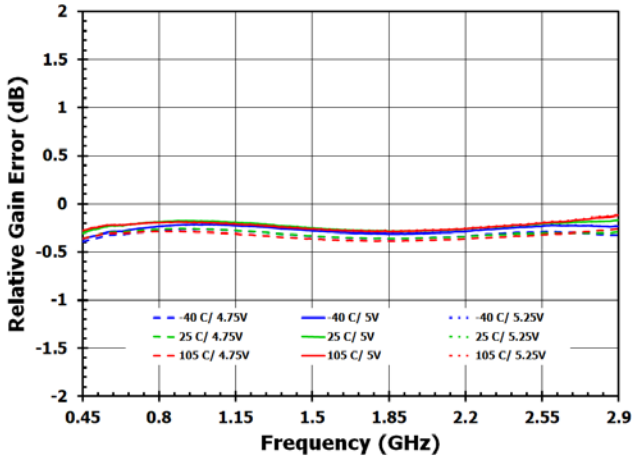



Figure 25. Relative Gain Error, DSA2 = 5dB, Bypass OFF

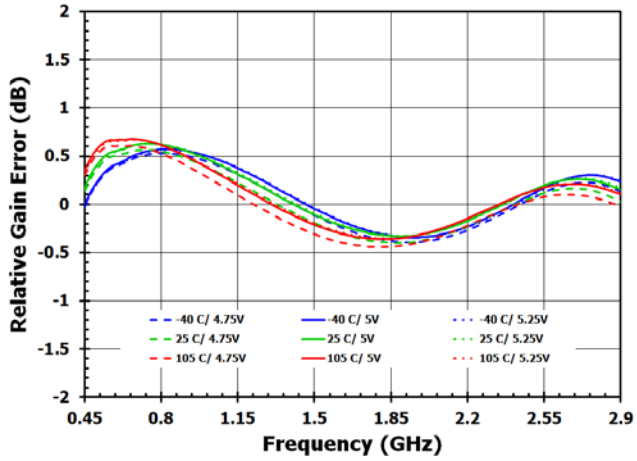



Figure 26. Relative Gain Error, DSA2 = 10dB, Bypass OFF

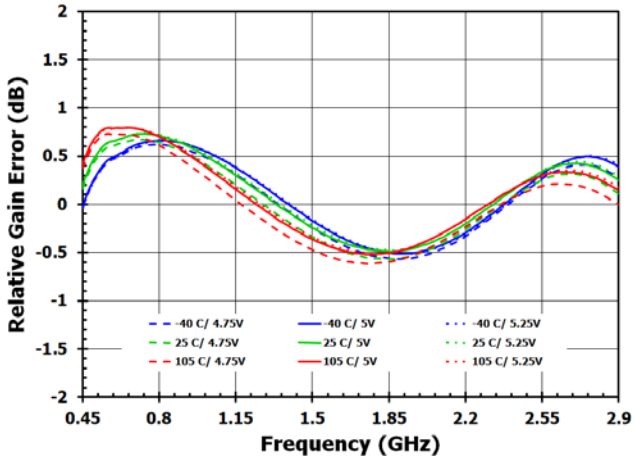


Figure 27. Relative Gain Error, DSA2 = 15dB, Bypass OFF

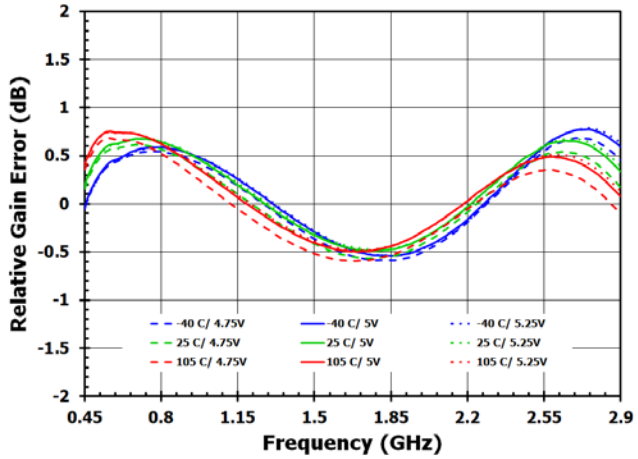



Figure 28. Relative Gain Error, DSA2 = 25dB, Bypass OFF

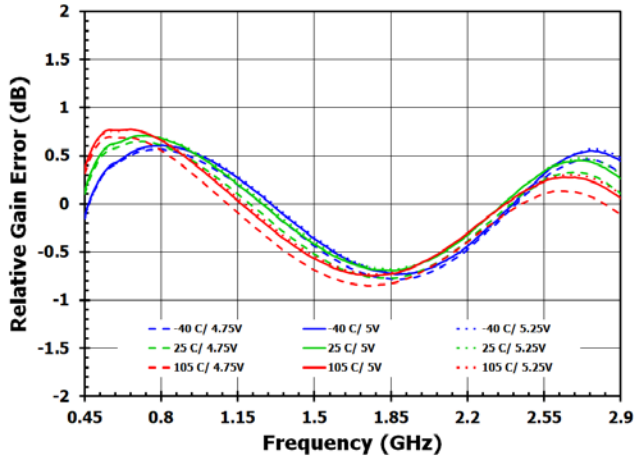



Figure 29. Relative Gain Error, DSA3 = 6dB, Bypass OFF

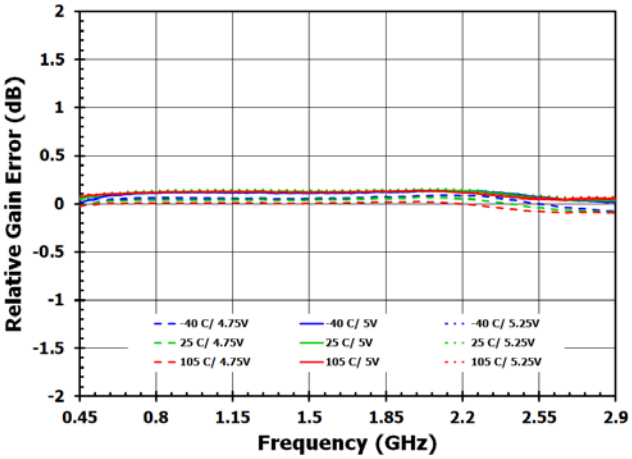



Figure 30. Relative Gain Error, DSA3 = 12dB, Bypass OFF

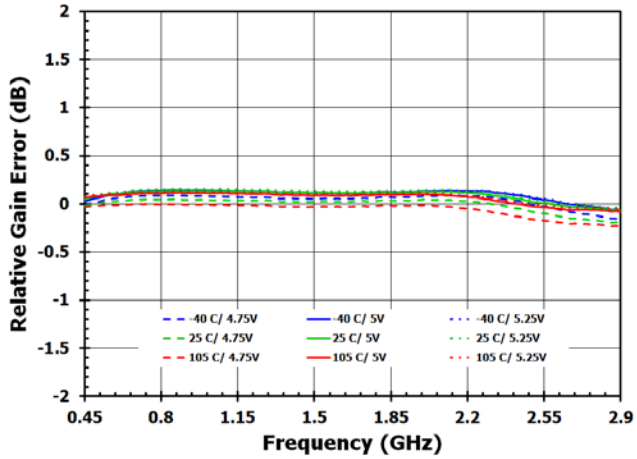



Figure 31. Relative Gain Error, DSA3 = 18dB, Bypass OFF

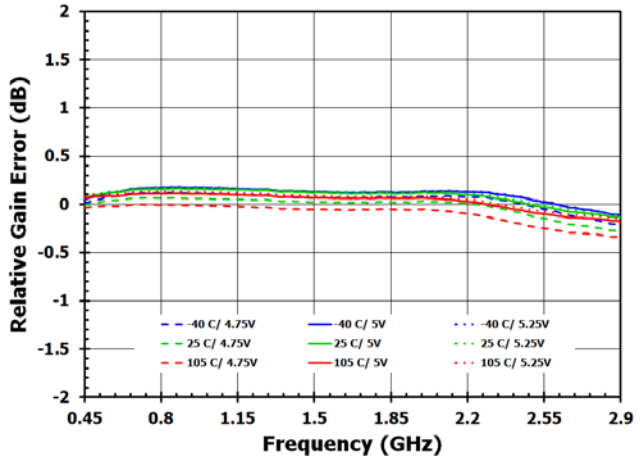



Figure 32. Gain, All DSA2 Attenuation Settings, Bypass OFF, 25°C

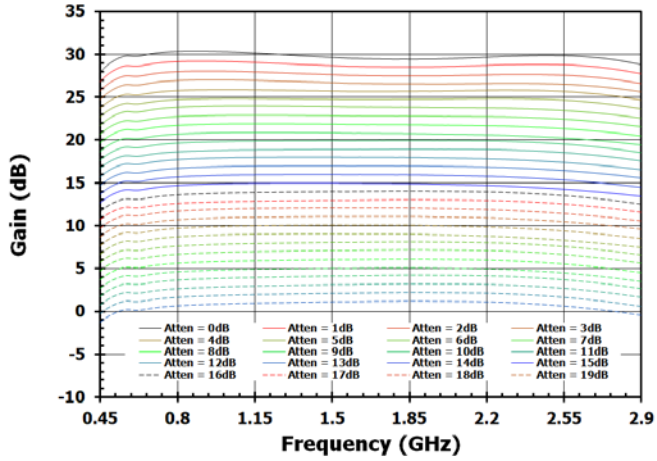


Figure 33. Gain, All DSA2 Attenuation Settings, Bypass ON, 25°C

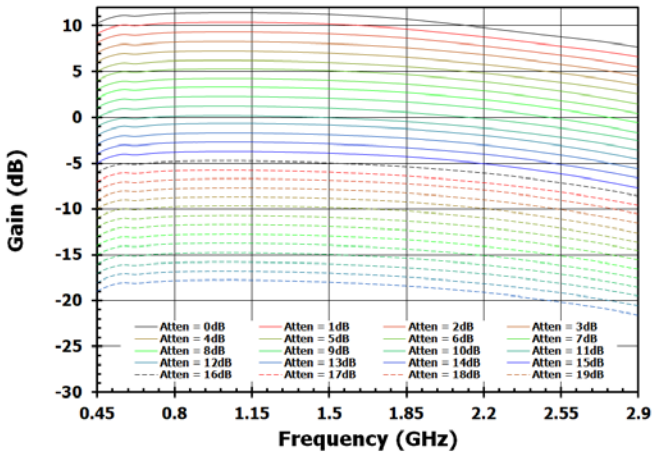



Figure 34. DSA2 INL (Absolute Attenuation Error) Bypass OFF

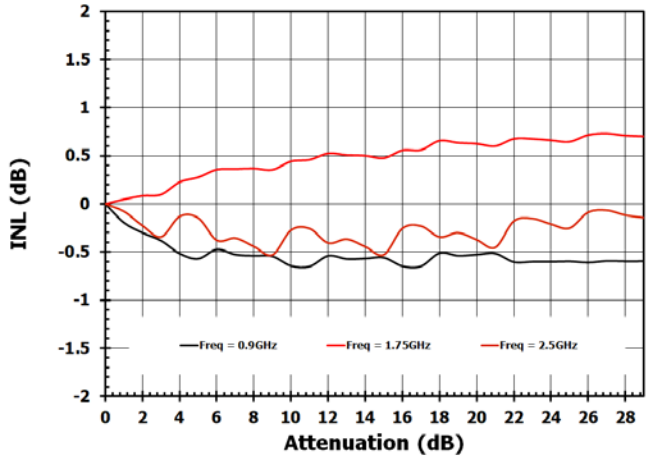



Figure 35. DSA2 DNL (Step Attenuation Error) Bypass OFF

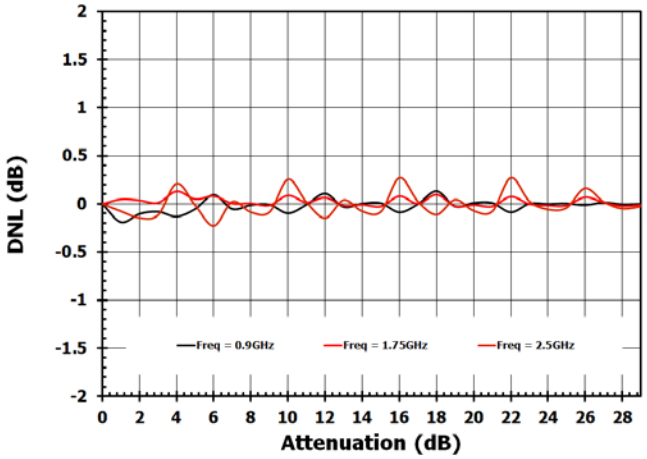



Figure 36. DSA2 INL (Absolute Attenuation Error) Bypass ON

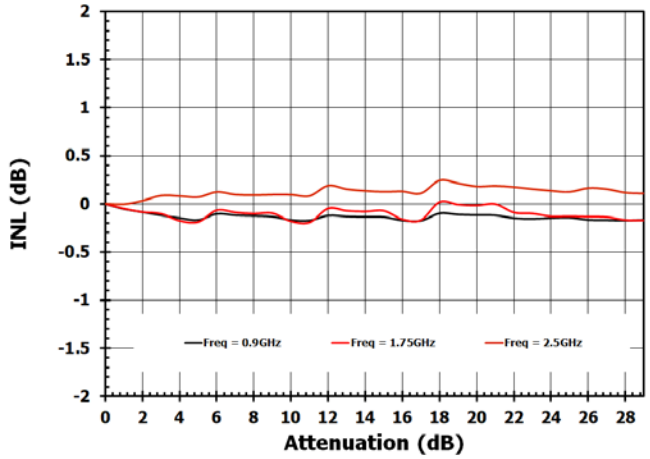



Figure 37. DSA2 DNL (Step Attenuation Error) Bypass ON

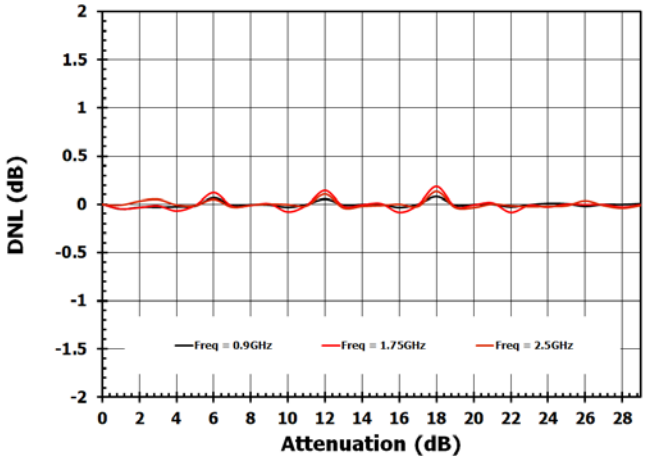



Figure 38. Gain, All DSA3 Attenuation Settings, Bypass OFF, 25°C

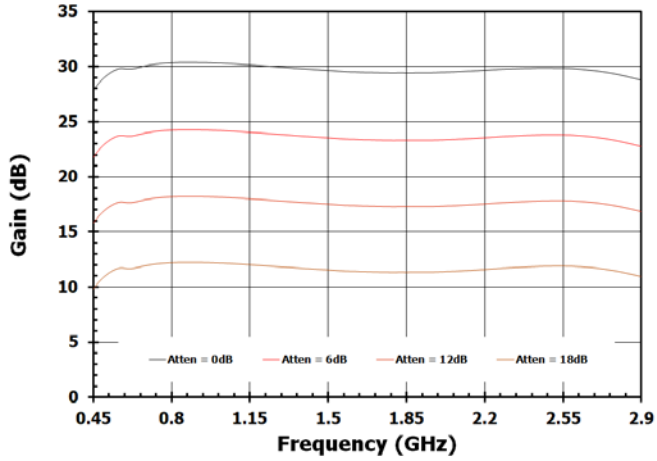


Figure 39. Gain, All DSA3 Attenuation Settings, Bypass ON, 25°C

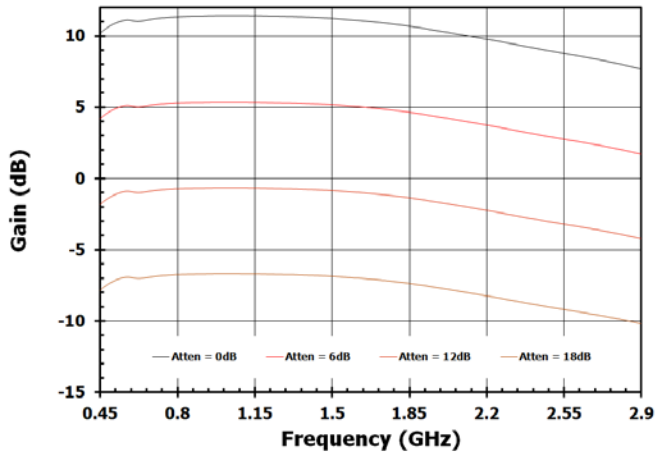



Figure 40. DSA3 INL (Absolute Attenuation Error) Bypass OFF

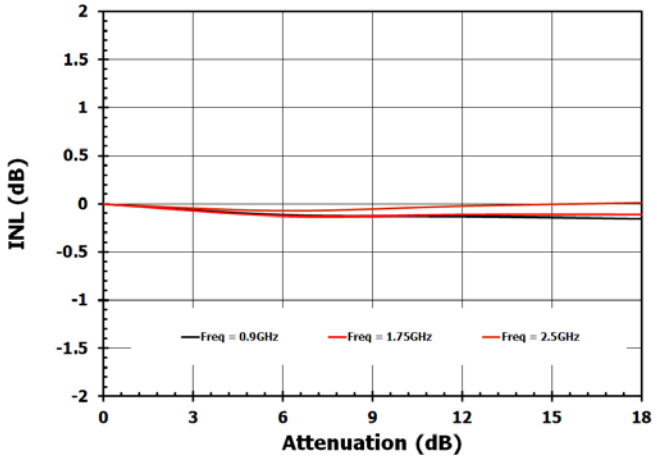



Figure 41. DSA3 DNL (Step Attenuation Error) Bypass OFF

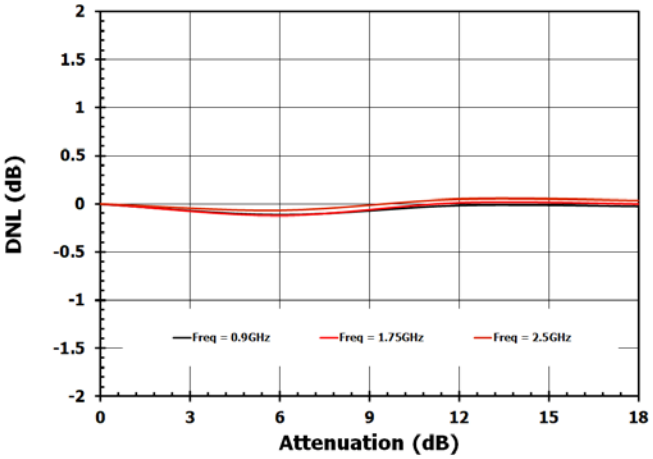



Figure 42. DSA3 INL (Absolute Attenuation Error) Bypass ON

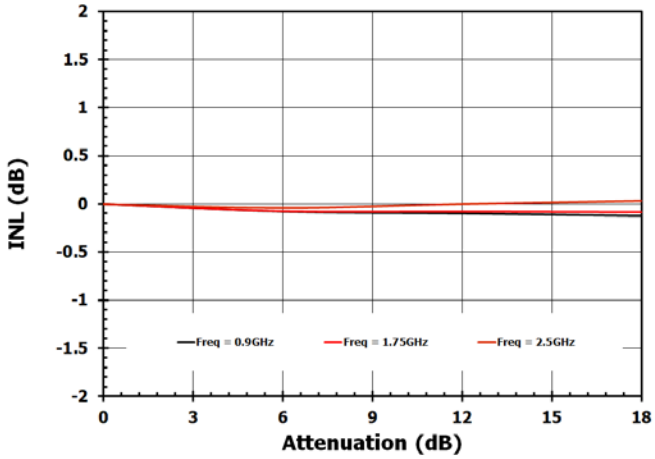



Figure 43. DSA3 DNL (Step Attenuation Error) Bypass ON

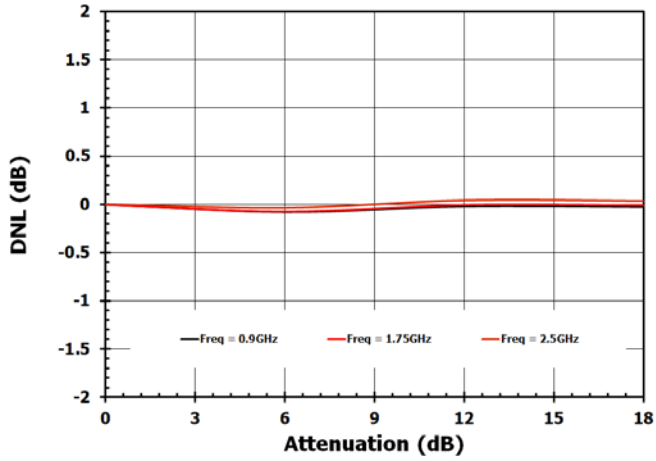



Figure 44. S11, All DSA = 0dB, Bypass OFF

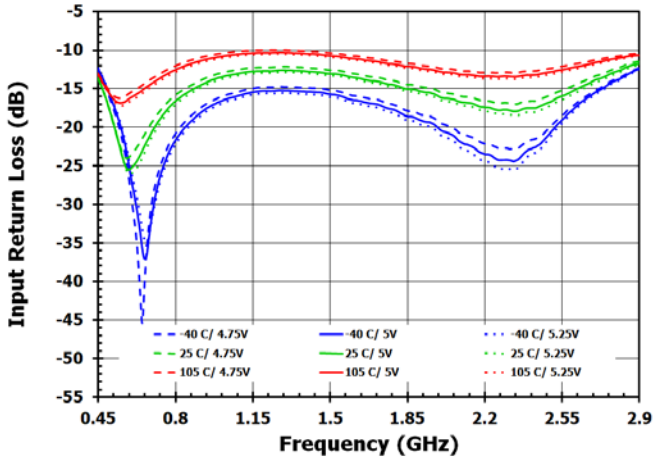


Figure 45. S11, All DSA = 0dB, Bypass ON

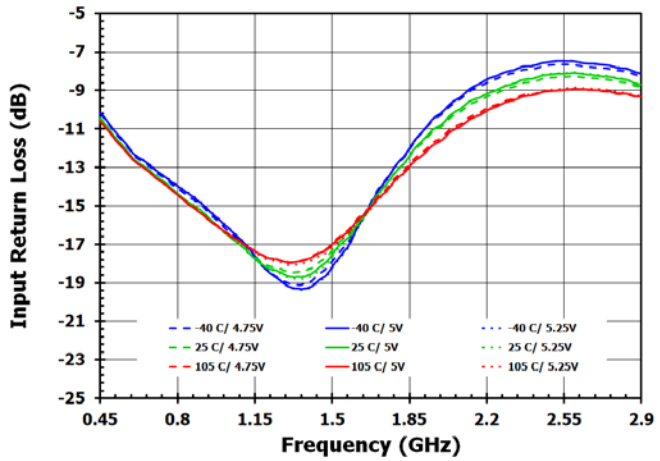



Figure 46. S11, DSA0 = 6dB, Bypass OFF

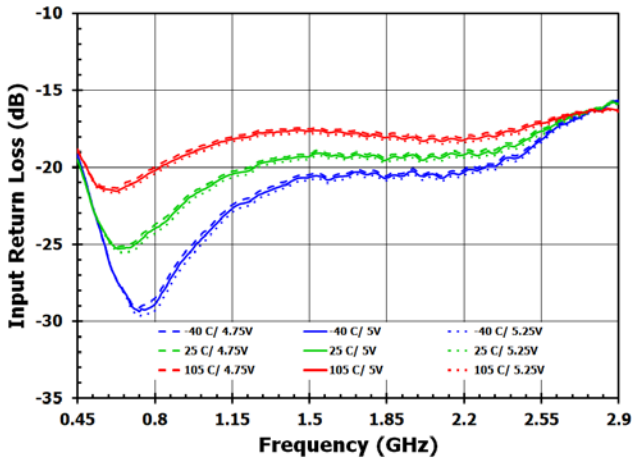



Figure 47. S11, DSA0 = 6dB, Bypass ON

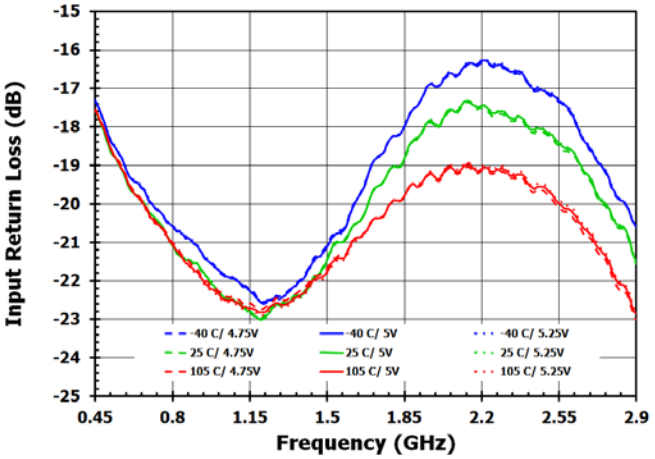



Figure 48. S11, DSA1 = 6dB, Bypass OFF

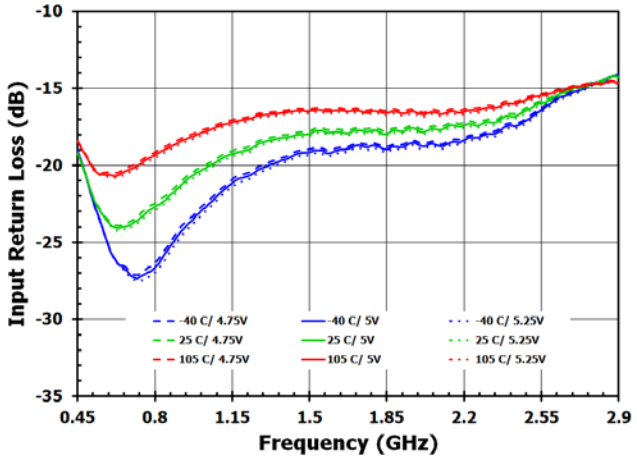



Figure 49. S11, DSA1 = 6dB, Bypass ON

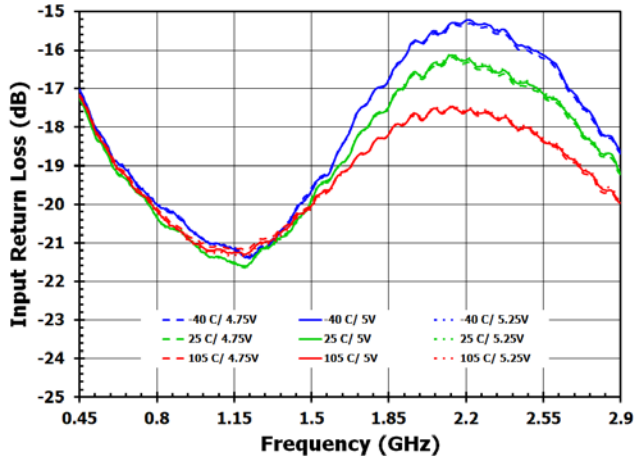



Figure 50. S11, DSA2 = 5dB, Bypass OFF

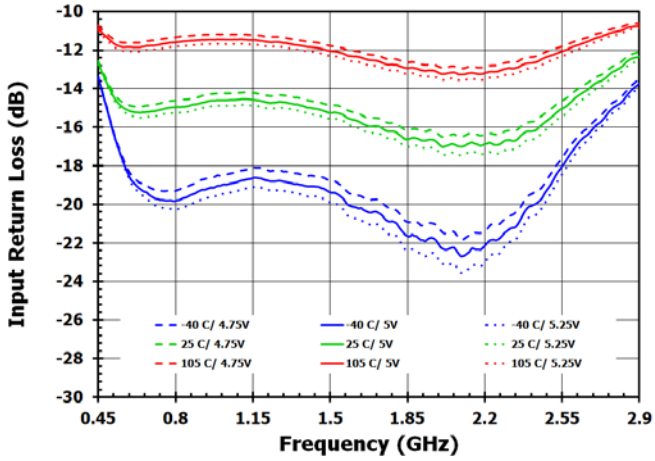


Figure 51. S11, DSA2 = 5dB, Bypass ON

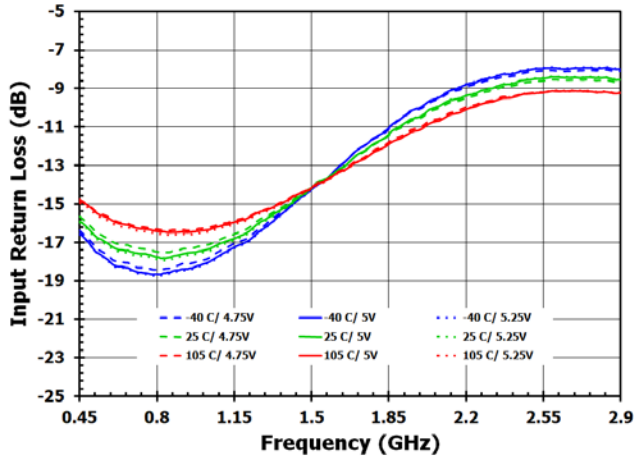



Figure 52. S11, DSA2 = 10dB, Bypass OFF

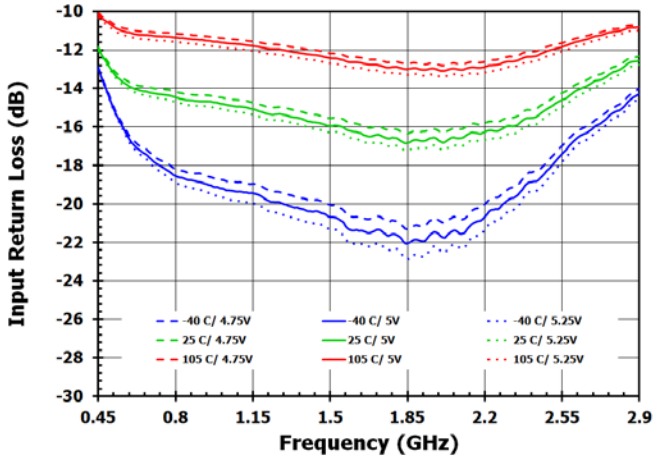



Figure 53. S11, DSA2 = 10dB, Bypass ON

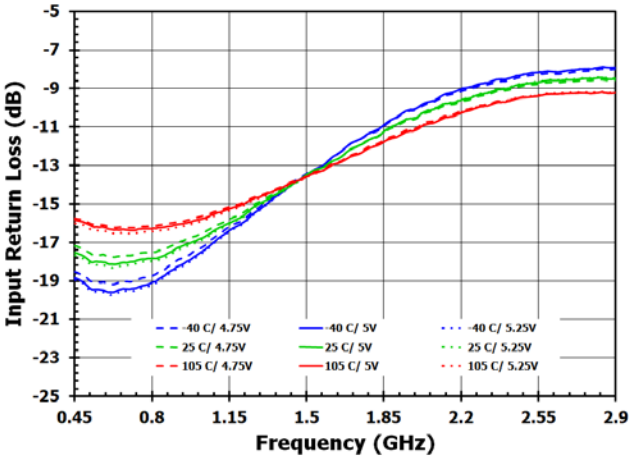



Figure 54. S11, DSA2 = 15dB, Bypass OFF

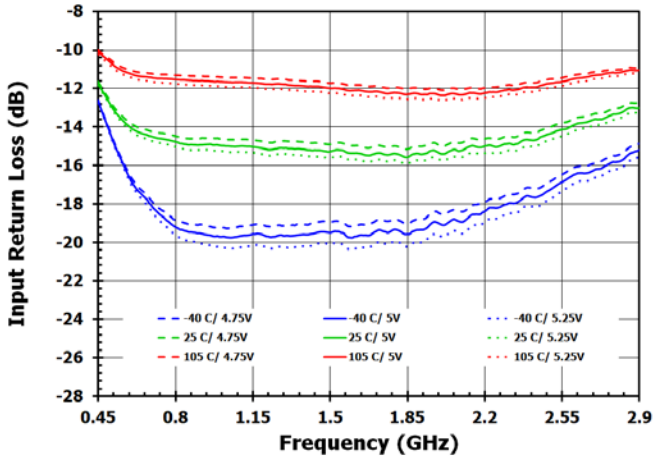



Figure 55. S11, DSA2 = 15dB, Bypass ON

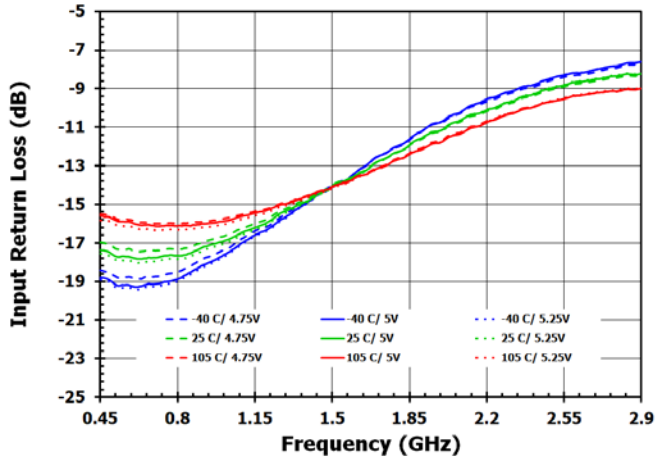



Figure 56. S11, DSA2 = 25dB, Bypass OFF

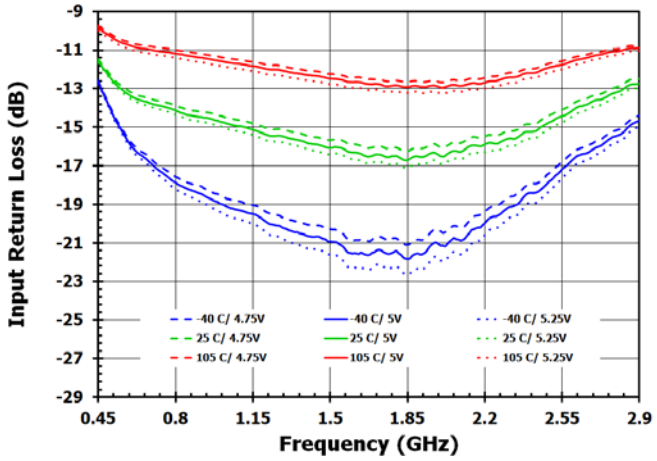


Figure 57. S11, DSA2 = 25dB, Bypass ON

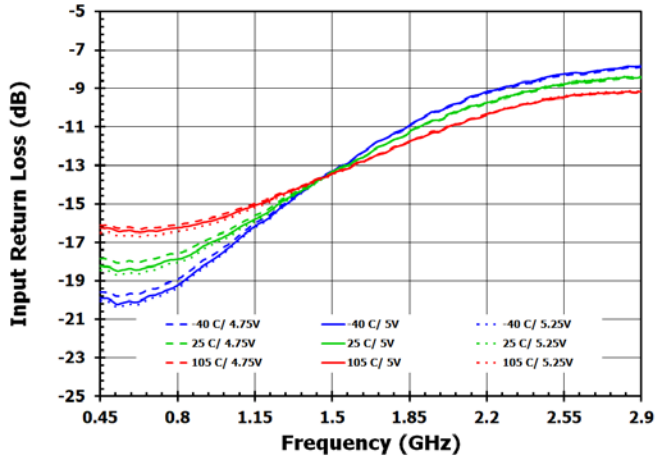



Figure 58. S11, DSA3 = 6dB, Bypass OFF

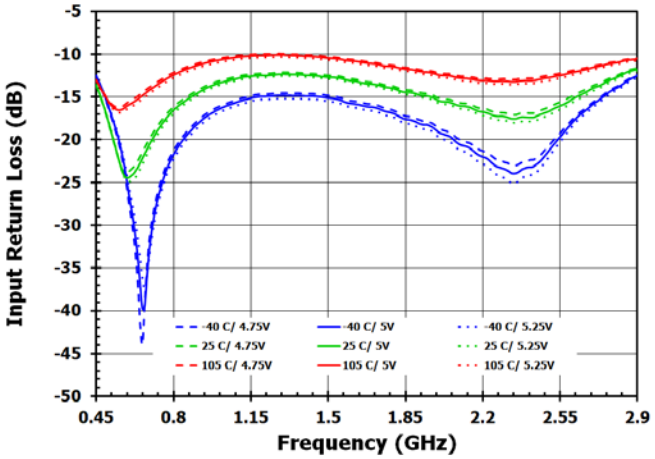



Figure 59. S11, DSA3 = 6dB, Bypass ON

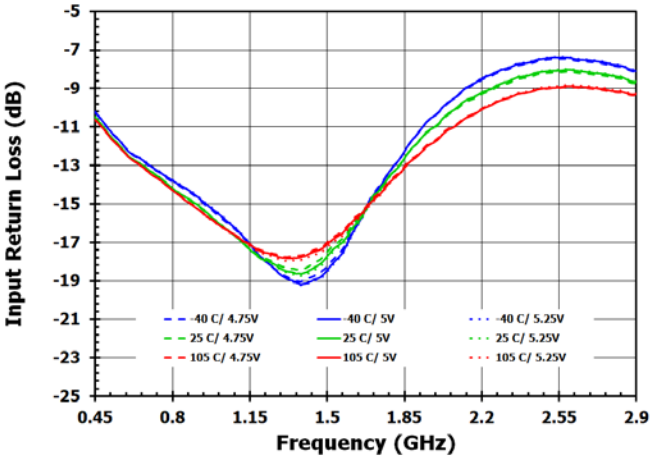



Figure 60. S11, DSA3 = 12dB, Bypass OFF

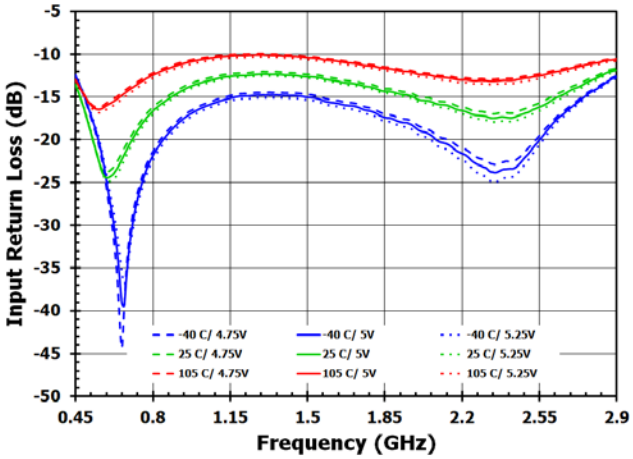



Figure 61. S11, DSA3 = 12dB, Bypass ON

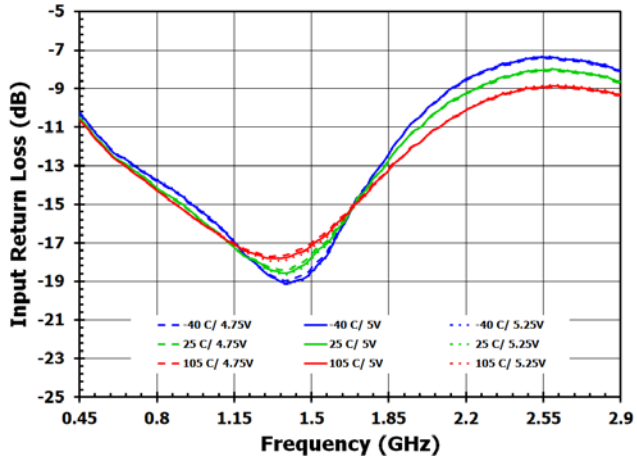



Figure 62. S11, DSA3 = 18dB, Bypass OFF

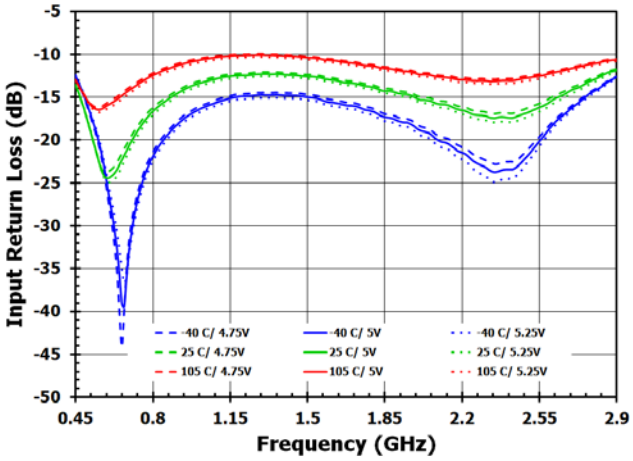


Figure 63. S11, DSA3 = 18dB, Bypass ON

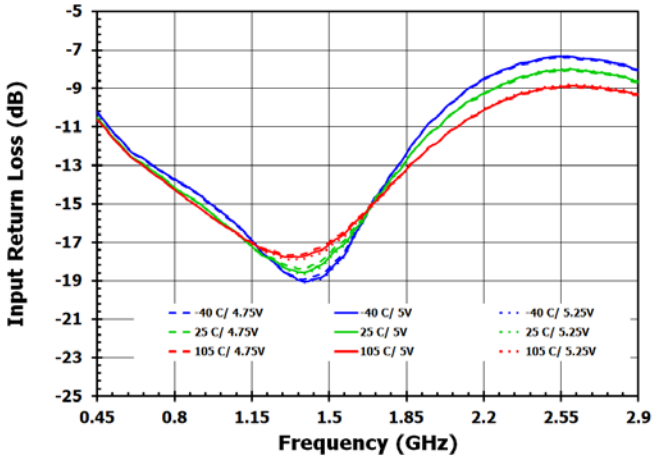



Figure 64. S22, All DSAs = 0dB, Bypass OFF

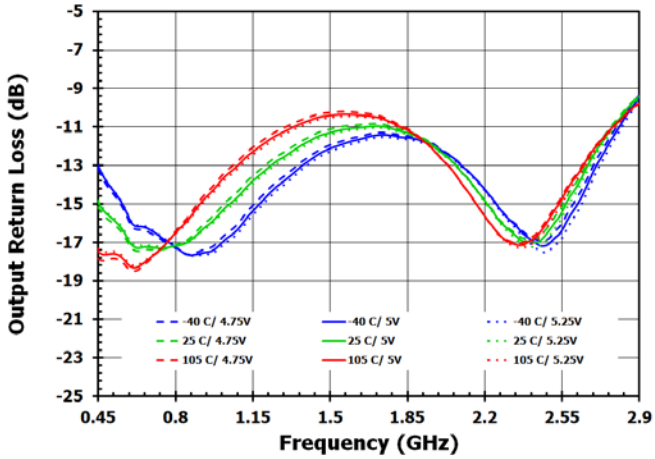



Figure 65. S22, All DSAs = 0dB, Bypass ON

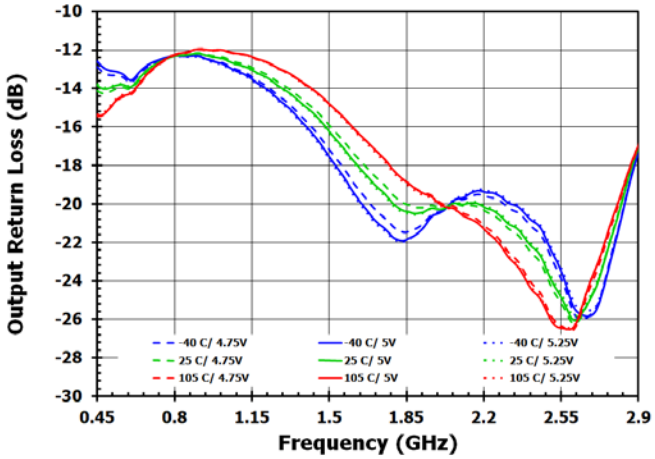



Figure 66. S22, DSA0 = 6dB, Bypass OFF

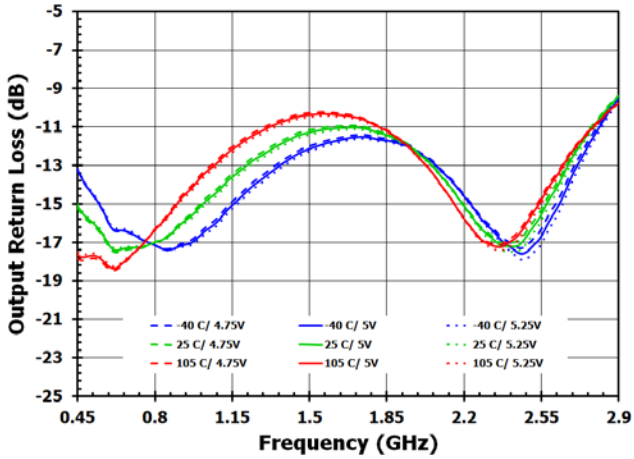



Figure 67. S22, DSA0 = 6dB, Bypass ON

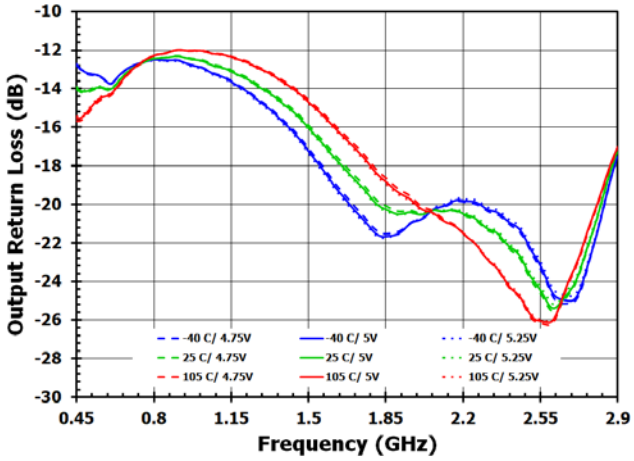



Figure 68. S22, DSA1 = 6dB, Bypass OFF

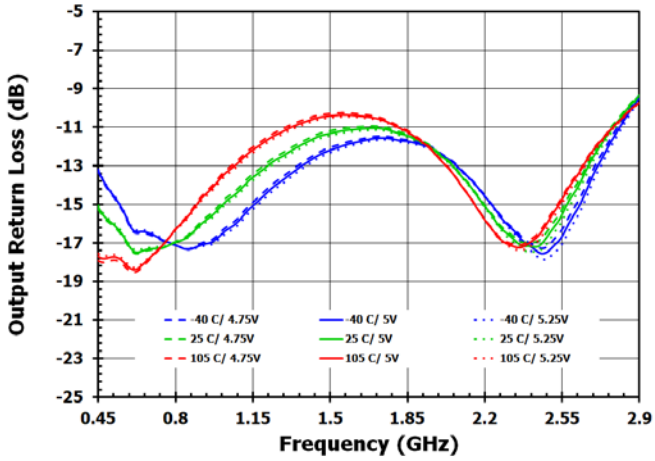


Figure 69. S22, DSA1 = 6dB, Bypass ON

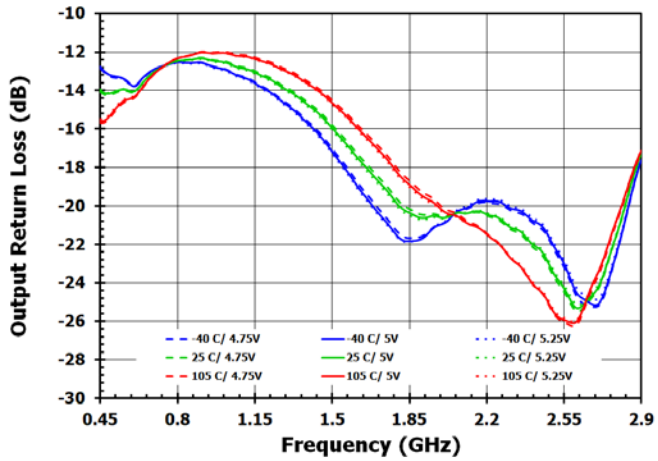



Figure 70. S22, DSA2 = 5dB, Bypass OFF

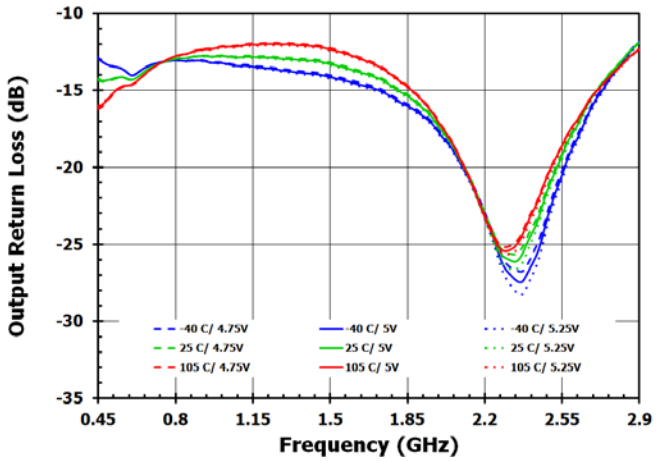



Figure 71. S22, DSA2 = 5dB, Bypass ON

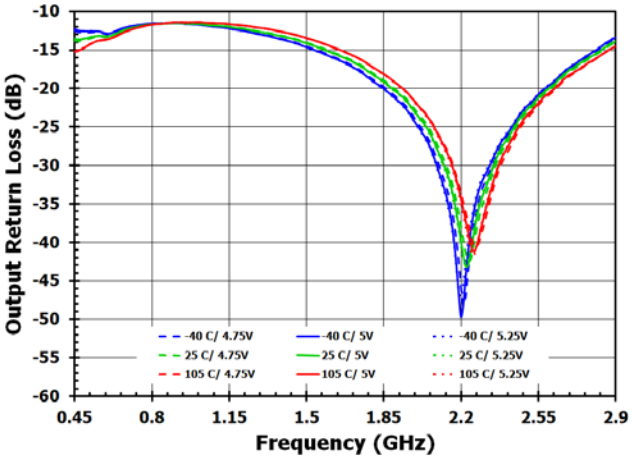



Figure 72. S22, DSA2 = 10dB, Bypass OFF

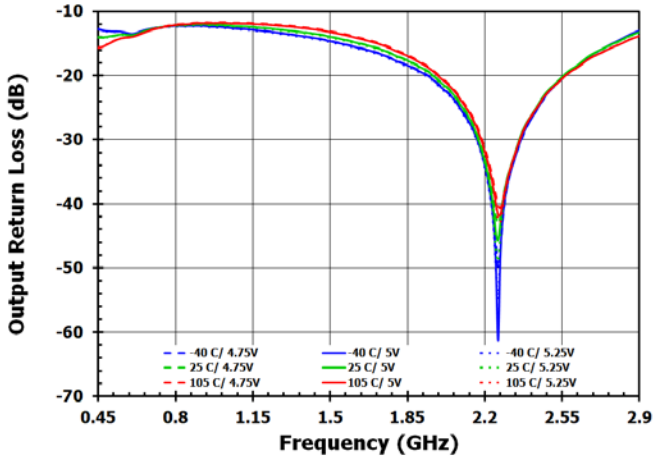



Figure 73. S22, DSA2 = 10dB, Bypass ON

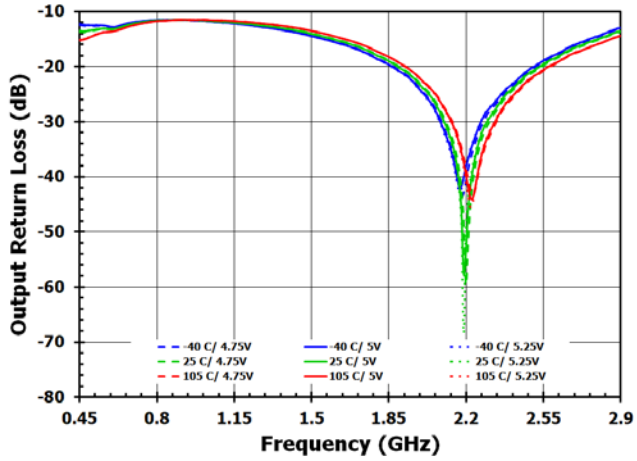



Figure 74. S22, DSA2 = 15dB, Bypass OFF

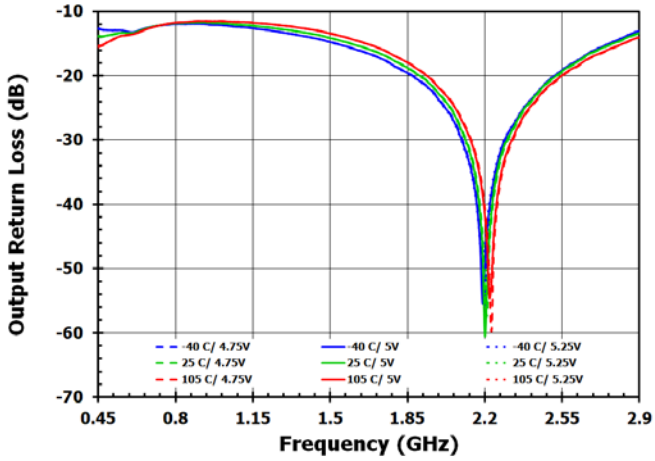


Figure 75. S22, DSA2 = 15dB, Bypass ON

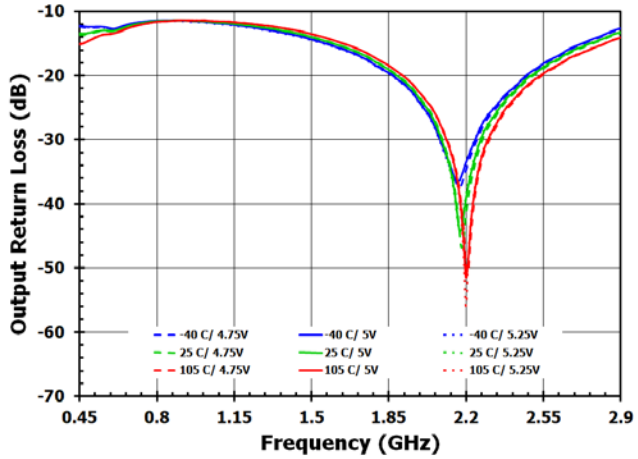



Figure 76. S22, DSA2 = 25dB, Bypass OFF

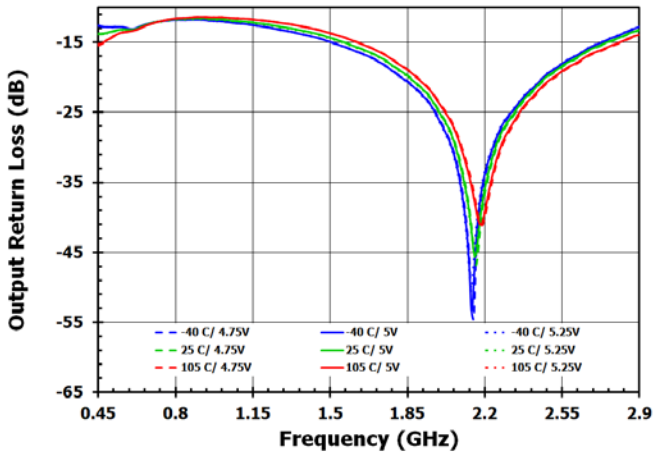



Figure 77. S22, DSA2 = 25dB, Bypass ON

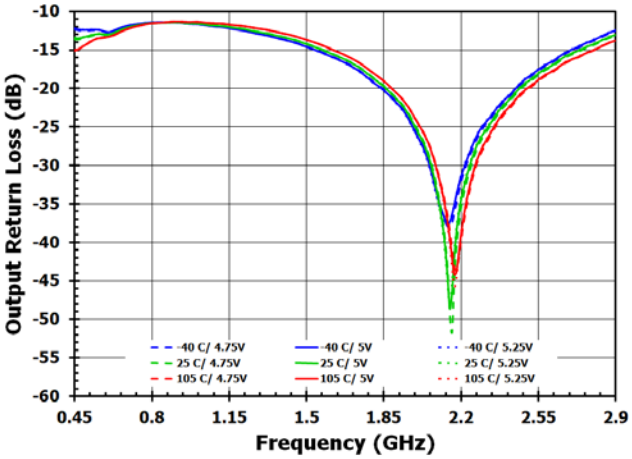



Figure 78. S22, DSA3 = 6dB, Bypass OFF

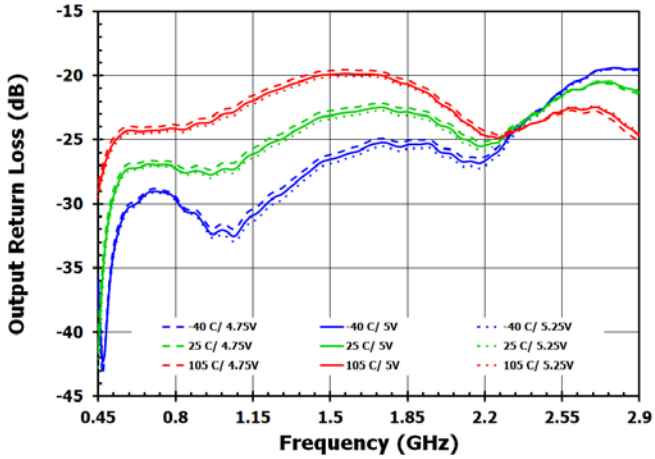



Figure 79. S22, DSA3 = 6dB, Bypass ON

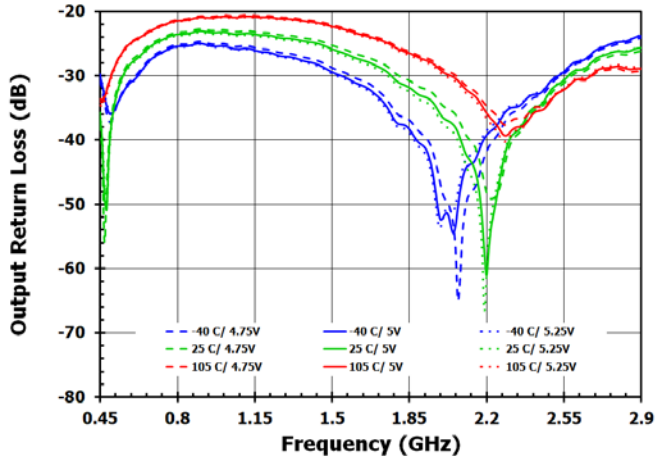



Figure 80. S22, DSA3 = 12dB, Bypass OFF

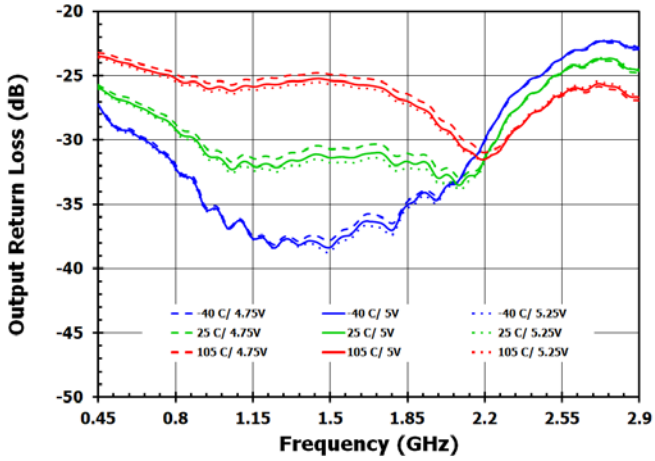


Figure 81. S22, DSA3 = 12dB, Bypass ON

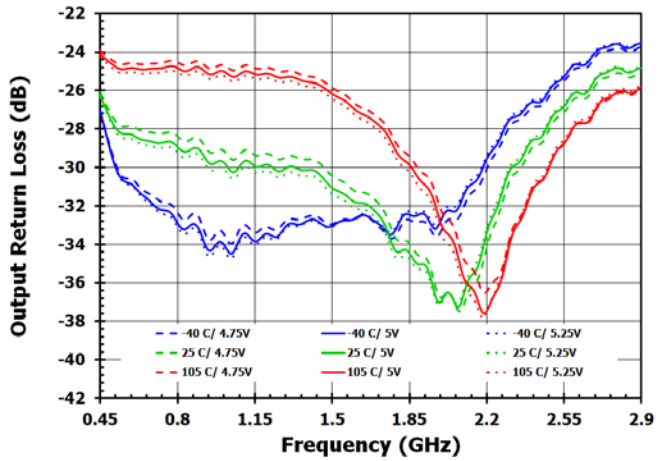



Figure 82. S22, DSA3 = 18dB, Bypass OFF

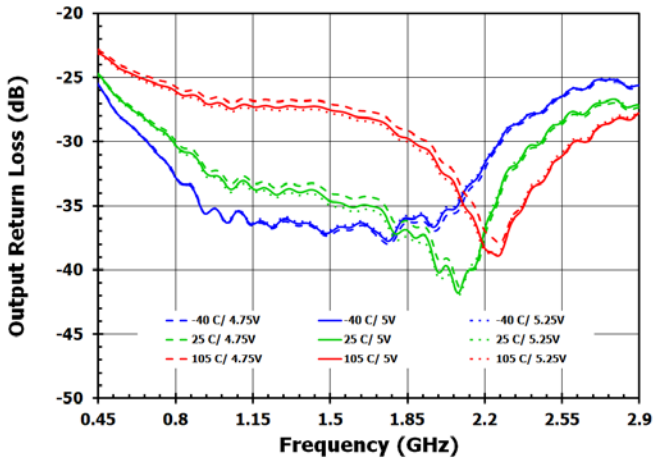



Figure 83. S22, DSA3 = 18dB, Bypass ON

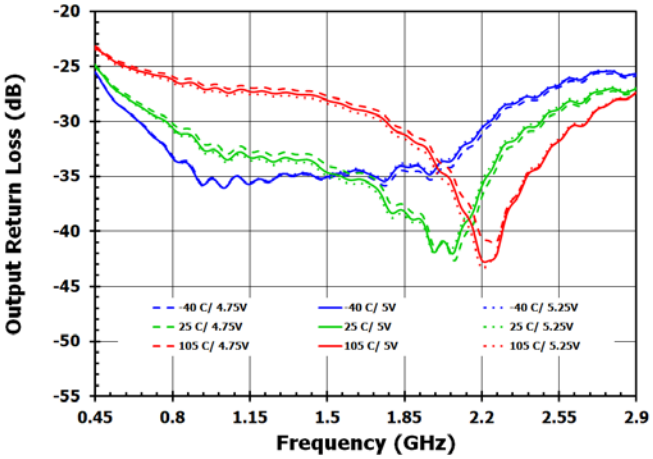



Figure 84. S12, Max Gain, Bypass OFF

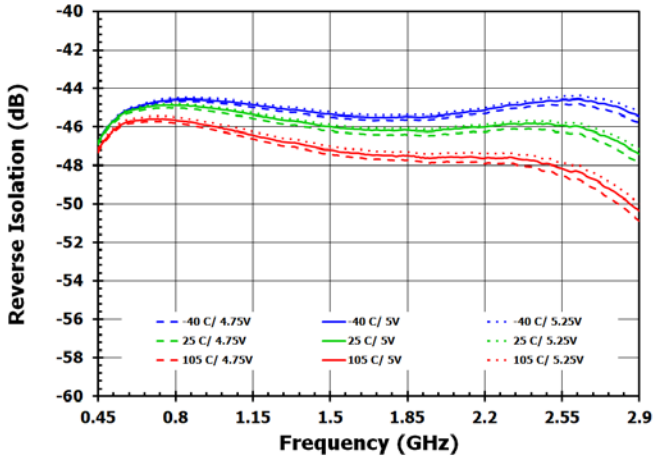



Figure 85. S12, Max Gain, Bypass ON

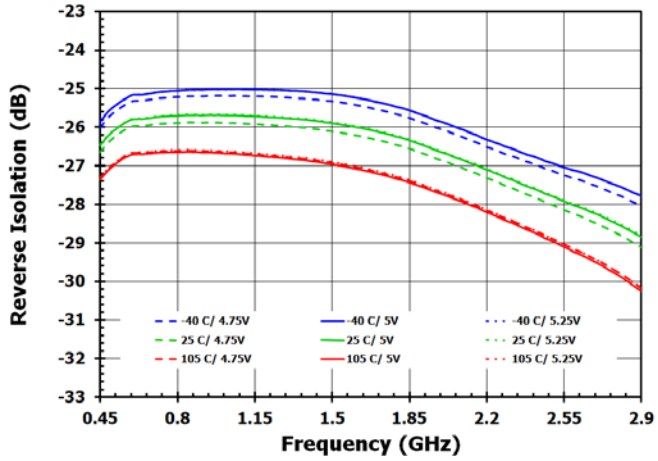



Figure 86. Noise figure, Max Gain, Bypass OFF

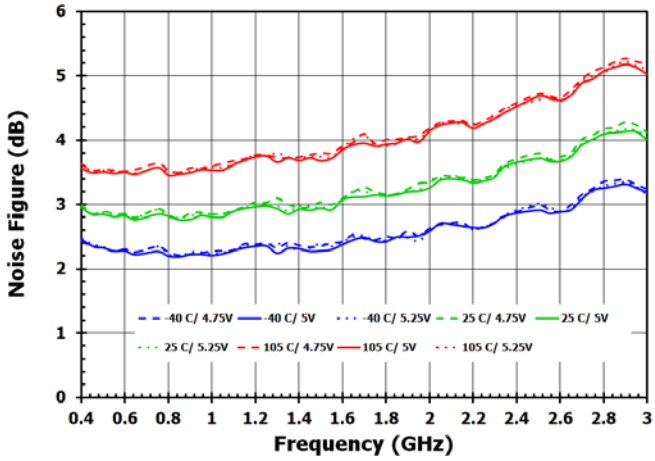


Figure 87. Noise Figure, DSA2 = 5dB, Bypass OFF

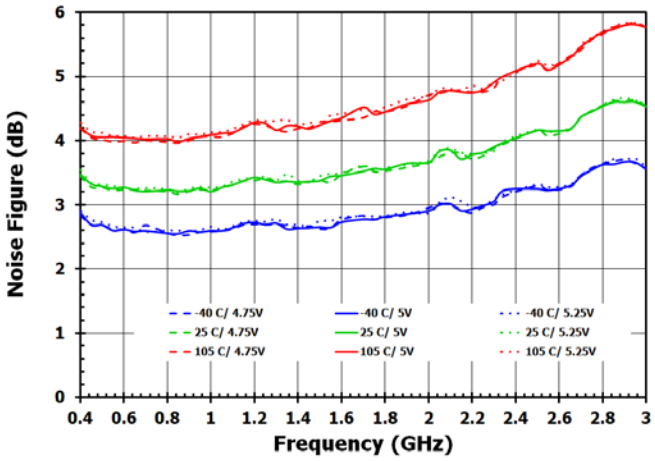



Figure 88. Noise Figure, DSA2 = 10dB, Bypass OFF

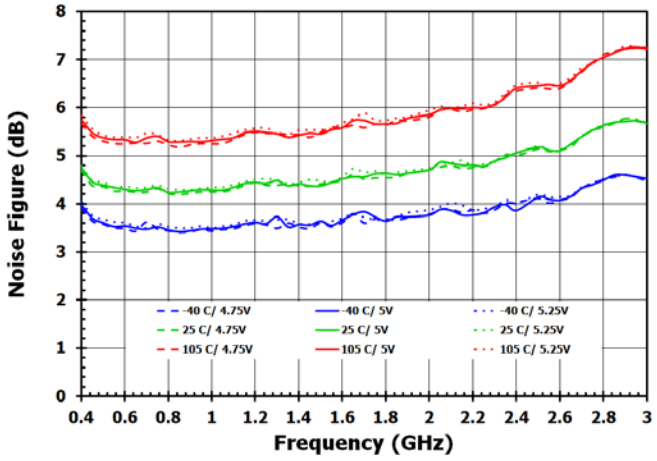



Figure 89. Noise Figure, DSA2 = 15dB, Bypass OFF

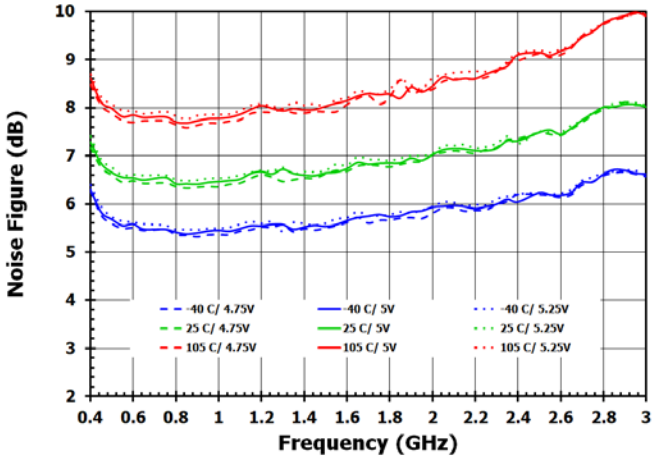



Figure 90. Noise Figure, DSA2 = 25dB, Bypass OFF

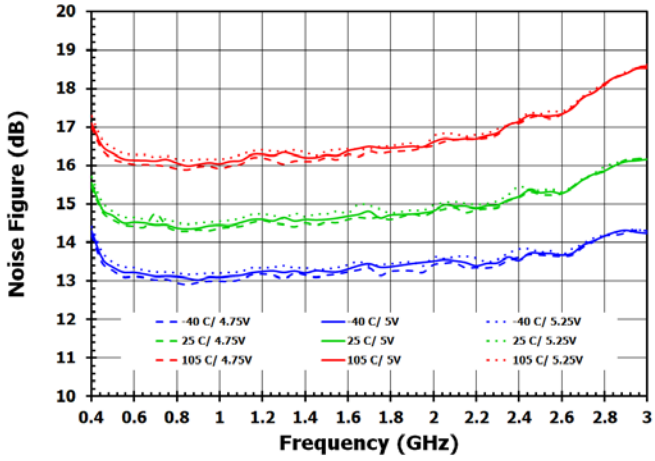



Figure 91. Noise figure, Max Gain, Bypass ON

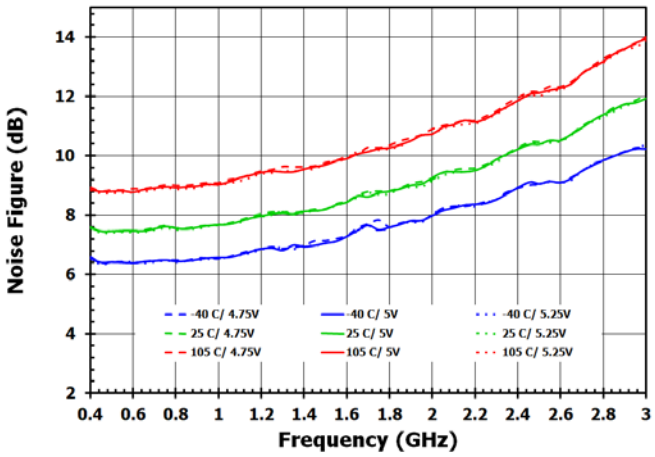



Figure 92. OP1dB at Max Gain, Bypass OFF

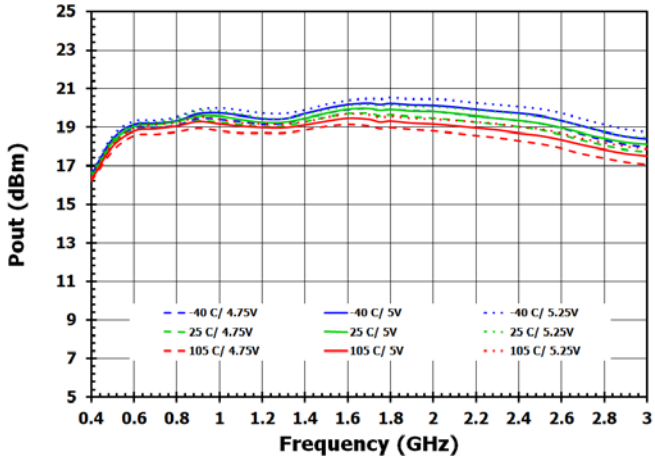


Figure 93. OP1dB at Max Gain, Bypass ON

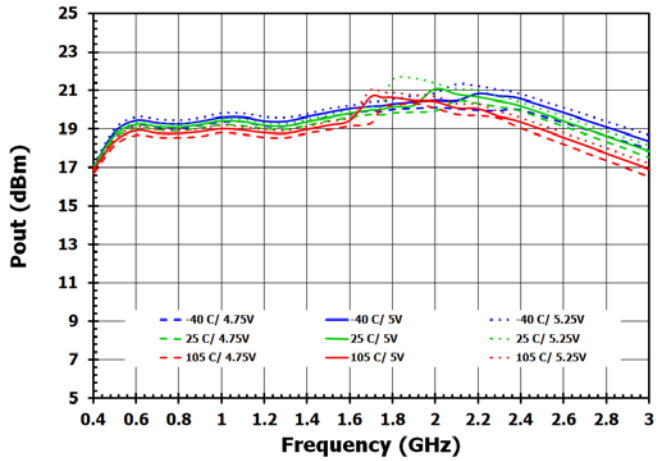



Figure 94. OP1dB at DSA2 = 5dB, Bypass OFF

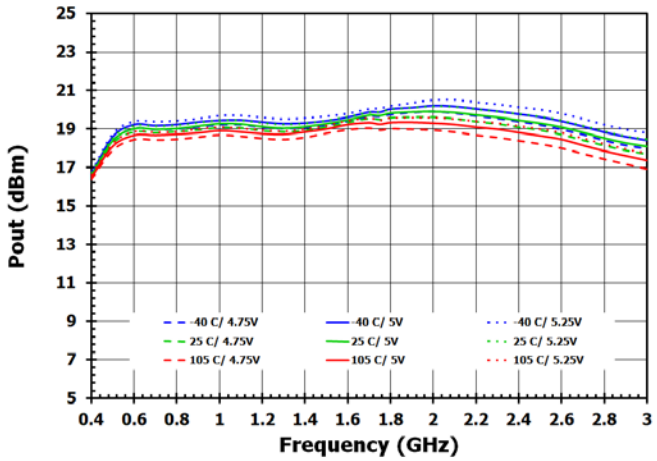



Figure 95. OP1dB at DSA2 = 10dB, Bypass OFF

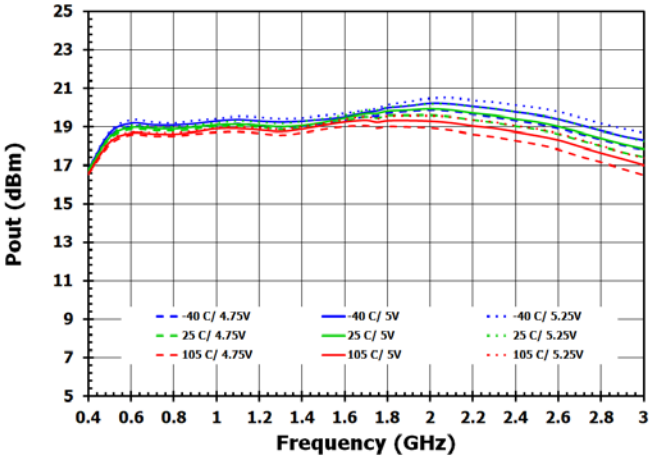



Figure 96. OP1dB at DSA2 = 15dB, Bypass OFF

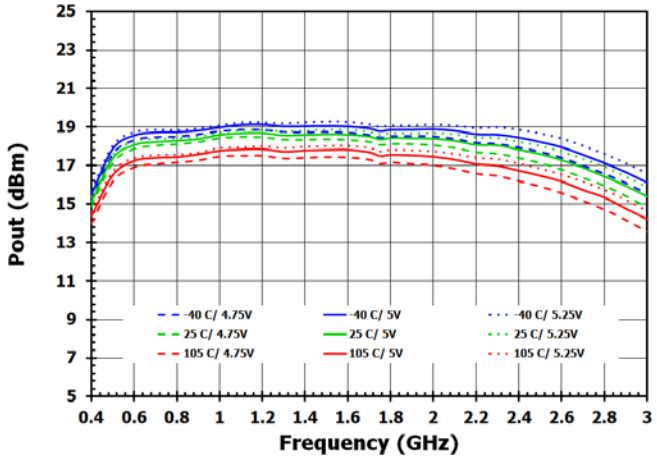



Figure 97. OP1dB at DSA2 = 25dB, Bypass OFF

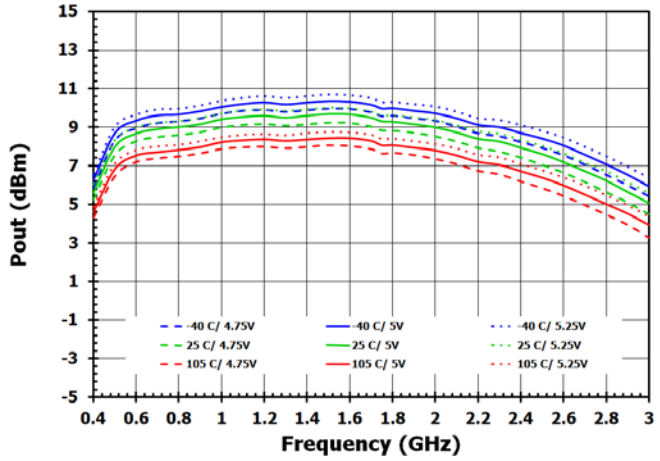



Figure 98. OIP3 at Max Gain, Bypass OFF

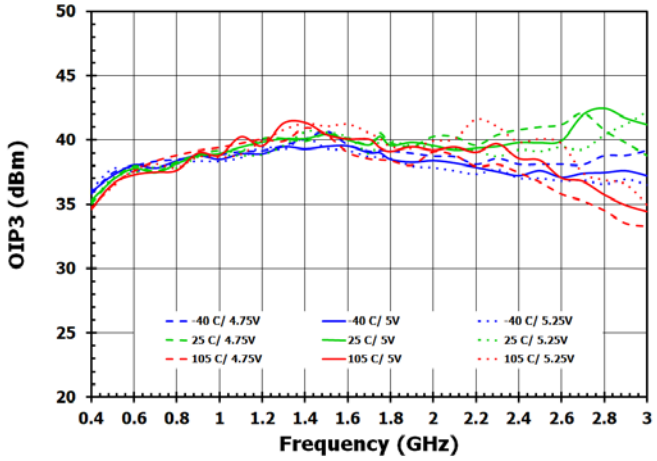


Figure 99. OIP3 at Max Gain, Bypass ON

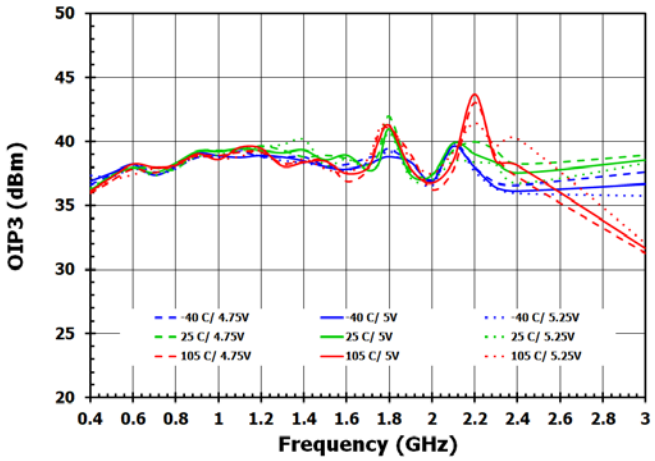



Figure 100. OIP3 at DSA2 = 5dB, Bypass OFF

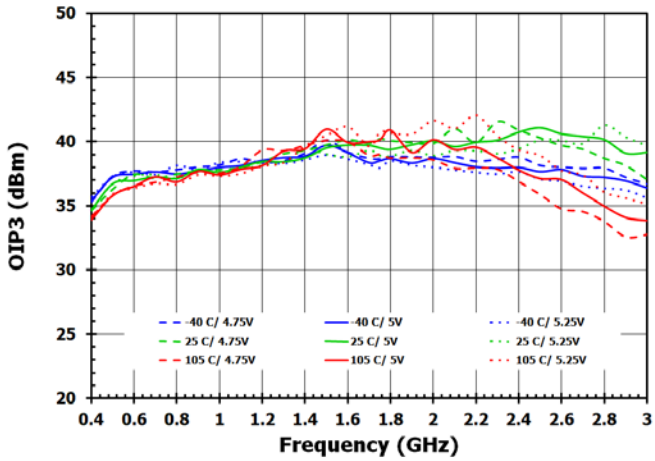



Figure 101. OIP3 at DSA2 = 10dB, Bypass OFF

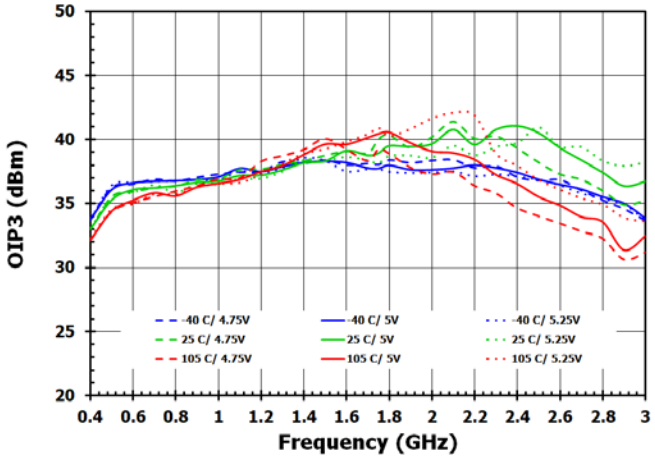



Figure 102. OIP3 at DSA2 = 15dB, Bypass OFF

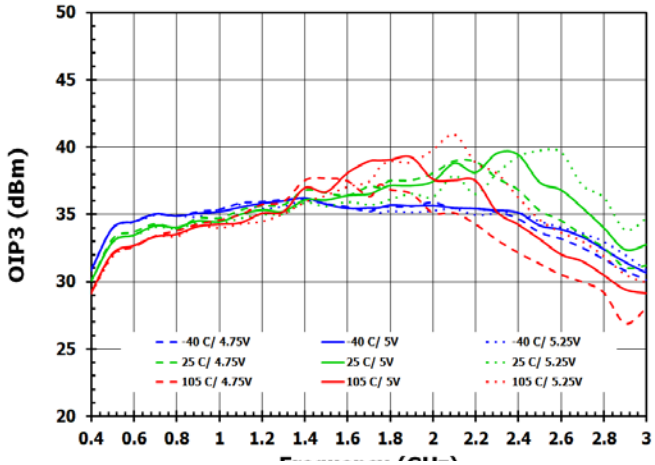
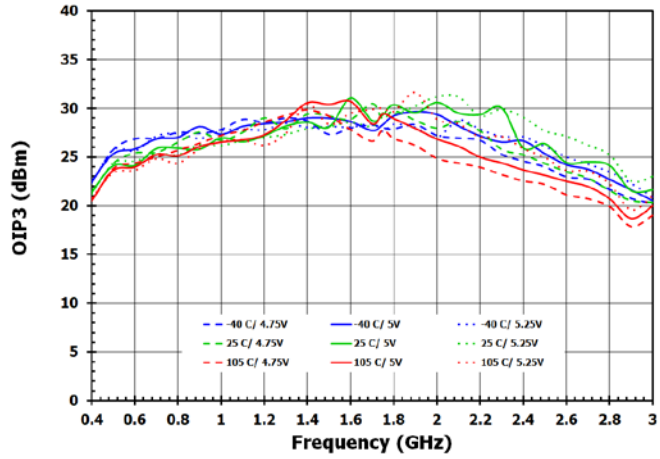



Figure 103. OIP3 at DSA2 = 25dB, Bypass OFF



# Functional Description

The F0443 employs a variety of programming options to control the device's standby (STBY) operation, the on-chip digital step attenuators (DSAs) and the amplifier bypass. The standby (STBY) function and four of the DSAs are programmed using external control pins (parallel mode), while the remaining DSAs and amplifiers are programmed serially via a SPI or I3C interface. The following sections provide specific details on each programming mode.

## Parallel Programming

### Standby (STBY) Mode Programming

The F0443 allows for the independent shutdown of each signal path. Simply apply the logic shown in Table 9 to control paths A and B.

Table 9. STBY Mode Truth Table

| Path | Pin | Logic | Path Power State |
|---|---|---|---|
| A | STBY_A (Pin 4) | 0 | Path A Power On |
| | | 1 (NC) | Path A Standby (SPI/I3C still active) |
| B | STBY_B (Pin 10) | 0 | Path B Power On |
| | | 1 (NC) | Path B Standby (SPI/I3C still active) |

When the STBY_A and STBY_B pins are toggled between the logic LOW and Logic HIGH modes, the register settings remain unchanged. Therefore the bypass setting and DSA2 attenuators will retain their settings during standby. The only exception is if a new programming command is received (via the SPI or I3C interface) during the STBY state. Since the SPI/I3C interface remains active during the Standby mode, the attenuator and bypass registers can still be reprogrammed during this time. When each path is brought out of Standby, the attenuators will be set per the latest register settings.

The default state for each of these pins is a logic HIGH which leaves the RF paths in the off state.

### Parallel Programming of DSA1

DSA1_A and DSA1_B programming is accomplished by applying the desired logic to the external control pins described below. By using parallel programming, fast switching of these DSAs can take place without experiencing the delays commonly associated with serial programming. Logic HIGH selects the 6dB attenuation state, while logic LOW selects the 0dB attenuation state as seen in Table 10.

Upon startup the DSA1 attenuator will be set per the logic level. If the pin is left floating (e.g. left in a 'no connect' or 'NC' state) the attenuator will be set for the maximum value of 6dB since the pin is set to logic HIGH internally.

Table 10. DSA1 Truth Table

| DSA1_A Logic (Pin 47)<br>DSA1_B Logic (Pin 14) | Attenuation |
|---|---|
| 0 | 0dB |
| 1 (NC) | 6dB |

## Parallel Programming of DSA3

DSA3 uses 2-bit logic to select up to 4 different states per attenuator with a 6dB step. By using parallel programming, fast switching of these DSAs can take place without experiencing the delays commonly associated with serial programming. Logic HIGH selects the 6dB attenuation state for Bit 0, while logic HIGH selects the 12dB attenuation state for Bit 1. When both pins are set for logic LOW, the DSA is set to the 0dB attenuation state. In all cases, the logic for each control bit will default to the HIGH state when the control pin is left floating (e.g. left in a 'no connect' or 'NC' state). The DSA states are listed in Table 11.

Upon startup, the DSA3 attenuator will be set per the logic level. If the pins are left floating (e.g. left in a 'no connect' or 'NC' state), the attenuator will be set for the maximum value of 18dB since the pin is set HIGH internally.

Table 11. DSA3 Truth Table

| DSA3_A_BIT1 (Pin 37)<br>DSA3_B_BIT1 (Pin 24) | DSA3_A_BIT0 (Pin 38)<br>DSA3_B_BIT0 (Pin 23) | Attenuation |
|---|---|---|
| 0 | 0 | 0dB |
| 0 | 1 (NC) | 6dB |
| 1 (NC) | 0 | 12dB |
| 1 (NC) | 1 (NC) | 18dB |

## Multi-IC Addressing Scheme

The F0443 has the ability to share the serial interface lines for up to four devices. This is accomplished by giving the device a specific, or static, address using pins ID_0 (pin 8), and ID_1 (pin 9). Use of these pins is specific to whether the serial programming is done using standard serial programming (SPI) or serial I3C programming.

Upon startup, the static address is set per the logic levels. If the pins are left floating (e.g. left in a 'no connect' or 'NC' state), the static address will be set to '00' since the pins are set to logic LOW internally.

Table 12. Static Address Truth Table

| ID_1 (Pin 9) | ID_0 (Pin 8) | Static Identifier |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

## Serial Communication

The F0443 has been designed to use standard 3-wire serial communication (SPI) or a 'Slave-Lite' version of the I3C protocol communication (I3C). The communication mode is set using SPI_I3C_SEL (pin 3). Logic LOW is for SPI and logic HIGH is for I3C.

Upon startup, the serial communication is set per the logic level. If the pin is left floating (e.g. left in a 'no connect' or 'NC' state), SPI communication is used since the pin is set to logic LOW internally.

Table 13. Serial Communication Mode Truth Table

| SPI_I3C_SEL (Pin 3) | Communication |
|---|---|
| 0 | SPI |
| 1 | I3C |

### Serial Programming

The serial programming is different for the SPI (SPI_I3C_SEL is logic LOW) or I3C (SPI_I3C_SEL is logic HIGH) modes of operation. The SPI interface requires a 16-bit word, whereas the I3C interface utilizes 23 bits. In both cases the information is shifted with the most significant bit (MSB) first.

Figure 104. SPI Word

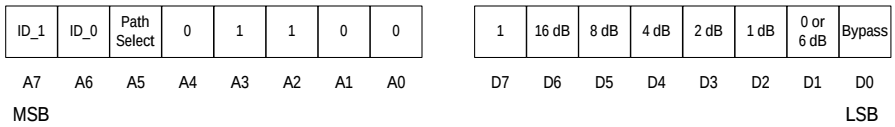
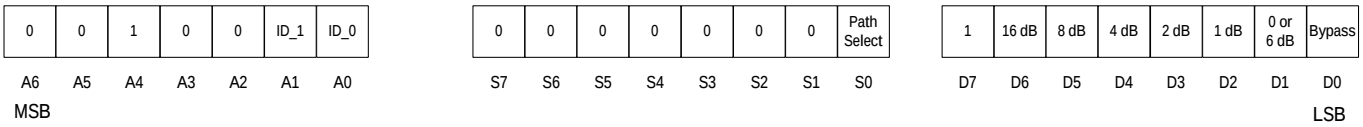



Figure 105. I3C Word




### Truth Tables

The settings for path selection (Path Select), bypassing the amplifier (AMP1_A and AMP1_B), the first attenuator (DSA0_A and DSA0_B), and the third attenuator (DSA2_A, and DSA2_B) are all programmed serially via the F0443's SPI or I3C interface. The truth tables for each digital bit or word remains the same regardless of the serial interface being used.

The Path Select bit, which uses one bit, directs the data word to control one of the two paths, A or B, in the F0443. All the serially controlled components, DSA0, DSA2 and Bypass Mode are controlled simultaneously.

Table 14. Path Select (Path A/Path B) Truth Table

| Path Select | Logic | Path |
|---|---|---|
| A5 (SPI)<br>S0 (I3C) | 0 | A |
| | 1 | B |

The Bypass mode which uses one bit will reduce the overall gain of the F0443 and is directed to the correct path (channel) with Path Select.

Table 15. Bypass Mode (Amp1_A/Amp1_B) Truth Table

| Bypass | Logic | Bypass Mode Setting |
|---|---|---|
| D0 | 0 | Bypass OFF (full gain) |
| | 1 | Bypass ON (reduced gain) |

The first digital attenuator, DSA0, is programmed using one bit and is used in conjunction with the Path Select bit.

Table 16. DSA0 Truth Table

| DSA0 | Logic | DSA0 Attenuation Setting |
|---|---|---|
| D1 | 0 | 0dB |
| | 1 | 6dB |

The third attenuator, DSA2, has 29dB of attenuation with 1 dB steps. DSA2 is programmed with a 5-bit data word. The maximum attenuation is 29dB and states greater than 29 (30, 31) will set the attenuator for 29dB. These bits are used in conjunction with the Path Select bit.

Table 17. DSA2 Abbreviated Truth Table

| D6 | D5 | D4 | D3 | D2 | DSA2 Attenuation Setting |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0dB |
| 0 | 0 | 0 | 0 | 1 | 1dB |
| 0 | 0 | 0 | 1 | 0 | 2dB |
| 0 | 0 | 1 | 0 | 0 | 4dB |
| 0 | 1 | 0 | 0 | 0 | 8dB |
| 1 | 0 | 0 | 0 | 0 | 16dB |
| 1 | 1 | 1 | 0 | 1 | 29dB (max) |
| 1 | 1 | 1 | 1 | 0 | 29dB (max) |
| 1 | 1 | 1 | 1 | 1 | 29dB (max) |

## SPI Programming

Programming the F0443 using the SPI communication requires that SPI_I3C_SEL be set to logic LOW.

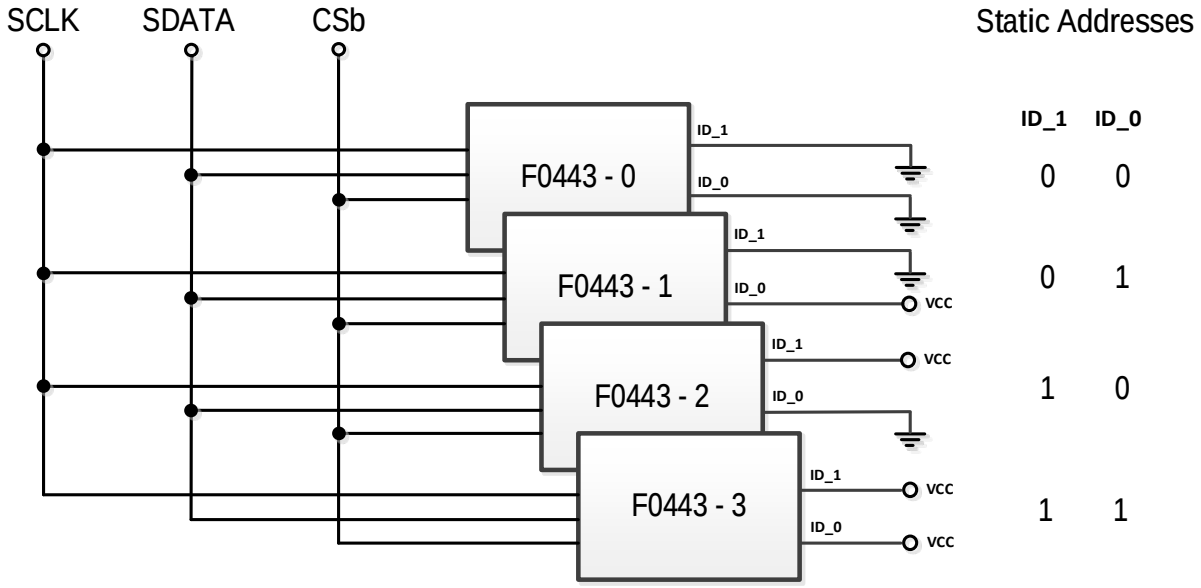
Standard SPI operation is possible using a dedicated control line CSb, SDATA and SCLK. Since ID_0 and ID_1 pins default to logic LOW (forming address 00), the serial bits ID_0 and ID_1 must also be set for logic LOW during the programming process.

The F0443 can also utilize the ID_0 and ID_1 addressing bits to support multi-chip SPI programming. Note that this alternative SPI addressing mode is completely optional. However, when used, this feature enables a *single CSb control line to program up to four separate F0443 devices*, thereby reducing the number of dedicated IC control lines by a factor of four. This is accomplished by:

- Sharing the CSb, SDATA, and SCLK control line for all devices
- Setting ID_0 and ID_1 to give each device a unique identification.
- Using the appropriate identification bits to control the device.

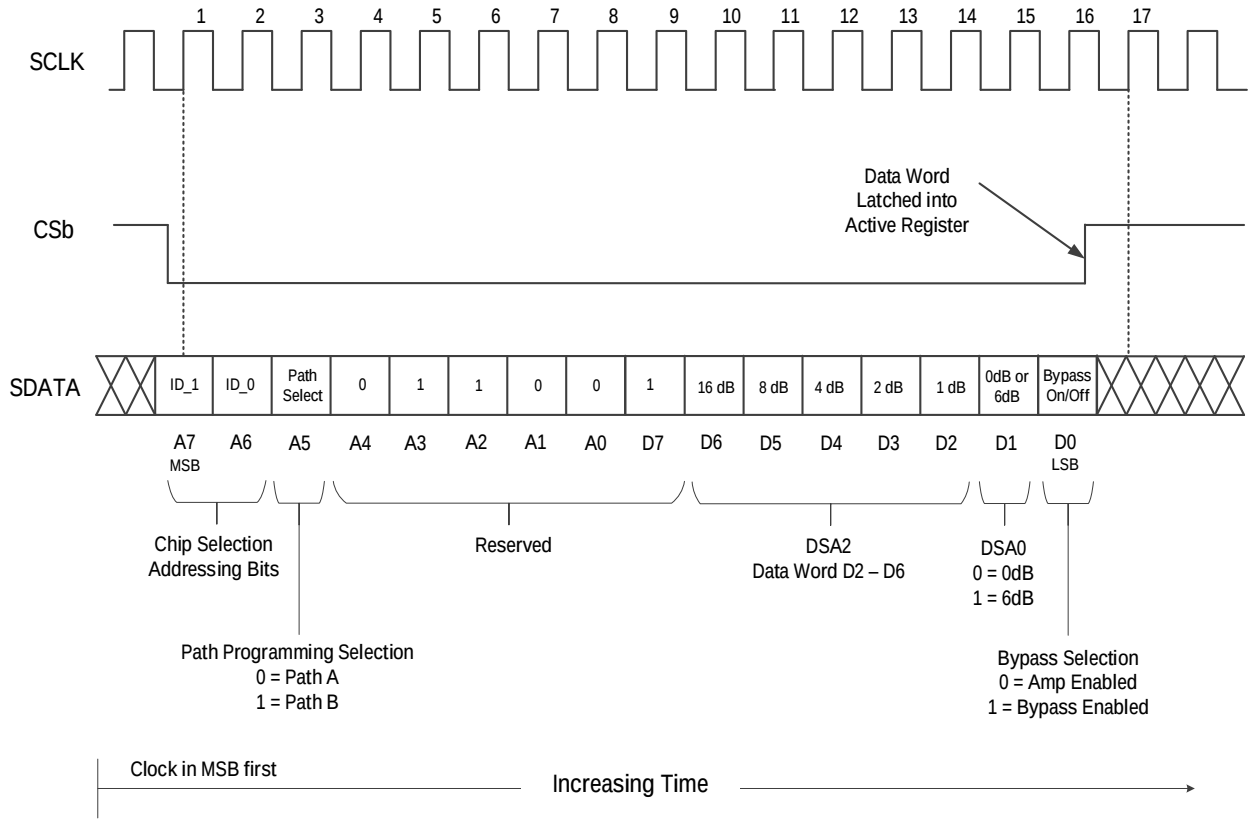
Most common applications would employ a static implementation where the bits are hardwired to a preset address based on the part's location on the circuit board. See Figure 106 for details. The logic present on pins ID_0 and ID_1 will be compared with the relevant sub-addressing bits that are delivered as part of the DATA payload. (Refer to the complete payload bit assignments shown in Figure 104). If the addressing in the payload matches the logic on ID_0 and ID_1, then the device recognizes the programming within the payload as being relevant, and the SPI commands are executed accordingly. If the addresses do not match, then the device simply ignores the programming command.

Figure 106. Multi-IC Addressing Scheme Using SPI




The SPI's DATA payload consists of an 8-bit addressing word followed by an 8-bit data word. See the SPI Timing Diagram in Figure 107. The serial words are clocked in with the most significant bit with the address word first (MSB A7).

Figure 107. SPI Timing Diagram




The addressing word includes three essential 'selection' bits, namely A7, A6 and A5. A7 and A6 pertain to the chip selection (using ID_0 and ID_1, as described above), whereas A5 selects the specific path to be programmed with the write command. Setting bit A5 to logic LOW selects Path A, and logic HIGH selects Path B. Note that the SPI payload only allows for the programming of a SINGLE PATH per write command. Separate, unique write commands will therefore be needed to fully program both paths on the F0443.

Bits A4-A0 and D7 are reserved. The values configured for these bits are set to extract optimal performance from the part. They MUST be included with each SPI command.

The 8-bit data word follows the addressing word. D6-D2 sets the attenuation level of DSA2, D1 sets the attenuation of DSA0, and D0 selects the amplifier bypass option. Refer to the truth tables (Table 14 to Table 17 listed above) for each block's programming code. The entire data word gets latched into the active register with the rising edge of CSb. One Additional clock cycle (Clock 17 in Figure 107) is required after setting the CSb high to reinitialize the SPI for further programming.

Note: After the SPI payload is delivered and latched into the active register, the F0443 must encounter at least two clock pulses before accepting a new SPI command. These additional clock cycles are required to reset the device's microcontroller, essentially clearing the buffer to accept a new payload.

Figure 108 shows the relevant SPI timing intervals.

Figure 108. SPI Serial Register Timing Diagram

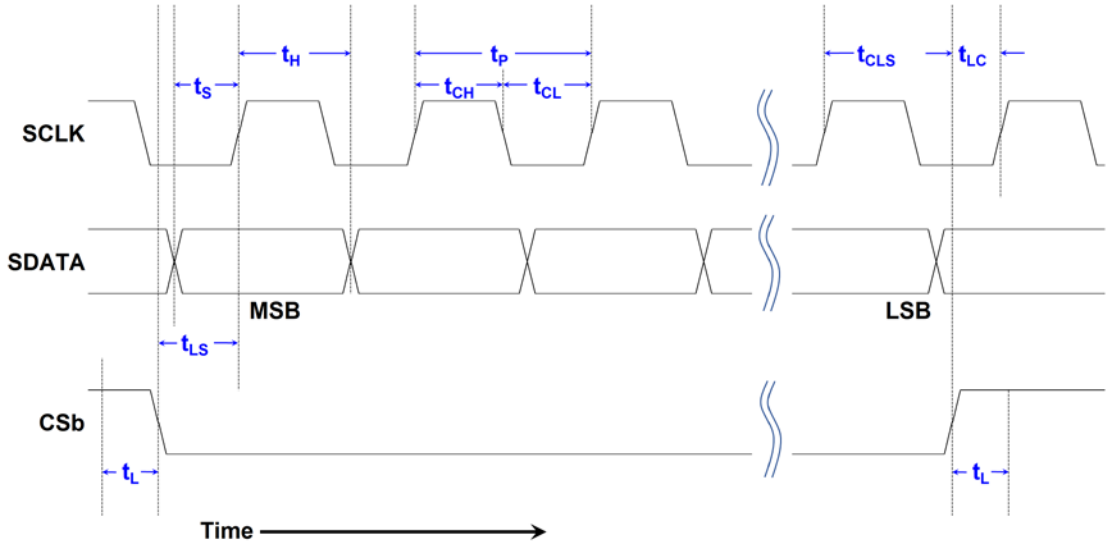



Table 18. SPI Timing Diagram Values Intervals

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| CLK Frequency | $f_C$ | | | | 12.5 [a] | MHz |
| CLK High Duration Time | $t_{CH}$ | | 20 | | | ns |
| CLK Low Duration Time | $t_{CL}$ | | 20 | | | ns |
| DATA to CLK Setup Time | $t_S$ | | 10 | | | ns |
| CLK Period [b] | $t_P$ | | 40 | | | ns |
| CLK to DATA Hold Time | $t_H$ | | 10 | | | ns |
| Final CLK Rising Edge to CSb Rising Edge | $t_{CLS}$ | | 10 | | | ns |
| CSb to CLK Setup Time | $t_{LS}$ | | 10 | | | ns |
| CSb Trigger Pulse Width | $t_L$ | | 10 | | | ns |
| CSb Trigger to CLK Setup Time [c] | $t_{LC}$ | | 10 | | | ns |

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] $(t_{CH} + t_{CL}) \geq 1/f_C$

[c] Once all desired DATA is clocked in, $t_{LC}$ represents the time a CSb high needs to occur before any subsequent CLK signals.

## SPI Programming - Default

When the device is first powered on, it will default to the register settings shown in Figure 109. Please note that these default settings are the recommended conditions for the F0443. DSA0 and DSA2 will be set to their maximum attenuation states, the amplifier will be enabled. These settings apply to a hard reset when first applying $V_{CC}$ and SPI_I3C_SE is set for logic LOW.

Figure 109. SPI Programming – Default Register Settings

| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| MSB | | | | | | | | | | | | | | | LSB |

## I3C Programming

The F0443 also supports a 'Slave-Lite' version of the I3C serial programming protocol where the addressing and data payloads are transferred between the master and slave via a single SDA line. Programming the device using the I3C bus will require the use of the SCL, SDA, ID_0 and ID_1pins.

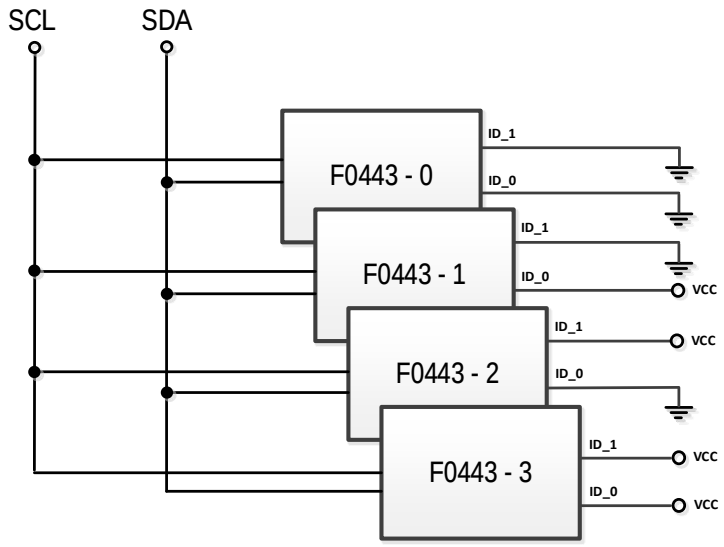
To enable I3C communication on the F0443, the SPI_I3C_SEL pin must be set to logic HIGH.

The addressing of each I3C slave requires a total of 7 bits. The F0443's first 5 addressing bits are internally fixed per Table 19, while the remaining 2 bits are defined by the external logic applied to pins ID_0 and ID_1. Most common applications will employ a static addressing implementation where these two bits are hardwired to a preset address based on the part's location on the circuit board. Since two bits are being used to set the address, a total of four F0443's can be included on any given I3C bus. See Figure 110 for details. Note that the ID_0 and ID_1 pins are internally pulled down to ground per the configuration shown in Figure 115 so these pins will default to a static address of 00 when left unconnected.

Table 19. I3C Slave Addressing

| SLAVE | Preset Address Bits (Non-Configurable on the F0443) | | | | | Configurable Address Bits | |
|---|---|---|---|---|---|---|---|
| | A6 | A5 | A4 | A3 | A2 | ID_1 A1 | ID_0 A0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

Figure 110. I3C Static Addressing Scheme




I3C Static Addresses

| Preset Address Bits | | | | | ID_1 | ID_0 |
|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 |

During the Initialization of the I3C bus, the master performs a “Dynamic Address Assignment” to assign addresses to slave devices. The method to do this uses the command code “Set dynamic address from static address” (SETDASA) to assign a predefined dynamic address to each slave which has a predefined static address. This can be seen in Figure 111. The slave static address is a sub-addressing word which determines the specific path (A or B) to be programmed. Bits D7 to D1 are reserved within this word; only bit D0 is used to select between paths A or B.

Programming the F0443 requires that the addressing word be sent across the SDA line first, followed by a 2-byte write command. See Figure 112 for details surrounding the required I3C payload. As shown, the first byte is the dynamic address that has been predefined in the Initialization phase.

The second byte contains the same 8 control bits which were defined in the SPI section above. As with the SPI mode, the I3C payload only allows for the programming of a SINGLE PATH per write command. Separate, unique write commands will therefore be needed to fully program both paths on the F0443.

For the 8-bit programming word, D6-D2 sets the attenuation level of DSA2, D1 sets the attenuation of DSA0, and D0 selects the amplifier bypass option. Refer to the truth tables listed above for each block’s programming code. When the device is first powered on, it will default to the Byte1 register settings shown in Figure 113 below. DSA0 and DSA2 will be set to their maximum attenuation states, the Amplifier will be fully enabled. These settings apply to a hard reset when first applying $V_{CC}$.

The entire data word gets latched into the active register with the execution of the STOP bit.

Figure 111. I3C Timing Diagram – Initialization

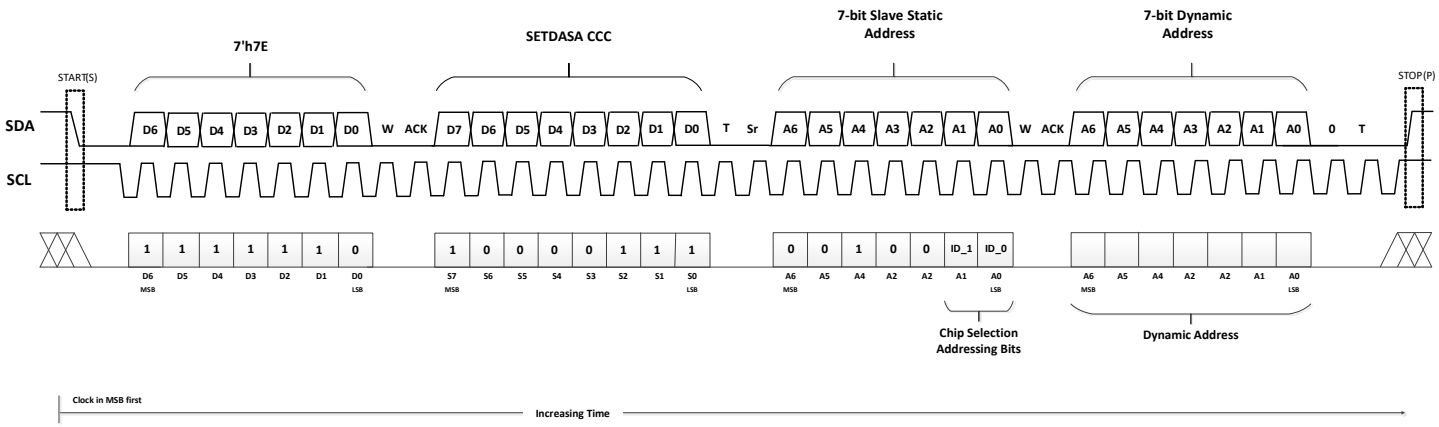



Figure 112. I3C Timing Diagram

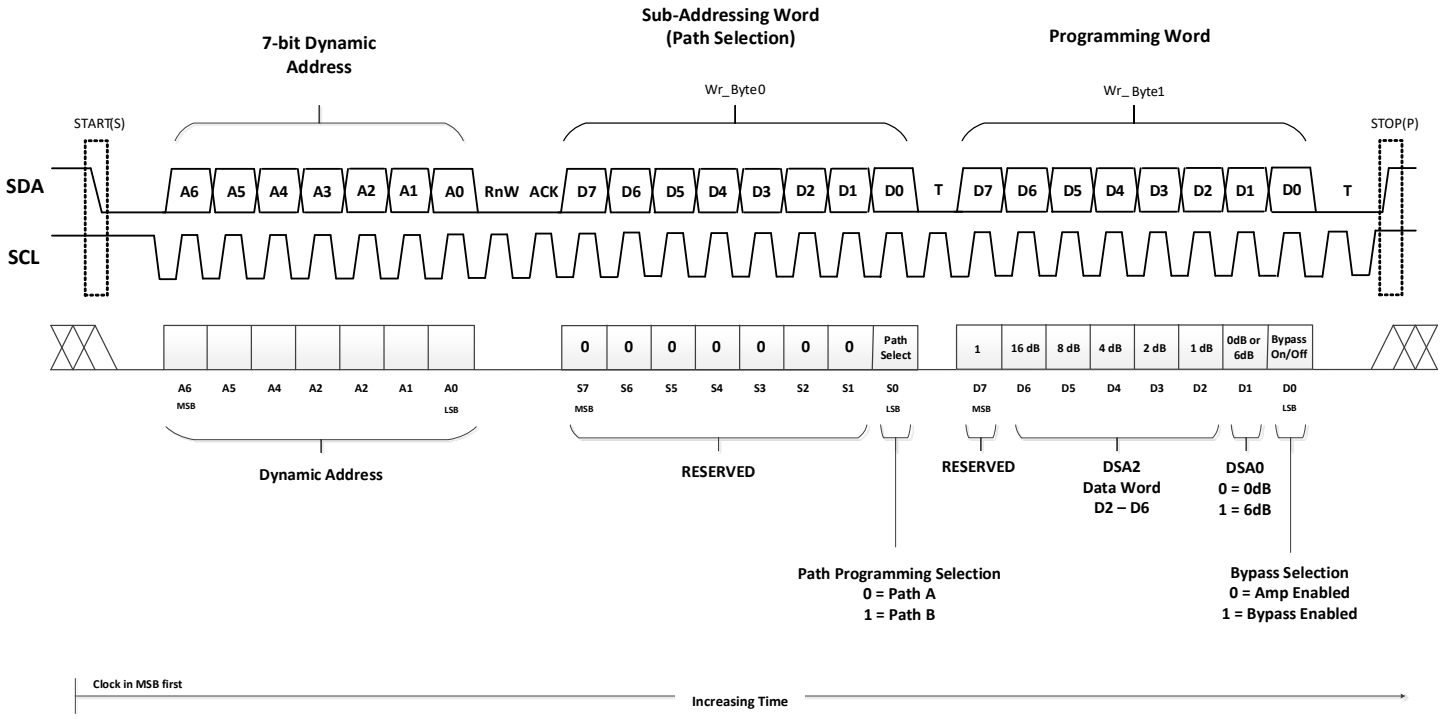


Figure 113. I3C Programming – Default Register Settings for Byte1 (Programming Word)

| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 MSB | D6 | D5 | D4 | D3 | D2 | D1 | D0 LSB |

Note: Applies to the register settings for paths A and B.

Figure 114 shows the relevant I3C timing intervals which are specified in Table 20.

Figure 114. I3C Timing Intervals (Pictorial View)

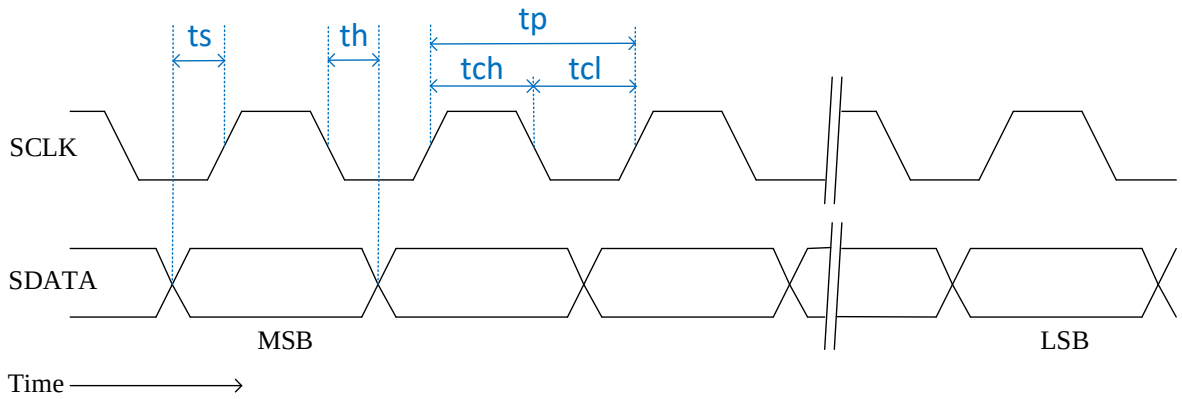



Table 20. I3C Timing Intervals (Tabulated Figures)

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| SCL Frequency | $f_C$ | | | | 12.5 [a] | MHz |
| SCL High Duration Time | $t_{CH}$ | | 20 | | | ns |
| SCL Low Duration Time | $t_{CL}$ | | 20 | | | ns |
| SDA to SCL Setup Time | $t_S$ | | 10 | | | ns |
| SCL Period [b] | $t_P$ | | 40 | | | ns |
| SCL to SDA Hold Time | $t_H$ | | 10 | | | ns |

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] $(t_{CH} + t_{CL}) \geq 1/f_C$

# Application Information

The F0443 has been optimized for use in high performance RF applications ranging in frequency from 0.6GHz to 2.7GHz in individual frequency bands.

## Power Supplies

A common $V_{CC}$ power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µs (50mV/µs). In addition, all control pins should remain at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

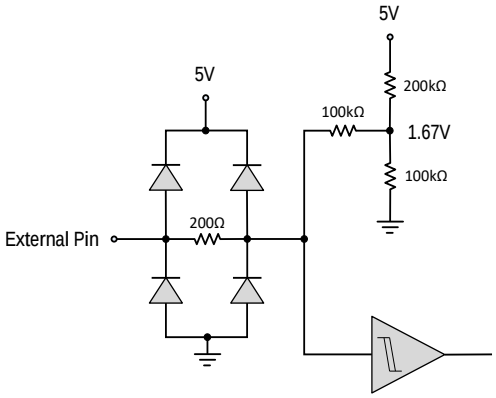
## Startup Condition

Upon device power-up, both channels will default to the STBY mode.

## Digital Pin Voltage and Resistance Values

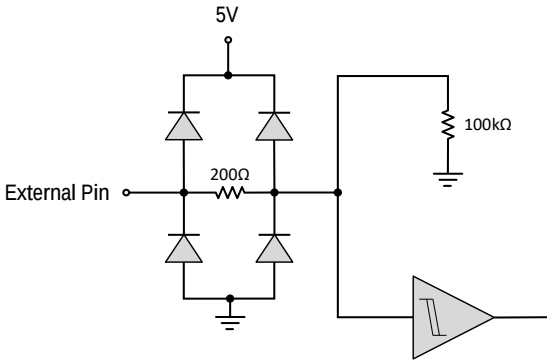
The logic for the control bits (STBY_A, STBY_B, DSA1_A, DSA1_B, DSA3_A and DSA3_B) will default to the HIGH state, 1.67 V when the control pin is left floating (i.e. left in a 'no connect' or 'NC' state). A simplified internal circuit is shown in Figure 114.

Figure 115. Internal Pull-up Configuration for STBY_A, STBY_B, DSA1 and DSA3 Control Pins




To enable SPI communication on the F0443, the SPI_I3C_SEL pin must be set to logic LOW or left open in a 'no connect' state. Internally, the SPI_I3C_SEL pin is pulled down to ground per the configuration shown in Figure 115.

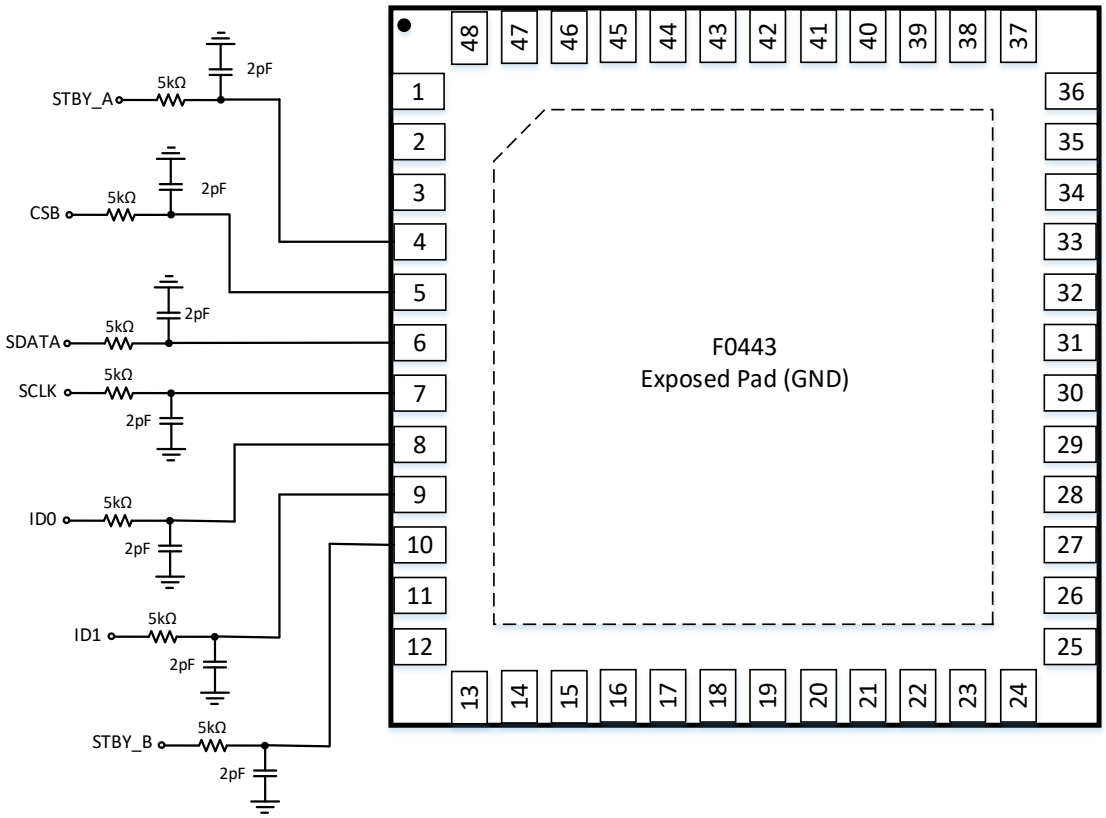
Figure 116. Internal Pull-down Configuration for the SPI_I3C_SEL, ID_0, and ID_1 Control Pins



## Signal Integrity

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to pins for the SPI (16, 17, 18), parallel (1, 19-24) and $V_{MODE}$ pin (3) as shown below. Note the recommended resistor and capacitor values do not necessarily match the EVKit BOM for the case of poor control signal integrity. For multiple devices driven by a single control line, the component values will need to be adjusted accordingly so as not to load down the control line.

Figure 117. Control Pin Interface for Signal Integrity



# Evaluation Kit Picture

Figure 118. Top View

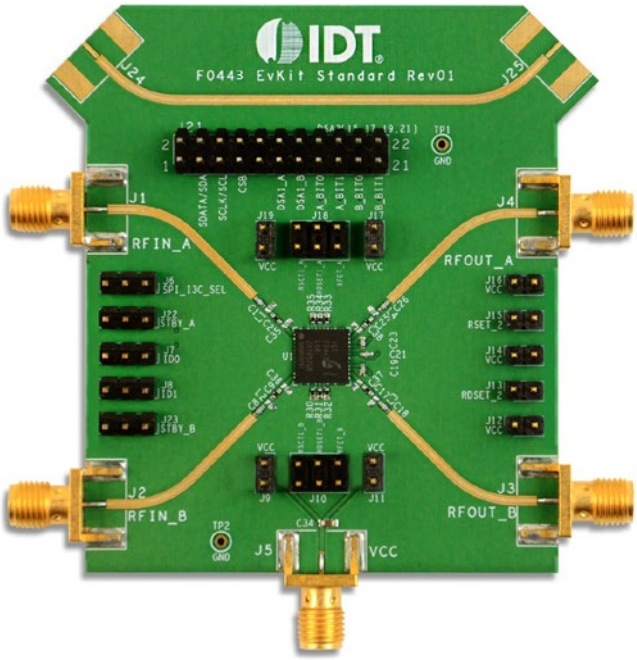
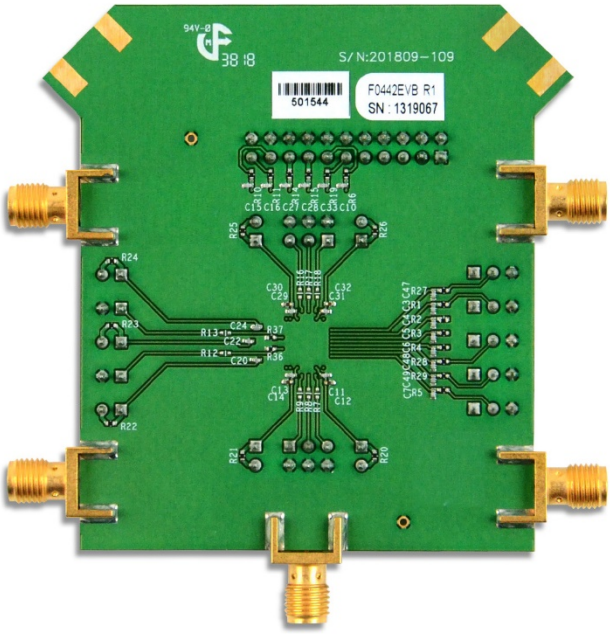
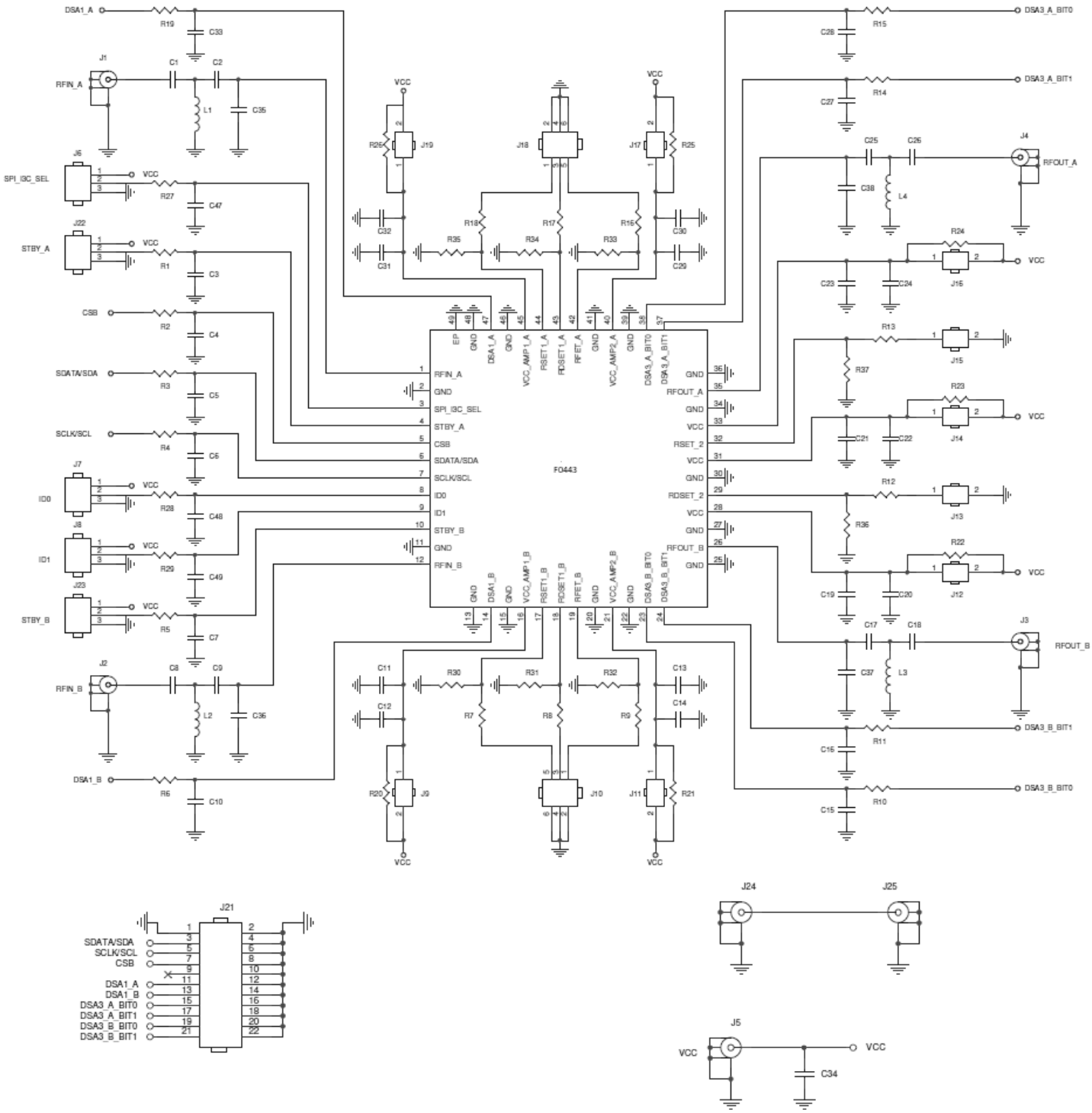



Figure 119. Bottom View



# Evaluation Kit / Applications Circuit

Figure 120. Electrical Schematic



# Evaluation Kit BOM

Table 21. Bill of Materials (BOM)

| Part Reference | QTY | Description | Manufacturer Part # | Manufacturer |
|---|---|---|---|---|
| C1, C8, C11, C13, C18, C19, C21, C23, C26, C29, C31, C47, C48, C49 | 14 | 100pF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H101J | MURATA |
| C20, C22, C24 | 3 | 1000pF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H102J | MURATA |
| C34 | 1 | 100nF ±10%, 50V (0603) | GRM188R7H104KA93D | MURATA |
| C12, C14, C30, C32 | 4 | 100nF ±10%, 16V, X7R Ceramic Capacitor (0402) | GRM155R71H104K | MURATA |
| R1-R6, R10, R11, R14, R15, R19, R27, R28, R29 | 14 | 100Ω ±1%, 1/10W, Resistor (0402) | ERJ-2RKF1000X | PANASONIC |
| R20-R26, C2, C9, C17, C25 | 11 | 0Ω Resistors (0402) | ERJ-2GE0R00X | PANASONIC |
| J1-J5 | 5 | Edge Launch SMA (0.375 inch pitch ground, tab) | 142-0701-851 | Emerson Johnson |
| J9, J11-J17, J19 | 9 | CONN HEADER VERT SGL 2 X 1 POS GOLD | 961102-6404-AR | 3M |
| J6, J7, J8, J22, J23 | 5 | CONN HEADER VERT SGL 3 X 1 POS GOLD | 961103-6404-AR | 3M |
| J10, J18 | 2 | CONN HEADER VERT DBL 3 X 2 POS GOLD | 67997-106HLF | AMPHENOL FCI |
| J21 | 1 | CONN HEADER VERT DBL 11 X 2 POS GOLD | 67997-122HLF | AMPHENOL FCI |
| C3,C4,C5,C6,C7,C10, C15,C16,C27,C28,C33 | 11 | 2pF ±0.1pF, 50V, C0G Ceramic Capacitor (0402) | GJM1555C1H2R0B | MURATA |
| R36 | 1 | 13 KΩ | ERK-2RKF1302X | PANASONIC |
| R37 | 1 | 2.94 KΩ | ERJ-2RKF2941X | PANASONIC |
| R30, R35 | 2 | 2.67 KΩ | ERJ-2RKF2671X | PANASONIC |
| R31, R34 | 2 | 9.1 KΩ | ERJ-2RKF9101X | PANASONIC |
| R32, R33 | 2 | 4.7 KΩ | ERJ-2GEJ472X | PANASONIC |
| U1 | 1 | Dual Broadband RF DVGA | F0443LGRI | RENESAS |
| | 1 | Printed Circuit Board Rev 01 | F0443 EVKit Rev 01 | RENESAS |
| J24, J25 | 2 | DNP | | |
| C35-C38, L1-L4, R12, R13, R7-R9, R16-R18 | 16 | DNP | | |

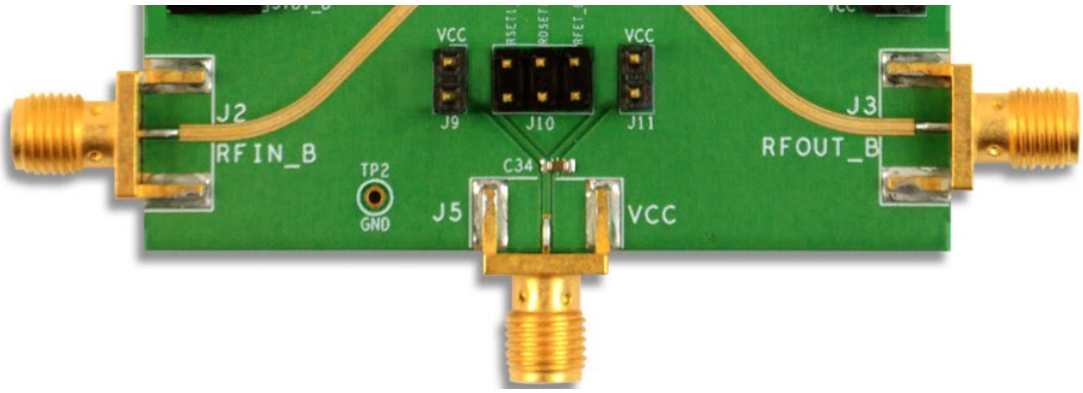
# Evaluation Kit Operation

## Power Supply Setup

Set up a power supply in the voltage range of 4.75V to 5.25V with the power supply output disabled. The voltage can be applied via one of the following connections (see Figure 121):

- Directly to J5 SMA connector
- Individually to J9, J11, J12, J14, J15, J17 and J19 header connections (note the polarity of the GND pin on this connector)

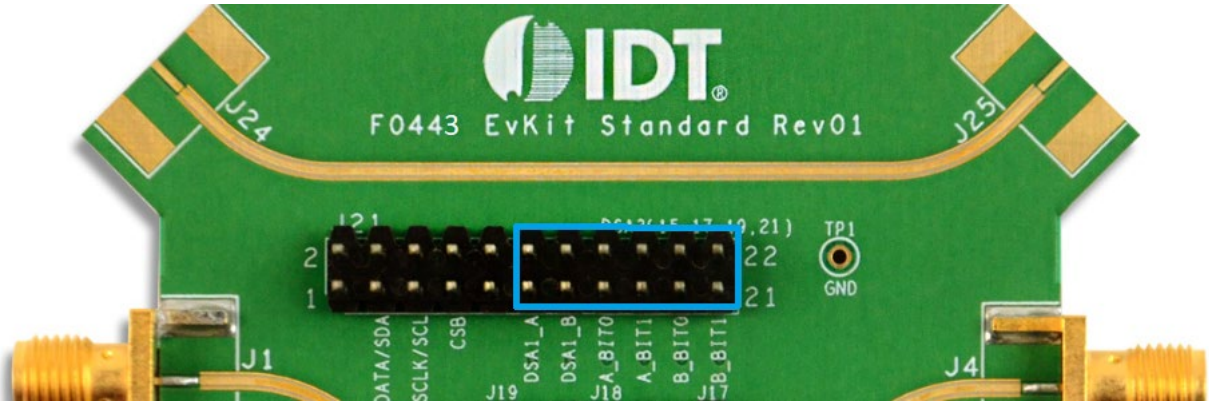
Figure 121. Power Supply and Logic Voltage Connections




## Parallel Logic Control Setup

The Evaluation Board can control the F0443 in the Parallel Mode. For external control, apply logic voltages to the J21 header pins 11 through 21 (see Figure 122). The logic voltage can be applied directly to connector J21.

Figure 122. Power Supply and Logic Voltage Connections



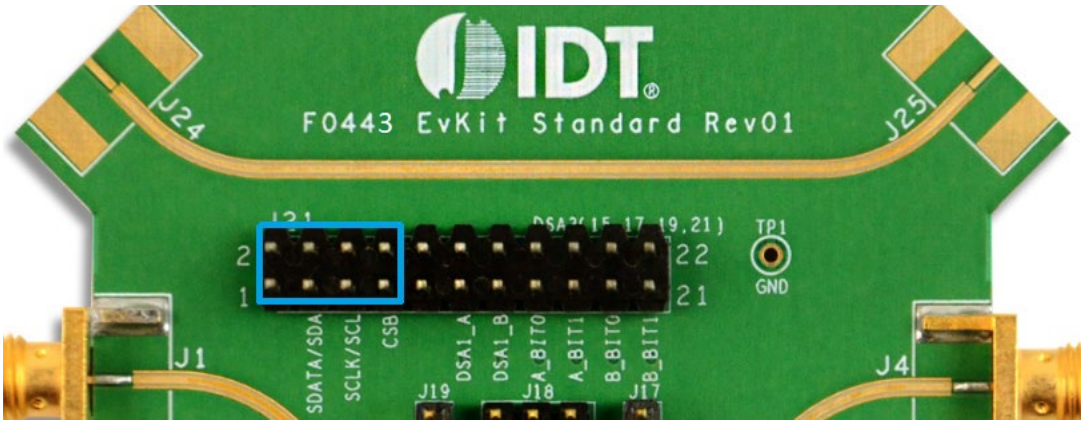

The F0443 uses parallel programming for its DSA1 and DSA3 Attenuators. The rest are controlled through SPI or I3C programming.

## Serial Logic Control Setup

The Evaluation Board has the ability to control the F0443 in the Serial Mode. Connect the serial controller to the J21 header (Pins 1 through 8) connection as shown in Figure 123.

The attenuation settings for DSA0 and DSA2 can be programmed according to Table 16 and Table 17, respectively.

Figure 123. Serial Logic Connections




## Power-On Procedure

Set up the voltage supplies and Evaluation Board as described in the “Power Supply Setup” section and either the “Parallel Logic Control Setup” and/or “Serial Logic Control Setup” sections above.

Enable the $V_{CC}$ supply.

Enable the proper attenuation setting for DSA0 and DSA2 through Serial Programming and for DSA1 and DSA3 through Parallel Programming as discussed earlier in the datasheet.

## Power-Off Procedure

Set the logic control pins to a logic LOW and Disable the $V_{CC}$ supply.

## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/lga-48-package-outline-drawing-70-x-70-mm-body-epad-50-x-50-mm-0mm-pitch-lgr48

## Ordering Information

| Orderable Part Number | Package | MSL Rating | Shipping Packaging | Temperature |
|---|---|---|---|---|
| F0443LGRI | 7 × 7 × 0.7 mm 48-LGA | 1 | Tray | -40° to +105°C |
| F0443LGRI8 | 7 × 7 × 0.7 mm 48-LGA | 1 | Reel | -40° to +105°C |
| F0443EVBI | Evaluation Board | | | |

## Marking Diagram

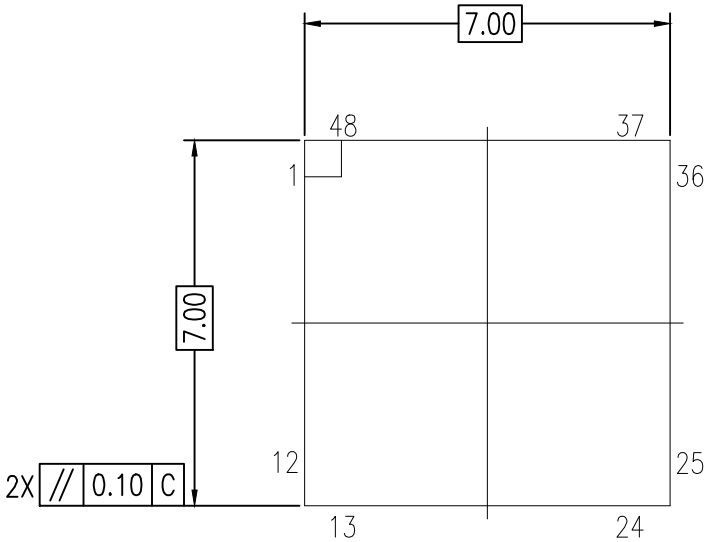
```
IDT
F0443
LGRI
ZS1629L
● Q54E042PY
```

- Line 1 indicates the manufacturer.
- Lines 2 and 3 indicate the part number.
- Line 4:
  - "ZS" is for die version.
  - 1629 has two digits for the year and week that the part was assembled.
  - "L" denotes assembly site.
- Line 5: "Q54E042PY" is the assembly lot number.

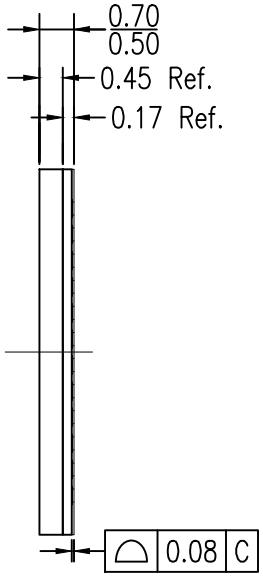
## Revision History

| Revision Date | Description of Change |
|---|---|
| Sep 1, 2020 | Added Footnote [c] to Recommended Operating Conditions table. |
| July 2, 2020 | Minor corrections to the DNL/INL plots made. NF plot with Bypass ON added. |
| May 18, 2020 | Logic control specifications updated in Table 4. |
| April 29, 2020 | Updated SPI/I3C timing diagram. |
| April 1, 2020 | Initial release. |

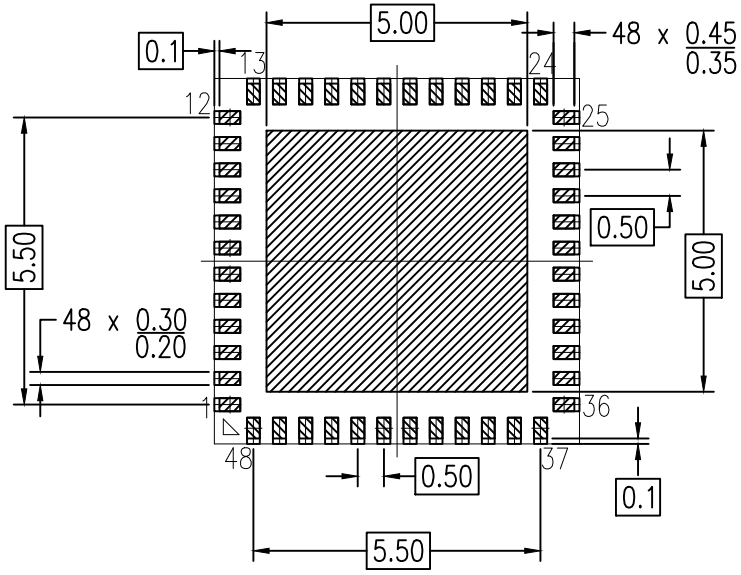
| DATE CREATED | REVISIONS | | |
|---|---|---|---|
| | REV | DESCRIPTION | AUTHOR |
| 06/12/18 | 00 | INITIAL RELEASE | CM |
| | | | |
| NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE | | | |




TOP VIEW

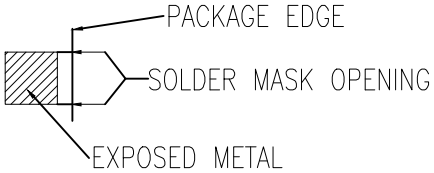



TOP VIEW




BOTTOM VIEW

PAD DETAILS:




NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
3. SM STANDS FOR SOLDER MASK.

TOLERANCES UNLESS SPECIFIED

| DECIMAL | ANGULAR |
|---|---|
| XX± | ± |
| XXX± | |
| XXXX± | |


IDT®
www.IDT.com
6024 Silver Creek Valley Road
San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

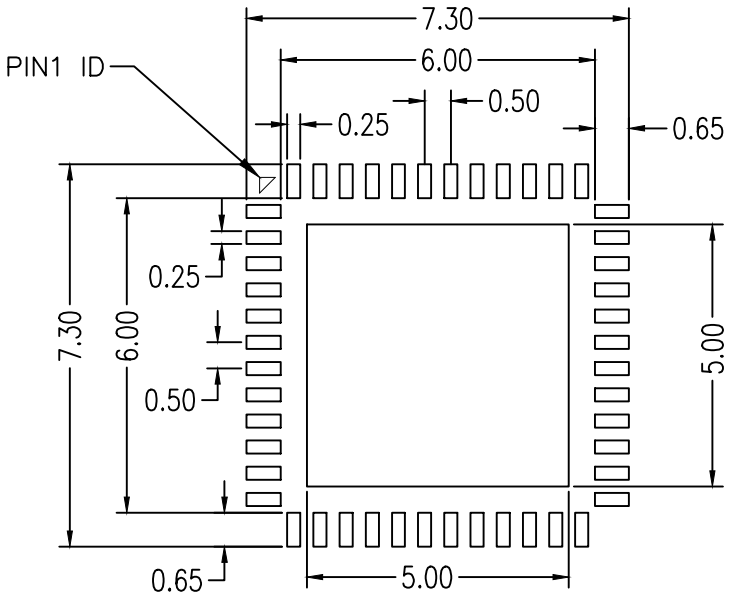

TITLE LGA-48 Package Outline Drawing 7.0 x 7.0 mm Body Epad 5.0 x 5.0 mm 0.5mm Pitch LGR48

| SIZE | DRAWING No. | REV |
|---|---|---|
| C | PSC-4760 | 00 |

DO NOT SCALE DRAWING

| DATE CREATED | REVISIONS | | |
|---|---|---|---|
| | REV | DESCRIPTION | AUTHOR |
| 06/12/18 | 00 | INITIAL RELEASE | CM |
| | | | |

NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE




RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX±
ANGULAR ±

IDT®
www.IDT.com
6024 Silver Creek Valley Road
San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

TITLE LGA-48 Package Outline Drawing
7.0 x 7.0 mm Body Epad 5.0 x 5.0 mm
0.5mm Pitch LGR48

| SIZE | DRAWING No. | REV |
|---|---|---|
| C | PSC-4760 | 00 |

DO NOT SCALE DRAWING

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.