OptiMOS™-T2 Power-Transistor

AEC Qualified

RoHS

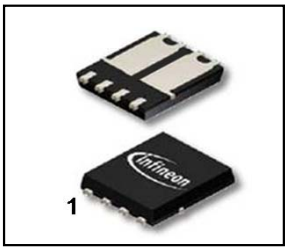
Product Summary

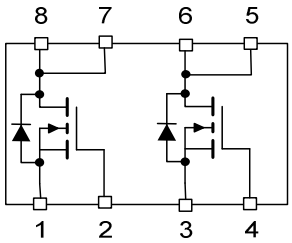
V_{DS}	60	V
$R_{DS(on),max}$ [4]	26	mΩ
I_D	20	A

Features

- Dual N-channel Logic Level - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested
- Feasible for automatic optical inspection (AOI)

PG-TDSON-8-10





Type	Package	Marking
IPG20N06S4L-26A	PG-TDSON-8-10	4N06L26

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current one channel active	I_D	T_C=25 °C, V_{GS}=10 V [1]	20	A
		T_C=100 °C, V_{GS}=10 V [2]	18	
Pulsed drain current [2] one channel active	$I_{D,pulse}$	-	80	
Avalanche energy, single pulse [2, 4]	E_{AS}	I_D=10A	35	mJ
Avalanche current, single pulse [4]	I_{AS}	-	15	A
Gate source voltage	V_{GS}	-	±16	V
Power dissipation one channel active	P_{tot}	T_C=25 °C	33	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	4.5	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	100	-	
		6 cm^2 cooling area[3]	-	60	-	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D= 1 mA	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D= 10µA	1.2	1.7	2.2	
Zero gate voltage drain current[4]	I_{DSS}	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C	-	0.01	1	µA
		V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C[2]	-	5	100	
Gate-source leakage current[4]	I_{GSS}	V_{GS}=16 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance[4]	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=10 A	-	31	46	mΩ
		V_{GS}=10 V, I_D=17 A	-	21	26	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance[4]	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	1100	1430	pF
Output capacitance[4]	C_{oss}		-	300	390	
Reverse transfer capacitance[4]	C_{rss}		-	18	36	
Turn-on delay time	$t_{d(on)}$	V_{DD}=30 V, V_{GS}=10 V, I_D=20 A, R_G=11 Ω	-	5	-	ns
Rise time	t_r		-	1.5	-	
Turn-off delay time	$t_{d(off)}$		-	18	-	
Fall time	t_f		-	10	-	
Gate Charge Characteristics[2, 4]						
Gate to source charge	Q_{gs}	V_{DD}=48 V, I_D=20 A, V_{GS}=0 to 10 V	-	4.3	5.6	nC
Gate to drain charge	Q_{gd}		-	1.7	3.4	
Gate charge total	Q_g		-	15	20	
Gate plateau voltage	$V_{plateau}$		-	3.9	-	V
Reverse Diode						
Diode continous forward current[2] one channel active	I_S	T_C=25 °C	-	-	20	A
Diode pulse current[2] one channel active	$I_{S,pulse}$		-	-	80	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=17 A, T_j=25 °C	-	0.95	1.3	V
Reverse recovery time[2]	t_{rr}	V_R=30 V, I_F=I_S, di_F/dt=100 A/µs	-	33	-	ns
Reverse recovery charge[2, 4]	Q_{rr}		-	30	-	nC

[1] Current is limited by bondwire; with an R_{thJC} = 4.5K/W the chip is able to carry 26.6A at 25°C.

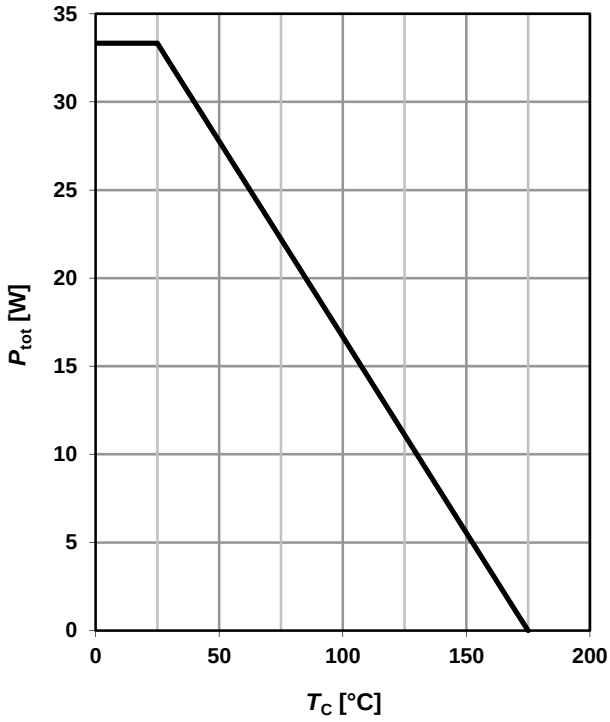
[2] Specified by design. Not subject to production test.

[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[4] Per channel

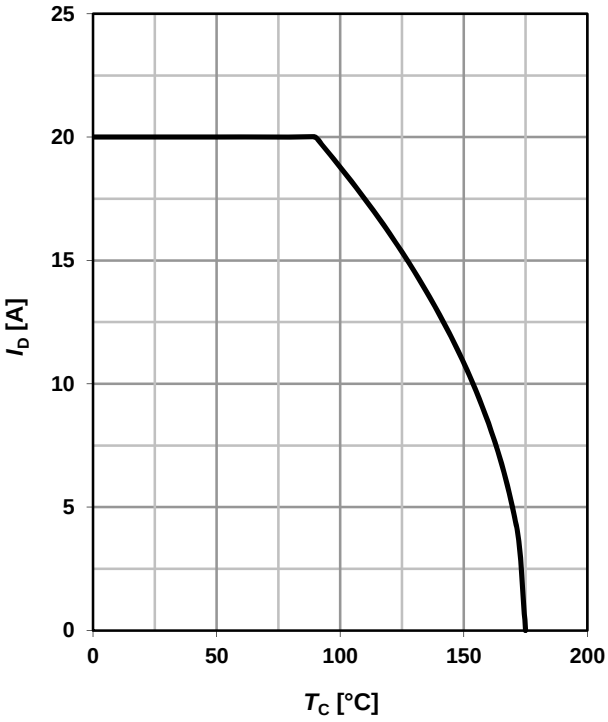
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V; one channel active



2 Drain current

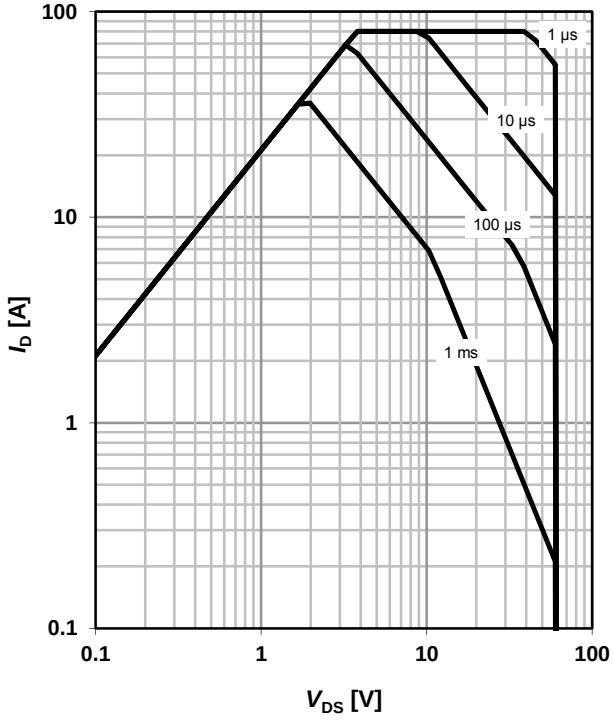
$I_D = f(T_C)$; $V_{GS} \geq 6$ V; one channel active



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$°C; $D = 0$; one channel active

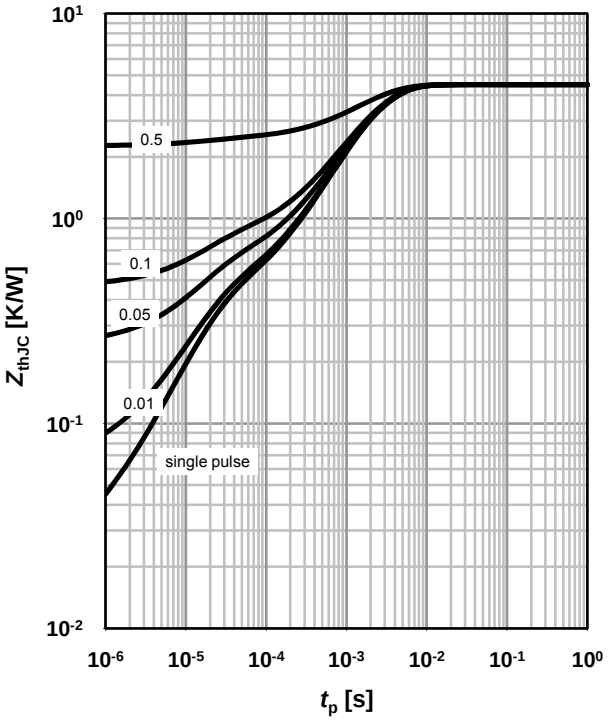
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

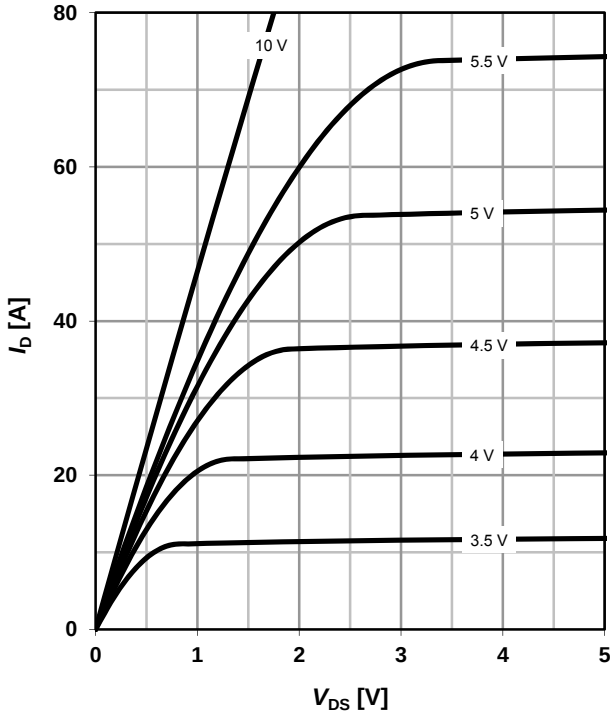
parameter: $D = t_p/T$



5 Typ. output characteristics[4)]

$I_D = f(V_{DS})$; $T_j = 25$ °C

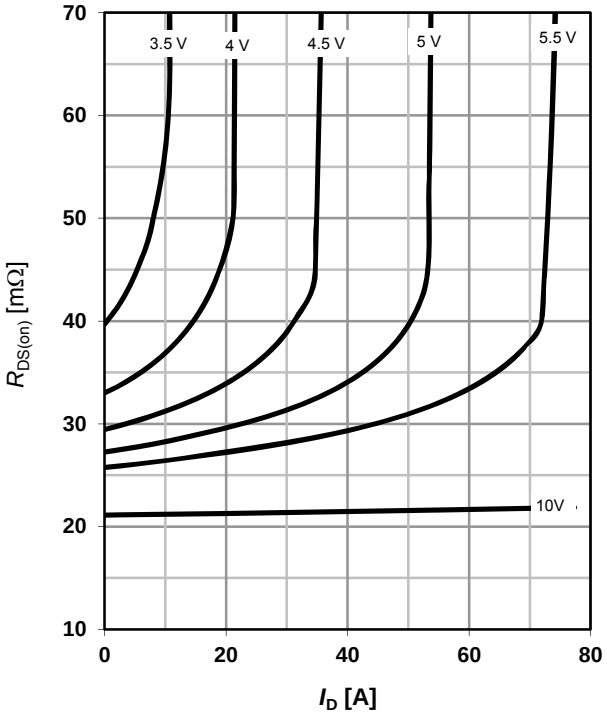
parameter: V_{GS}



6 Typ. drain-source on-state resistance[4)]

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C

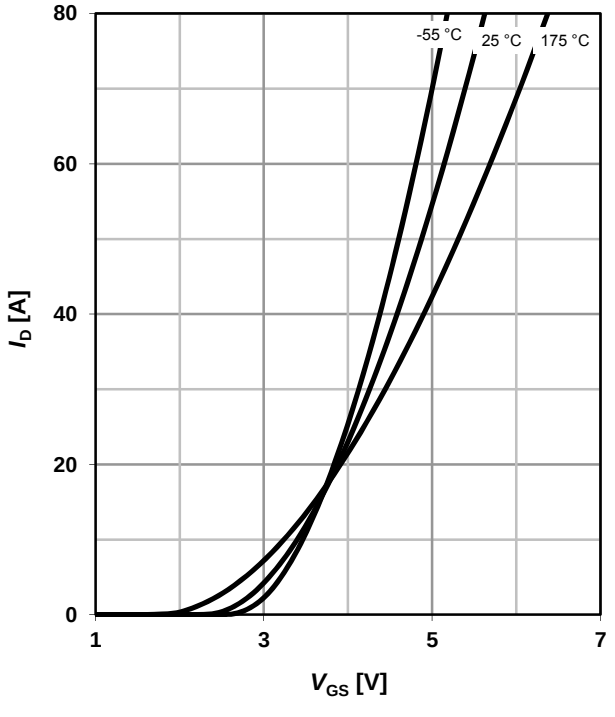
parameter: V_{GS}



7 Typ. transfer characteristics[4)]

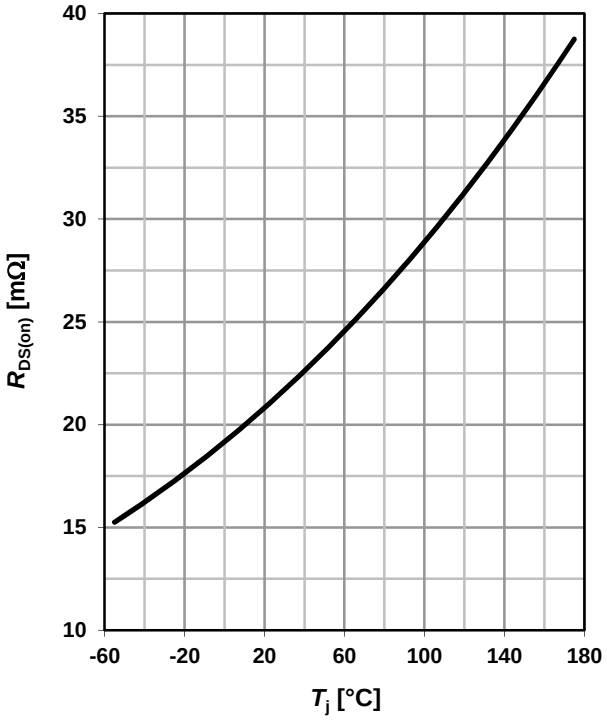
$I_D = f(V_{GS})$; $V_{DS} = 6$V

parameter: T_j



8 Typ. drain-source on-state resistance[4)]

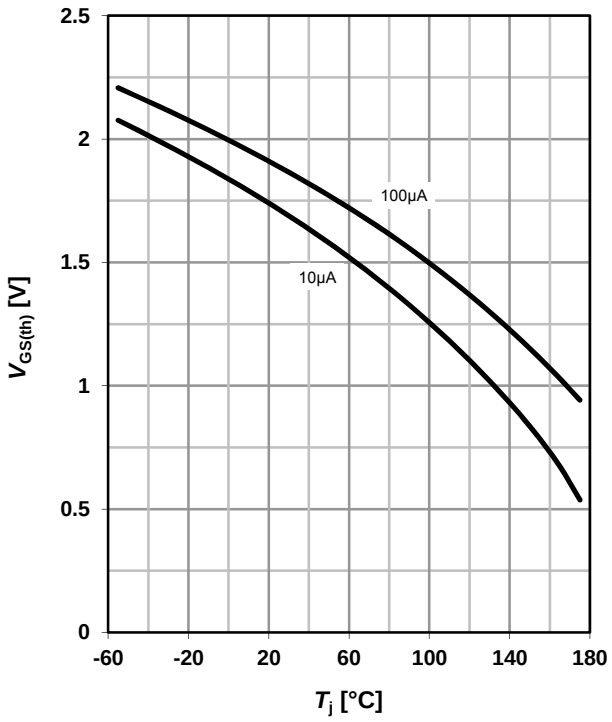
$R_{DS(on)} = f(T_j)$; $I_D = 17$ A; $V_{GS} = 10$ V



9 Typ. gate threshold voltage

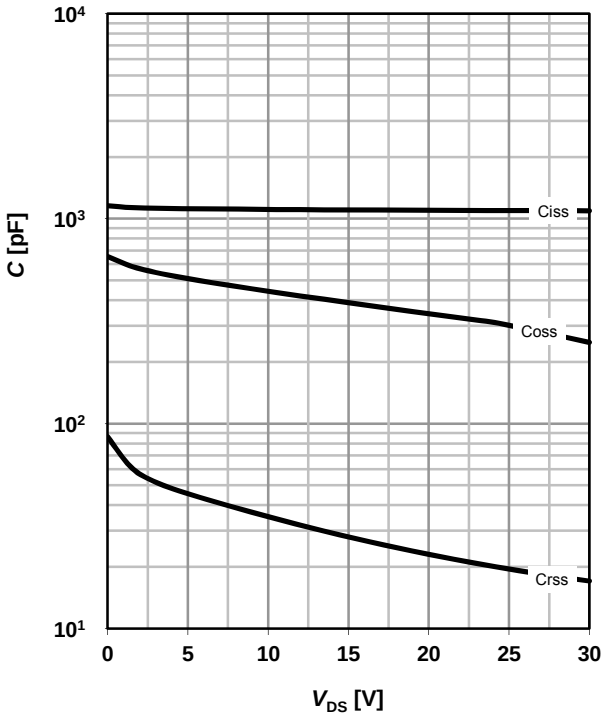
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. Capacitances[4)]

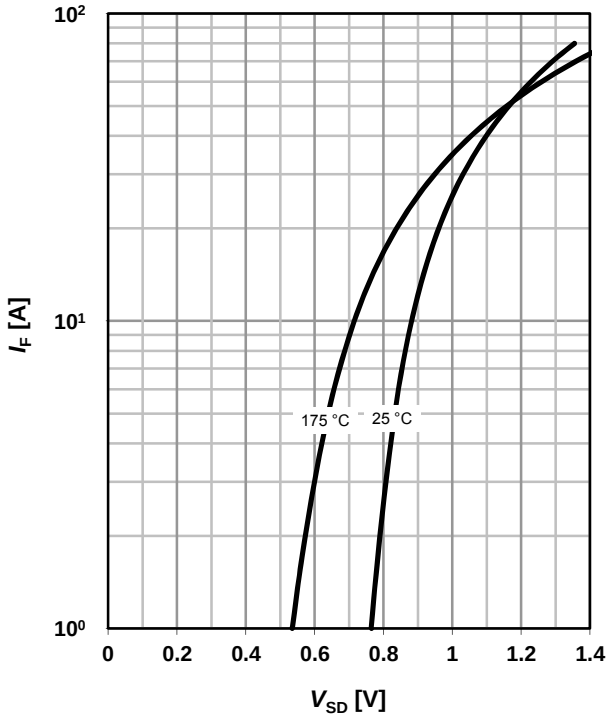
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristicis[4)]

IF = f(V_{SD})

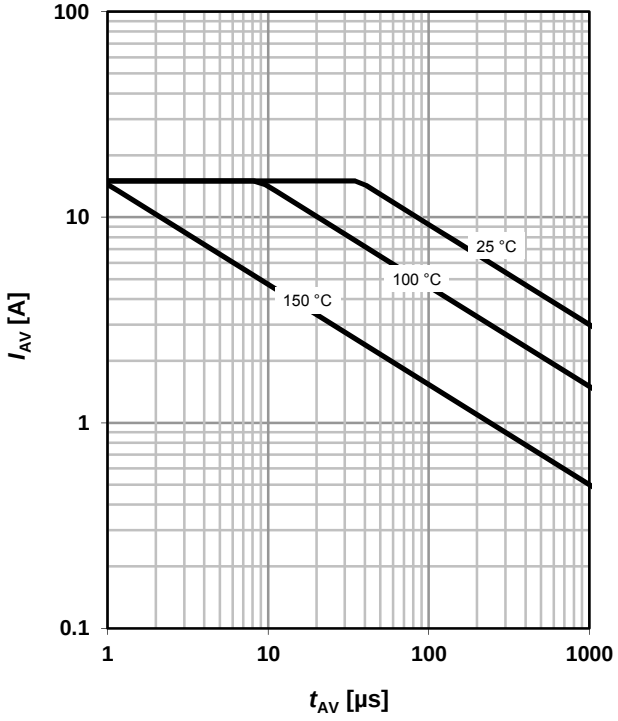
parameter: T_j



12 Avalanche characteristics[4)]

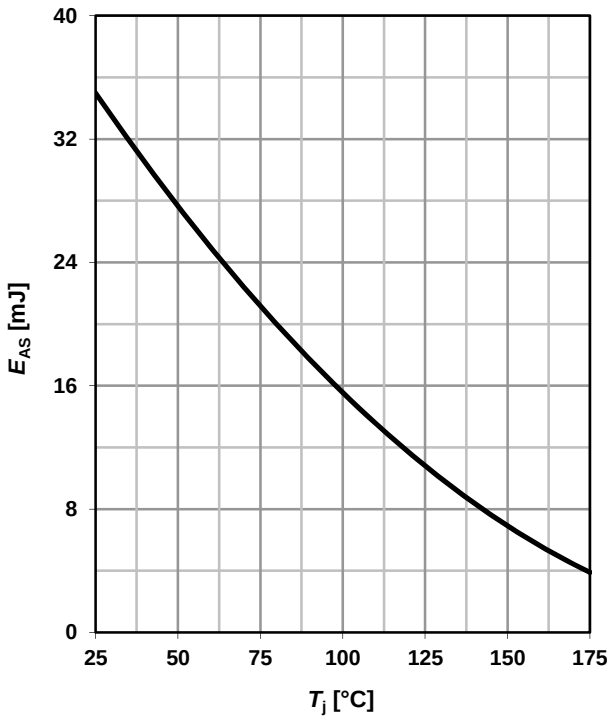
$I_{AS} = f(t_{AV})$

parameter: $T_{j(start)}$



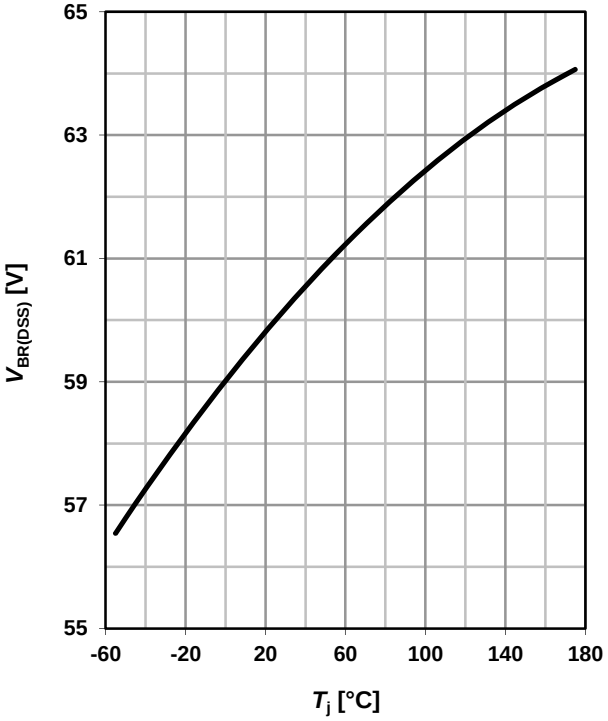
13 Avalanche energy[4)]

$E_{AS} = f(T_j)$, I_D = 10A



14 Drain-source breakdown voltage

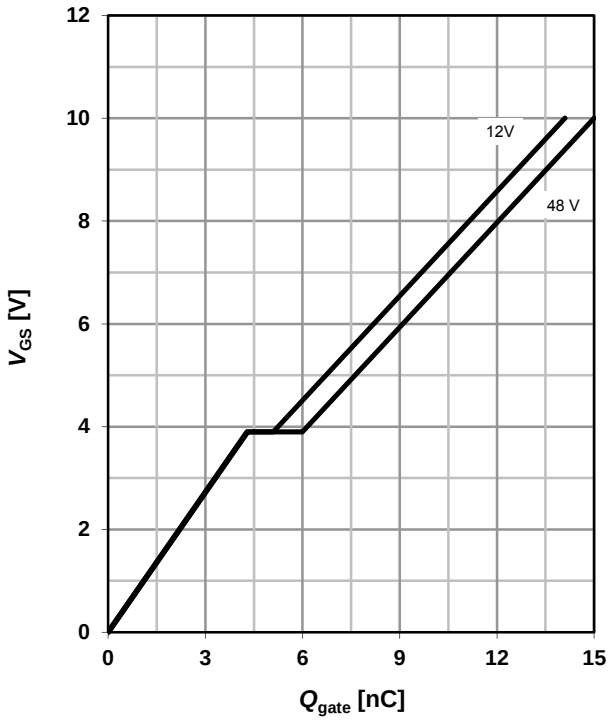
$V_{BR(DSS)} = f(T_j)$; I_D = 1 mA



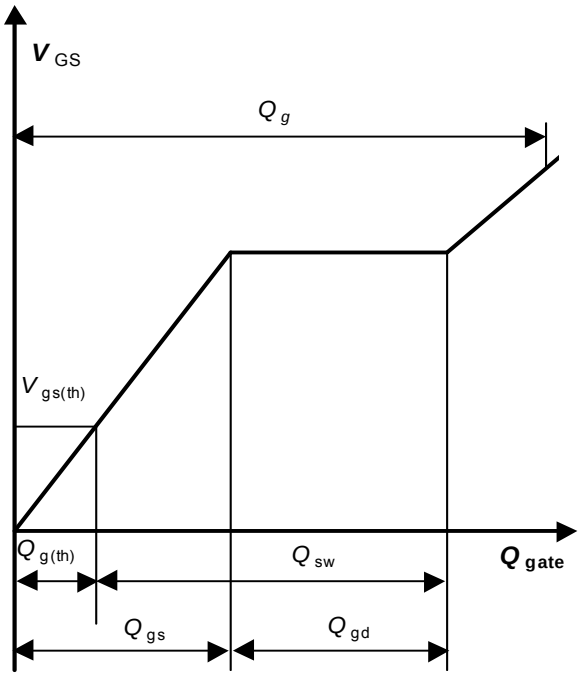
15 Typ. gate charge[4)]

$V_{GS} = f(Q_{gate})$; I_D = 20 A pulsed

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Revision 1.0	14.11.2012	Data Sheet revision 1.0