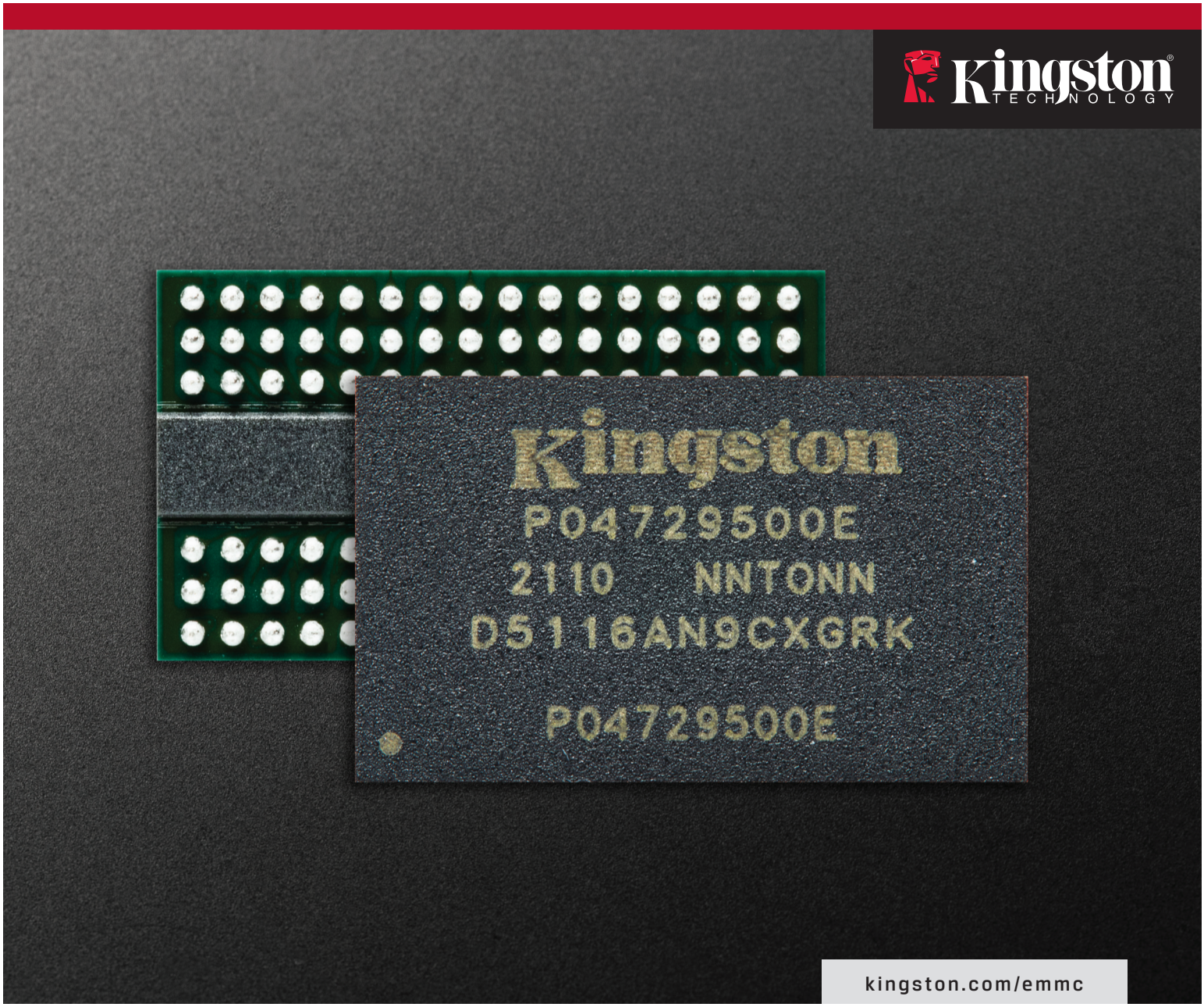


DRAM

Kingston DDR4 DRAM for embedded applications

Kingston on-board DDR4 DRAM is designed to meet the needs of embedded applications and offers a high speed option with lower power consumption.

MARKET SEGMENTS



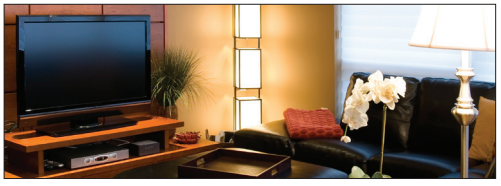
Industrial IoT / Robotics & Factory Automation



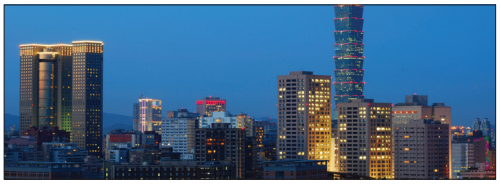
5G Networking/Telecommunications Communication Modules (WiFi Routers and Mesh Devices)



Office Equipment, Medical Devices, ATM, Vending Machines



Smart Home (Sound Bars, Thermostats, Fitness Equipment, Vacuums, Beds, Faucets)



Smart City (HVAC, Lighting, Power Monitoring/ Metering, Parking Meters)

DDR4 PART NUMBERS AND SPECIFICATIONS

Part Number	Capacity	Description	Package	Configuration (Words x Bits)	Speed Mbps	VDD, VDDQ	Operating Temperature
D5116AN9CXGRK	8Gb	96 ball FBGA DDR4 C-Temp	7.5x13x1.2	512Mx16	2666 Mbps	1.2V	0°C ~ +95°C

KEY FEATURES

- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center- aligned with data for WRITEs
- Differential clock inputs (CK_t and CK_c)
- DLL aligns DQ and DQS transitions with CK transitions
- Data mask (DM) write data-in at the both rising and falling edges of the data strobe
- Write Cycle Redundancy Code (CRC) is supported
- Programmable preamble for read and write is supported
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- Driver strength selected by MRS
- Dynamic On Die Termination supported
- Two Termination States such as RTT_PARK and RTT_NOM switchable by ODT pin
- Asynchronous RESET pin supported
- ZQ calibration supported
- Write Levelization supported
- This product in compliance with the RoHS directive
- Internal Vref DQ level generation is available
- TCAR (Temperature Controlled Auto Refresh) mode is supported.
- LP ASR (Low Power Auto Self Refresh) mode is supported
- Command Address (CA) Parity (command/address) mode is supported
- Per DRAM Addressability (PDA)
- Fine granularity refresh is supported
- Geardown Mode(1/2 rate, 1/4 rate) is supported
- Self Refresh Abort is supported
- Maximum power saving mode is supported
- Banks Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- DMI pin support for write data masking and DBIdc functionality

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