

Four Output Differential Fanout Buffer for PCI Express Gen 1 & 2

ICS9DBL411A

Recommended Application:

PCI-Express fanout buffer

Output Features:

- 4 - low power differential output pairs
- Individual OE# control of each output pair

Key Specifications:

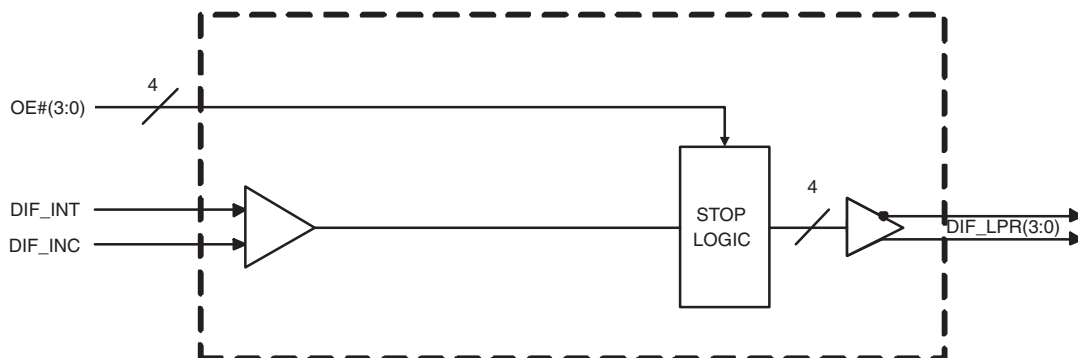
- Output cycle-cycle jitter < 25ps additive
- Output to output skew: < 50ps

Power Groups

| Pin Number (TSSOP) | | Description |
|--------------------|-------|-----------------------|
| VDD | GND | |
| 9,18 | 10,17 | VDD_IO for DIF(3:0) |
| 4 | 5 | 3.3V Analog VDD & GND |

| Pin Number (MLF) | | Description |
|------------------|------|-----------------------|
| VDD | GND | |
| 6,15 | 7,14 | VDD_IO for DIF(3:0) |
| 1 | 2 | 3.3V Analog VDD & GND |

Functional Block Diagram



Pin Configuration

| | | | | |
|-----------|----|-------------------|----|-----------|
| OE0# | 1 | ICS9DBL411 | 20 | DIF0T_LPR |
| DIF_INC | 2 | | 19 | DIF0C_LPR |
| DIF_INT | 3 | | 18 | VDD_IO |
| VDDA | 4 | | 17 | GND |
| GND | 5 | | 16 | OE1# |
| OE3# | 6 | | 15 | DIF1T_LPR |
| DIF3C_LPR | 7 | | 14 | DIF1C_LPR |
| DIF3T_LPR | 8 | | 13 | OE2# |
| VDD_IO | 9 | | 12 | DIF2T_LPR |
| GND | 10 | | 11 | DIF2C_LPR |

20-pin TSSOP

| | | | | | | | | | |
|-----------|---|--------|---------|-----------|-----------|-----------|-----------|-----------|--|
| | | | DIF_INT | DIF_INC | OE0# | DIF0T_LPR | DIF0C_LPR | | |
| | | 20 | 19 | 18 | 17 | 16 | | | |
| VDDA | 1 | | | | | | 15 | VDD_IO | |
| GND | 2 | | | | | | 14 | GND | |
| OE3# | 3 | | | | | | 13 | OE1# | |
| DIF3C_LPR | 4 | | | | | | 12 | DIF1T_LPR | |
| DIF3T_LPR | 5 | | | | | | 11 | DIF1C_LPR | |
| | | 6 | 7 | 8 | 9 | 10 | | | |
| | | VDD_IO | GND | DIF2C_LPR | DIF2T_LPR | OE2# | | | |

20-pin MLF

TSSOP Pin Description

| PIN # (TSSOP) | PIN NAME | PIN TYPE | DESCRIPTION |
|------------------|-----------|----------|--|
| 1 | OE0# | IN | Output Enable for DIF0 output. Control is as follows: 0 = enabled, 1 = Low-Low |
| 2 | DIF_INC | IN | Complement side of differential input clock |
| 3 | DIF_INT | IN | True side of differential input clock |
| 4 | VDDA | PWR | 3.3V Power for the Analog Core |
| 5 | GND A | GND | Ground for the Analog Core |
| 6 | OE3# | IN | Output Enable for DIF3 output. Control is as follows: 0 = enabled, 1 = Low-Low |
| 7 | DIF3C_LPR | OUT | Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 8 | DIF3T_LPR | OUT | True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 9 | VDD_IO | PWR | Power supply for low power differential outputs, nominal 1.05V to 3.3V |
| 10 | GND | GND | Ground pin |
| 11 | DIF2C_LPR | OUT | Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 12 | DIF2T_LPR | OUT | True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 13 | OE2# | IN | Output Enable for DIF2 output. Control is as follows: 0 = enabled, 1 = Low-Low |
| 14 | DIF1C_LPR | OUT | Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 15 | DIF1T_LPR | OUT | True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 16 | OE1# | IN | Output Enable for DIF1 output. Control is as follows: 0 = enabled, 1 = Low-Low |
| 17 | GND | GND | Ground pin |
| 18 | VDD_IO | PWR | Power supply for low power differential outputs, nominal 1.05V to 3.3V |
| 19 | DIF0C_LPR | OUT | Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 20 | DIF0T_LPR | OUT | True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |

MLF Pin Description

| PIN # (MLF) | PIN NAME | PIN TYPE | DESCRIPTION |
|-------------|-----------|----------|--|
| 1 | VDDA | PWR | 3.3V Power for the Analog Core |
| 2 | GNDA | GND | Ground for the Analog Core |
| 3 | OE3# | IN | Output Enable for DIF3 output. Control is as follows: 0 = enabled, 1 = Low-Low |
| 4 | DIF3C_LPR | OUT | Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 5 | DIF3T_LPR | OUT | True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 6 | VDD_IO | PWR | Power supply for low power differential outputs, nominal 1.05V to 3.3V |
| 7 | GND | GND | Ground pin |
| 8 | DIF2C_LPR | OUT | Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 9 | DIF2T_LPR | OUT | True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 10 | OE2# | IN | Output Enable for DIF2 output. Control is as follows: 0 = enabled, 1 = Low-Low |
| 11 | DIF1C_LPR | OUT | Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 12 | DIF1T_LPR | OUT | True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 13 | OE1# | IN | Output Enable for DIF1 output. Control is as follows: 0 = enabled, 1 = Low-Low |
| 14 | GND | GND | Ground pin |
| 15 | VDD_IO | PWR | Power supply for low power differential outputs, nominal 1.05V to 3.3V |
| 16 | DIF0C_LPR | OUT | Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 17 | DIF0T_LPR | OUT | True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed) |
| 18 | OE0# | IN | Output Enable for DIF0 output. Control is as follows: 0 = enabled, 1 = Low-Low |
| 19 | DIF_INC | IN | Complement side of differential input clock |
| 20 | DIF_INT | IN | True side of differential input clock |

Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|------------------------|-----------------|-------------------------------------|-----------------------|-----|-------|-------|
| Maximum Supply Voltage | VDDA | Core Supply Voltage | | 4.6 | V | 1,7 |
| Maximum Supply Voltage | VDD_IO | Low-Voltage Differential I/O Supply | 0.99 | 3.8 | V | 1,7 |
| Maximum Input Voltage | V _{IH} | 3.3V LVCMOS Inputs | | 4.6 | V | 1,7,8 |
| Minimum Input Voltage | V _{IL} | Any Input | V _{SS} - 0.5 | | V | 1,7 |
| Storage Temperature | T _s | - | -65 | 150 | °C | 1,7 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | V | 1,7 |

Electrical Characteristics - Input/Supply/Common Output Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|---------------------------------|-------------------------|--|-----------------------|-----------------------|---------|-------|
| Ambient Operating Temp | T _{ambient} | - | 0 | 70 | °C | 1 |
| Supply Voltage | VDDxxx | Supply Voltage | 3.135 | 3.465 | V | 1 |
| Supply Voltage | VDDxxx_IO | Low-Voltage Differential I/O Supply | 0.99 | 3.465 | V | 1 |
| Input High Voltage | V _{IHSE} | Single-ended inputs | 2 | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{ILSE} | Single-ended inputs | V _{SS} - 0.3 | 0.8 | V | 1 |
| Differential Input High Voltage | V _{IHDIF} | Differential inputs (single-ended measurement) | 600 | 1.15 | V | 1 |
| Differential Input Low Voltage | V _{ILDIF} | Differential inputs (single-ended measurement) | V _{SS} - 0.3 | 300 | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | 8 | V/ns | 2 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | 5 | uA | 1 |
| Operating Supply Current | I _{DD_3.3V} | 3.3V supply | | 25 | mA | 1 |
| | I _{DD_IO+100M} | VDD_IO supply @ fOP = 100MHz | | 15 | mA | 1 |
| | I _{DD_IO_400M} | VDD_IO supply @ fOP = 400MHz | | 54 | mA | 1 |
| Standby Current | I _{DD_SB33} | 3.3V supply, Input stopped, OE# pins all high | | 1 | mA | 1 |
| | I _{DD_SBio} | VDD_IO supply, Input stopped | | 0.1 | mA | 1 |
| Input Frequency | F _i | V _{DD} = 3.3 V | 33 | 400 | MHz | 2 |
| Pin Inductance | L _{pin} | | | 7 | nH | 1 |
| Input Capacitance | C _{IN} | Logic Inputs | 1.5 | 5 | pF | 1 |
| | C _{OUT} | Output pin capacitance | | 6 | pF | 1 |
| OE# latency | T _{OE#LAT} | Number of clocks to enable or disable output from assertion/deassertion of OE# | 1 | 3 | periods | 1 |
| Tdrive_OE# | T _{DROE#} | Output enable after OE# de-assertion | | 10 | ns | 1 |
| Tfall_OE# | T _{FALL} | Fall/rise time of OE# inputs | | 5 | ns | 1 |
| Trise_OE# | T _{RISE} | | | 5 | ns | 1 |

AC Electrical Characteristics - DIF Low Power Differential Outputs

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|-----------------------------------|--------------------|---|------|------|--------|-------|
| Rising Edge Slew Rate | t_{SLR} | Differential Measurement | 1 | 2.5 | V/ns | 1,2 |
| Falling Edge Slew Rate | t_{FLR} | Differential Measurement | 1 | 2.5 | V/ns | 1,2 |
| Slew Rate Variation | t_{SLVAR} | Single-ended Measurement | | 20 | % | 1 |
| Maximum Output Voltage | V_{HIGH} | Includes overshoot | | 1150 | mV | 1 |
| Minimum Output Voltage | V_{LOW} | Includes undershoot | -300 | | mV | 1 |
| Differential Voltage Swing | V_{SWING} | Differential Measurement | 1200 | | mV | 1 |
| Crossing Point Voltage | V_{XABS} | Single-ended Measurement | 300 | 550 | mV | 1,3,4 |
| Crossing Point Variation | $V_{XABSVAR}$ | Single-ended Measurement | | 140 | mV | 1,3,5 |
| Duty Cycle Distortion | $D_{CYCDIS0}$ | Differential Measurement, $f_{IN} \leq 100\text{MHz}$ | | 0.5 | % | 1,6 |
| | $D_{CYCDIS1}$ | Differential Measurement $100\text{MHz} < f_{IN} \leq 267\text{MHz}$ | | +5 | % | 1,6 |
| | $D_{CYCDIS2}$ | Differential Measurement, $f_{IN} > 267\text{MHz}$ | | +7 | % | 1,6 |
| DIF Jitter - Cycle to Cycle | $DIFJ_{C2C}$ | Differential Measurement, Additive | | 25 | ps | 1 |
| DIF[3:0] Skew | DIF_{SKEW} | Differential Measurement | | 50 | ps | 1 |
| Propagation Delay | t_{PD} | Input to output Delay | 2.5 | 3.5 | ns | 1 |
| PCIe Gen2 Phase Jitter - Additive | t_{phase_addHI} | $1.5\text{MHz} < f_{IN} < \text{Nyquist} (50\text{MHz})$ | | 0.8 | ps rms | 1 |
| PCIe Gen2 Phase Jitter - Additive | t_{phase_addLO} | $10\text{KHz} < f_{IN} < 1.5\text{MHz}$ | | 0.1 | ps rms | 1 |

Notes on Electrical Characteristics:

¹Guaranteed by design and characterization, not 100% tested in production.

²Slew rate measured through V_{swing} centered around differential zero

³ V_{xabs} is defined as the voltage where $CLK = CLK\#$

⁴Only applies to the differential rising edge (CLK rising and CLK# falling)

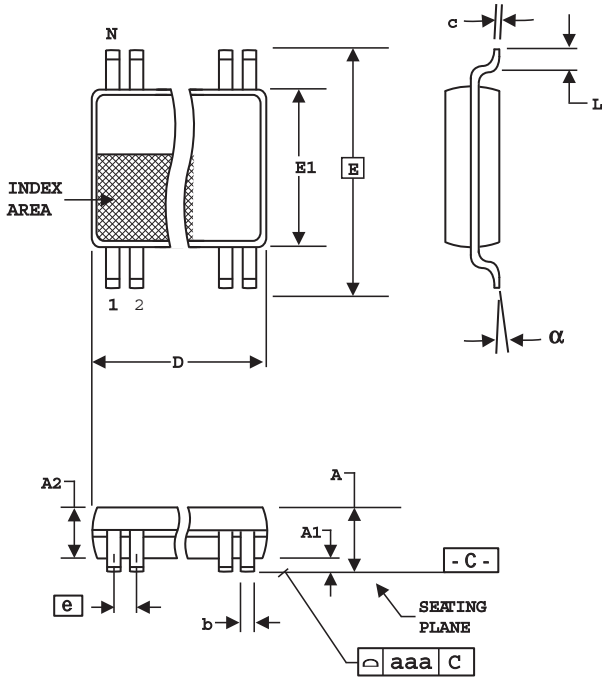
⁵Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

⁶This is the figure refers to the maximum distortion of the input wave form.

⁷Operation under these conditions is neither implied, nor guaranteed.

⁸Maximum input voltage is not to exceed maximum VDD

20-pin TSSOP Package Drawing and Dimensions



20-Lead, 4.40 mm. Body, 0.65 mm. Pitch TSSOP
(173 mil) (25.6 mil)

| SYMBOL | In Millimeters | | In Inches | |
|--------|-------------------|-------------------|-------------------|-------------------|
| | COMMON DIMENSIONS | COMMON DIMENSIONS | COMMON DIMENSIONS | COMMON DIMENSIONS |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.19 | 0.30 | .007 | .012 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | .169 | .177 |
| e | 0.65 BASIC | | 0.0256 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| a | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

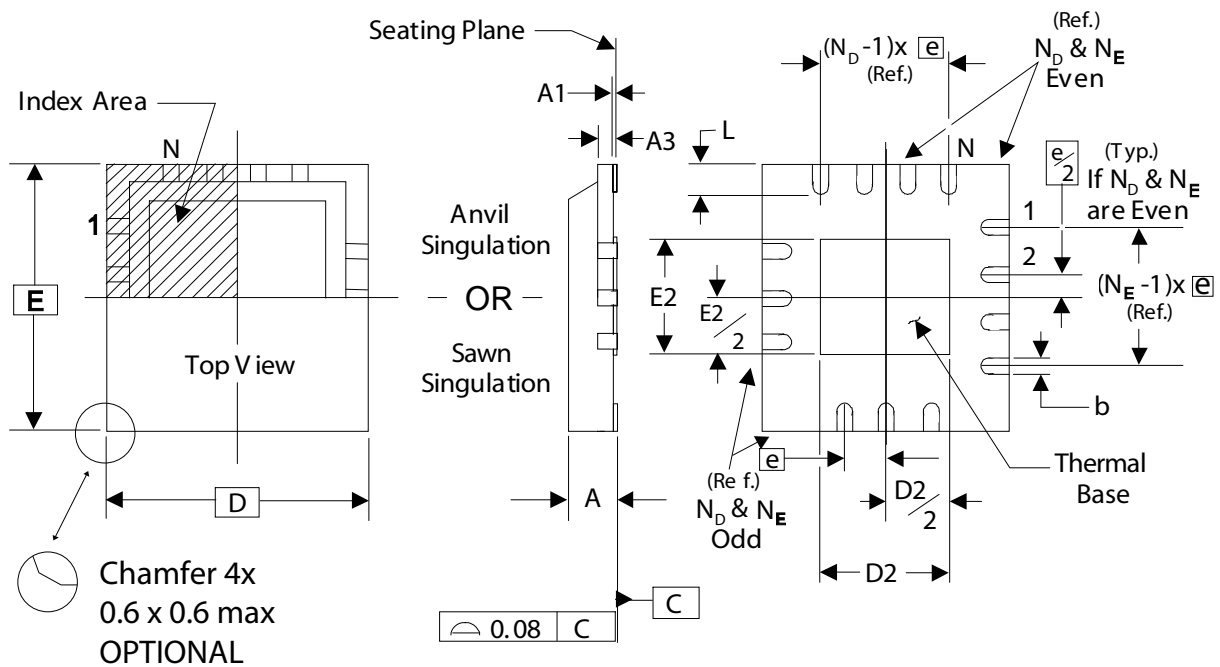
VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|------|----------|------|
| | MIN | MAX | MIN | MAX |
| 20 | 6.40 | 6.60 | .252 | .260 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

20-pin MLF Package Drawing and Dimensions



THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS

| SYMBOL | MIN. | MAX. |
|--------|----------------|------|
| A | 0.8 | 1.0 |
| A1 | 0 | 0.05 |
| A3 | 0.20 Reference | |
| b | 0.18 | 0.3 |
| e | 0.50 BASIC | |

DIMENSIONS

| SYMBOL | ICS 20L TOLERANCE |
|----------------|-------------------|
| N | 20 |
| N_D | 5 |
| N_E | 5 |
| D x E BASIC | 4.00 x 4.00 |
| D2 MIN. / MAX. | 2.00 / 2.25 |
| E2 MIN. / MAX. | 2.00 / 2.25 |
| L MIN. / MAX. | 0.45 / 0.65 |

Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---------------------|--------------------|--------------|-------------|
| 9DBL411AKLF | Tubes | 20-pin MLF | 0 to +70°C |
| 9DBL411AKLFT | Tape and Reel | 20-pin MLF | 0 to +70°C |
| 9DBL411AGLF | Tubes | 20-pin TSSOP | 0 to +70°C |
| 9DBL411AGLFT | Tape and Reel | 20-pin TSSOP | 0 to +70°C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"A" is the device revision designator (will not correlate to the datasheet revision).

Revision History

| Rev. | Issue Date | Description | Page # |
|------|------------|--|--------|
| 0.1 | 8/1/2006 | Initial Release. | - |
| 0.2 | 9/22/2006 | Updated MLF Package Dimensions. | 8 |
| A | 7/31/2007 | 1. Updated electrical characteristics - additive jitter, cycle-to-cycle, tpd, skews, slew rates, Idd, etc. 2. Corrected power grouping table for TSSOP pkg 3. Final Release | 1,5,6 |
| B | 2/21/2008 | 1. Highlighted that V_{IHDIF} and V_{ILDIF} are single ended measurments. 2. Corrected VSWING paramater from 300mV to 1200mV. 3. Updated duty cycle distortion table with a 3rd figure for speeds $\leq 100\text{MHz}$. | 5 |
| C | 6/28/2012 | Typo for "Differential Input Low Voltage" units; changed "V" to "mV" | |

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