NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
TW2837

TW2824

FN7738
Rev. 0.00
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4-Channel Video QUAD/MUX Controller for Security Applications

The TW2824 has four high quality NTSC/PAL video decoders, dual color display controllers and dual video encoders. The TW2824 contains four 10-bit analog-to-digital converters, proprietary digital gain/clamp controller, high quality Y/C separator to reduce cross-noise and high performance dual scaler to provide various pictures. Four built-in motion and blind detectors can increase the feature of the security system. The TW2824 has a flexible video display controller including QUAD and MUX basic functions. The TW2824 also has an excellent graphic overlay function which displays character/bitmap, box and mouse pointer. The TW2824 contains two video encoders with four 10-bit digital-to-analog converters for providing 2 composite or S-video.

Features

Four Video Decoders

- Accepts all NTSC/PAL standard formats with auto detection
- Integrated four anti-aliasing filters and 10-bit CMOS ADCs
- High performance adaptive comb filters for all NTSC/PAL standards
- IF compensation filter for improvement of color demodulation
- PAL delay lines for correcting PAL phase errors
- Programmable hue, saturation, contrast, brightness and sharpness
- Dual high performance horizontal and vertical scaler for each channel.
- Four built-in motion detectors with 16x12 cells and blind detectors

Dual Video Controllers

- Additional 1-channel digital input for playback or cascade operation
- Full live/strobe/switch function
- Auto sequence switch with 64 queues and/or manual switch by interrupt
- Various channel attribute control
- Image enhancement for still image
- High performance 2x zoom for horizontal and vertical direction
- Supports save and recall function
- Last image capture when video-loss
- Extendable to 8-/12-/16-channel video controller using cascade connection
- Path-to-path cascade
- Character/bitmap overlay for OSD
- 16 programmable single boxes
- 4 2D arrayed boxes for motion result display
- Mouse pointer overlay

Dual Video Encoders

- 2 path digital outputs with ITU-R BT.656 standards
- 2 path analog outputs with all analog NTSC/PAL standards
- Supports CVBS or S-video for each path
- Programmable bandwidth for luminance and chrominance path
- Four 10-bit video CMOS DACs

Applications

- Analog QUAD/MUX system
- 4-/8-/16-channel DVR system
- Car rear vision system
- Hair shop system

Block Diagram

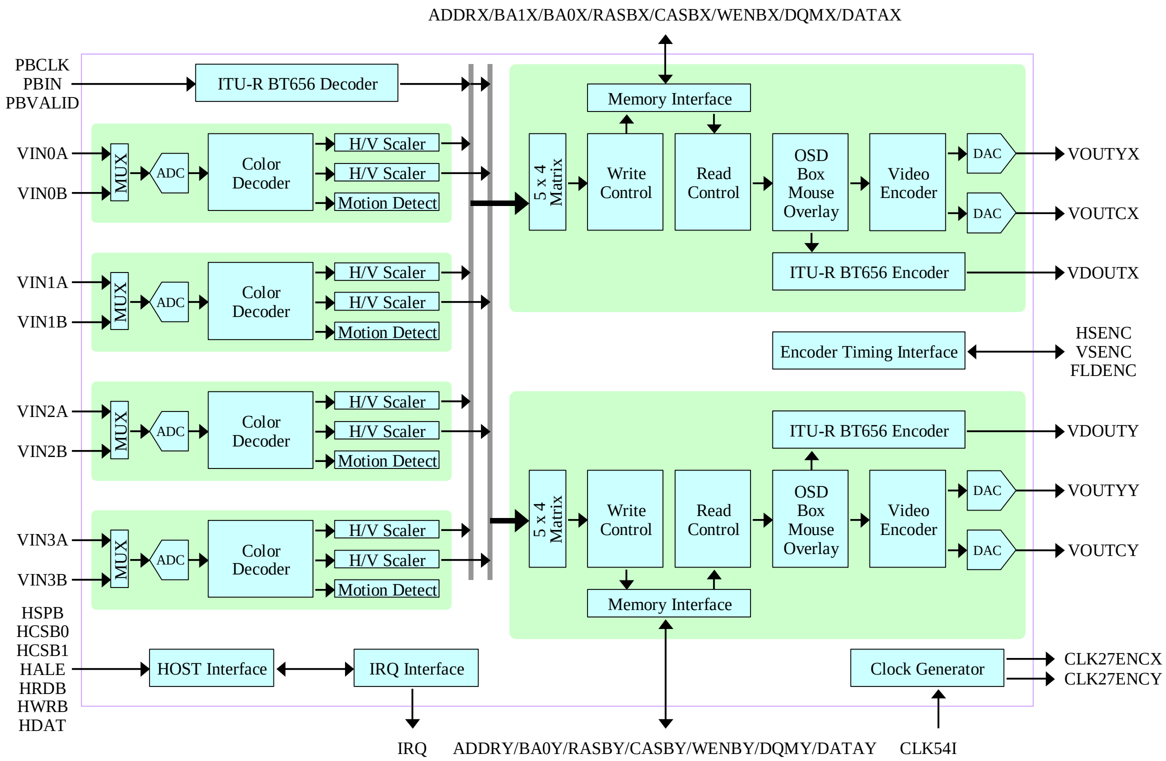


Table of Contents

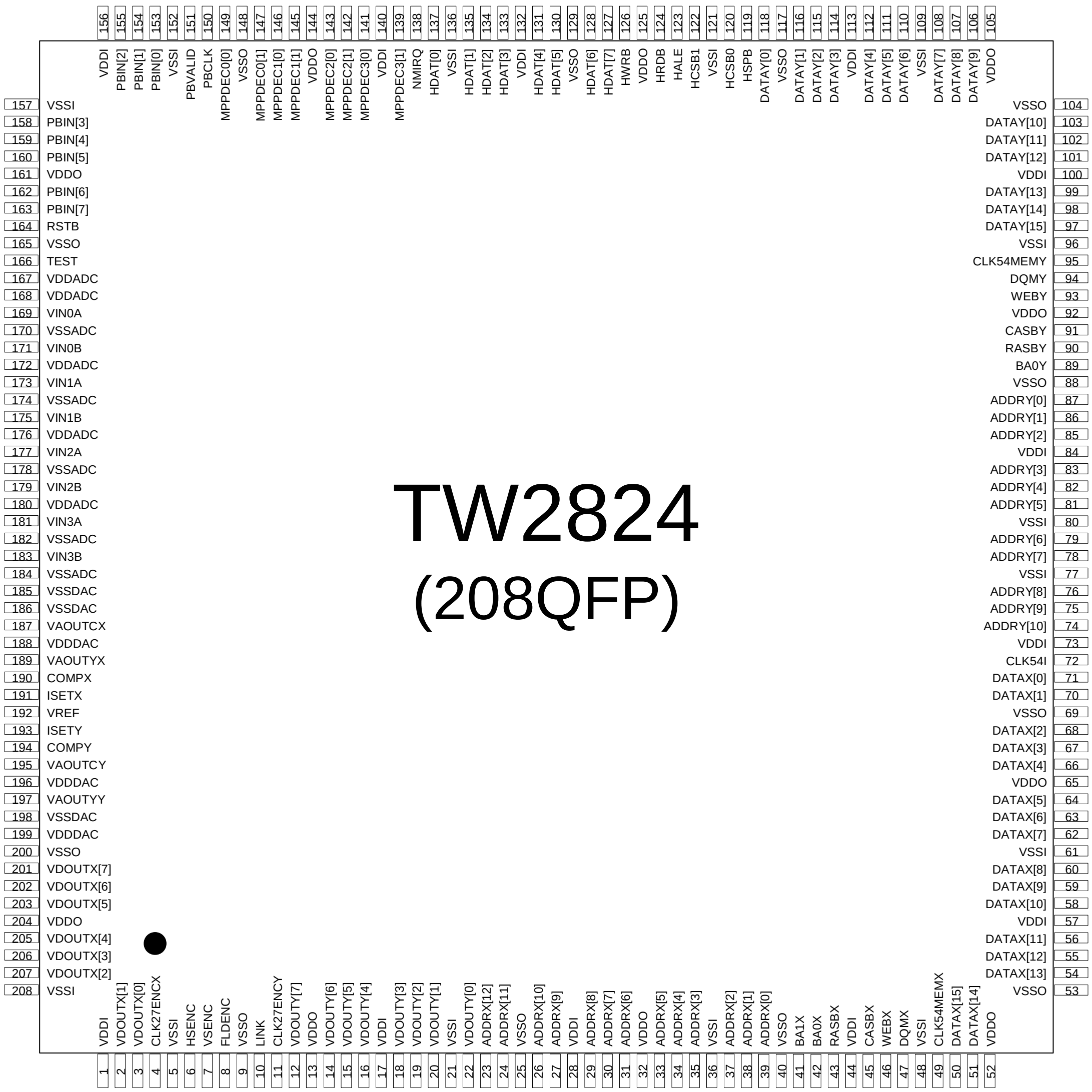
Device Options

Device Name	Description	MUX Function *1	Dual Output *2
TW2824M	QUAD/MUX function with dual outputs	O	O
TW2824Q	QUAD function with dual outputs	X	O
TW2824MS	QUAD/MUX function with single output	O	X
TW2824QS	QUAD function with single output	X	X

* Note 1. Refer to page 37 for device option of MUX function.

2. Refer to page 60 for device option of dual output.

Pin Diagram



Pin Description

Analog Interface Pins

Name	Number	Type	Description
VIN0A	169	A	Composite video input 0A. Must be connected through 2.2uF to input.
VIN0B	171	A	Composite video input 0B. Must be connected through 2.2uF to input.
VIN1A	173	A	Composite video input 1A. Must be connected through 2.2uF to input.
VIN1B	175	A	Composite video input 1B. Must be connected through 2.2uF to input.
VIN2A	177	A	Composite video input 2A. Must be connected through 2.2uF to input.
VIN2B	179	A	Composite video input 2B. Must be connected through 2.2uF to input.
VIN3A	181	A	Composite video input 3A. Must be connected through 2.2uF to input.
VIN3B	183	A	Composite video input 3B. Must be connected through 2.2uF to input.
VOUTYX	189	A	Composite/Luminance video output of X path.
VOUTCX	187	A	Composite/Chrominance video output of X path.
VOUTYY	197	A	Composite/Luminance video output of Y path.
VOUTCY	195	A	Composite/Chrominance video output of Y path.
COMPX	190	A	Compensation capacitance. Must be connected though 0.1uF to VDDDAC.
COMPY	194	A	Compensation capacitance. Must be connected though 0.1uF to VDDDAC.
ISETX	191	A	Current setting resistor for X path.
ISETY	193	A	Current setting resistor for Y path.
VREF	192	A	Voltage reference. Must be connected though 0.1uF to VSSDAC.

Digital Video Interface Pins

Name	Number	Type	Description
VDOUTX [7:0]	201,202,203, 205,206,207, 2,3	O	Digital video data output for X path or Chip-to-chip cascade connection pin.
VDOUTY [7:0]	12,14,15, 16,18,19, 20,22	O	Digital video data output for Y path.
CLK27ENCX	4	O	Clock of VDOUTX.
CLK27ENCY	11	O	Clock of VDOUTY.
HSENC	6	I/O	Encoder horizontal sync.
VSENC	7	I/O	Encoder vertical sync or Chip-to-chip cascade connection pin.
FLDENC	8	I/O	Encoder field flag.
LINK	10	I/O	Chip-to-chip cascade connection pin.
PBIN[7:0]	163,162,160, 159,158,155, 154,153	I	Video data of playback input or Chip-to-chip cascade connection pin.
PBVALID	151	I	Valid data indicator of PBIN or Chip-to-chip cascade connection pin.
PBCLK	150	I	Clock of PBIN.
MPPDEC3[1:0]	139,141	O	Multi-purpose output for VIN3 or CH3.
MPPDEC2[1:0]	142,143	O	Multi-purpose output for VIN2 or CH2.
MPPDEC1[1:0]	145,146	O	Multi-purpose output for VIN1 or CH1.
MPPDEC0[1:0]	147,149	O	Multi-purpose output for VIN0 or CH0.

Memory Interface Pins

Name	Number	Type	Description
DATAX[15:0]	50,51,54, 55,56,58, 59,60,62, 63,64,66, 67,68,70, 71	I/O	SDRAM data bus of X path.
ADDRX[12:0]	23,24,26, 27,29,30, 31,33,34, 35,37,38, 39	O	SDRAM address bus of X path . ADDRX[10] is AP.
BA1X	41	O	SDRAM bank1 selection of X path.
BA0X	42	O	SDRAM bank0 selection of X path.
RASBX	43	O	SDRAM row address selection of X path.
CASBX	45	O	SDRAM column address selection of X path.
WEBX	46	O	SDRAM write enable of X path.
DQMX	47	O	SDRAM write mask of X path.
CLK54MEMX	49	O	SDRAM clock of X path.
DATAY[15:0]	97,98,99, 101,102,103, 106,107,108, 110,111,112, 114,115,116, 118	I/O	SDRAM data bus of Y path.
ADDRY[10:0]	74,75,76, 78,79,81, 82,83,85, 86,87	O	SDRAM address bus of Y path. ADDRY[10] is AP.
BA0Y	89	O	SDRAM Bank0 Selection of Y path.
RASBY	90	O	SDRAM row address selection of Y path.
CASBY	91	O	SDRAM column address selection of Y path.
WEBY	93	O	SDRAM write enable of Y path.
DQMY	94	O	SDRAM write mask of Y path.
CLK54MEMY	95	O	SDRAM clock of Y path. Clock phase can be controlled via register.

System Control Pins

Name	Number	Type	Description
TEST	166	I	Only for the test purpose. Must be connected to VSSO.
RSTB	164	I	System reset.
NMIRQ	138	O	Interrupt request signal.
HDAT[7:0]	127,128,130, 131,133,134, 135,137	I/O	Data bus for parallel interface. HDAT[7] is serial data for serial interface. HDAT[6:1] is slaver address[6:1] for serial interface.
HWRB	126	I	Write enable for parallel interface. VSSO for serial interface.
HRDB	124	I	Read enable for parallel interface. VSSO for serial interface.
HALE	123	I	Address line enable for parallel interface. Serial clock for serial interface.
HCSB1	122	I	Chip select 1 for parallel interface. VSSO for serial interface.
HCSB0	120	I	Chip select 0 for parallel interface. Slaver address[0] for serial interface.
HSPB	119	I	Select serial/parallel host interface.
CLK54I	72	I	54MHz system clock.
LINK	10	I/O	Cascade connection.

Power / Ground Pins

Name	Number	Type	Description
VDDO	204,161,144, 125,105,92, 65,52,32, 13	P	Digital power for output driver. 3.3V.
VSSO	200,165,148, 129,117,104, 88,69,53, 40,25,9	G	Digital ground for output driver.
VDDI	156,140,132, 113,100,84, 73,57,44, 28,17,1	P	Digital power for internal logic. 2.5V.
VSSI	208,157,152, 136,121,109, 96,80,77, 61,48,36, 21,5	G	Digital ground for internal logic.
VDDDAC	199, 196,188	P	Analog power for DAC. 2.5V.
VSSDAC	198,186, 185	G	Analog ground for DAC.
VDDADC	180,176,172, 168, 167	P	Analog power for ADC. 2.5V.
VSSADC	184, 182,178, 174, 170	G	Analog ground for ADC.

Functional Description

Video Input

The TW2824 has 5 input interfaces that consist of 1 digital video input from external video decoder and 4 analog composite video inputs. Digital video input is decoded by internal ITU-R BT656 decoder and then fed to X and Y video control part. 4 analog video inputs are converted to digital video stream through 10bit ADC and luminance/chrominance processor in built-in video decoder. Each built-in video decoder has its own motion detector and dual scaler also. The scaled digital video data are transferred to X and Y video control part. The structure of video input and decoder part is shown in the following Fig 1.

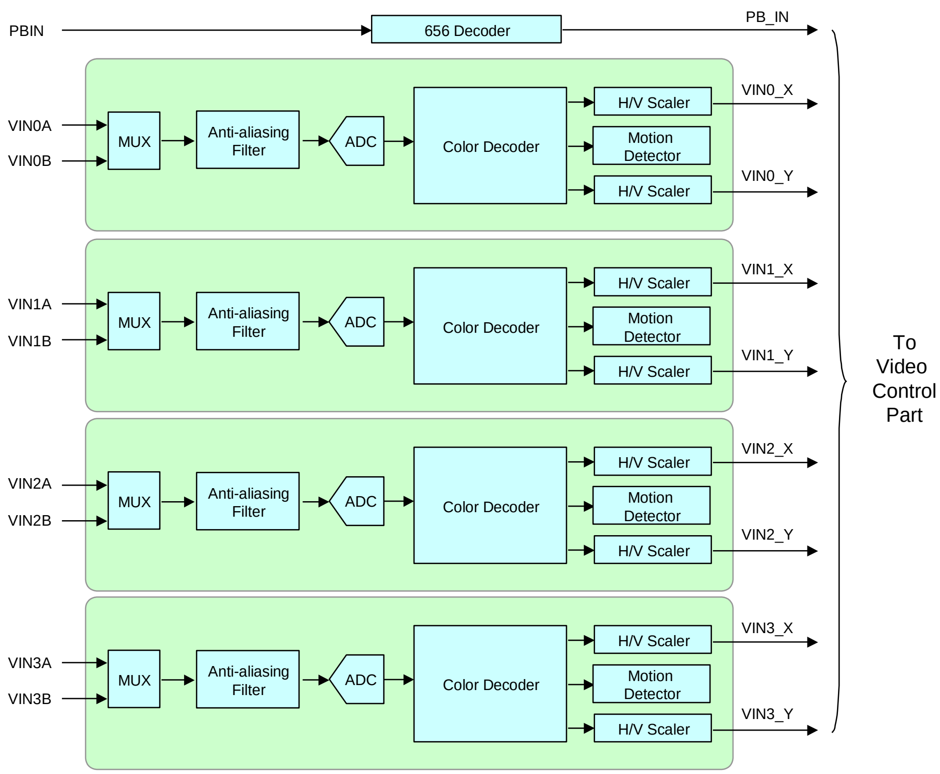


Fig 1 Structure of video input and decoder part

ANALOG VIDEO INPUT

The TW2824 supports all NTSC/PAL video standards for analog input and contains automatic standard detection circuit. Automatic standard detection can be overridden by writing the value into the IFMTMAN and IFORMAT (0x01, 0x41, 0x81, 0xC1) registers. Even if video loss is detected, the TW2824 can be forced to free-running in a particular video standard mode for fast locking by programming IFORMAT register. The Table 1 shows the video input standards supported by TW2824.

Table 1 Video input standards

Format	Line/Fv (Hz)	Fh (KHz)	Fsc (MHz)
NTSC-M* NTSC-J	525/59.94	15.734	3.579545
NTSC-4.43*	525/59.94	15.734	4.43361875
NTSC-N	625/50	15.625	3.579545
PAL-BDGHI PAL-N*	625/50	15.625	4.43361875
PAL-M*	525/59.94	15.734	3.57561149
PAL-NC	625/50	15.625	3.58205625
PAL-60	525/59.94	15.734	4.43361875

Notes: * 7.5 IRE Setup

Analog-to-Digital Converter

The TW2824 contains four 10-bit Analog to Digital converters that digitizes the analog video inputs. As the inputs are digitized at greater than two times that of the Nyquist sampling rate, only simple external anti-aliasing LPF are needed to prevent out-of-band frequencies. Each ADC has two analog switches that are controlled by the ANA_SW (0x22, 0x62, 0xA2, 0xE2) register. The A/D converters can also be put into power-down mode by the ADC_PWDN (0x78) register.

Sync Processing

The sync processor of TW2824 detects horizontal synchronization and vertical synchronization signals in the composite video signal. The TW2824 utilizes proprietary technology for locking to weak, noisy, or unstable signals such as those from on air signal or fast forward/backward play of VCR system.

A digital gain and clamp control circuit restores the ac coupled video signal to a fixed dc level. The clamping circuit provides line-by-line restoration of the video pedestal level to a fixed dc reference voltage. In no AGC mode, the gain control circuit adjusts only the video sync gain to achieve desired sync amplitude so that the active video is bypassed regardless of the gain control. But when AGC mode is enabled, both active video and sync are adjusted by the gain control.

The horizontal synchronization processor contains a sync separator, a PLL and the related decision logic. The horizontal sync separator detects the horizontal sync by examining low-pass filtered video input whose level is lower than a threshold. Additional logic is also used to avoid false detection on glitches. The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide jitter free image output. In case of missing horizontal sync, the PLL is on free running status that matches the standard raster frequency.

The vertical sync separator detects the vertical synchronization pattern in the input video signals. The field status is determined at vertical synchronization time. When the location of the detected vertical sync is inline with a horizontal sync, it indicates a frame start or the odd field start. Otherwise, it indicates an even field.

Color Decoding

The digitized composite video data at 2X pixel clock rate first passes through decimation filter. The decimation filter is required to achieve optimum performance and prevent high frequency components from being aliased back into the video image. Fig 2 shows the frequency characteristic of the decimation filter.

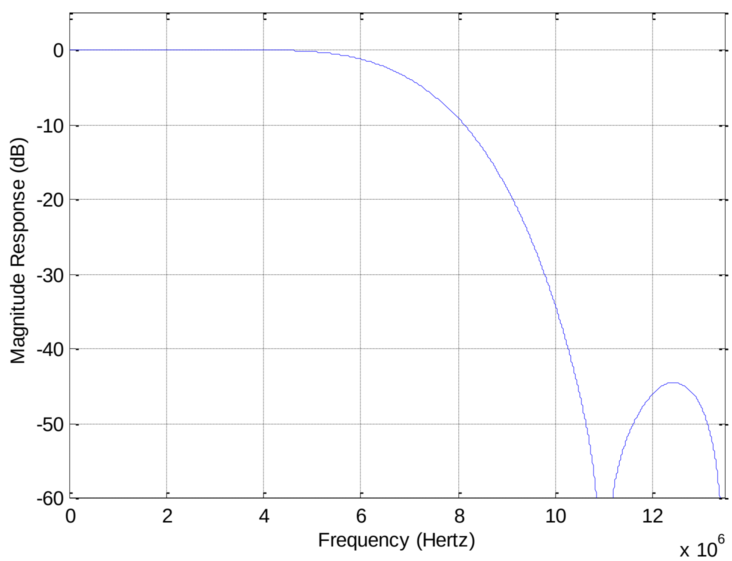


Fig 2 The frequency characteristic of the decimation Filter

The adaptive comb filter is used for high performance luminance/chrominance separation from NTSC/PAL composite video signals. The comb filter improves the luminance resolution and reduces noise such as cross-luminance and cross-color. The adaptive algorithm eliminates most of errors without introducing new artifacts or noise. To accommodate some viewing preferences, additional chrominance trap filters are also available in the luminance path.

Fig 3 and Fig 4 show the frequency response of notch filter for each system NTSC and PAL.

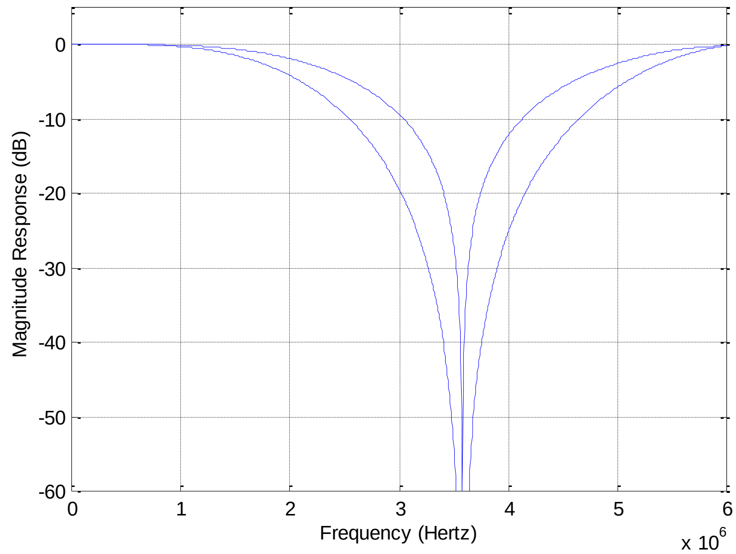


Fig 3 The frequency response of luminance notch filter for NTSC

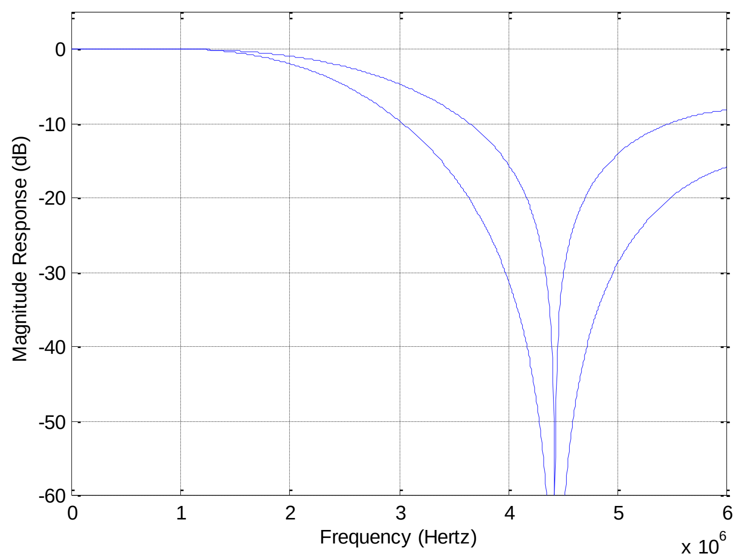


Fig 4 The frequency response of luminance notch filter for PAL

Luminance Processing

The luminance signal that is separated by adaptive comb or trap filter is then fed to a peaking circuit. The peaking filter enhances the high frequency components of the luminance signal via the Y_PEAK (0x14, 0x54, 0x94, 0xD4) register. The following Fig 5 shows the characteristics of the peaking filter for four different gain modes.

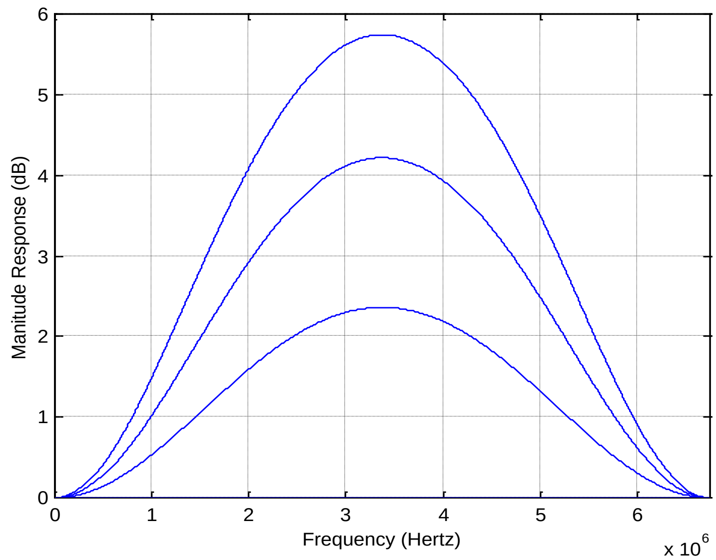


Fig 5 The frequency characteristic of luminance peaking filter

The picture contrast and brightness adjustment is provided through the CONT (0x11, 0x51, 0x91, 0xD1) and BRT (0x12, 0x52, 0x92, 0xD2) registers. The contrast adjustment range is from approximately 0 to 200 percent and the brightness adjustment is in the range of ±25 IRE. Moreover, a high frequency coring function is also embedded in TW2824 to minimize a high frequency noise. The coring level is adjustable through the Y_H_CORE (0xF8) register.

Chrominance Processing

The chrominance demodulation is done by first quadrature mixing for NTSC and PAL. The mixing frequency is equal to the sub-carrier frequency of NTSC and PAL. After the mixing, a LPF is used to remove 2X carrier signal and yield chrominance components. The characteristic of LPF can be selected for optimized transient color performance. Fig 6 is showing the frequency response of chrominance LPF.

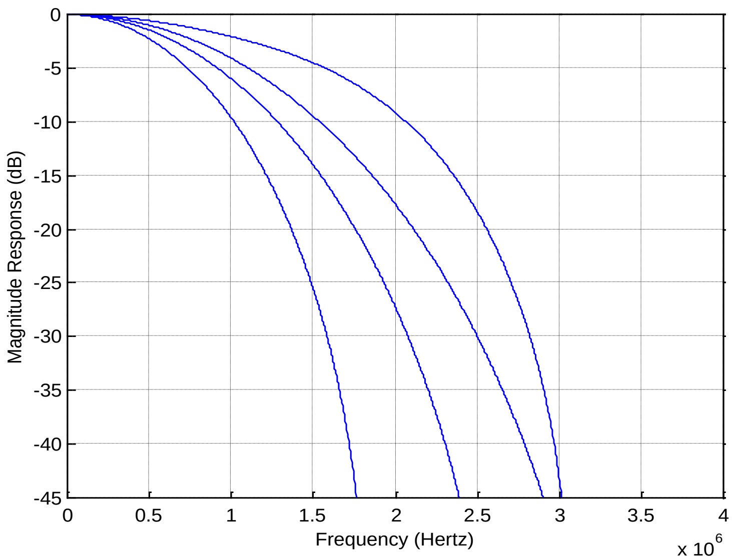


Fig 6 The frequency response of chrominance LPF

In case of a mistuned IF source, IF compensation filter makes up for any attenuation at higher frequencies or asymmetry around the color sub-carrier. The gain for the upper chrominance side band is controlled by the IFCOMP (0x13, 0x53, 0x93, 0xD3) register. Fig 7 shows the frequency response of IF-compensation filter.

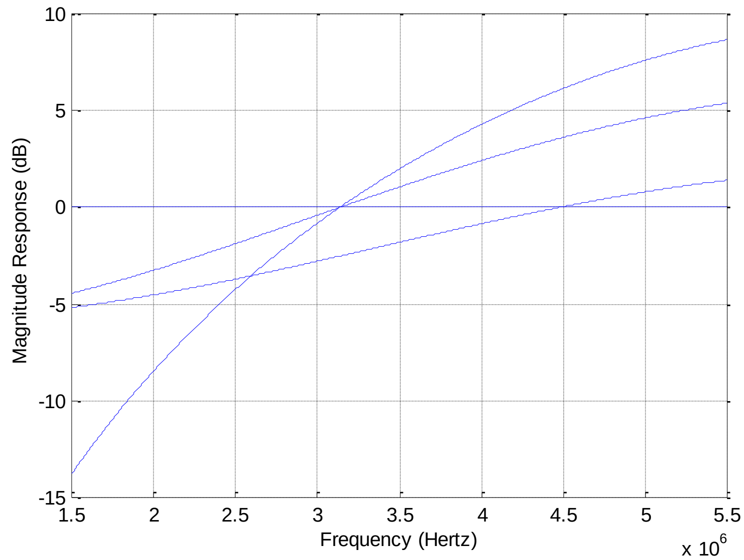


Fig 7 The frequency characteristics of IF-compensation filter

The ACC (Automatic Color gain Control) compensates for reduced chrominance amplitudes caused by high frequency suppression in video signal. The range of ACC is from –6dB to 30dB approximately. For black & white video or very weak & noisy signals, the color will be turned off by the internal color killing circuit. The color killing function can also be always enabled or disabled by programming CKIL (0x14, 0x54, 0x94, 0xD4) register.

The color saturation can be adjusted by changing SAT (0x10, 0x50, 0x90, 0xD0) register. The Cb and Cr gain can be also adjusted independently by programming UGAIN (0x3C) and VGAIN (0x3D) registers. Likewise, the Cb and Cr offset can be programmed through the U_OFF (0x3E) and V_OFF (0x3F) registers. Hue control is achieved with phase shift of the digitally controlled oscillator. The phase shift can be programmed through the HUE (0x0F, 0x4F, 0x8F, 0xCF) register.

Scaling and Cropping

The TW2824 provides two methods to reduce the amount of video pixel data, scaling and cropping. The scaling function provides video image at lower resolution while the cropping function supplies only a portion of the video image.

The TW2824 includes a high quality horizontal and vertical down scaler. The video images can be downscaled in both horizontal and vertical direction to an arbitrary size. The luminance horizontal scaler includes an anti-aliasing filter to reduce image artifacts in the resized image and a 32 poly-phase filter to accurately interpolate the value of a pixel. This results in more aesthetically pleasing video as well as higher compression ratio in bandwidth-limited application. Fig 8 shows the frequency response of anti-aliasing filter for horizontal scaling.

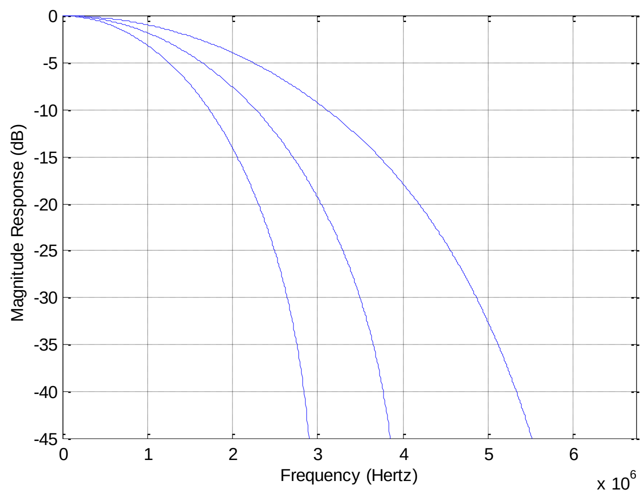


Fig 8 The frequency response of anti-aliasing filter for horizontal scaling

Similarly, the vertical scaler also contains an anti-aliasing filter and 16 poly-phase filters for down scaling. The filter characteristics are shown in Fig 9.

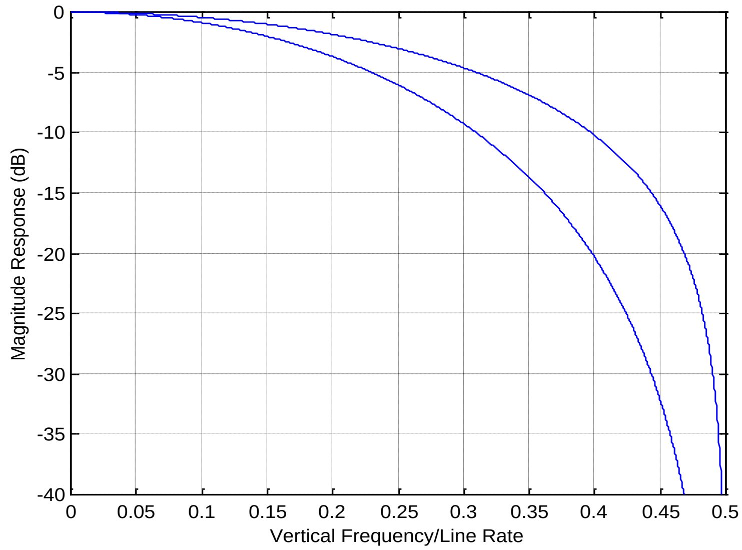


Fig 9 The characteristics of anti-aliasing filter for vertical scaling

Down scaling is achieved by programming the horizontal scaling register HSCALE (0x1C ~ 0x1F, 0x5C ~ 0x5F, 0x9C ~ 0x9F, 0xDC ~ 0xDF) and vertical scaling register VSCALE (0x18 ~ 0x1B, 0x58 ~ 0x5B, 0x98 ~ 0x9B, 0xD8 ~ 0xDB). When no scaled video image, the TW2824 will output the number of pixels per line as specified by the HACTIVE (0x04 ~ 0x07, 0x44 ~ 0x47, 0x84 ~ 0x87, 0xC4 ~ 0xC7) register. If the number of output pixels required is smaller than the number specified by the HACTIVE register, the 16bit HSCALE register is used to reduce the output pixels to the desired number.

The following equation is used to determine the horizontal scaling ratio to be written into the 16bit HSCALE register.

$$HSCALE = [N_{pixel\_desired} / HACTIVE] * (2^{16} - 1)$$

Where $N_{pixel\_desired}$ is the desired number of active pixels per line

For example, to scale picture from full size (HACTIVE = 720) to CIF (360 pixels), the HSCALE value can be found as:

$$HSCALE = [320/720] * (2^{16} - 1) = 0x7FFF$$

The following equation is used to determine the vertical scaling ratio to be written into the 16bit VSCALE register.

$$VSCALE = [N_{line\_desired} / VACTIVE] * (2^{16} - 1)$$

Where $N_{line\_desired}$ is the desired number of active lines per field

For example, to scale picture from full size (VACTIVE = 240 lines for NTSC and 288 lines for PAL) to CIF (120 lines for NTSC and 144 lines for PAL), the VSCALE value can be found as:

$$VSCALE = [120 / 240] * (2^{16} - 1) = 0x7FFF \text{ for NTSC}$$

$$VSCALE = [144 / 288] * (2^{16} - 1) = 0x7FFF \text{ for PAL}$$

The scaling ratios of popular case are listed in Table 2.

Table 2 HSCALE and VSCALE value for popular video formats

Scaling Ratio	Format	Output Resolution	HSCALE	VSCALE
1	NTSC PAL	720x480 720x576	0xFFFF 0xFFFF	0xFFFF 0xFFFF
1/2 (CIF)	NTSC PAL	360x240 360x288	0x7FFF 0x7FFF	0x7FFF 0x7FFF
1/4 (QCIF)	NTSC PAL	180x120 180x144	0x3FFF 0x3FFF	0x3FFF 0x3FFF

The cropping function allows only subsection of a video image to be output. The active video region is determined by the HDELAY, HACTIVE (0x04 ~ 0x07, 0x44 ~ 0x47, 0x84 ~ 0x87, 0xC4 ~ 0xC7), VDELAY and VACTIVE (0x09 ~ 0x0D, 0x49 ~ 0x4D, 0x89 ~ 0x8D, 0xC9 ~ 0xCD) registers. The first active line is defined by the VDELAY register and the first active pixel is defined by the HDELAY register. The VACTIVE register can be programmed to define the number of active lines in a video field, and the HACTIVE register can be programmed to define the number of active pixels in a video line. This function is used to implement for panning and tilt.

The horizontal delay register HDELAY determines the number of pixel delays between the horizontal reference and the leading edge of the active region. The horizontal active register HACTIVE determines the number of active pixels to be processed. Note that these values are referenced to the pixel number before scaling. Therefore, even if the scaling ratio is changed, the active video region used for scaling remains unchanged as set by the HDEALY and HACTIVE register. In order for the cropping to work properly, the following equation should be satisfied.

HDELAY + HACTIVE < Total number of pixels per line

Where the total number of pixels per line is 858 for NTSC and 864 for PAL

To process full size region, the HDELAY should be set to 32 and HACTIVE set to 720 for both NTSC and PAL system.

The vertical delay register (VDELAY) determines the number of line delays from the vertical reference to the start of the active video lines. The vertical active register (VACTIVE) determines the number of lines to be processed. These values are referenced to the incoming scan lines before the vertical scaling. In order for the vertical cropping to work properly, the following equation should be satisfied.

VDELAY + VACTIVE < Total number of lines per field

Where the total number of lines per field is 262 for NTSC and 312 for PAL

To process full size region, the VDELAY should be set to 6 and VACTIVE set to 240 for NTSC and the VDELAY should be also set to 5 and VACTIVE set to 288 for PAL.

The effect of scaling and cropping is shown in Fig 10.

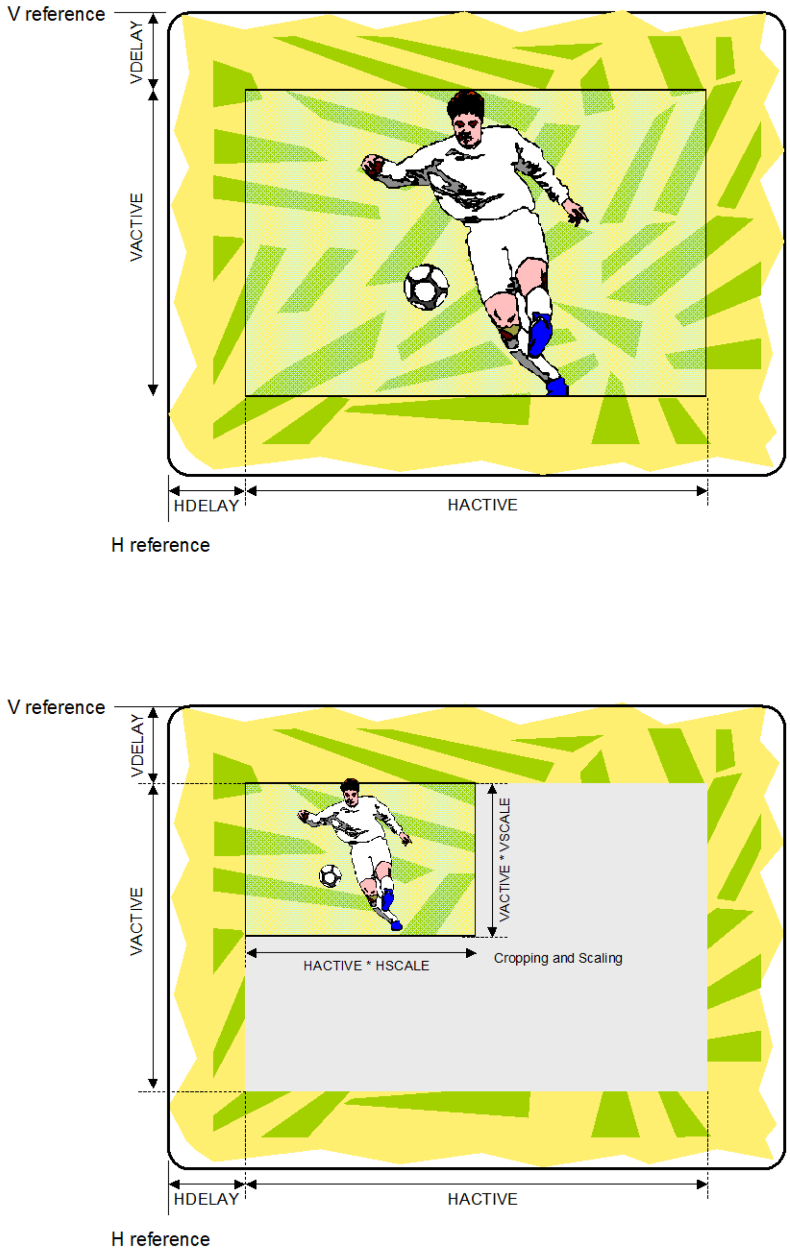


Fig 10 The effect of cropping and scaling

DIGITAL VIDEO INPUT

The TW2824 supports 1 digital video input from external decoder with 8bit ITU-R BT.656 standard for playback or cascade operation. This digital input is decoded in built-in ITU-R BT 656 decoder and fed to video channel control part with 4 decoded video data from built-in decoder. External decoder should have scaler to display scaled picture and supply valid signal to indicate valid pixel data in scaled video data because the TW2824 does not have scaler for digital video input. The TW2824 supports error correction code for decoding ITU-R BT.656. The timing of digital video input is illustrated in Fig 11.

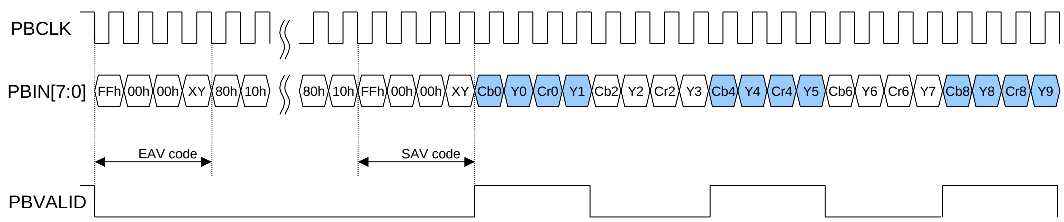


Fig 11 Timing diagram of ITU-R BT.656 format for digital video input

The SAV and EAV sequences are shown in Table 3.

Table 3 ITU-R BT.656 SAV and EAV code sequence

Condition			656 FVH Value			SAV/EAV Code Sequence			
Field	Vertical	Horizontal	F	V	H	First	Second	Third	Fourth
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1
		SAV			0				0xEC
EVEN	Active	EAV	1	0	1				0xDA
		SAV			0				0xC7
ODD	Blank	EAV	0	1	1				0xB6
		SAV			0				0xAB
ODD	Active	EAV	0	0	1				0x9D
		SAV			0				0x80

Motion Detector

The TW2824 supports motion detector individually for 4 analog video inputs. The built-in motion detection algorithm uses the difference of luminance level between current and reference field. The TW2824 also supports blind input detection for 4 analog video inputs. To detect motion properly according to situation, TW2824 provides several sensitivity and velocity control parameters for each motion detector.

When motion or blind is detected in any video inputs, TW2824 provides the interrupt request to host via IRQ pin. The host processor (i.e. Micom or CPU) can take the information of motion or blind by accessing the DET_MOTION (0x39), DET_BLIND (0x3A), MD_MASK (2x84 ~ 2x9B, 2xA4 ~ 2xBB, 2xC4 ~ 2xDB, 2xE4 ~ 2xFB) register. This status information is updated in the vertical blank period of each input.

The TW2824 also provides the motion detection result through MPPDEC pin with the control of MPPSET (0x7C) register.

MASK AND DETECTION REGION

The motion detection algorithm utilizes the full screen video data and detects individual motion of 16x12 cell. This full screen for motion detection consists of 704 pixels and 240 for NTSC and 288 for PAL video lines. Starting pixel on horizontal direction can be shifted from 0 to 15 pixel using the MD_ALIGN (2x80, 2xA0, 2xC0, 2xE0) register.

Each cell can be masked via the MD_MASK (2x84 ~ 2x9B, 2xA4 ~ 2xBB, 2xC4 ~ 2xDB, 2xE4 ~ 2xFB) register as illustrated in Fig 12. If the mask bit in specific cell is programmed to high, the related cell is ignored for motion detection.

The MD_MASK register has different function for reading and writing mode. For writing mode, setting “1” to MD_MASK register inhibits the specific cell from detecting motion. For reading mode, the state of MD_MASK register has two kinds of information depending on MASK_MODE (2x80, 2xA0, 2xC0, 2xE0) register. For MASK_MODE = “1”, the state of MD_MASK register means masking information of cell. For MASK_MODE = “0”, the state of MD_MASK register means the result of motion detection that “1” indicates detecting motion and “0” denotes no motion detection in the cell.

704 Pixels (44 Pixels/Cell)

240 Lines for 60Hz (20 Lines/Cell), 288 Lines for 50Hz (24 Lines/Cell)

MD_MASK0 [0]	MD_MASK0 [1]	MD_MASK0 [2]	MD_MASK0 [3]	MD_MASK0 [4]	MD_MASK0 [5]	MD_MASK0 [6]	MD_MASK0 [7]	MD_MASK0 [8]	MD_MASK0 [9]	MD_MASK0 [10]	MD_MASK0 [11]	MD_MASK0 [12]	MD_MASK0 [13]	MD_MASK0 [14]	MD_MASK0 [15]
MD_MASK1 [0]	MD_MASK1 [1]	MD_MASK1 [2]	MD_MASK1 [3]	MD_MASK1 [4]	MD_MASK1 [5]	MD_MASK1 [6]	MD_MASK1 [7]	MD_MASK1 [8]	MD_MASK1 [9]	MD_MASK1 [10]	MD_MASK1 [11]	MD_MASK1 [12]	MD_MASK1 [13]	MD_MASK1 [14]	MD_MASK1 [15]
MD_MASK2 [0]	MD_MASK2 [1]	MD_MASK2 [2]	MD_MASK2 [3]	MD_MASK2 [4]	MD_MASK2 [5]	MD_MASK2 [6]	MD_MASK2 [7]	MD_MASK2 [8]	MD_MASK2 [9]	MD_MASK2 [10]	MD_MASK2 [11]	MD_MASK2 [12]	MD_MASK2 [13]	MD_MASK2 [14]	MD_MASK2 [15]
MD_MASK3 [0]	MD_MASK3 [1]	MD_MASK3 [2]	MD_MASK3 [3]	MD_MASK3 [4]	MD_MASK3 [5]	MD_MASK3 [6]	MD_MASK3 [7]	MD_MASK3 [8]	MD_MASK3 [9]	MD_MASK3 [10]	MD_MASK3 [11]	MD_MASK3 [12]	MD_MASK3 [13]	MD_MASK3 [14]	MD_MASK3 [15]
MD_MASK4 [0]	MD_MASK4 [1]	MD_MASK4 [2]	MD_MASK4 [3]	MD_MASK4 [4]	MD_MASK4 [5]	MD_MASK4 [6]	MD_MASK4 [7]	MD_MASK4 [8]	MD_MASK4 [9]	MD_MASK4 [10]	MD_MASK4 [11]	MD_MASK4 [12]	MD_MASK4 [13]	MD_MASK4 [14]	MD_MASK4 [15]
MD_MASK5 [0]	MD_MASK5 [1]	MD_MASK5 [2]	MD_MASK5 [3]	MD_MASK5 [4]	MD_MASK5 [5]	MD_MASK5 [6]	MD_MASK5 [7]	MD_MASK5 [8]	MD_MASK5 [9]	MD_MASK5 [10]	MD_MASK5 [11]	MD_MASK5 [12]	MD_MASK5 [13]	MD_MASK5 [14]	MD_MASK5 [15]
MD_MASK6 [0]	MD_MASK6 [1]	MD_MASK6 [2]	MD_MASK6 [3]	MD_MASK6 [4]	MD_MASK6 [5]	MD_MASK6 [6]	MD_MASK6 [7]	MD_MASK6 [8]	MD_MASK6 [9]	MD_MASK6 [10]	MD_MASK6 [11]	MD_MASK6 [12]	MD_MASK6 [13]	MD_MASK6 [14]	MD_MASK6 [15]
MD_MASK7 [0]	MD_MASK7 [1]	MD_MASK7 [2]	MD_MASK7 [3]	MD_MASK7 [4]	MD_MASK7 [5]	MD_MASK7 [6]	MD_MASK7 [7]	MD_MASK7 [8]	MD_MASK7 [9]	MD_MASK7 [10]	MD_MASK7 [11]	MD_MASK7 [12]	MD_MASK7 [13]	MD_MASK7 [14]	MD_MASK7 [15]
MD_MASK8 [0]	MD_MASK8 [1]	MD_MASK8 [2]	MD_MASK8 [3]	MD_MASK8 [4]	MD_MASK8 [5]	MD_MASK8 [6]	MD_MASK8 [7]	MD_MASK8 [8]	MD_MASK8 [9]	MD_MASK8 [10]	MD_MASK8 [11]	MD_MASK8 [12]	MD_MASK8 [13]	MD_MASK8 [14]	MD_MASK8 [15]
MD_MASK9 [0]	MD_MASK9 [1]	MD_MASK9 [2]	MD_MASK9 [3]	MD_MASK9 [4]	MD_MASK9 [5]	MD_MASK9 [6]	MD_MASK9 [7]	MD_MASK9 [8]	MD_MASK9 [9]	MD_MASK9 [10]	MD_MASK9 [11]	MD_MASK9 [12]	MD_MASK9 [13]	MD_MASK9 [14]	MD_MASK9 [15]
MD_MASK10 [0]	MD_MASK10 [1]	MD_MASK10 [2]	MD_MASK10 [3]	MD_MASK10 [4]	MD_MASK10 [5]	MD_MASK10 [6]	MD_MASK10 [7]	MD_MASK10 [8]	MD_MASK10 [9]	MD_MASK10 [10]	MD_MASK10 [11]	MD_MASK10 [12]	MD_MASK10 [13]	MD_MASK10 [14]	MD_MASK10 [15]
MD_MASK11 [0]	MD_MASK11 [1]	MD_MASK11 [2]	MD_MASK11 [3]	MD_MASK11 [4]	MD_MASK11 [5]	MD_MASK11 [6]	MD_MASK11 [7]	MD_MASK11 [8]	MD_MASK11 [9]	MD_MASK11 [10]	MD_MASK11 [11]	MD_MASK11 [12]	MD_MASK11 [13]	MD_MASK11 [14]	MD_MASK11 [15]

Fig 12 Motion mask and detection cell

SENSITIVITY CONTROL

The motion detector has 4 sensitivity parameters to control threshold of motion detection such as level sensitivity via the MD_LVSENS (2x81, 2xA1, 2xC1, 2xE1) register, cell sensitivity via MD_CELSENS (2x81, 2xA1, 2xC1, 2xE1) register, spatial sensitivity via the MD_SPSENS (2x83, 2xA3, 2xC3, 2xE3) register, and temporal sensitivity parameter via the MD_TMPSENS (2x83, 2xA3, 2xC3, 2xE3) register. The interval between current and reference field for motion velocity is controlled via the MD_SPEED (2x82, 2xA2, 2xC2, 2xE2) register.

Level Sensitivity

In built-in motion detection algorithm, motion is detected when luminance level difference between current and reference field is greater than MD_LVSENS value. Motion detector is more sensitive for the smaller MD_LVSENS value and less sensitive for the larger. When the MD_LVSENS is too small, the motion detector may be weak in noise.

Spatial Sensitivity

The TW2824 uses 196 (16x12) detection cells in full screen for motion detection. Each detection cell is composed of 44 pixels and 20 lines for NTSC and 24 lines for PAL. Motion detection from only luminance level difference between two fields is very weak in spatial random noise. To remove the fake motion detection from the random noise, a spatial filter is used. The MD_SPSENS defines the number of detected cell to decide motion detection in full size image. The large MD_SPSENS value increases the immunity of spatial random noise.

Each detection cell has 4 sub-cells also. Actually motion detection of each cell comes from comparison of sub-cells in it. The MD_CELSENS defines the number of detected sub-cell to decide motion detection in cell. Likewise, the large MD_CELSENS value increases the immunity of spatial random noise in small area.

Temporal Sensitivity

Similarly, temporal filter is used to remove the fake motion detection from the temporal random noise. The MD_TMPSENS regulates the number of taps in the temporal filter to control the temporal sensitivity so that the large MD_TMPSENS value increases the immunity of temporal random noise.

VELOCITY CONTROL

Motion has various velocities. That is, in a fast motion an object appears and disappears rapidly between the adjacent fields while in a slow motion it is to the contrary. As the built-in motion detection algorithm uses the only luminance level difference between two adjacent fields, a slow motion is inferior in detection rate to a fast motion. To compensate this weakness, MD_SPEED (2x82, 2xA2, 2xC2, 2xE2) parameter is used which is controllable up to 64 fields. MD_SPEED parameter adjusts the field interval in which the luminance level is compared. Thus, for detection of a fast motion a small value is needed and for a slow motion a large value is required. The parameter MD_SPEED value should be greater than MD_TMPSENS value.

Additionally, the TW2824 has 2 more parameters to control the selection of reference field. The MD_FLD (2x80, 2xA0, 2xC0, 2xE0) register is a field selection parameter such as odd, even or any field selection.

The MD_REFFLD (2x82, 2xA2, 2xC2, 2xE2) register is provided to control the updating period of reference field. For MD_REFFLD = “0”, the interval from current field to reference field is always same as the MD_SPEED. It means that the reference filed is always updated every field. Fig 13 shows the relationship between current and reference field for motion detection when MD_REFFLD is “0”.

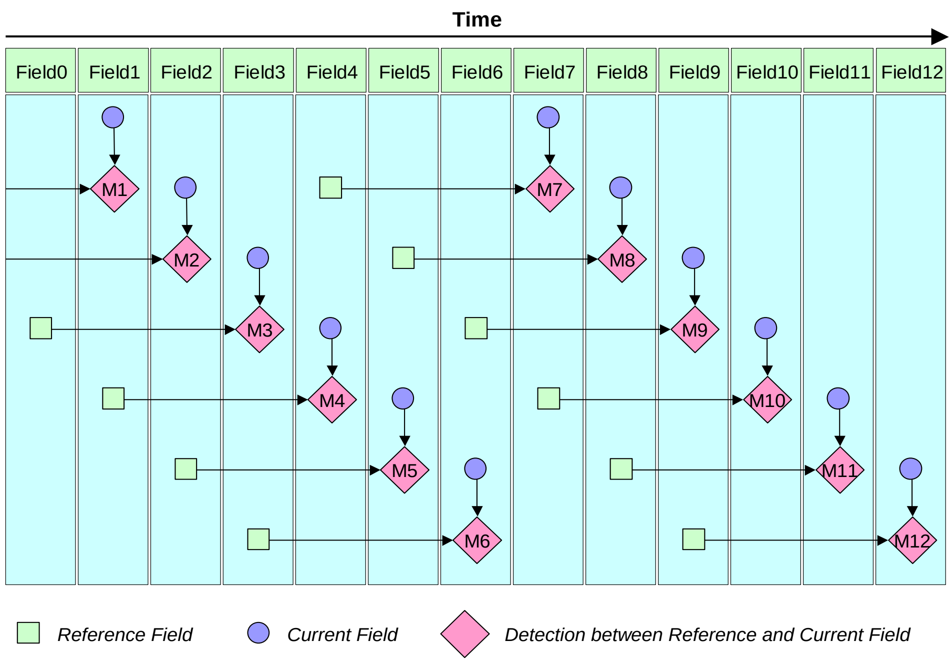


Fig 13 The relationship between current and reference field when MD_REFFLD = “0”

The TW2824 can update reference field only at the period of MD_SPEED when MD_REFFLD is high. For this case, TW2824 can detect a motion with sense of a various velocity. Fig 14 shows the relationship between current and reference field for motion detection when MD_REFFLD is high.

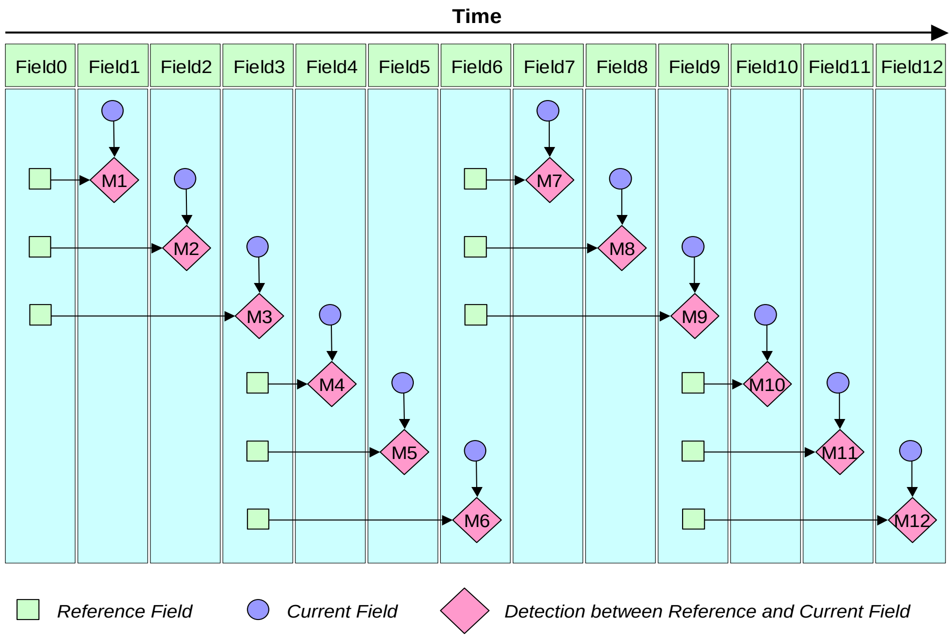


Fig 14 The relationship between current and reference when MD_REFFLD = “1”

BLIND DETECTION

The TW2824 supports a blind input detection individually for 4 analog video inputs and makes an interrupt of blind detection to host. If video level in wide area of field is almost equal to average video level of field due to camera shaded by something, this input is defined as blind input.

The TW2824 has two sensitivity parameters to detect blind input such as level sensitivity via the BD_LVSENS (2x7F) register and spatial sensitivity via the BD_CELSENS (2x7F) register. The BD_LVSENS parameter controls threshold of level between cell and field average. The BD_CELL parameter defines the number of cells to detect blind. The TW2824 uses total 768 (32x24) cells of full screen. For BD_CELSENS = “0”, the number of cell whose level is same as average of field should be over than 60% to detect blind. The large value of BD_LVSENS and BD_CELSENS makes blind detector less sensitive.

Video Control

The TW2824 has identical dual video controllers for display and capture path. These 2 paths have same functionality except extension capability of external SDRAM. For display path, external SDRAM can be extended from 16M to 512M. This capability is related to only save and recall function. Therefore, hereafter the display and capture path will not be discriminated in the following description and they will be represented just as X and Y path. The block diagram of video controller is shown in following Fig 15.

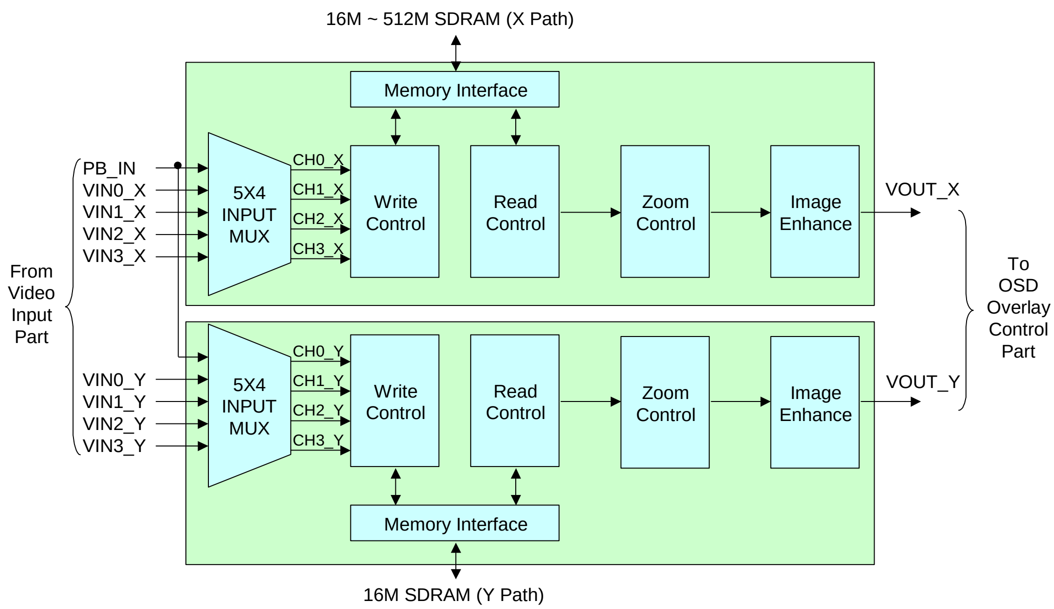


Fig 15 Block diagram of video controller

The TW2824 supports channel blanking, boundary on/off and blink, horizontal mirroring, and freeze function for each channel. The TW2824 can capture last 4 images automatically for each channel when video loss is detected. The TW2824 can save video to external SDRAM and recall for X path. The TW2824 supports image enhancement function for non-real time video such as freezing video or playback video. The TW2824 also provides high performance 2X zoom function with interpolation filter and image enhancement technique.

The TW2824 has three operating modes such as live, strobe and switch mode. Each channel can be operated in its individual operating mode. That is, the TW2824 can be operated as multi-operating mode if each channel has different operating mode. Live mode is used to display real time video as QUAD, strobe mode is used to display non-real time video with strobe signal from host and switch mode is used to display time-multiplexed video from several channels. For switch mode, the TW2824 supports two different types such as switch live and switch still mode.

The TW2824 also provides two picture display modes such as monitor display mode and DVR display mode. For DVR display mode, there are some limitations to control channel size and position.

The TW2824 supports chip-to-chip cascade and path-to-path overlay operation as well.

INPUT SELECTION

Each video controller for X and Y paths can accept 5 different video sources but can control only 4 video out of 5 video sources. First step is selecting 4 channels to be controlled via the DEC_PATH (1x10, 1x17, 1x1E, 1x25 for X Path, 1x40, 1x47, 1x4E, 1x55 for Y Path) register. X and Y paths are operated independently and each path has four 5x1 MUX respectively. The selected 4 channel videos are controlled in next step with various operations. Fig 16 shows the internal channel input selection.

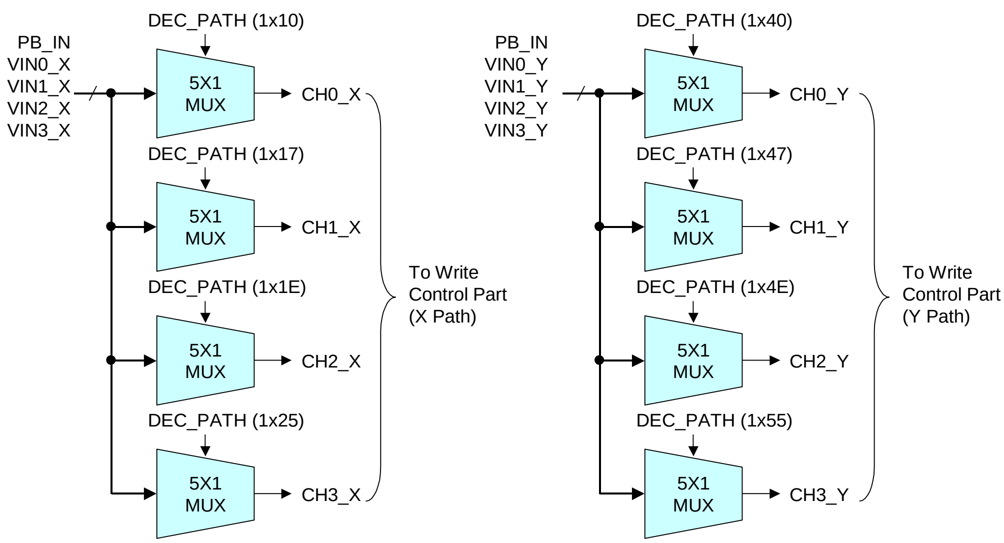


Fig 16 Channel input selection

OPERATION MODE

Each channel can be working with three kinds of operating mode such as live, strobe and switch mode via the FUNC_MODE (1x10, 1x17, 1x1E, 1x25 for X Path, 1x40, 1x47, 1x4E, 1x55 for Y Path) register. The operation mode can be selected individually for each channel so that multi-operating mode can be implemented.

Live Mode

If FUNC_MODE is “0”, channel is operated in live mode. For the live mode, video display is updated with real time field rate. This mode is used to display a live video such as QUAD, PIP, and POP.

Strobe Mode

If FUNC_MODE is “1”, channel is operated in strobe mode. For strobe mode, video display is updated whenever the TW2824 receives strobe command from host like CPU or Micom. If host doesn’t send a strobe command to TW2824 anymore, the channel displays the last strobe image until getting a new strobe command. This mode is useful to display non-real time video input such as playback video with multiplexed signal input and to implement pseudo 8 channel application or dual page mode or panorama channel display. Specially, the TW2824 supports easy interface for pseudo 8 channels application and refer to later in dummy channel function section.

Strobe operation is performed independently for each channel via the STRB_REQ (1x04, 1x34) register. But the STRB_REQ register has a different mode for reading and writing. Writing “1” into STRB_REQ in each channel makes the TW2824 updated by each incoming video. The updating status after strobe command can be known by reading the STRB_REQ register. If reading value is “1”, updating is not completed after getting the strobe command. In that case, this channel cannot accept a new strobe command or a disabling strobe command from host. To send a new strobe command, host should wait until STRB_REQ state is “0”. For freeze or non-strobe channel, the TW2824 can ignore the strobe command even though host sends it. In this case, the STRB_REQ register is cleared to “0” automatically without any updating video. The status of STRB_REQ register can also be read through MPPDEC pin with control of the MPPSET (0x7C) register.

When updating video with a strobe command, the TW2824 supports field or frame updating mode via the STRB_FLD (1x04, 1x34) register. Odd field of input video can be updated and displayed for STRB_FLD = “0”, even field for “1”. For “2” of STRB_FLD register, the TW2824 doesn’t care for even or odd field, and updates video by next any field. If the STRB_FLD register is “3”, the strobe command updates video by frame. The following Fig 17 shows the example for various STRB_FLD value.

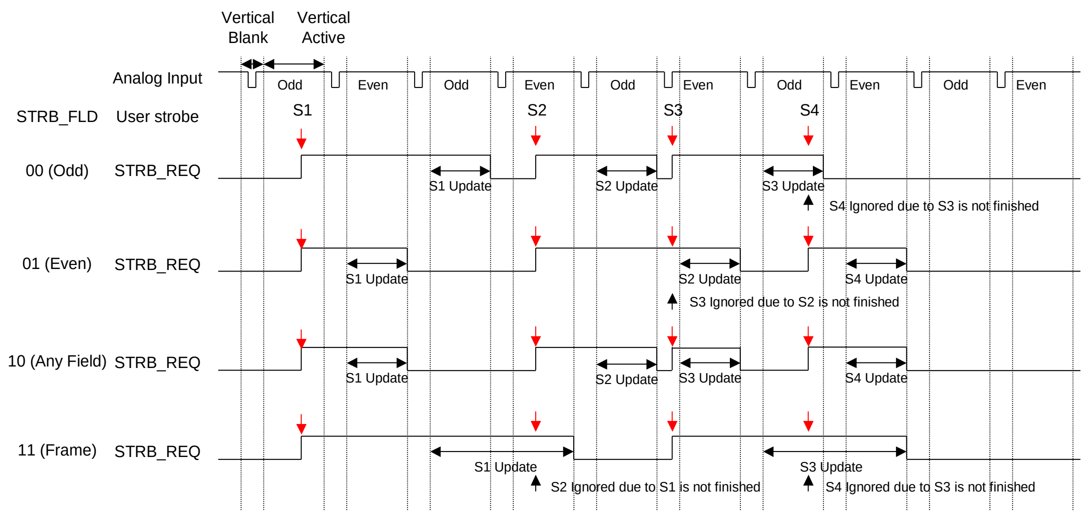


Fig 17 Example of strobe sequence for various STRB_FLD setting

The timing of strobe operation is related only with input video timing and strobe operation can be performed independently for each channel. So each channel is updated with different timing. The TW2824 provides a special feature as dual page mode using the DUAL_PAGE (1x04, 1x34) register. Although each channel is updated with different time, all channels can be displayed simultaneously in dual page mode. This means that the TW2824 waits until all channels are updated and then displays all channels with updated video at the same time. When dual page mode is enabled, host should send a strobe command for all channels and host should wait until all channels complete their strobe operations to send a new strobe command. Fig 18 shows the example of 4 channel strobe sequences for dual page.

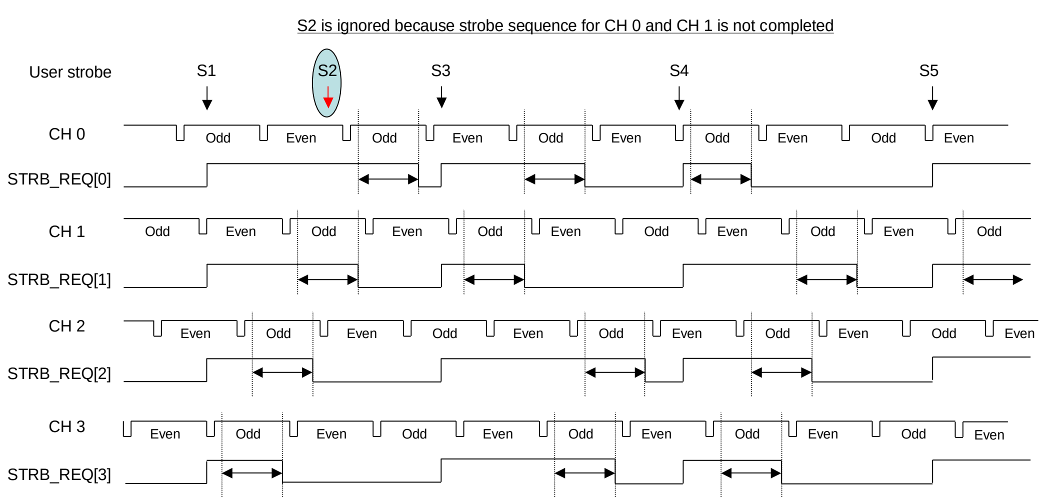


Fig 18 The example of 4 channel strobe sequences for dual page mode

Switch Mode

If FUNC_MODE is “2”, channel is operated in switch mode. The TW2824 supports 2 different types of switching mode such as still switching and live switching mode via the MUX_MODE (1x05, 1x35) register. For still switching mode, the TW2824 maintains the switched channel video as still image until next switching request, but for live switching mode the TW2824 updates every field of switched channel video until next switching request. The live switching mode is used for channel sequencer without any timing loss or disturbing. In switch mode, there is a constraint that picture size of the switched channel should be same even though their size can be varied. The TW2824 can switch the channel by fields or frames that can be controlled up to 1 field or 1 frame rate. But if the channel is on freeze state or disabled, the TW2824 ignores the request for switch mode.

The TW2824 contains two internal 64 depth queues which have channel sequence information, and can be operated with internal or external triggering. Actual queue size can be defined by the QUE_SIZE (1x06, 1x36) register. To change the channel switching sequence in internal queue, set “1” to QUE_WR register after defining queue address with the QUE_ADDR (1x09, 1x39) register and channel number with the QUE_CH (1x08, 1x38) register. The QUE_WR register will be cleared automatically after updating queue. The channel sequence information in the queue can be read through the QUE_CH register also.

To operate the switching function properly, the channel switching should be requested with triggering that has three kind modes such as internal triggering from internal field counter, external triggering from external host and interrupted triggering like alarm. The triggering mode can be selected by the TRIG_MODE (1x05, 1x35) register. This switching architecture is shown in the following Fig 19.

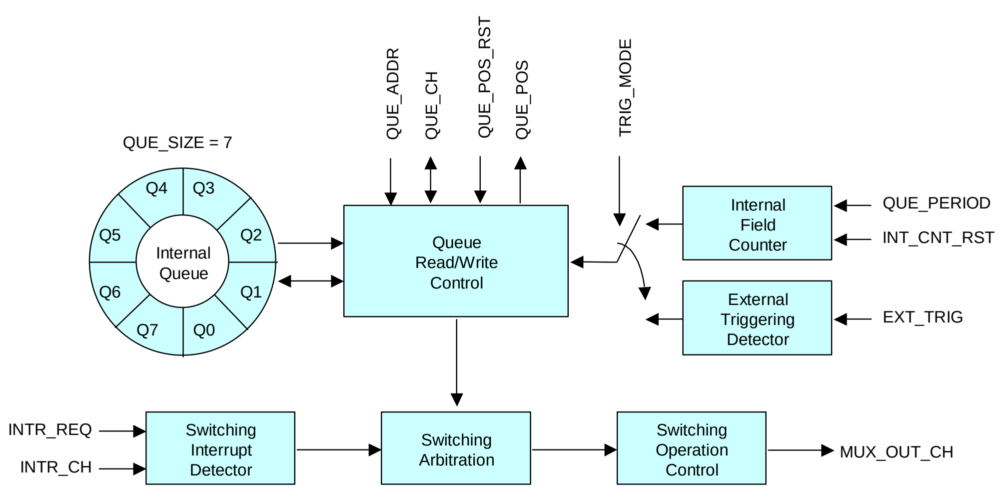


Fig 19 The Switching control structure when QUE_SIZE = 7

For internal triggering mode, the switching period can be specified in the QUE_PERIOD (1x07, 1x37) register that has 1 ~ 1024 field range. The internal field counter can be reset at anytime using the INT_CNT_RST (1x08, 1x38) register and restarted automatically after reset. To reset an internal queue position, set "1" to QUE_POS_RST (1x08, 1x38) register and then the queue position will be restarted after reset. Both INT_CNT_RST and QUE_POS_RST register can be cleared automatically after set to "1". The following Fig 20 shows an illustration of QUE_POS_RST and INT_CNT_RST.

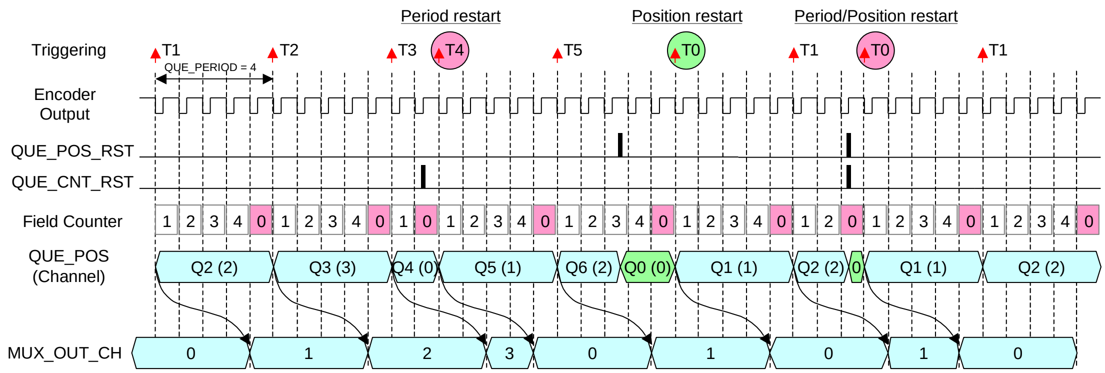


Fig 20 The illustration of QUE_POS_RST and INT_CNT_RST

For external triggering mode, the request of channel switching comes from the EXT_TRIG (1x05, 1x35) register. Like internal triggering mode, QUE_POS_RST = "1" can reset the queue position in external triggering mode.

For interrupted mode, host can request the channel switching at anytime via the INTR_REQ and INTR_CH (1x05, 1x35) register for internal or external triggering mode. Because the interrupted trigger has priority over internal or external triggering, the channel defined by INTR_CH can be inserted into the programmed channel sequence immediately. The next queue position can be read via the QUE_POS (1x0A, 1x3A) register.

The TW2824 also provides various switching types as odd field, even field or frame switching via the MUX_FLD (1x08, 1x38) register. For MUX_FLD = "0", it is working as field switching mode with only odd field, but with only even field for MUX_FLD = "1". For MUX_FLD = "2" or "3", it is working as frame switching with both odd and even field.

Actually the channel switching is executed just before vertical sync of video output in field switching mode or before vertical sync of only odd field in frame switching mode. So all registers for switching should be set before that timing. Otherwise, the control values will be applied to the next field or frame. For the reference timing of switching, the TW2824 provides the VSENC pin whose timing can be varied via ENC_VSDEL (1x74) and ENC_VSOFF (1x74) registers. So the timing of VSENC pin can be equal to the vertical sync of video output if the ENC_VSDEL is set to "16" for 60Hz system or to "22" for 50Hz system.

Basically it takes 4 fields duration to display the switching channel from any triggering (field or frame). The host can read the current switching channel information through the MUX_OUT_CH (1x0B, 1x3B) register. The switching channel information is updated just before vertical sync of video output in field switching mode or before vertical sync of only odd field in frame switching mode. The illustration of channel switching is shown in Fig 21 and Fig 22.

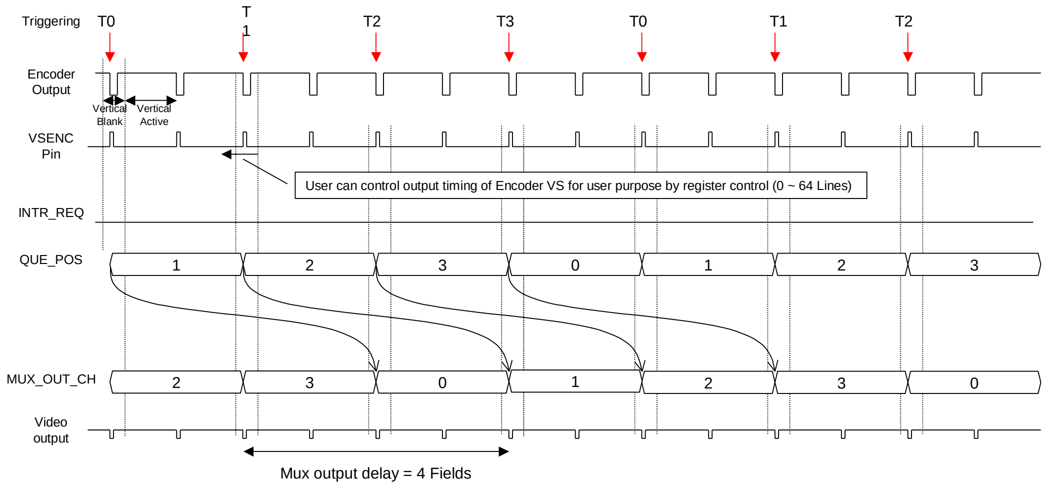


Fig 21 The illustration of switching sequence when Q_SIZE = 3, Q_PERIOD = 1

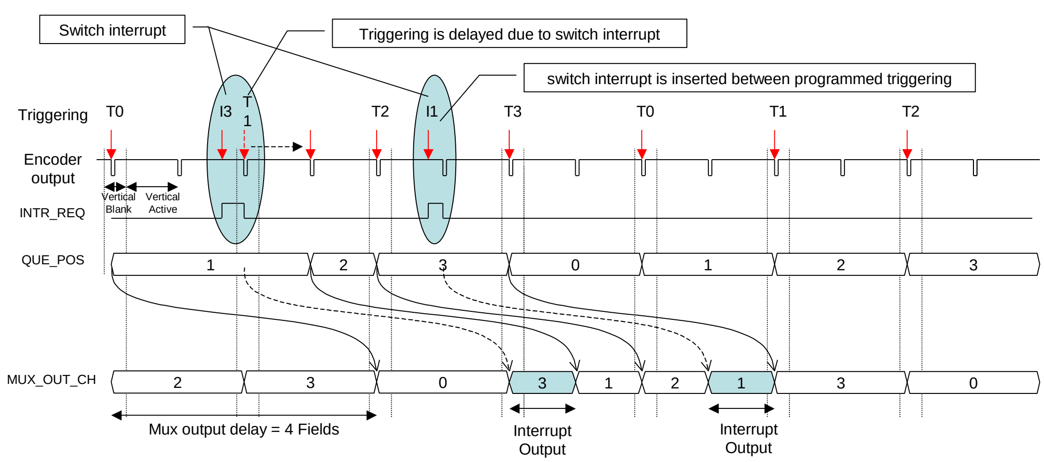


Fig 22 The illustration of the interrupted switching sequence when Q_SIZE = 3, Q_PERIOD = 1

The TW2824 has device option for switching operation such as TW2824Q and TW2824QS that have several limitations. The first limitation is that switching mode is fixed to switch live mode. The second limitation is that switching period should be greater than 12 fields.

CHANNEL ATTRIBUTE

The TW2824 provides various channel attributes such as channel enable, boundary selection, blank enable, freeze, horizontal mirroring and image enhancement. As special feature, TW2824 supports save-and-recall function and dummy channel display function for each channel.

Background Control

Summation of all active channel regions can be called as active region and the rest region except active region is defined as background region. The TW2824 supports background overlay and the overlay color is controlled via the BGDCOL (1x0F, 1x3F) register.

Boundary Control

The TW2824 can overlay channel boundary on each channel region using the BOUND (1x11, 1x18, 1x1F, 1x26 for X Path, 1x41, 1x48, 1x4F, 1x56 for Y Path) register and it can be blinked via the BLINK (1x11, 1x18, 1x1F, 1x26 for X Path, 1x41, 1x48, 1x4F, 1x56 for Y Path) register when BOUND is high. The boundary color can be selected through the BNDCOL (1x0F, 1x3F) register. The blink period can be also controlled through the TBLINK (1x04, 1x34) register. For last image capture mode, channel boundary can be blinked automatically.

Blank Control

Each channel can be blanked with specified color using the BLANK (1x11, 1x18, 1x1F, 1x26 for X Path, 1x41, 1x48, 1x4F, 1x56 for Y Path) register and BLKCOL (1x0F, 1x3F) register. The channel blank control is related with last image capture mode. For last image capture mode, channel can be blanked automatically.

Freeze Control

Each channel can capture last 4 field images whenever freeze function is enabled and display 1 field image out of the captured 4 field images using the FRZ_FLD (1x0F, 1x3F) register. The freeze function can be enabled or disabled independently for each channel via the FREEZE (1x11, 1x18, 1x1F, 1x26 for X Path, 1x41, 1x48, 1x4F, 1x56 for Y Path) register.

Last Image Capture

When video loss has occurred or gone, the TW2824 provides 4 kinds of indication such as bypass of incoming video, blank, capture of last image and capture of last image with blinking channel boundary depending on the NOVID_MODE (1x0A, 1x3A) register. This function is working automatically on video loss. The capturing last image is same as freeze function described above. To select 1 field image out of captured 4 filed images, control the FRZ_FLD (1x0F, 1x3F) register which is shared with freeze function.

Horizontal Mirroring

The TW2824 supports image mirroring function in horizontal direction via the MIRROR (1x11, 1x18, 1x1F, 1x26 for X Path, 1x41, 1x48, 1x4F, 1x56 for Y Path) register. It is useful to display a reflection image.

Image Enhancement

The TW2824 supports special filter to enhance image quality for non real time video display. In non real time video such as freeze image, recalled image from saving images and playback video which records multi-channel video using field switching, so many line flicker noise can be found in image because it displays same field image for both odd and even field. The embedded filter in TW2824 can remove effectively this line flicker noise and be enabled via the ENHANCE (1x11, 1x18, 1x1F, 1x26 for X Path, 1x41, 1x48, 1x4F, 1x56 for Y Path) register for each channel.

Save and Recall Function

The TW2824 can save images in external memory and recall them to display. This function can be working for X path only because external memory can be extended from 16M to 512M only in X path. The number of images to be saved depends on extended memory capability, picture size and field type (field or frame). This function is working independently for each channel.

The TW2824 can save image only in live channel so that it cannot be saved in freezing channel. If channel is working on strobe operating mode, this channel can be saved with new strobe command. For switch operating mode, the channel can be saved only on switching time because this channel can be updated at this moment.

To save image, several parameters should be controlled which are the SAVE_FLD, SAVE_HID, SAVE_REQ (1x03) and SAVE_ADDR (1x02) registers. The SAVE_FLD determines field or frame type for image to be saved. Even though the channel to be saved is hidden by upper layer picture, it can be saved using the SAVE_HID register that makes no effect on current display. The saving function is requested by writing "1" on the SAVE_REQ register and this register will be cleared when saving is done. Before it is cleared, the TW2824 cannot accept new saving request. The SAVE_ADDR register defines address where an image will be saved. Because 4M bit is allocated for each 1 field image, SAVE_ADDR unit is 4M bit and can have range 0 ~ 127 for 512M. The first 0~3 are reserved for normal operation so that it cannot be used for saving function.

To recall image, several parameters are required such as RECALL_FLD (1x03), RECALL_EN and RECALL_ADDR (1x12, 1x19, 1x20, 1x27) register. If RECALL_EN is "1", the TW2824 recalls saved image which is located at RECALL_ADDR in external memory and display it just like incoming video. The RECALL_FLD register determines 1 field or 1 frame mode to display. The following Fig 23 illustrates the relationship between SDRAM size and SAVE_ADDR / RECALL_ADDR.

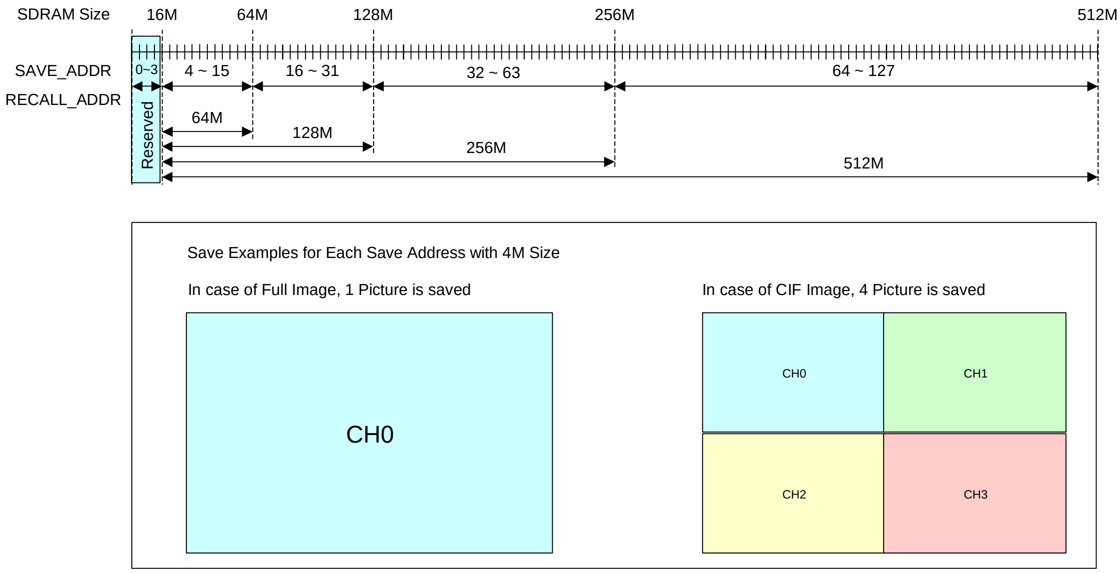


Fig 23 The Relationship between SDRAM size and SAVE_ADDR / RECALL_ADDR

Dummy Channel Function

The TW2824 supports additional 4 dummy channel controllers to display up to 8 channel videos even though it is not real time. This dummy channel function is useful to implement low cost and high feature application system such as pseudo 8-channel QUAD system.

The TW2824 has 4 main channel controllers as described before and each main channel has its own corresponding dummy channel. Except channel location and size defined in the PICHL, PICHR, PICVT, and PICVB registers, all attributes of main channel such as boundary, blank, input source selection and pop-up priority are applied to dummy channel also. But the several functions including freeze, save-and-recall and switch operation mode are not supported for dummy channel. Dummy channel can be used for either X or Y path, but picture location and size information of dummy channel is shared in both paths.

To use dummy channel function, dummy channel region should be defined in the DMPICHL (1x60, 1x64, 1x68 and 1x6C), DMPICHR (1x61, 1x65, 1x69 and 1x6D), DMPICVT (1x62, 1x66, 1x6A and 1x6E), and DMPICVB (1x63, 1x67, 1x6B and 1x6F) registers and dummy channel should be enabled using the DMCH_EN (1x11, 1x17, 1x1E and 1x25 for X Path, 1x41, 1x47, 1x4E and 1x55 for Y Path) register. The path to be updated is selected via the DMCH_PATH (1x11, 1x17, 1x1E and 1x25 for X Path, 1x41, 1x47, 1x4E and 1x55 for Y Path) register. For DMCH_PATH = “1”, dummy channel will be updated, but for DMCH_PATH = “0”, main channel will be updated. So the updating path should be defined before updating, for example, during vertical blanking time or between completed strobe and new strobe.

Fig 24 shows an example of dummy channel function. This is pseudo 8 channel operation using dummy channel function, strobe operating mode and internal analog mux switch in front of video decoder.

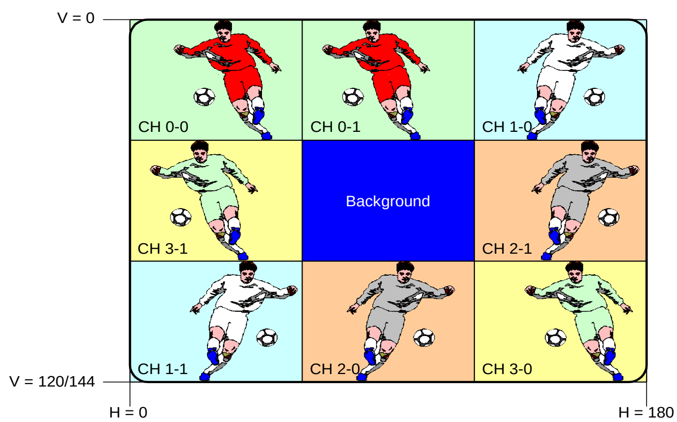


Fig 24 Pseudo 8 channel operation

PICTURE DISPLAY MODE

The TW2824 supports four picture display modes such as monitor display mode, frame display mode, DVR display mode and DVR frame display mode. The DVR display mode and DVR frame display mode generate continuous video stream for each channel and transfer it to compression part (M-JPEG or MPEG) so that they are very useful for DVR application.

The TW2824 provides the independent picture display mode for X and Y path through the DIS_MODE and FRAME_OP (1x01, 1x31) register. If FRAME_OP is “0”, DIS_MODE = “0” stands for monitor display mode and DIS_MODE = “1” represents DVR display mode. If FRAME_OP is “1”, DIS_MODE = “0” stands for frame mode and DIS_MODE = “1” represents DVR frame mode.

Monitor Display Mode

Each channel region can be defined using its own PICHL (1x13, 1x1A, 1x21, 1x28 for X Path, 1x43, 1x4A, 1x51, 1x58 for Y Path), PICHR (1x14, 1x1B, 1x22, 1x29 for X Path, 1x44, 1x4B, 1x52, 1x59 for Y Path), PICVT (1x15, 1x1C, 1x23, 1x2A for X Path, 1x45, 1x4C, 1x53, 1x5A for Y Path), PICVB (1x16, 1x1D, 1x24, 1x2B for X Path, 1x46, 1x4D, 1x54, 1x5B for Y Path) register. If more than 2 channels have same region, there will be a confliction how to display for that area. Generally TW2824 defines that channel 0 has priority over channel 3. So if a conflicting happens between more than 2 channels, channel 0 will be displayed first as top layer and then channel 1 and 2 and 3 are hidden beneath. The TW2824 also provides channel pop-up attribute via the POP_UP (1x11, 1x17, 1x1E, 1x25 for X Path, 1x41, 1x47, 1x4E, 1x55 for Y Path) register to give priority for another display. If a channel has pop-up attribute, it will be displayed as top layer. Fig 25 shows the channel definition and priority for display. This feature is used to configure PIP (Picture-In-Picture) or POP (Picture-out-Picture).

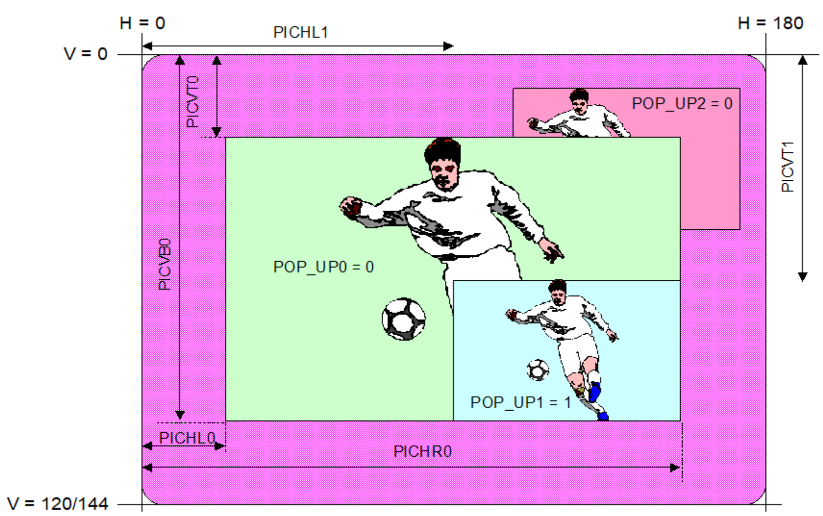


Fig 25 Channel position and overlay in monitor display mode

Frame Display Mode

The frame display mode is similar to monitor display mode except that the definition of picture size is extended to frame area and only one field data is output in 1 frame. The odd or even field selection is controlled via FRAME_FLD (1x01, 1x31) register. Like monitor display mode, the frame display mode also provides the full flexibility of the picture size and position using PICVT, PICVB, PICHL, PICHR registers and pop-up control using POP_UP register. But the picture size step for vertical direction is twice as large as monitor display mode. Fig 26 shows the example of channel position and overlay in frame display mode.

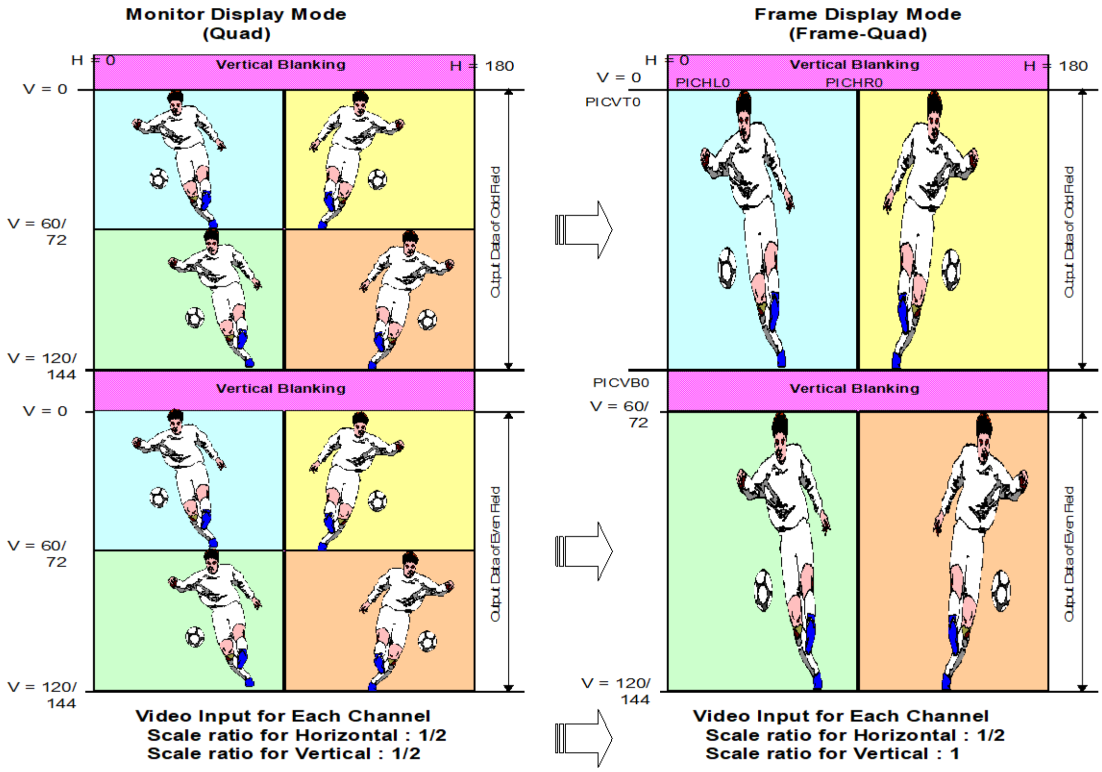


Fig 26 Channel position and overlay in frame display mode

The TW2824 supports the full function such as live/strobe/switch operation, save & recall and dummy channel function in frame display mode. However, there are three limitations in it. The first is that the zoom operation is not supported. The second is that all operation is controlled by frame rate. The third is that the vertical scale ratio should be twice as large as monitor display mode and picture size for vertical direction should be less than one field size.

DVR Display Mode

The DVR display mode outputs the continuous video stream for compression part (M-JPEG or MPEG) in DVR application. Like frame display mode, there is one constraint that all channels should have same picture size and it should be one of 1, 1/2, 1/3 and 1/4 scale ratio for horizontal and vertical direction independently. Channel size can be defined using the HDIV and VDIV (1x01, 1x31) registers. The HDIV controls horizontal scale ratio and the VDIV controls vertical scale ratio. Because all channels have same picture size, all channels have the same value of HDIV and VDIV. So the maximum channel number to be displayed in this mode is "(HDIV+1) * (VDIV+1)".

The picture position for each channel in DVR display mode is defined via the PICHL[7:6] (1x13, 1x1A, 1x21, 1x28 for X Path, 1x43, 1x4A, 1x51, 1x58 for Y Path) and PICVT[7:6] (1x15, 1x1C, 1x23, 1x2A for X Path, 1x45, 1x4C, 1x53, 1x5A for Y Path) register. The value of PICHL [7:6] should be less than or equal to the value of HDIV and likewise the value of PICVT [7:6] should be less than or equal to the value of VDIV. If the channel is defined out of range, it will not be displayed. The following equation is used to determine the position of channel and Fig 27 shows the example of DVR display mode.

Channel position = (HDIV+1) * PICVT [7:6] + PICHL [7:6]

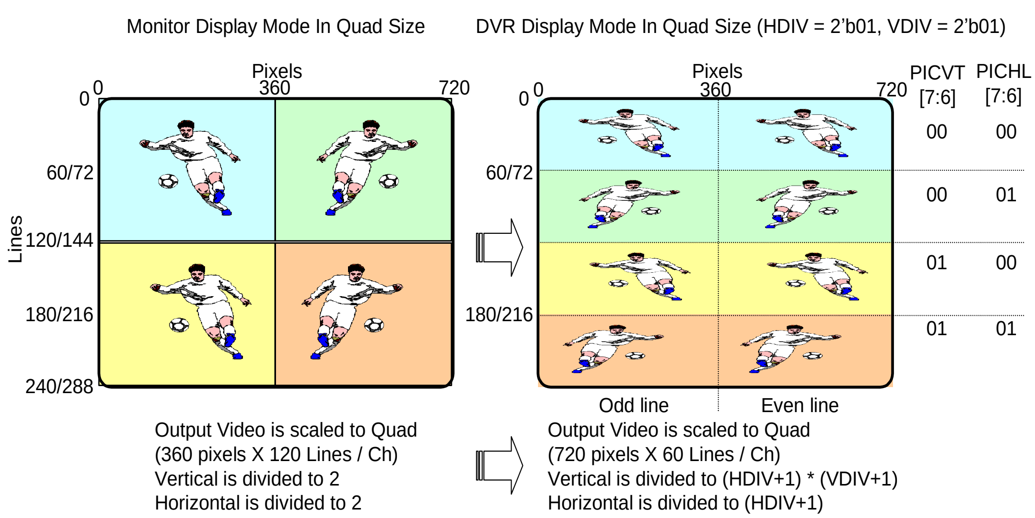


Fig 27 Channel position and overlay for DVR display mode

The TW2824 supports the full function such as live/strobe/switch operation, save & recall and dummy channel function in DVR display mode. However, The channel boundary and zoom operation is not supported in DVR display mode.

DVR Frame Display Mode

The DVR frame display mode is generated from the combination of frame display mode and DVR display mode. The odd or even field selection is controlled via FRAME_FLD register like frame display mode. The following Fig 28 shows the example of DVR frame display mode.

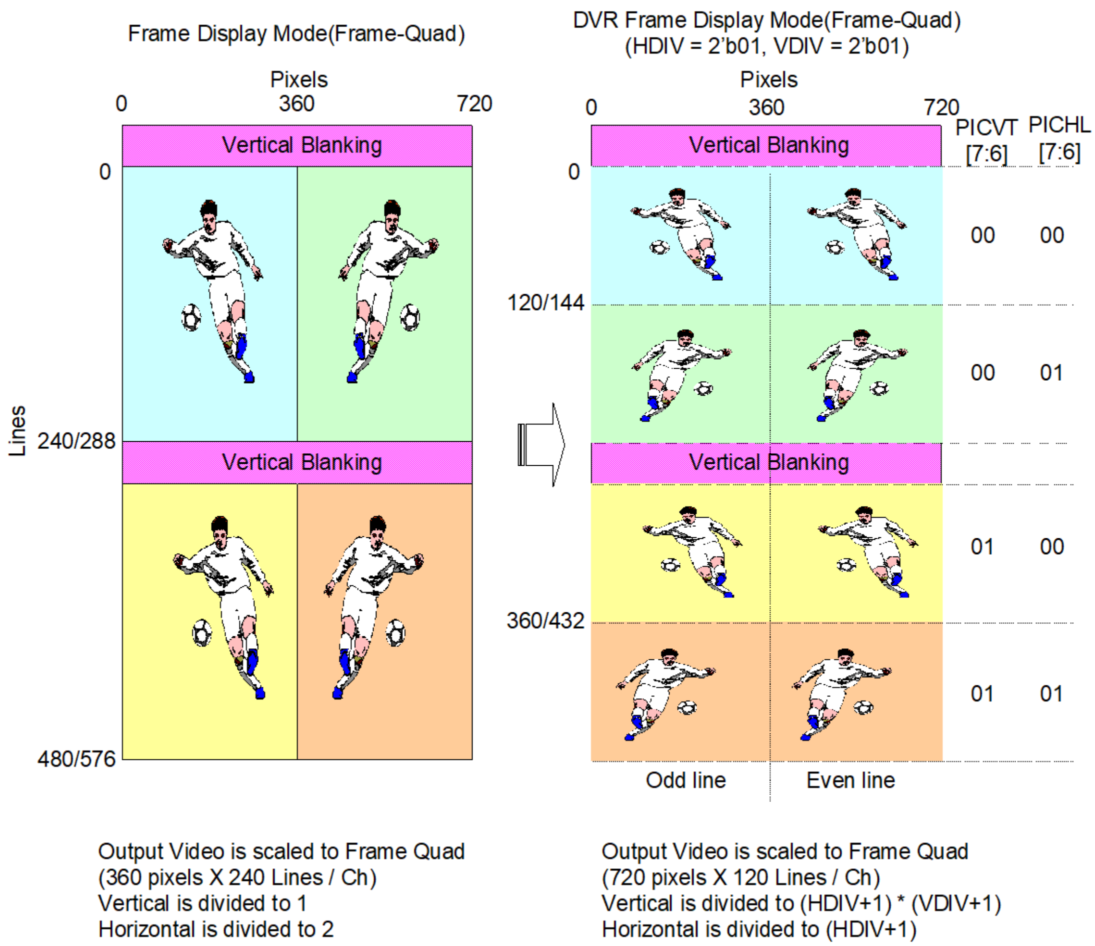


Fig 28 Channel position and overlay for DVR frame display mode

The TW2824 supports the full function such as live/strobe/switch operation, save & recall and dummy channel function in DVR frame display mode. However, there are three limitations in DVR frame display mode. The first is that the channel boundary and zoom operation is not supported. The second is that all operation is based on frame rate like frame display mode. The third is that all channels should have same picture size such as DVR display mode but the vertical scale ratio should be twice as large as DVR display mode.

ZOOM FUNCTION

The TW2824 supports high performance 2X zoom function in vertical and horizontal direction. This function is working in any operation mode such as live, strobe and switch mode in monitor display mode, but it is not working for DVR display mode and frame mode and DVR frame mode because the region to be zoomed cannot be defined and actually this function is needed in only monitor display mode.

Conventional system also has zoom function, but it has a very poor quality due to line flicker noise even though interpolation filter is adapted. The TW2824 provides high quality zoom characteristics using high performance interpolation filter and image enhancement technique. When zoom is executed, the image enhancement is operated automatically.

The zoomed region will be defined with the ZOOMH (1x0D, 1x3D) and ZOOMV (1x0E, 1x3E) registers and can be displayed depending on the ZMBNDCOL, ZMBNDEN, ZMAREAEN, ZMAREA (1x0C, 1x3C) register. The zoom operation is enabled via the ZMENA (1x0C, 1x3C) register.

CASCADE CONNECTION

The TW2824 supports chip-to-chip cascade connection up to 4 chips for 16 channel application and path-to-path cascade for 5 channels application in all of display mode.

Chip-to-Chip Cascade

The TW2824 can be extended up to 16 channel application using cascade connection and cascade operation is working independently for X and Y path. This means that X path can be operated with cascaded connection even though Y path is working in normal operation. For chip-to-chip cascade connection, the PB_IN and PB_VALID pin in master chip should be connected to VDOUTX and VSENC pin in slaver chips. So the playback input is available only in lowest slaver chips and VDOUTX and VSENC output pin is available only in master device when cascaded.

For cascade operation, LINK_EN, LINK_NUM and LINK_LAST (1x00) registers should be controlled properly. The following Fig 29 illustrates cascade connection for dual path.

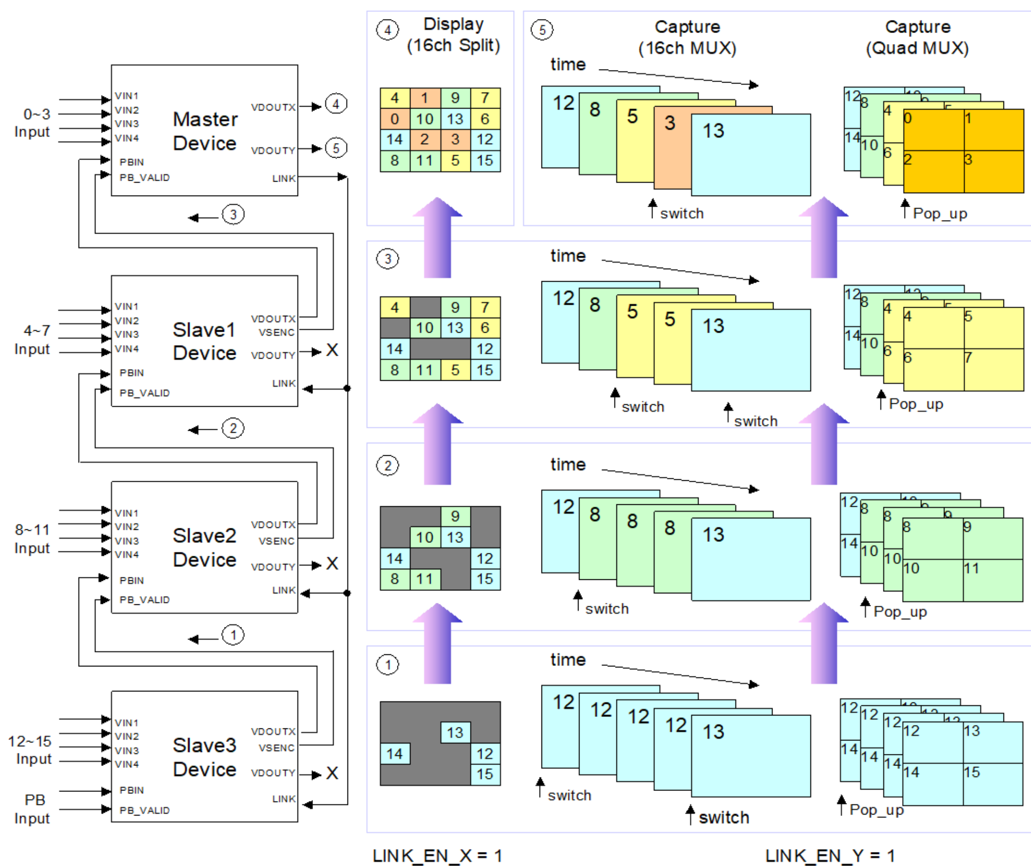


Fig 29 Cascade connection with dual path

When operating with cascade connection, the TW2824 transfers all information of slaver chip to master chips including video data, zoom factors and switching information except overlay information such as box, mouse pointer and OSD information. Therefore, master chip should be controlled for overlay and the lowest slaver chip should be controlled for the others such as video data, zoom and switching. The information of switching channel, MUX_OUT_CH (1x0B, 1x3B) can be taken from master chip.

When 2 channels are merged by chip-to-chip cascade, there is a priority from top to bottom layer, popup attributed channel of master device, popup attributed channel of slaver device, non-popup attributed channel of master device and non-popup attributed channel of slaver device. Using this popup attribute, the TW2824 can implement QUAD MUX operation or channel overlay in chip-to-chip cascade connection.

The following Fig 30 illustrates cascade connection with X path only. In this case, user can increase recording rate up to 480 frame/sec with 4 chip cascade connection.

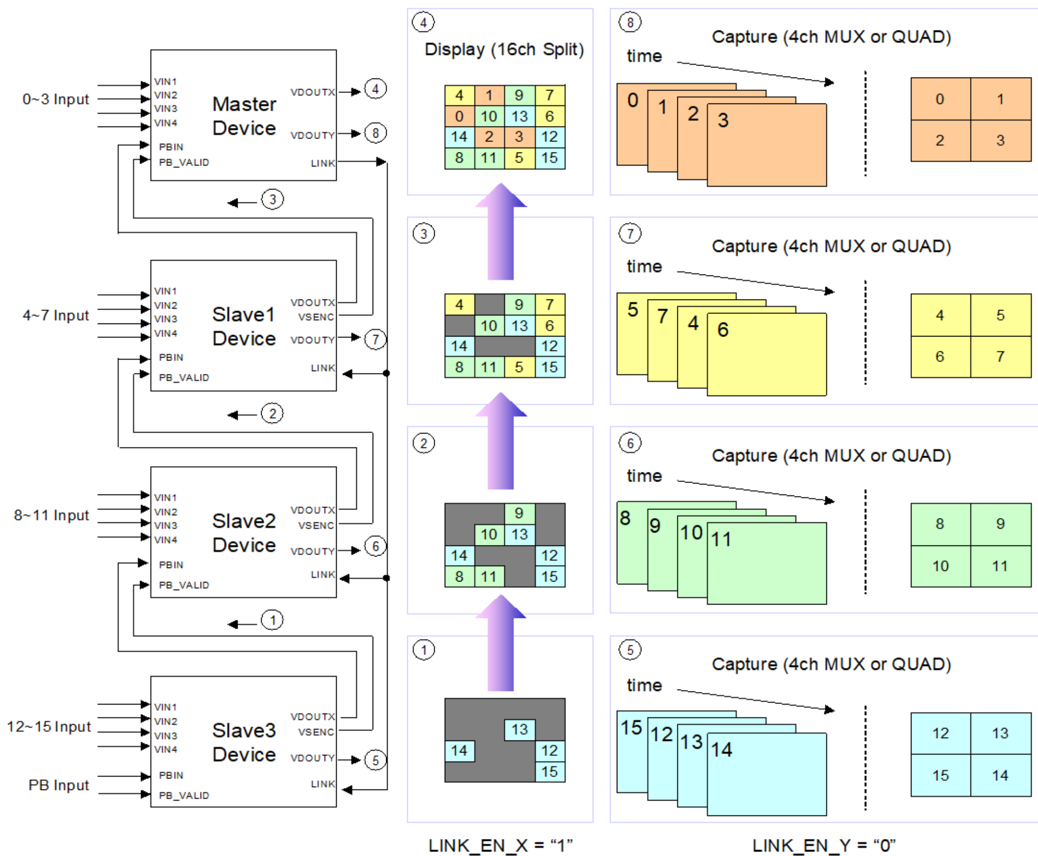


Fig 30 Cascade connection with X path only

Path-to-Path Cascade

The TW2824 also supports overlay function between X path and Y path. Path-to-path overlay function makes X path overlay on Y path or Y path overlay on X path. This function is useful to display 5 channel video for only single path application.

By enabling the OVERLAY_X (1x00) register, active video of Y path can be overlaid on X path and the opposite case is also possible via OVELAY_Y (1x00) register. When 2 paths are merged by overlay function, there is a priority from top to bottom layer, popup attributed channel of main path, popup attributed channel of overlaid path, non-popup attributed channel of main path and non-popup attributed channel of overlaid path. The example of path-to-path overlay function is shown in Fig 31. In this example, a main path is X path which has 4 channels (CH0, CH1 CH2, CH3) with non-popup attributed, and the overlaid path is Y path which has 1 channel (CH0) with popup attributed.

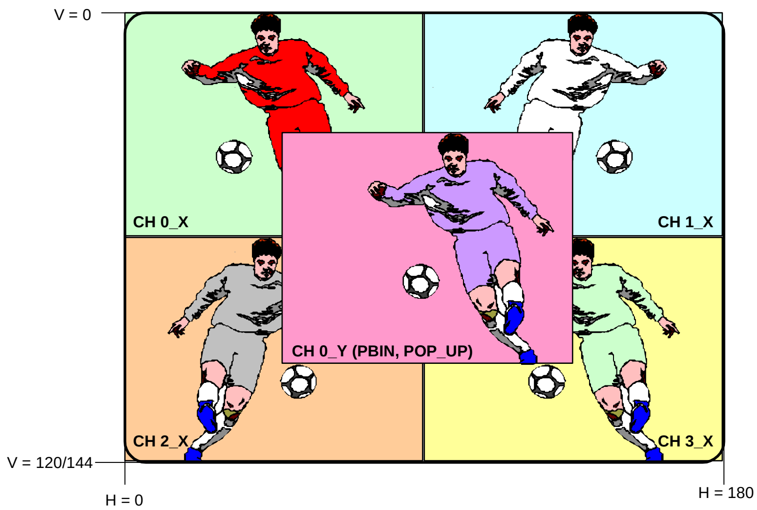


Fig 31 Example of path-to-path overlay function

OSD (On Screen Display) Overlay

The TW2824 provides various OSD (On Screen Display) overlays such as character/bitmap overlay, box overlay and mouse pointer that can be overlaid on X and Y path independently. The following Fig 32 shows OSD overlay block diagram. The font data can be downloaded from host and supported up to 128 fonts. The TW2824 has 16 programmable single boxes and four 2D arrayed boxes that are programmable for size, position and color.

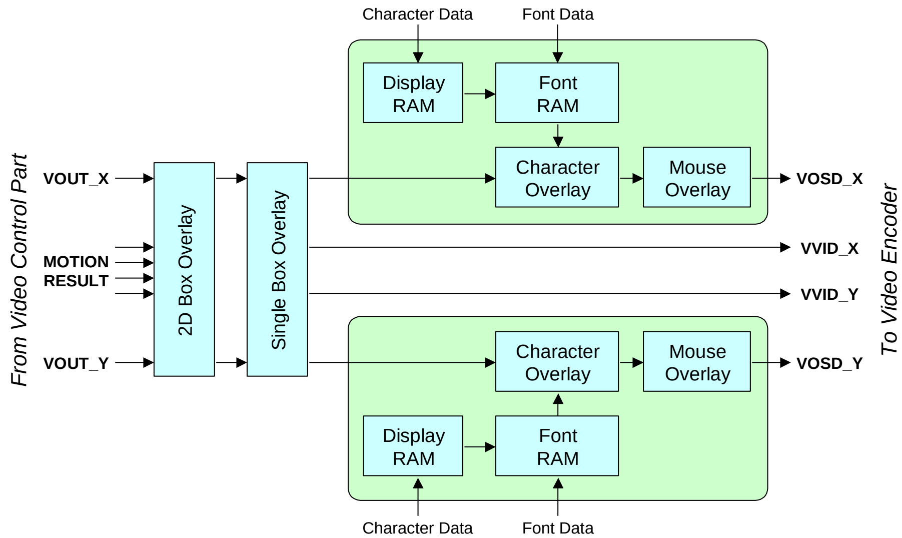


Fig 32 OSD overlay block diagram

Dual analog video outputs and dual digital video outputs can enable or disable a character and mouse pointer respectively. The overlay priority of OSD layer is shown in Fig 33. The various OSD overlay function is very useful to build GUI interface.

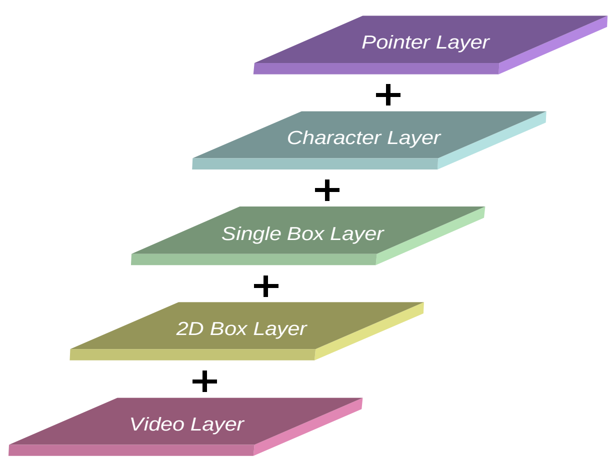


Fig 33 The overlay priority of OSD layer

CHARACTER/BITMAP OVERLAY

The TW2824 has character overlay function for X and Y path independently. Each character overlay function block consists of a font RAM, a display RAM and an overlay control block. A font RAM stores font data that can be downloaded from host at anytime. A display RAM stores index, position and attributes of character to be displayed. Character size can be defined as 8~14 dots in horizontal and 10 ~ 16 lines in vertical direction.

Bitmap data can also be downloaded from host just like character. That is, Bitmap is almost same as character except the control of class 0 color. A character type has a blank for class 0 color in default mode, but a bitmap color has a selectable color for it. However, if CLASSEN0 (1x81) is set to “1”, even a character type can have a selectable color like bitmap type. In that case, a character type is completely same as a bitmap type. The character and bitmap types can be selected via TYPE bit of character attributes in display RAM.

Download Font Group

The TW2824 supports 4 different font groups and each font group can have 128 fonts. A font consists of several dots such as 8 (10, 12, 14) x 10 (12, 14, 16) dots. 1 dot is composed of 2 pixels x 1 video line and each dot has 2 bits to define colors (class 0, class1, class2 and class3). The following Fig 34 shows a font RAM structure.

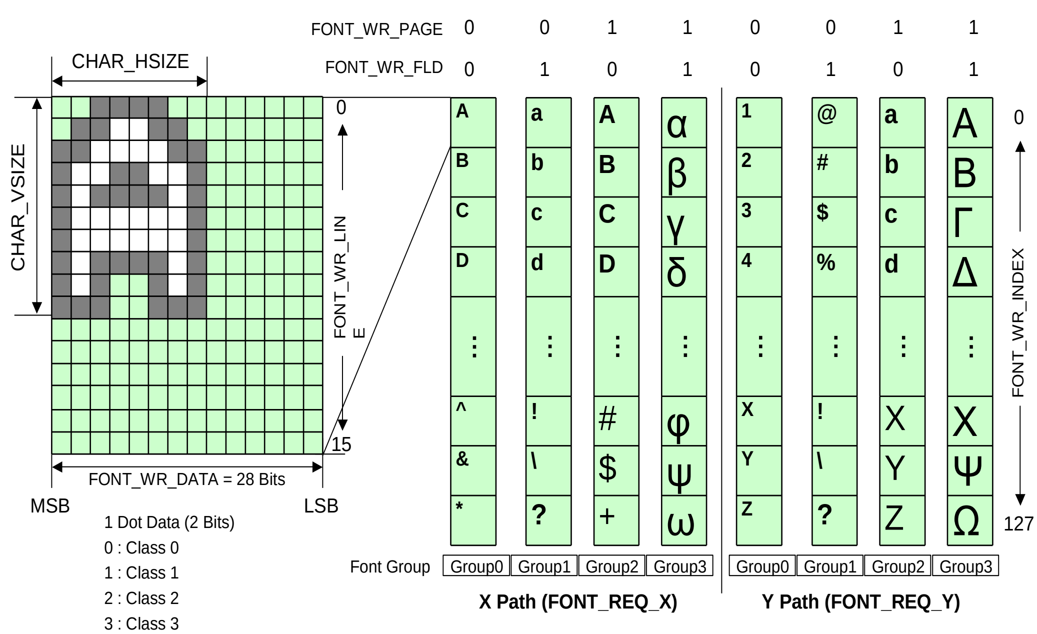


Fig 34 Font RAM structure

Font data can be written to font RAM via FONT_WR_DATA (1x7A ~ 1x7D), FONT_WR_INDEX (1x7E), FONT_WR_LINE, FONT_WR_FLD, FONT_WR_PAGE and FONT_REQ (1x7F) register. By setting “1” to FONT_REQ, font data in the FONT_WR_DATA is transferred to font RAM addressed by FONT_WR_INDEX, FONT_WR_LINE, FONT_WR_FLD and FONT_WR_PAGE. The FONT_REQ register has status information of transferring in read mode. If FONT_REQ = “1” in read mode, it means that the TW2824 is busy in transferring font data. In this case, additional request cannot be accepted. The TW2824 has individual 2 FONT_REQ for X and Y path so that the different font data can be stored in font RAM of X and Y path. The TW2824 requires special font data for index 0 to define blank character that will be discussed in write character section. Fig 35 shows the flow chart of transferring font data to font RAM.

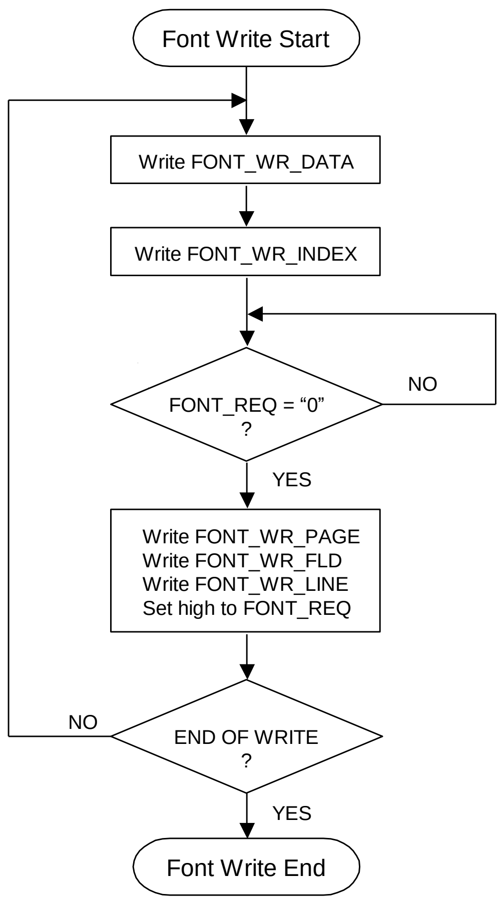


Fig 35 Flow chart of downloading font data

Select Font Group

The font group can be divided into 4 groups for X and Y path as shown in Fig 34. The FONT_RD_PAGE register selects one of two pages. Setting "0" to FONT_RD_FLD register makes a character overlay function disabled. If the FONT_RD_FLD register is set to "1" or "2", one group fonts are displayed for both odd and even field. But by setting "3" on FONT_RD_FLD register, the different font groups are displayed on odd and even field respectively so that the character resolution can be enhanced 2 times in vertical direction. The following Fig 36 is shown for the structure of the font group.

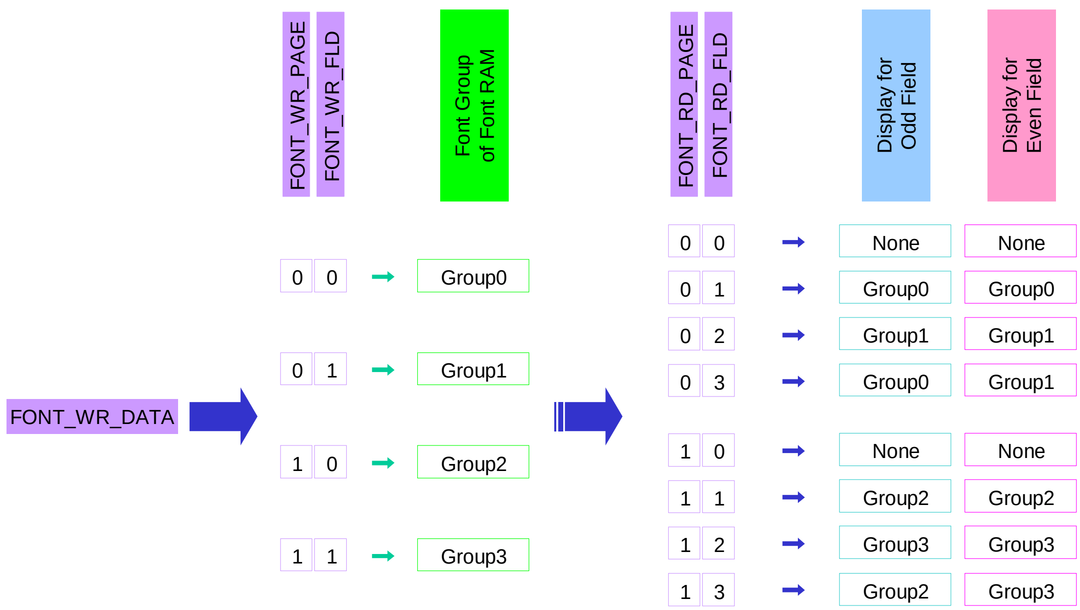


Fig 36 Structure of font group

Write Character

The TW2824 has independent 2 display RAM for X and Y path and each character in display RAM has its own character's attributes which include mix, blink, class 3 color, type and font index. The display RAM consists of 45x29 character's attributes. Actually the number of displayed characters depends on character size. The horizontal and vertical address of display RAM represents character position to be displayed. The following Fig 37 shows the structure of display RAM.

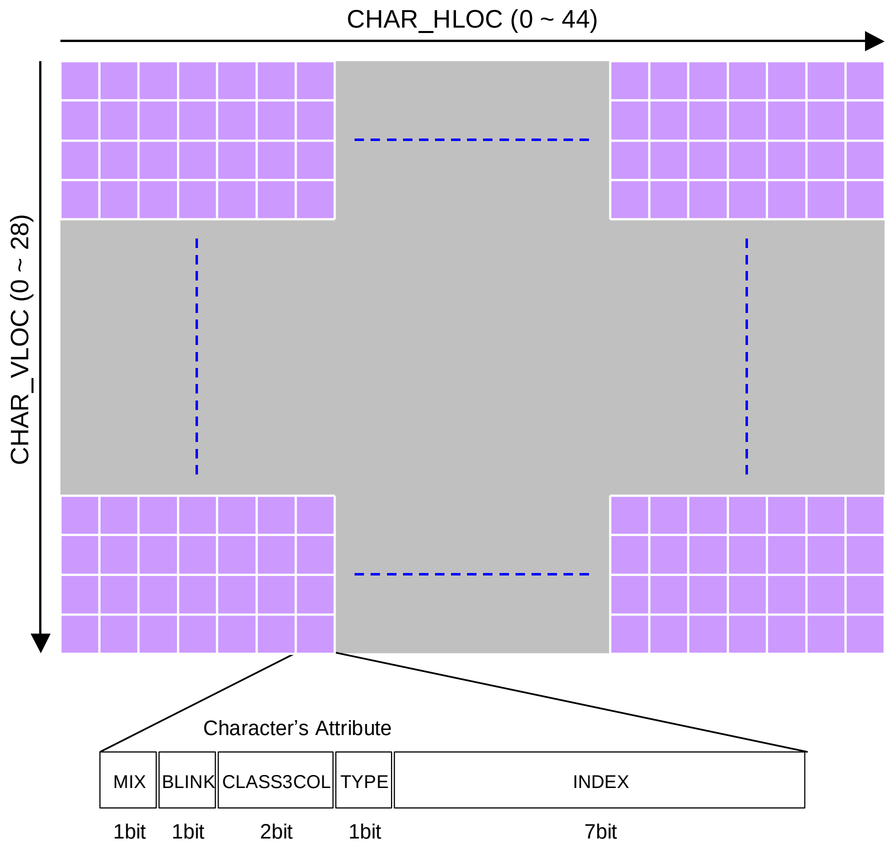


Fig 37 Display RAM structure

Before writing character's attribute, the CHAR_PATH, CHAR_VLOC (1x9Ch) and CHAR_HLOC (1x9Dh) register should be written previously to define the location of displayed character. CHAR_PATH defines the path (X or Y path) and CHAR_VLOC / CHAR_HLOC defines the vertical / horizontal location of displayed character. The character's attribute consists of 12bit so that 2 bytes are required to write in display RAM. The TW2824 supports the special procedure for writing to and reading from display RAM as shown in Fig 38. If the character's attributes are written continuously with the same path and vertical location, CHAR_HLOC value increases by 1 automatically.

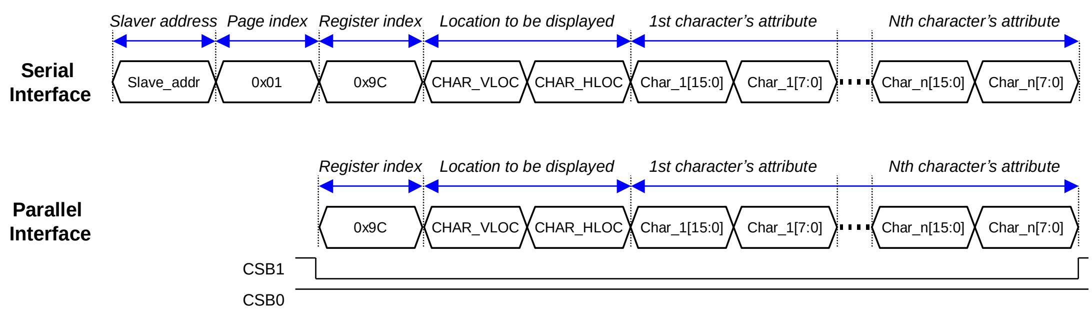


Fig 38 Writing procedure to display RAM

The TW2824 also supports a useful function that writes blank character to whole display RAM automatically by setting "1" to RAMCLR (1x81). This function requires that font data in index 0 should be blank character and the CLASSEN0 (1x81) register should be set to "0" because it writes this character in index 0 to whole display RAM. This RAM clear function takes about 100usec and the RAMCLR register will be cleared by itself after finished.

Character Attribute

Each character has its own attributes in display RAM that includes mix, blink, class 3 color of character, type and font index. The mix attribute makes character mixed with video data by half tone and blink attribute makes blinked character with the period defined in PHIGH and PLOW (1x81) register. The class 3 color of character takes one of 4 colors defined in the CLASS3COL (1x89 ~ 1x8C) register. The type attribute defines one of 2 types, character or bitmap type for each character and the font index attribute defines address of font. The mix and blink attributes can be enabled for each class via the CHAR_MIX (1x87), CHAR_BLK (1x88) register for each character or bitmap.

Character Color

The TW2824 provides 16 different colors that consist of fixed 12 colors (8 colors from color bar of 75% amplitude 100% saturation and 100% white, 50% gray, 25% gray and 75% blue) and user's defined 4 colors using the CLUT (1x90 ~ 1x9B) register. The class 0, 1 and 2 color of character will be one of 16 colors via the CLASS0COL, CLASS1COL and CLASS2COL (1x8D ~ 1x8F) registers and are applied to all of characters to be displayed. For class 3 color, 4 colors are predefined via the CLASS3COL (1x89 ~ 1x8C) register and each character can take one of these 4 colors using character's attribute as described previously. The different color selection for each character and bitmap can be supported also.

Character Size and Space

The TW2824 supports different character size for X path and Y path and the character size can be varied horizontally and vertically. The CHAR_HSIZE (1x82) register defines horizontal character size that can be one of 8, 10, 12 and 14 dots and the CHAR_VSIZE (1x82) register defines vertical character size that can be one of 10, 12, 14 and 16 lines. The character size is not required to be same with font size. If character size is greater than downloaded font size, garbage data are displayed in character region and if character size is smaller than downloaded font size, font will be cropped by character size.

Likewise, the space between characters can be varied horizontally and vertically. The CHAR_HSPC (1x83, 1x85) register defines horizontal character space that can be increased by 1 dot unit and the CHAR_VSPC (1x83, 1x85) register defines vertical character space that can be increased by 1 line unit. The TW2824 can define the horizontal and vertical position for first dot of first character. The CHAR_HDEL (1x84, 1x86) register defines horizontal delay and the CHAR_VDEL (1x84, 1x86) register defines vertical delay. Each unit is same as CHAR_HSPC and CHAR_VSPC unit. The following Fig 39 shows the definition of character size and space.

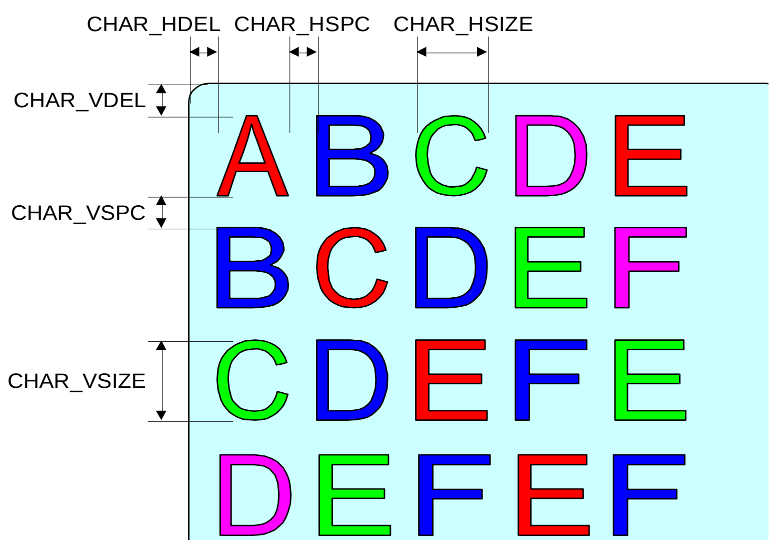


Fig 39 Definition of character size and space

BOX OVERLAY

The TW2824 supports two kinds of box overlay such as 16 single boxes and 4 2-dimensional arrayed boxes.

Single Box

The TW2824 provides 16 single boxes that can be a flat type or 3D type using the BOX_TYPE (2x03) register. The flat type is just simple rectangular box and 3D type looks like 3 dimension view. Each single box has programmable location and size parameters with the BOX_HL (2x08 + 5N, N = 0 ~ 15), BOX_HW (2x09 + 5N, N = 0 ~ 15), BOX_VT (2x0A + 5N, N = 0 ~ 15) and BOX_VW (2x0B + 5N, N = 0 ~ 15) registers. The BOX_HL is the horizontal location of box with 2 pixel unit and the BOX_HW is the horizontal size of box with 4 pixel unit. The BOX_VT is the vertical location of box with 1 line unit and BOX_VW is the vertical size of box with 2 line unit. There are some definitions about single box as shown in Fig 40.

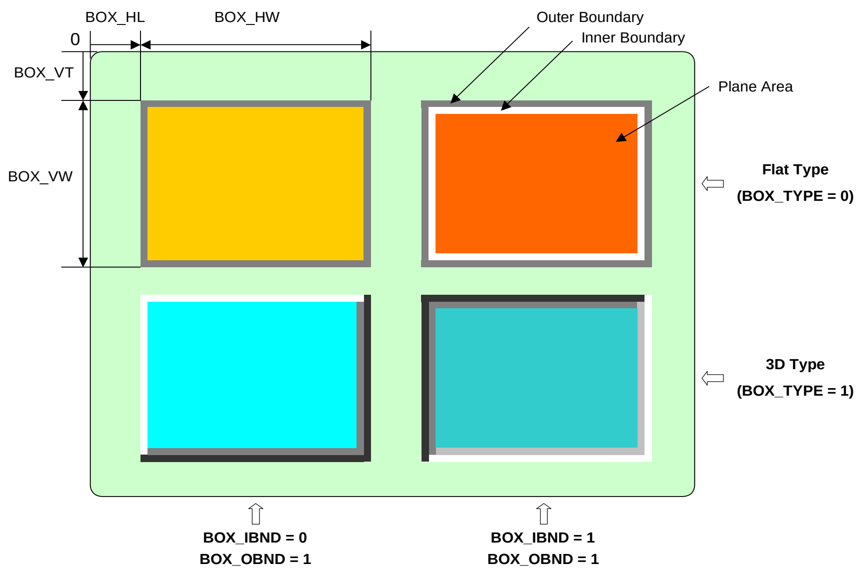


Fig 40 Single box structure

The other controllable parameters are plane color, boundary color, boundary enable, luminance level control of plane. The single box plane is controlled via BOX_OBND (2x07 + 5N, N = 0~15) and BOX_IBND (2x07 + 5N, N = 0~15) register as described in Table 4. BOX_PLNEN (2x03) register enables each plane color and its color is defined by BOX_PLNSEL (2x07 + 5N, N = 0~15) and BOX_PLNCOL (2x05, 2x06) register. Using BOX_PLNSEL, the plane of each single box can have one of 4 colors defined by BOX_PLNCOL as described in character color section. Actually the TW2824 provides total 16 different colors that consist of fixed 12 colors (8 colors from color bar and 100%, 50%, 25% gray and 75% blue) and user's defined 4 colors using CLUT (1x90 ~ 1x9B) register. This color table is used in common with plane color for single box and character color. The color of box boundary is defined by BOX_TYPE (2x03), BOX_OBND (2x07 + 5N, N = 0~15), BOX_IBND (2x07 + 5N, N = 0~15) and BOX_BNDCOL (2x04) registers

Table 4 The Color of Single Box Boundary

Boundary		Control Register			Color Description	
		BOX_TYPE	BOX_OBND	BOX_IBND	Register	Color
Outer		0 (Flat Type)	0	0	BOX_ BNDCOL [7:4]	Box off
			0	1		Boundary off
			1	0		0~10 : 0, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100 IRE Gray 11~14 : Selected by BOX_PLNCOL0 ~ BOX_PLNCOL3. 15 : Same as plane color with 20IRE down of luminance
			1	1		
Inner			0	0	BOX_ BNDCOL [3:0]	Box off
			1	0		Same as inner area
			0	1		0~10 : 0, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100 IRE Gray 11~14 : Selected by BOX_PLNCOL0~BOX_PLNCOL3. 15 : Same as plane color with 20IRE up of luminance
			1	1		
Outer	Left & Top	1 (3D Type)	0	0	BOX_ BNDCOL [7:6]	Box off
			0	1		Boundary off
			1	0		0~3 : 90, 80, 70, 60 IRE Gray
			1	1		0~3 : 0, 10, 20, 30 IRE Gray
	Right & Bottom		0	0	BOX_ BNDCOL [5:4]	Box off
			0	1		Boundary off
			1	0		0~3 : 0, 10, 20, 30 IRE Gray
			1	1		0~3 : 90, 80, 70, 60 IRE Gray
Inner	Left & Top		0	0	BOX_ BNDCOL [3:2]	Box off
			0	1		Boundary off
			1	0		Same as inner area
			1	1		0~3 : 30, 40, 50, 60 IRE Gray
	Right & Bottom		0	0	BOX_ BNDCOL [1:0]	Box off
			0	1		Boundary off
			1	0		0~3 : 30, 40, 50, 60 IRE Gray
			1	1		0~3 : 70, 60, 50, 40 IRE Gray

For the box plane, luminance level can be controlled through the BOX_IBND register when BOX_EMP (2x03) register = ‘1”. BOX_IBND = “1” makes luminance level of plane down by 20IRE and BOX_IBND = “0” makes up by 20IRE. The each box plane can be mixed with video data via the BOX_PLNMIX (2x07 + 5N, N = 0~15) register. The BOX_PATH (2x07 + 5N, N = 0~15) register determines the boxes to be displayed on X or Y path because box overlay is supported by only one path.

In case that more than 2 boxes have same region, there will be confliction how to display for that region. Generally TW2824 defines that box 0 has priority over box 15. So if a conflicting happens between more than 2 boxes, box 0 will be displayed first as top layer and box 1 to box 15 are hidden beneath that are not supported for pop-up attribute unlike channel display.

2Dimensional Arrayed Box

The TW2824 supports 4 2D arrayed boxes that have programmable cell size up to 16x16. The 2D arrayed box is useful to make a table or display motion detection result for analog input.

The 2DBOX_HNUM and 2DBOX_VNUM (2x66, 2x6D, 2x74, 2x7B) registers define the number of row and column cells. For each 2D arrayed box, the horizontal location of left-top for 2D box is defined by the 2DBOX_HL (2x63, 2x6A, 2x71, 2x78) register with 2 pixels step and the vertical location of left-top is defined by the 2DBOX_VT (2x62, 2x69, 2x70, 2x77) register with 1 line step. The vertical size of each cell is defined by the 2DBOX_VW (2x64, 2x6B, 2x72, 2x79) register with 1 line step and the horizontal size is defined by the 2DBOX_HW (2x65, 2x6C, 2x73, 2x7A) register with 2 pixel step. So the whole size of 2D arrayed box is same as the sum of cells in row and column.

The boundary of 2D arrayed box can be enabled by the 2DBOX_BNDEN (2x61, 2x68, 2x6F, 2x76) register and its color is controlled via the 2DBOX_BNDCOL (2x60) register which selects one of 4 colors such as 0% black, 25% gray, 50% gray and 75% white.

The plane of 2D arrayed box can be enabled by the 2DBOX_PLNEN (2x61, 2x68, 2x6F, 2x76) register and its color is controlled by the 2DBOX_PLNCOL (2x60) register which selects one of 16 colors as described in character color and plane color of single box section. The plane can be mixed with video data by the 2DBOX_MIX (2x61, 2x68, 2x6F, 2x76) register.

Specially, the TW2824 provides the function to indicate cursor cell inside 2D arrayed box. The cursor cell can be enabled by 2DBOX_CUREN (2x61, 2x68, 2x6F and 2x76) register and its location to be displayed is defined by 2DBOX_CUR_HP and 2DBOX_CUR_VP (2x67, 2x6E, 2x75 and 2x7C) registers. Its color is a reverse color of cell boundary. It is useful function to control motion mask region.

Even though 2D arrayed box is available for drawing a table, its function is used mainly to display motion information. 2D arrayed box can be selected to work in table mode or motion display mode through the 2DBOX_MODE (2x61, 2x68, 2x6F, 2x76) register. When 2D arrayed box is working in motion display mode, the plane of 2D arrayed box shows the mask information according to the MD_MASK register automatically. For the motion display mode, additional narrow boundary of each cell is provided to display motion detection result for each cell and its color is a reverse color of cell boundary like cursor cell.

The TW2824 has 4 2D arrayed boxes so that 4 video channels can have its own 2D arrayed box for motion display mode. To overlay mask information and motion result on video data properly, the scaling ratio of video should be matched with 2D arrayed box size.

Each 2D arrayed box can be displayed in only one path that is defined by the 2DBOX_PATH (2x61, 2x68, 2x6F and 2x76) register. The following Fig 41 shows the 2D arrayed box in table mode and Fig 42 shows 2D arrayed box in motion display mode.

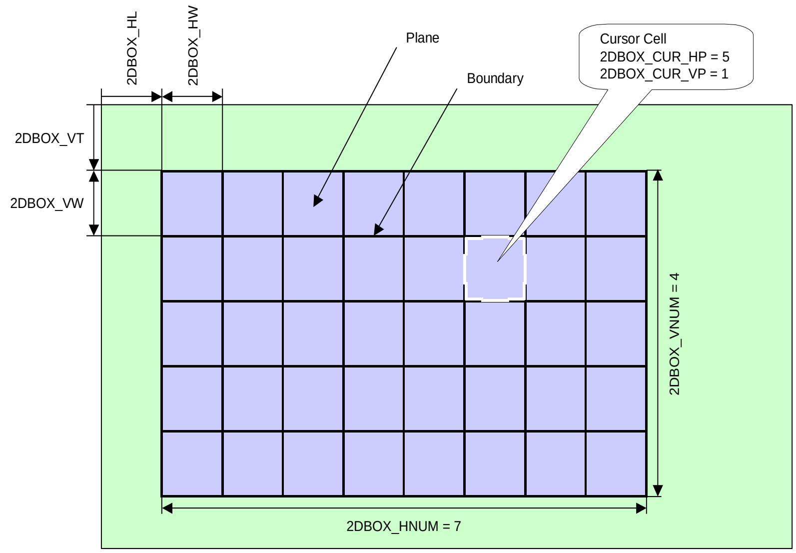


Fig 41 2D arrayed box in table mode

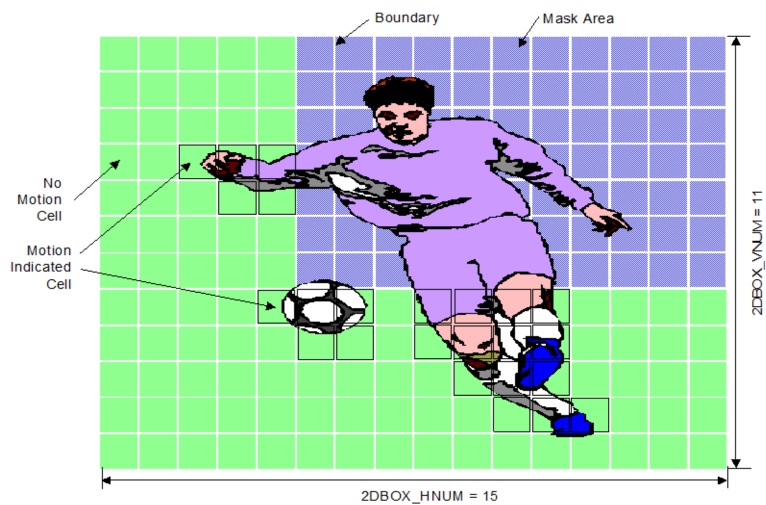


Fig 42 2D arrayed box in motion display mode

In case that more than 2 2D arrayed boxes have same region, there will be confliction how to display for that region. Generally TW2824 defines that 2D arrayed box 0 has priority over 2D arrayed box 3. So if a conflicting happens between more than 2 2D arrayed boxes, 2D arrayed box 0 will be displayed first as top layer and 2D arrayed box 1, box 2, box 3 are hidden beneath that are not supported for pop-up attribute like single box.

MOUSE POINTER

The TW2824 supports two kinds of mouse pointer that has attributes such as pointer enable, pointer location, blink enable and sub-layer enable. Mouse pointer can be overlaid on both X and Y path independently even though all attributes are applied to both paths in common.

The mouse pointer is located in the full screen according to the CUR_HP (2x01) register with 2 pixel step and CUR_VP (2x02) register with 1 line step. Two kinds of mouse pointer are provided through the CUR_TYPE (2x00) register. The CUR_SUB (2x00) register determines a pointer inside area to be filled with 100% white or to be transparent and CUR_BLINK (2x00) register controls a blink function of mouse. Actually the CUR_ON (2x00) register enables or disables mouse pointer for X and Y path independently. The following Fig 43 describes the parameters of mouse pointer.

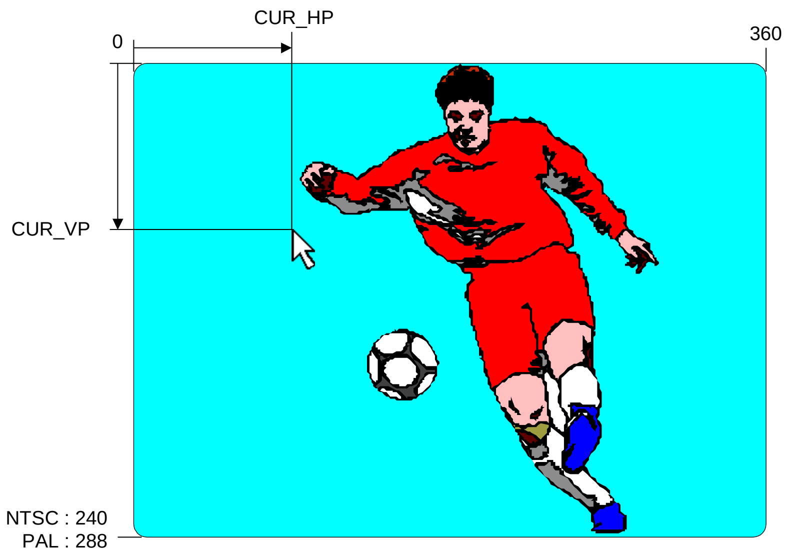


Fig 43 Parameters of mouse pointer

Video Output

The TW2824 supports dual digital video outputs with ITU-R BT.656 format and 2 analog video outputs with built-in video encoder at the same time. Dual video controllers described above generate 4 kinds of video data, X path video data with or without OSD and Y path video data with or without the OSD. CCIR_IN (1x70) register selects one of 4 video data for the digital video output and ENC_IN (1x70) register selects one of 4 video data for the analog video output as shown in Fig 44.

The TW2824 supports all NTSC and PAL standards for analog output which can be composite or S-video video for both X and Y path. All outputs can be operated as master mode to generate timing signal internally or slave mode to be synchronized with external timing.

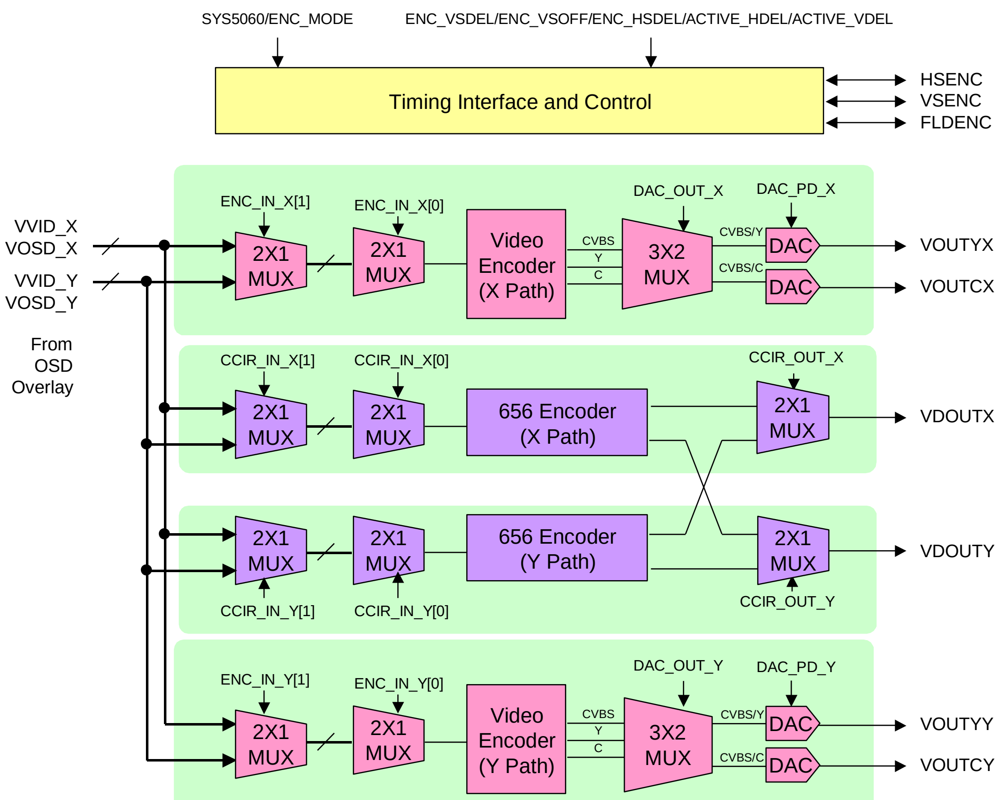


Fig 44 Video output selection

The TW2824 has device option for dual output such as TW2824MS and TW2824QS. These devices have a limitation for output selection. That is, the value of CCIR_IN_X [1], CCIR_IN_Y [1] and ENC_IN_Y [1] is equal to ENC_IN_X [1] so that only one path is available for output selection.

ANALOG VIDEO OUTPUT

The TW2824 supports analog video output using built-in video encoder which generates composite or S-video with 10 bits dual DAC for both X and Y path. The incoming digital video are adjusted for gain and offset according to NTSC or PAL standard. Both the luminance and chrominance are band-limited and interpolated to 27MHz sampling rate for digital to analog conversion. The NTSC output can be selected to include a 7.5IRE pedestal. The TW2824 also provides internal test color bar generation.

Output Standard Selection

The TW2824 supports various video standard outputs via the SYS5060 (1x00) and ENC_FSC, ENC_PHALT, ENC_PED (1x77) registers as described in the following Table 5.

Table 5 Analog output video standards

Format	Specification			Register			
	Line/Fv (Hz)	Fh (KHz)	Fsc (MHz)	SYS5060	ENC_ FSC	ENC_PHALT	ENC_PED
NTSC-M	525/59.94	15.734	3.579545	0	0	0	1
NTSC-J							0
NTSC-4.43	525/59.94	15.734	4.43361875	0	1	0	1
NTSC-N	625/50	15.625	3.579545	1	0	0	0
PAL-BDGHI	625/50	15.625	4.43361875	1	1	1	0
PAL-N							1
PAL-M	525/59.94	15.734	3.57561149	0	2	1	0
PAL-NC	625/50	15.625	3.58205625	1	3	1	0
PAL-60	525/59.94	15.734	4.43361875	0	1	1	0

If the ENC_ALTRST (1x77) register is set to “1”, phase alternation can be reset every 8 field so that phase alternation keeps same phase every 8 field.

Luminance Filter

The band of luminance signal can be selected as shown in the following Fig 45.

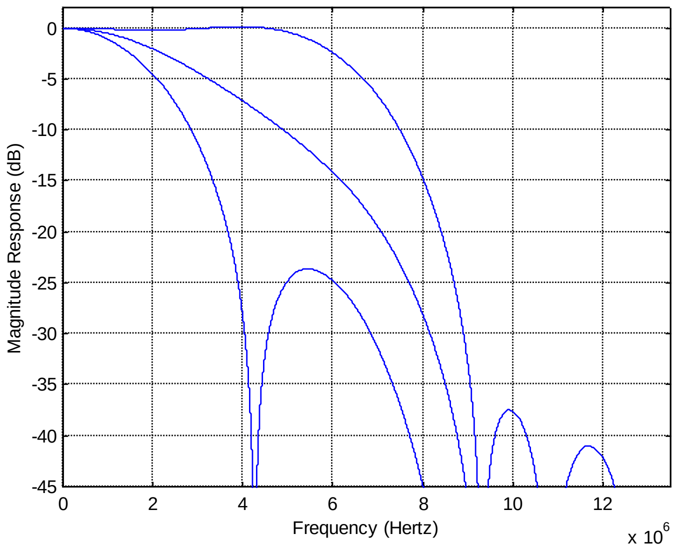


Fig 45 Characteristics of luminance filter

Chrominance Filter

The band of chrominance signal can be selected as shown in the following Fig 46.

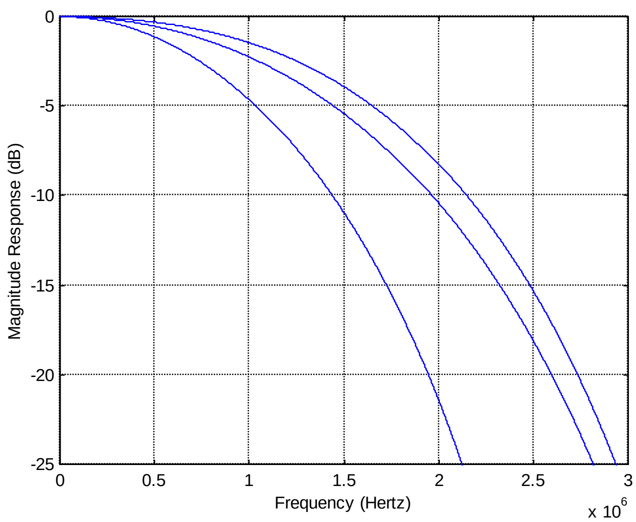


Fig 46 Characteristics of chrominance Filter

Digital-to-Analog Converter

Digital video data from video encoder is converted to analog video signal by DAC (Digital to Analog Converter). Analog video signal format can be selected for both X and Y path independently via the DAC_OUT (1x71) register as dual composite when DAC_OUT = “1” and S-video when DAC_OUT = “0”. Each DAC can be disabled independently to save power by the DAC_PD (1x71) register.

A simple reconstruction filter is required externally to reject noise as shown in Fig 47.

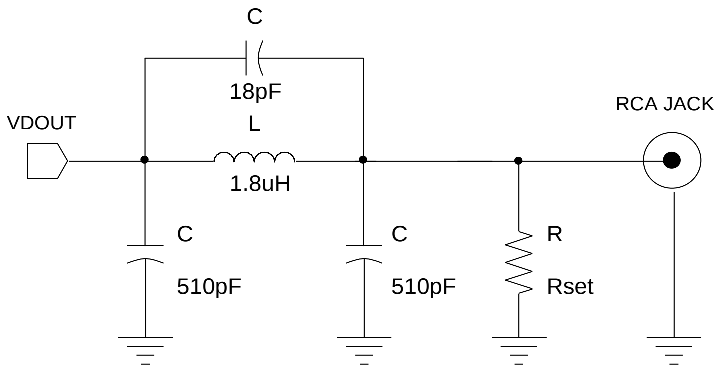


Fig 47 Example of reconstruction filter

The frequency responses of above reconstruction filters are shown in the following Fig 48.

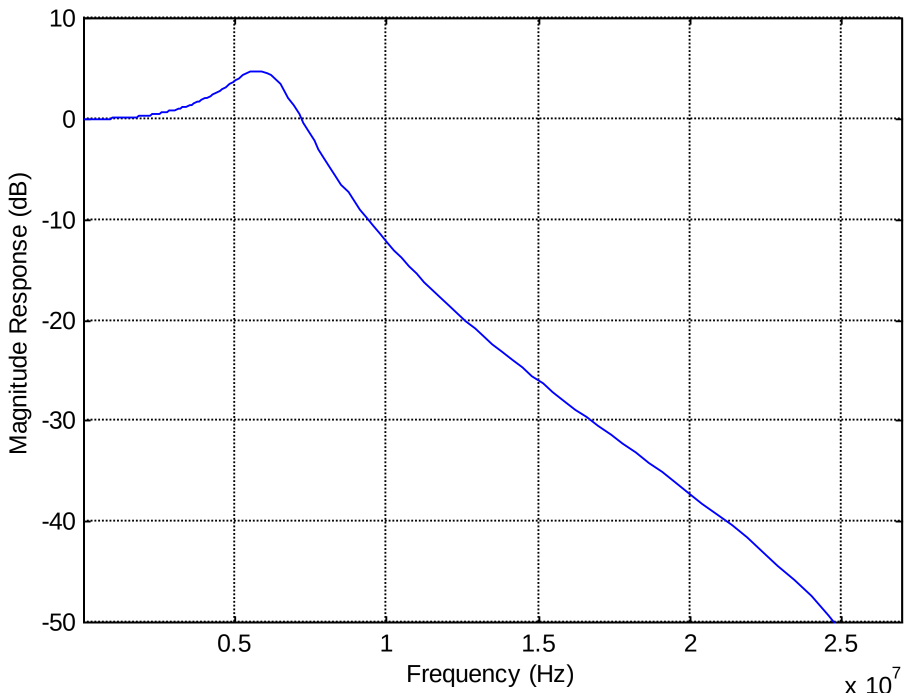


Fig 48 Frequency response of reconstruction filter

DIGITAL VIDEO OUTPUT

The digital output data with ITU-R BT.656 format is synchronized with CLK27ENC pin which is 27MHz for single output or 54MHz for dual output. Each digital data of X and Y path can be output through VDOUTX and VDOUTY pin respectively on single output mode. For the dual output mode, both X and Y path output can come out through only one VDOUTX or VDOUTY. The level of active video of ITU-R BT.656 can be limited to 16 ~ 235 level by the CCIR_LMT (1x73h) register.

Table 6 ITU-R BT.656 SAV and EAV code sequence

	Line		Condition			FVH			SAV/EAV Code Sequence			
	From	To	Field	Vertical	Horizontal	F	V	H	First	Second	Third	Fourth
60Hz (525Lines)	523	3	EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1
					SAV			0				0xEC
	4	19	ODD	Blank	EAV	0	1	1				0xB6
					SAV			0				0xAB
	20	259	ODD	Active	EAV	0	0	1				0x9D
					SAV			0				0x80
	260	265	ODD	Blank	EAV	0	1	1				0xB6
					SAV			0				0xAB
	266	282	EVEN	Blank	EAV	1	1	1				0xF1
					SAV			0				0xEC
	283	522	EVEN	Active	EAV	1	0	1				0xDA
					SAV			0				0xC7
50Hz (625Lines)	1	22	ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6
					SAV			0				0xAB
	23	310	ODD	Active	EAV	0	0	1				0x9D
					SAV			0				0x80
	311	312	ODD	Blank	EAV	0	1	1				0xB6
					SAV			0				0xAB
	313	335	EVEN	Blank	EAV	1	1	1				0xF1
					SAV			0				0xEC
	336	623	EVEN	Active	EAV	1	0	1				0xDA
					SAV			0				0xC7
	624	625	EVEN	Blank	EAV	1	1	1				0xF1
					SAV			0				0xEC

Single Output Mode

For the single output mode, each digital output data in X and Y path can be output at 27MHz through VDOUTX and VDOUTY pin that are synchronized with CLK27ENCX and CLK27ENCY respectively. The polarity and frequency of CLK27ENCX and CLK27ENCY can be controlled independently by ENCCLK_X, ENCCLK_Y, ENCCLKP_X and ENCCLKP_Y (1x5F) registers. The data to be output is selected by the CCIR_OUT (1x72) register which selects X path data for "0" and Y path data for "1". The timing diagram of single output mode is shown in following Fig 49.

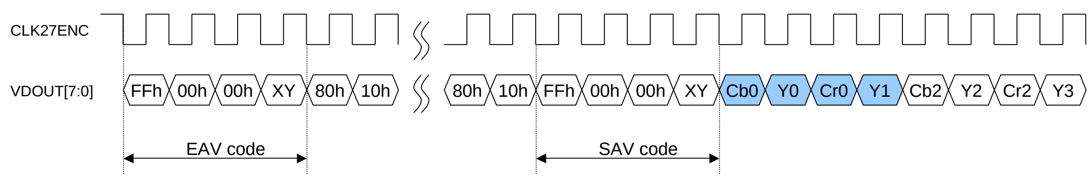


Fig 49 Timing diagram of single output mode

Dual Output Mode

The TW2824 also supports dual output mode that is time-multiplexed with X and Y path data at 54MHz clock rate. The sequence is related with the CCIR_OUT (1x72) register that X path data precedes Y path for CCIR_OUT = "2" and Y path data precedes X path for CCIR_OUT = "3". The data to be output is synchronized with 54MHz CLK27ENCX and CLK27ENCY pins. The polarity and frequency of CLK27ENCX and CLK27ENCY can be controlled independently by ENCCLK_X, ENCCLK_Y, ENCCLKP_X and ENCCLKP_Y (1x5F) registers. The timing diagram of dual output mode is illustrated in Fig 50. The dual output mode is useful to reduce number of pins for interface with other devices.

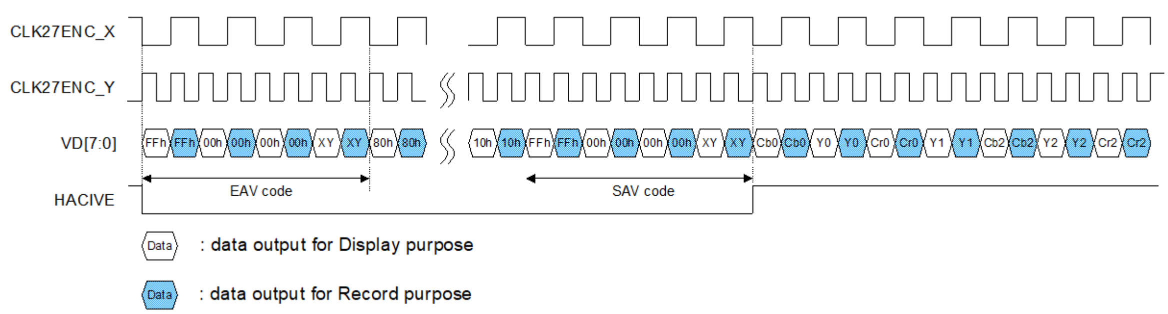


Fig 50 Timing diagram of dual output mode

TIMING INTERFACE AND CONTROL

The TW2824 can be operated in master mode or slave mode via the ENC_MODE (1x73) register. In master mode, TW2824 can generate all of timing signals internally while TW2824 receives all of timing signals from external device in slave mode.

The polarity of horizontal, vertical sync and field flag can be controlled by the ENC_HSPOL, ENC_VSPOL and ENC_FLDPOL (1x73) register respectively for both master and slaver mode. The TW2824 can detect field polarity from vertical sync and horizontal sync via the ENC_FLD (1x73) register or can detect vertical sync from the field flag via the ENC_VS (1x73) register.

The TW2824 provides or receives timing signal through the HSENC, VSENC and FLDENC pins. To adjust the timing of those pins, the TW2824 has the ENC_HSDEL (1x75), ENC_VSDEL and ENC_VSOFF (1x74) registers which control only the related signal timing regardless of analog and digital video output. Likewise, by controlling the ACTIVE_VDEL (1x76) register and ACTIVE_HDEL (1x76) registers, only active video period can be shifted on horizontal and vertical direction independently. The shift of active video period produces the cropped video image because the timing signal is not changed even though active period is moved. So this feature is restricted to adjust video location in monitor for example. The active video data period of analog video output is same as digital video output so that the video timing of both outputs can be controlled in common. The detailed timing diagram is illustrated in the following Fig 51.

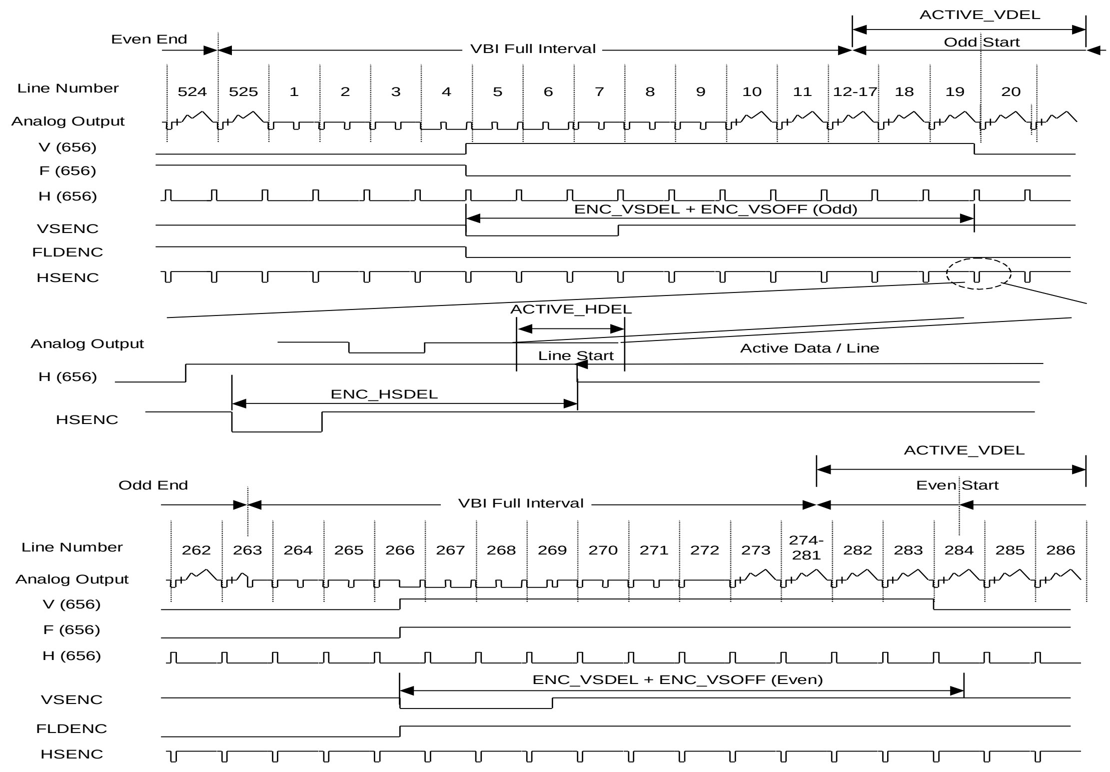


Fig 51 Horizontal and vertical timing control

Host Interface

The TW2824 provides serial and parallel interfaces that can be selected by HSPB pin. When HSPB is low, the parallel interface is selected, the serial interface for high. Some of the interface pins serve a dual purpose depending on the working mode. The pins HALE and HDAT [7] in parallel mode become SCLK and SDAT pins in serial mode and the pins HDAT [6:1] and HCSB0 in parallel mode become slave address in serial mode respectively. Each interface protocol is shown in the following figures.

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Table 7 Pin assignment for serial and parallel interface

Pin Name	Serial Mode	Parallel Mode
HSPB	HIGH	LOW
HALE	SCLK	AEN
HRDB	Not Used (VSSO)	RENB
HWRB	Not Used (VSSO)	WENB
HCSB0	Slave Address[0]	CSB0
HCSB1	Not Used (VSSO)	CSB1
HDAT[0]	Not Used (VSSO)	PDATA[0]
HDAT[1]	Slave Address[1]	PDATA[1]
HDAT[2]	Slave Address[2]	PDATA[2]
HDAT[3]	Slave Address[3]	PDATA[3]
HDAT[4]	Slave Address[4]	PDATA[4]
HDAT[5]	Slave Address[5]	PDATA[5]
HDAT[6]	Slave Address[6]	PDATA[6]
HDAT[7]	SDAT	PDATA[7]

Serial Interface

HDAT [6:1] and HCSB0 pins define slave address in serial mode. Therefore, any slave address can be assigned for full flexibility. The Fig 52 shows an illustration of serial interface for the case of slave address (7bit) = “0x42”.

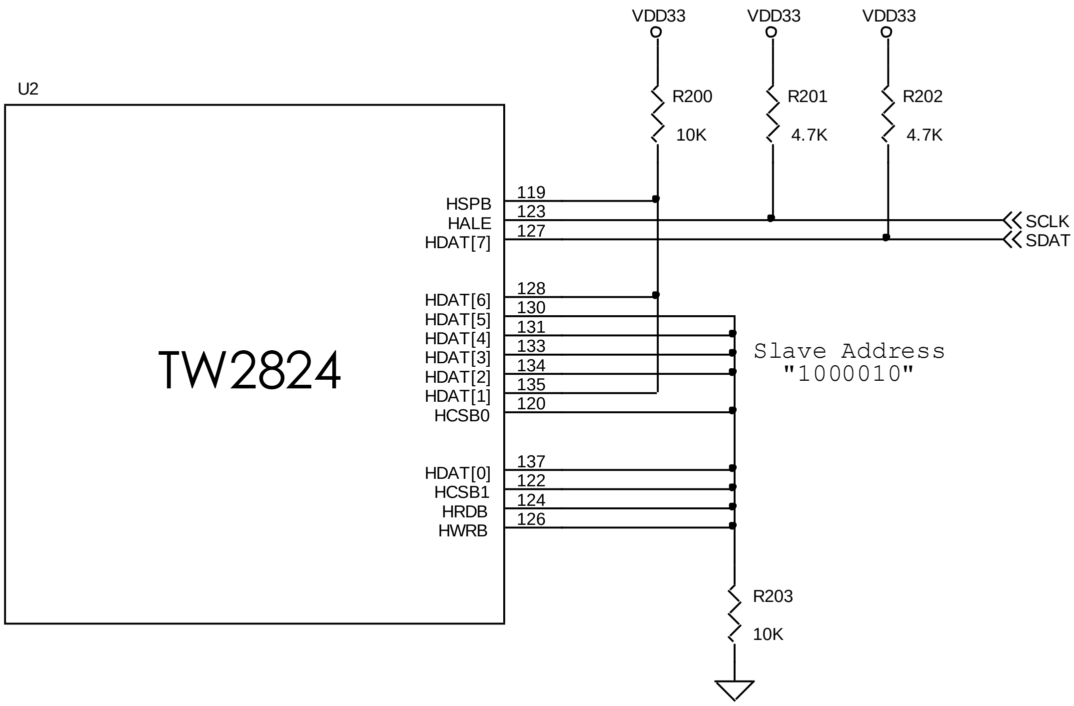


Fig 52 An illustration of serial interface for the case of slave address (7bit) = “0x42”.

The TW2824 has total 3 pages for registers (1 page can contain 256 registers) so that the page index [1:0] is used for selecting page of registers. Page 0 is assigned for video decoder, Page 1 is for video controller / OSD / encoder and Page 2 is for motion detector / Box / Mouse pointer. The detailed timing diagram is illustrated in Fig 53 and Fig 54.

The TW2824 also supports automatic index increment so that it can read or write continuous multi-bytes without restart. Therefore, the host can read or write multiple bytes in sequential order without writing additional slave address, page index and index address. The data transfer rate on the bus is up to 400 Kbits/s.

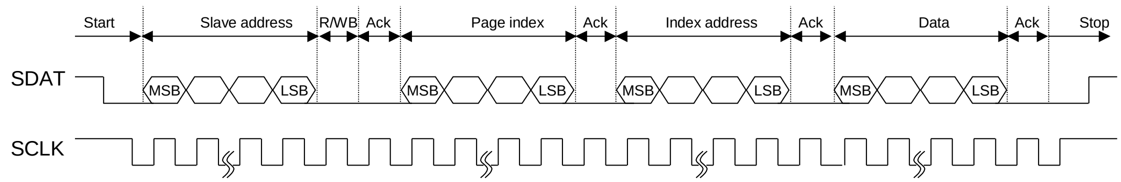


Fig 53 Write timing of serial interface

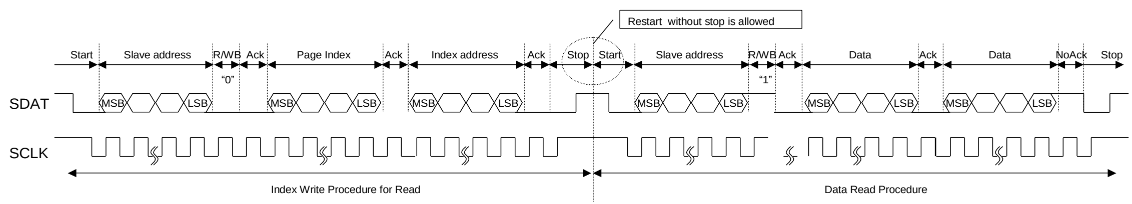


Fig 54 Read timing of serial interface

Parallel Interface

In parallel interface, page of registers can be selected by CSB0 and CSB1 pins which are working as page index [1:0] in serial interface. Page number 0 is selected by CSB1 = "0" and CSB0 = "0", page number 1 is by CSB1 = "0" and CSB0 = "1", and page number 2 is by CSB1 = "1" and CSB0 = "0". The TW2824 also supports automatic index increment for parallel interface. The writing and reading timing is shown in Fig 55 and Fig 56 respectively. The detail timing parameters are in Table 8.

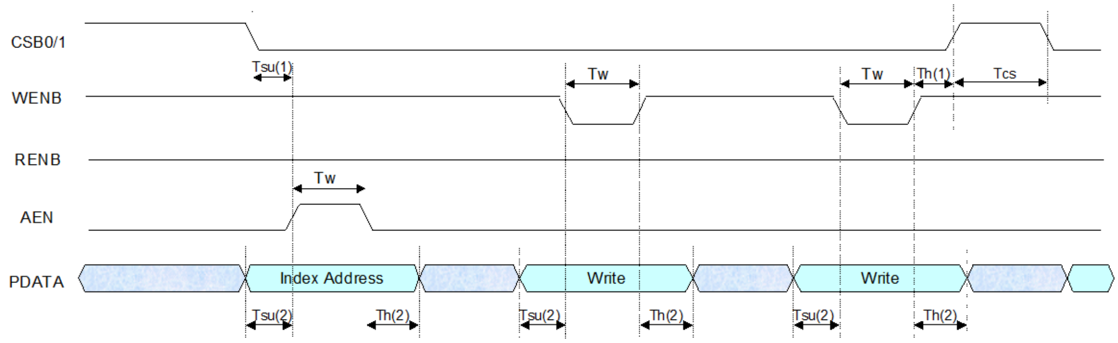


Fig 55 Write timing of parallel interface with auto index increment mode

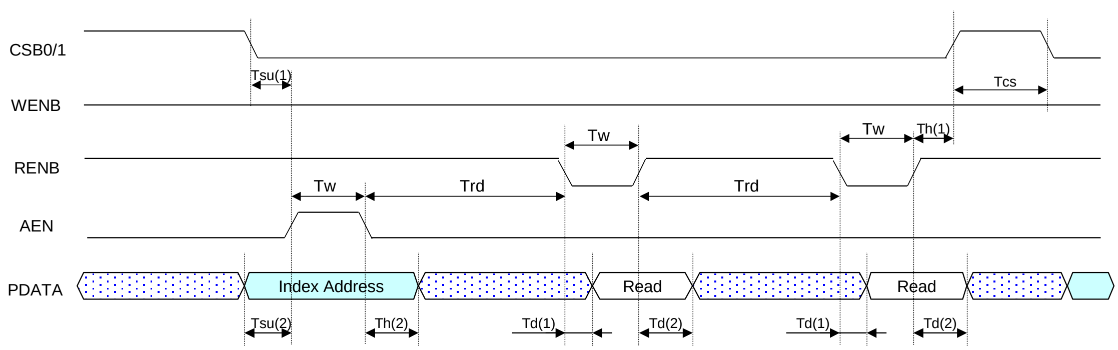


Fig 56 Read timing of parallel interface with auto index increment mode

Table 8 Timing parameters of parallel interface

Parameter	Symbol	Min	Typ	Max	Units
CSB setup until AEN active	Tsu(1)	10			ns
PDATA setup until AEN,WENB active	Tsu(2)	10			ns
AEN, WENB, RENB active pulse width	Tw	40			ns
CSB hold after WENB, RENB inactive	Th(1)	60			ns
PDATA hold after AEN,WENB inactive	Th(2)	20			ns
PDATA delay after RENB active	Td(1)			12	ns
PDATA delay after RENB inactive	Td(2)	60			ns
CSB inactive pulse width	Tcs	60			ns
RENB active delay after AEN inactive RENB active delay after RENB inactive	Trd	60			ns

Interrupt Interface

The TW2824 provides the interrupt request function via an IRQ pin. Any video loss, motion or blind detection will make the IRQ pin low until cleared via the register. Writing high to the corresponding bit of the interrupt clear register IRQCLR_NOVID, IRQCLR_MDBD (0x38) will clear the interrupt request. The host can distinguish what event makes interrupt request to IRQ pin by reading the status of IRQCLR_NOVID, IRQCLR_MDBD (0x38) registers before clearing. Then, the host has to read another status of DET_NOVID, DET_MOTION, DET_BLIND (0x39, 0x3A) registers to find out whether the event is generated by video loss or video detection, or whether it is made by motion or blind detection. To disable each interrupt, the interrupt status also has its own mask register such as IRQENA_NOVID, IRQENA_MOTION (0x37), and IRQENA_BLIND (0x3A) register. An illustration of the interrupt sequence is shown in the following Fig 57.

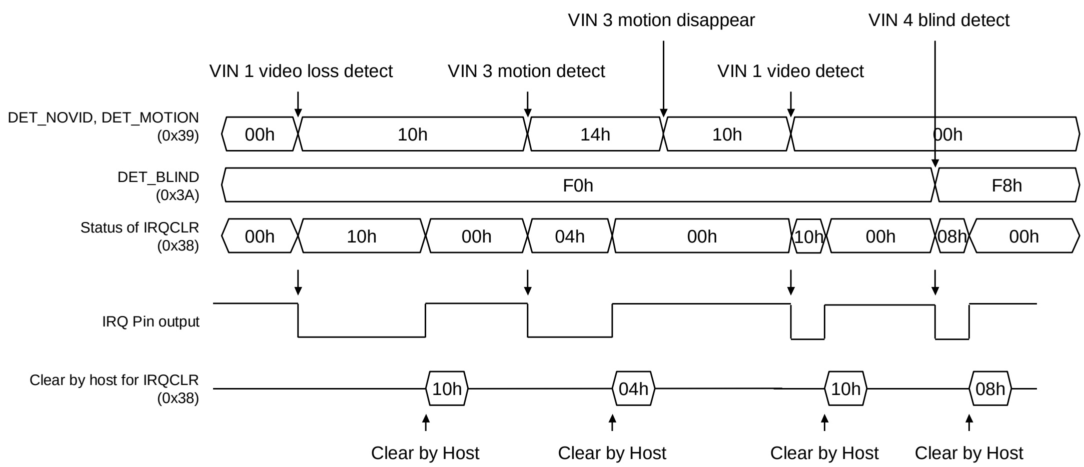


Fig 57 Timing Diagram of Interrupt Interface

The TW2824 also provides the status of video loss, motion detection or the strobe acknowledge for individual channel through MPPDEC pins with the control of the MPPSET (0x7C) register.

Control Register

REGISTER MAP

For Video Decoder

Address VIN0	VIN1	VIN2	VIN3	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x00	0x40	0x80	0xC0	DET_FORMAT *			DET_COLOR *	LOCK_COLOR *	LOCK_GAIN *	LOCK_OFST *	LOCK_PLL *
0x01	0x41	0x81	0xC1	IFMTMAN	IFORMAT			0	1	DET_NONSTD *	DET_FLD60 *
0x02	0x42	0x82	0xC2	AGC	PEDEST	1	0	GNTIME		OSTIME	
0x03	0x43	0x83	0xC3	HDELAY_X [7:0]							
0x04	0x44	0x84	0xC4	HACTIVE_X [7:0]							
0x05	0x45	0x85	0xC5	HDELAY_Y [7:0]							
0x06	0x46	0x86	0xC6	HACTIVE_Y [7:0]							
0x07	0x47	0x87	0xC7	HACTIVE_Y [9:8]		HDELAY_Y [9:8]		HACTIVE_X [9:8]		HDELAY_X [9:8]	
0x08	0x48	0x88	0xC8	0		HSWIDTH					
0x09	0x49	0x89	0xC9	VDELAY_X [7:0]							
0x0A	0x4A	0x8A	0xCA	VACTIVE_X [7:0]							
0x0B	0x4B	0x8B	0xCB	VDELAY_Y [7:0]							
0x0C	0x4C	0x8C	0xCC	VACTIVE_Y [7:0]							
0x0D	0x4D	0x8D	0xCD	HPLLMAN	HPLLTIME			VACTVE_Y [8]	VDELAY_Y [8]	VACTVE_X [8]	VDELAY_X [8]
0x0E	0x4E	0x8E	0xCE	FLDMODE		VSMODE	FLDPOL	HSPOL	VSPOL	1	0
0x0F	0x4F	0x8F	0xCF	HUE							
0x10	0x50	0x90	0xD0	SAT							
0x11	0x51	0x91	0xD1	CONT							
0x12	0x52	0x92	0xD2	BRT							
0x13	0x53	0x93	0xD3	IFCOMP		CLPF		ACCTIME		APCTIME	
0x14	0x54	0x94	0xD4	YPEAK_Y		YPEAK_X		0		CKIL	
0x15	0x55	0x95	0xD5	VSFLT_Y		VSFLT_X		HSFLT_Y		HSFLT_X	
0x16	0x56	0x96	0xD6	YBWI_X	COMBMD_X		0				
0x17	0x57	0x97	0xD7	YBWI_Y	COMBMD_Y		0				
0x18	0x58	0x98	0xD8	VSCALE_X [15:8]							
0x19	0x59	0x99	0xD9	VSCALE_X [7:0]							
0x1A	0x5A	0x9A	0xDA	VSCALE_Y [15:8]							
0x1B	0x5B	0x9B	0xDB	VSCALE_Y [7:0]							
0x1C	0x5C	0x9C	0xDC	HSCALE_X [15:8]							
0x1D	0x5D	0x9D	0xDD	HSCALE_X [7:0]							
0x1E	0x5E	0x9E	0xDE	HSCALE_Y [15:8]							
0x1F	0x5F	0x9F	0xDF	HSCALE_Y [7:0]							
0x20	0x60	0xA0	0xE0	0	VFLT_MD_X	VBW_X		PAL_DLY_X	ODD_EN_X	EVEN_EN_X	1
0x21	0x61	0xA1	0xE1	0	VFLT_MD_Y	VBW_Y		PAL_DLY_Y	ODD_EN_Y	EVEN_EN_Y	1
0x22	0x62	0xA2	0xE2	BLKEN	BLKCOL	0	LMTOUT	SW_RESET	ANA_SW	0	
0x23	0x63	0xA3	0xE3	0	0	0	1	0	0	0	1

Address				BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VIN0	VIN1	VIN2	VIN3								
0x37				IRQENA_NOVID				IRQENA_MOTION			
0x38				IRQCLR_NOVID				IRQCLR_MDBD			
0x39				DET_NOVID *				DET_MOTION *			
0x3A				IRQENA_BLIND				DET_BLIND *			
0x3B				1	0	0		0	0	IRQPOL	IRQRPT
0x3C				U_GAIN							
0x3D				V_GAIN							
0x3E				U_OFF							
0x3F				V_OFF							
0x78				0	0	0	0	ADC_PWDN			
0x79				1	0	0	0	0	0	0	0
0x7A				0	0	0	0	0	0	0	0
0x7B				TST_FLDLY4Y	TST_FLDLY4X	TST_FLDLY3Y	TST_FLDLY3X	TST_FLDLY2Y	TST_FLDLY2X	TST_FLDLY1Y	TST_FLDLY1X
0x7C				0	MPPSET1			0	MPPSET0		
0x7D				0	0	0	0	0	0	0	0
0xB8				0	0	0	0	0	0	0	0
0xF8				HAV_VALID	CKILCOMB	0	0	C_CORE		Y_H_CORE	
0xF9				0	CDEL			0	0	0	0
0xFA				0	0	1	1	1	1	0	0
0xFB				0	0	0	1	0	0	0	0
0xFC				1	1	1	1	0	0	0	0
0xFD				0	0	0	0	0	0	0	0
0xFE				0x08							

Notes 1. “*” stand for read only register

2. VIN0 ~ VIN3 stand for video input 0 ~ video input 3.

For Video Controller

Address X	Address Y	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1x00		SYS_5060	OVERLAY_X	OVERLAY_Y	LINK_LAST	LINK_EN_X	LINK_EN_Y	LINK_NUM	
1x30		MCLKDEL_Y				MCLKDEL_X			
1x01	1x31	0	FRAME_OP	FRAME_FLD	DIS_MODE	HDIV		VDIV	
1x02	1x32	0/1	SAVE_ADDR						
1x03	1x33	RECALL_FLD	0	SAVE_FLD	SAVE_HID	SAVE_REQ			
1x04	1x34	TBLINK	STRB_FLD		DUAL_PAGE	STRB_REQ			
1x05	1x35	MUX_MODE	TRIG_MODE	EXT_TRIG	INTR_REQ	INTR_CH			
1x06	1x36	QUE_PERIOD[9:8]		QUE_SIZE					
1x07	1x37	QUE_PERIOD[7:0]							
1x08	1x38	MUX_FLD		INT_CNT_RST	QUE_POS_RST	QUE_CH			
1x09	1x39	QUE_WR	0	QUE_ADDR					
1x0A	1x3A	NOVID_MODE		QUE_POS *					
1x0B	1x3B	0	0	0	0	MUX_OUT_CH *			
1x0C	1x3C	ZMENA	0	ZMBNDCOL		ZMBNDEN	ZMAREAEN	ZMAREA	
1x0D	1x3D	ZOOMH							
1x0E	1x3E	ZOOMV							
1x0F	1x3F	FRZ_FLD		BNDCOL		BGDCOL		BLKCOL	
1x2C		0	0	0	0	0	0	0	0
1x2D		0	0	0	0	0	0	0	0
1x2E		0	0	0	0	0	0	0	0
1x2F		0	0	0	0	0	0	0	0
1x5C		0	0	0	0	1	0	0	0
1x5D		0	0	0	0	0	0	0	0
1x5E		0	0	0	0	0	0	0	0
1x5F		MEM_INIT	ENCCLK_Y	ENCCLK_X	0	0	ENCCLKP_Y	ENCCLKP_X	0

Notes 1. “*” stand for read only register

2. X, Y stand for X path and Y path.

For Channel Size

Address								BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH0		CH1		CH2		CH3									
X	Y	X	Y	X	Y	X	Y								
1x10	1x40	1x17	1x47	1x1E	1x4E	1x25	1x55	CH_EN	DMCH_EN	DMCH_PATH	FUNC_MODE		DEC_PATH		
1x11	1x41	1x18	1x48	1x1F	1x4F	1x26	1x56	0	FREEZE	MIRROR	ENHANCE	POP_UP	BLANK	BOUND	BLINK
1x12	1x42	1x19	1x49	1x20	1x50	1x27	1x57	RECALL_EN	RECALL_ADDR						
1x13	1x43	1x1A	1x4A	1x21	1x51	1x28	1x58	PICHL							
1x14	1x44	1x1B	1x4B	1x22	1x52	1x29	1x59	PICHR							
1x15	1x45	1x1C	1x4C	1x23	1x53	1x2A	1x5A	PICVT							
1x16	1x46	1x1D	1x4D	1x24	1x54	1x2B	1x5B	PICVB							
1x60		1x64		1x68		1x6C		DMPICHL							
1x61		1x65		1x69		1x6D		DMPICHR							
1x62		1x66		1x6A		1x6E		DMPICVT							
1x63		1x67		1x6B		1x6F		DMPICVB							

Notes 1. X, Y stand for X path and Y path.

2. CH0 ~ CH3 stand for Channel 0 ~ Channel 3.

For Video Output

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1x70	ENC_IN_X		ENC_IN_Y		CCIR_IN_X		CCIR_IN_Y	
1x71	0	DAC_PD_X		DAC_OUT_X	0	DAC_PD_Y		DAC_OUT_Y
1x72	0	0	CCIR_OUT_X		0	0	CCIR_OUT_Y	
1x73	ENC_MODE	CCIR_LMT	ENC_VS	ENC_FLD	CCIR_FLDPOL	ENC_HSPOL	ENC_VSPOL	ENC_FLDPOL
1x74	ENC_VSOFF		ENC_VSDEL					
1x75	ENC_HSDEL							
1x76	ACTIVE_HDEL					ACTIVE_VDEL		
1x77	ENC_FSC		0		1	ENC_PHALT	ENC_ALTRST	ENC_PED
1x78	ENC_CBW_X		ENC_YBW_X		ENC_CBW_Y		ENC_YBW_Y	
1x79	ENC_BAR_X	ENC_CKILL_X	ENC_BAR_Y	ENC_CKILL_Y	ENC_VS_READ *	ENC_FLD_READ *		

Notes 1. "*" stand for read only register

For Character Overlay

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1x7A	FONT_WR_DATA[27:20]							
1x7B	FONT_WR_DATA[19:12]							
1x7C	FONT_WR_DATA[11:4]							
1x7D	FONT_WR_DATA[3:0]				0			
1x7E	0	FONT_WR_INDEX						
1x7F	FONT_REQ_X	FONT_REQ_Y	FONT_WR_PAGE	FONT_WR_FLD	FONT_WR_LINE			
1x80	0	FONT_RD_PAGE_X	FONT_RD_FLD_X		0	FONT_RD_PAGE_Y	FONT_RD_FLD_Y	
1x81	0	0	RAMCLR_Y	RAMCLR_X	CLASSEN0_Y	CLASSEN0_X	PHIGH	PLOW
1x82	CHAR_VSIZE_Y		CHAR_HSIZE_Y		CHAR_VSIZE_X		CHAR_HSIZE_X	
1x83	CHAR_VSPC_X				CHAR_HSPC_X			
1x84	CHAR_VDEL_X				CHAR_HDEL_X			
1x85	CHAR_VSPC_Y				CHAR_HSPC_Y			
1x86	CHAR_VDEL_Y				CHAR_HDEL_Y			
1x87	CHAR_MIX_C				CHAR_MIX_B			
1x88	CHAR_BLK_C				CHAR_BLK_B			
1x89	CLASS3COL1_C				CLASS3COL0_C			
1x8A	CLASS3COL3_C				CLASS3COL2_C			
1x8B	CLASS3COL1_B				CLASS3COL0_B			
1x8C	CLASS3COL3_B				CLASS3COL2_B			
1x8D	CLASS2COL_C				CLASS2COL_B			
1x8E	CLASS1COL_C				CLASS1COL_B			
1x8F	CLASS0COL_C				CLASS0COL_B			
1x90	CLUT0_Y							
1x91	CLUT0_CB							
1x92	CLUT0_CR							
1x93	CLUT1_Y							
1x94	CLUT1_CB							
1x95	CLUT1_CR							
1x96	CLUT2_Y							
1x97	CLUT2_CB							
1x98	CLUT2_CR							
1x99	CLUT3_Y							
1x9A	CLUT3_CB							
1x9B	CLUT3_CR							
1x9C	CHAR_PATH	0	0	CHAR_VLOC				
1x9D	0	0	CHAR_HLOC					
1x9E	0				CHAR_ATTR [11:8]			
	CHAR_ATTR [7:0]							

For Mouse Pointer

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2x00	CUR_ON_X	CUR_ON_Y	CUR_TYPE	CUR_SUB	CUR_BLINK	0	CUR_HP [0]	CUR_VP [0]
2x01	CUR_HP [8:1]							
2x02	CUR_VP [8:1]							

For Single Box

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2x03	BOX_TYPE	BOX_EMP	0	0	BOX_PLNEN			
2x04	BOX_BNDCOL							
2x05	BOX_PLNCOL3				BOX_PLNCOL2			
2x06	BOX_PLNCOL1				BOX_PLNCOL0			

Address								BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
B0	B1	B2	B3	B4	B5	B6	B7								
2x07	2x0C	2x11	2x16	2x1B	2x20	2x25	2x2A	BOX_PATH	BOX_OBND	BOX_IBND	BOX_PLNMIX	BOX_PLNSEL		BOX_HL[0]	BOX_VT[0]
2x08	2x0D	2x12	2x17	2x1C	2x21	2x26	2x2B	BOX_HL[8:1]							
2x09	2x0E	2x13	2x18	2x1D	2x22	2x27	2x2C	BOX_HW							
2x0A	2x0F	2x14	2x19	2x1E	2x23	2x28	2x2D	BOX_VT[8:1]							
2x0B	2x10	2x15	2x1A	2x1F	2x24	2x29	2x2E	BOX_VW							

Address								BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
B8	B9	B10	B11	B12	B13	B14	B15								
2x2F	2x34	2x39	2x3E	2x43	2x48	2x4D	2x52	BOX_PATH	BOX_OBND	BOX_IBND	BOX_PLNMIX	BOX_PLNSEL		BOX_HL[0]	BOX_VT[0]
2x30	2x35	2x3A	2x3F	2x44	2x49	2x4E	2x53	BOX_HL[8:1]							
2x31	2x36	2x3B	2x40	2x45	2x4A	2x4F	2x54	BOX_HW							
2x32	2x37	2x3C	2x41	2x46	2x4B	2x50	2x55	BOX_VT[8:1]							
2x33	2x38	2x3D	2x42	2x47	2x4C	2x51	2x56	BOX_VW							

Notes 1. B0 ~ B15 stand for single box 0 to 15.

For 2D Arrayed Box

Address				BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2DB0	2DB1	2DB2	2DB3								
2x60				0	0	2DBOX_BNDCOL		2DBOX_PLNCOL			
2x61	2x68	2x6F	2x76	2DBOX_VT[0]	2DBOX_HL[0]	2DBOX_MODE	2DBOX_PATH	2DBOX_MIX	2DBOX_PLNEN	2DBOX_CUREN	2DBOX_BNDEN
2x62	2x69	2x70	2x77	2DBOX_VT[8:1]							
2x63	2x6A	2x71	2x78	2DBOX_HL[8:1]							
2x64	2x6B	2x72	2x79	2DBOX_VW							
2x65	2x6C	2x73	2x7A	2DBOX_HW							
2x66	2x6D	2x74	2x7B	2DBOX_VNUM				2DBOX_HNUM			
2x67	2x6E	2x75	2x7C	2DBOX_CUR_HP				2DBOX_CUR_VP			

Notes 1. 2DB0 ~ 2DB3 stand for 2D arrayed box 0 to 3.

For Motion Detector

<table>
<tr><th colspan="4">Address</th><th rowspan="2">BIT7</th><th rowspan="2">BIT6</th><th rowspan="2">BIT5</th><th rowspan="2">BIT4</th><th rowspan="2">BIT3</th><th rowspan="2">BIT2</th><th rowspan="2">BIT1</th><th rowspan="2">BIT0</th></tr>
<tr><th>VIN0</th><th>VIN1</th><th>VIN2</th><th>VIN3</th></tr>
<tr><td colspan="4">2x7E</td><td colspan="4">MB_DIS</td><td colspan="4">0</td></tr>
<tr><td colspan="4">2x7F</td><td>0</td><td>0</td><td colspan="2">BD_CELSENS</td><td colspan="4">BD_LVSENS</td></tr>
<tr><td>2x80</td><td>2xA0</td><td>2xC0</td><td>2xE0</td><td>MASK_MODE</td><td>0</td><td colspan="2">MD_FLD</td><td colspan="4">MD_ALIGN</td></tr>
<tr><td>2x81</td><td>2xA1</td><td>2xC1</td><td>2xE1</td><td colspan="2">MD_CELSENS</td><td>0</td><td colspan="5">MD_LVSENS</td></tr>
<tr><td>2x82</td><td>2xA2</td><td>2xC2</td><td>2xE2</td><td>MD_REFFLD</td><td>0</td><td colspan="6">MD_SPEED</td></tr>
<tr><td>2x83</td><td>2xA3</td><td>2xC3</td><td>2xE3</td><td colspan="4">MD_TMPSENS</td><td colspan="4">MD_SPSENS</td></tr>
<tr><td>2x84</td><td>2xA4</td><td>2xC4</td><td>2xE4</td><td colspan="8" rowspan="12">MD_MASK[15:8]</td></tr>
<tr><td>2x86</td><td>2xA6</td><td>2xC6</td><td>2xE6</td></tr>
<tr><td>2x88</td><td>2xA8</td><td>2xC8</td><td>2xE8</td></tr>
<tr><td>2x8A</td><td>2xAA</td><td>2xCA</td><td>2xEA</td></tr>
<tr><td>2x8C</td><td>2xAC</td><td>2xCC</td><td>2xEC</td></tr>
<tr><td>2x8E</td><td>2xAE</td><td>2xCE</td><td>2xEE</td></tr>
<tr><td>2x90</td><td>2xB0</td><td>2xD0</td><td>2xF0</td></tr>
<tr><td>2x92</td><td>2xB2</td><td>2xD2</td><td>2xF2</td></tr>
<tr><td>2x94</td><td>2xB4</td><td>2xD4</td><td>2xF4</td></tr>
<tr><td>2x96</td><td>2xB6</td><td>2xD6</td><td>2xF6</td></tr>
<tr><td>2x98</td><td>2xB8</td><td>2xD8</td><td>2xF8</td></tr>
<tr><td>2x9A</td><td>2xBA</td><td>2xDA</td><td>2xFA</td></tr>
<tr><td>2x85</td><td>2xA5</td><td>2xC5</td><td>2xE5</td><td colspan="8" rowspan="12">MD_MASK[7:0]</td></tr>
<tr><td>2x87</td><td>2xA7</td><td>2xC7</td><td>2xE7</td></tr>
<tr><td>2x89</td><td>2xA9</td><td>2xC9</td><td>2xE9</td></tr>
<tr><td>2x8B</td><td>2xAB</td><td>2xCB</td><td>2xEB</td></tr>
<tr><td>2x8D</td><td>2xAD</td><td>2xCD</td><td>2xED</td></tr>
<tr><td>2x8F</td><td>2xAF</td><td>2xCF</td><td>2xEF</td></tr>
<tr><td>2x91</td><td>2xB1</td><td>2xD1</td><td>2xF1</td></tr>
<tr><td>2x93</td><td>2xB3</td><td>2xD3</td><td>2xF3</td></tr>
<tr><td>2x95</td><td>2xB5</td><td>2xD5</td><td>2xF5</td></tr>
<tr><td>2x97</td><td>2xB7</td><td>2xD7</td><td>2xF7</td></tr>
<tr><td>2x99</td><td>2xB9</td><td>2xD9</td><td>2xF9</td></tr>
<tr><td>2x9B</td><td>2xBB</td><td>2xDB</td><td>2xFB</td></tr>
</table>

Notes 1. VIN0 ~ VIN3 stand for video input 0 ~ video input 3.

RECOMMENDED VALUE

For Video Decoder

Address				NTSC				PAL			
VIN0	VIN1	VIN2	VIN3	1 CH	4 CH	9 CH	16 CH	1 CH	4 CH	9 CH	16 CH
0x00	0x40	0x80	0xC0	8'h00				8'h00			
0x01	0x41	0x81	0xC1	C4				84			
0x02	0x42	0x82	0xC2	E5				A5			
0x03	0x43	0x83	0xC3	20				20			
0x04	0x44	0x84	0xC4	D0				D0			
0x05	0x45	0x85	0xC5	20				20			
0x06	0x46	0x86	0xC6	D0				D0			
0x07	0x47	0x87	0xC7	88				88			
0x08	0x48	0x88	0xC8	20				20			
0x09	0x49	0x89	0xC9	06				05			
0x0A	0x4A	0x8A	0xCA	F0				20			
0x0B	0x4B	0x8B	0xCB	06				05			
0x0C	0x4C	0x8C	0xCC	F0				20			
0x0D	0x4D	0x8D	0xCD	40				4A			
0x0E	0x4E	0x8E	0xCE	D2				D2			
0x0F	0x4F	0x8F	0xCF	80				80			
0x10	0x50	0x90	0xD0	80				80			
0x11	0x51	0x91	0xD1	80				80			
0x12	0x52	0x92	0xD2	80				80			
0x13	0x53	0x93	0xD3	2F				2F			
0x14	0x54	0x94	0xD4	00	10			00	10	00	00
0x15	0x55	0x95	0xD5	00	21	22	33	00	20	22	33
0x16	0x56	0x96	0xD6	00				40	C0		
0x17	0x57	0x97	0xD7	00				40			
0x18	0x58	0x98	0xD8	FF	7F	55	3F	FF	7F	55	3F
0x19	0x59	0x99	0xD9	FF				FF			
0x1A	0x5A	0x9A	0xDA	FF				FF			
0x1B	0x5B	0x9B	0xDB	FF				FF			
0x1C	0x5C	0x9C	0xDC	FF	7F	55	3F	FF	7F	55	3F
0x1D	0x5D	0x9D	0xDD	FF				FF			
0x1E	0x5E	0x9E	0xDE	FF				FF			
0x1F	0x5F	0x9F	0xDF	FF				FF			
0x20	0x60	0xA0	0xE0	07	07	67	67	0F	07	67	67
0x21	0x61	0xA1	0xE1	07				0F			
0x22	0x62	0xA2	0xE2	00	00			00			
0x23	0x63	0xA3	0xE3	11	11			11			
0x38				00				00			
0x39				00				00			
0x3A				FF				FF			
0x3B				82				82			
0x3C				80				80			
0x3D				80				80			
0x3E				82				82			
0x3F				82				82			
0x78				00				00			
0x79				80				80			
0x7A				00				00			

Address				NTSC				PAL			
VIN0	VIN1	VIN2	VIN3	1 CH	4 CH	9 CH	16 CH	1 CH	4 CH	9 CH	16 CH
0x7B				00				00			
0x7C				00				00			
0x7D				00				00			
0xB8				00				00			
0xF8				0A				0A			
0xF9				42				42			
0xFA				3C				3C			
0xFB				10				10			
0xFC				F0				F0			
0xFD				00				00			

For Video Controller

Address		NTSC				PAL			
X	Y	1 CH	4 CH	9 CH	16 CH	1 CH	4 CH	9 CH	16 CH
1x00		8'h00				8'h80			
1x30		AA				AA			
1x01	1x31	00				00			
1x02	1x32	00/80				00/80			
1x03	1x33	00				00			
1x04	1x34	00				00			
1x05	1x35	00				00			
1x06	1x36	00				00			
1x07	1x37	00				00			
1x08	1x38	00				00			
1x09	1x39	00				00			
1x0A	1x3A	00				00			
1x0B	1x3B	00				00			
1x0C	1x3C	20				20			
1x0D	1x3D	00				00			
1x0E	1x3E	00				00			
1x0F	1x3F	B7				B7			
1x10	1x40	80				80			
1x11	1x41	02				02			
1x12	1x42	00				00			
1x13	1x43	00	00	00	00	00	00	00	00
1x14	1x44	B4	5A	3C	2D	B4	5A	3C	2D
1x15	1x45	00	00	00	00	00	00	00	00
1x16	1x46	78	3C	28	1E	90	48	30	24
1x17	1x47	90				90			
1x18	1x48	02				02			
1x19	1x49	00				00			
1x1A	1x4A	00	5A	3C	2D	00	5A	3C	2D
1x1B	1x4B	B4	B4	78	5A	B4	B4	78	5A
1x1C	1x4C	00	00	00	00	00	00	00	00
1x1D	1x4D	78	3C	28	1E	90	48	30	24
1x1E	1x4E	A0				A0			
1x1F	1x4F	02				02			
1x10	1x50	00				00			
1x11	1x51	00	00	78	5A	00	00	78	5A

Address		NTSC				PAL			
X	Y	1 CH	4 CH	9 CH	16 CH	1 CH	4 CH	9 CH	16 CH
1x12	1x52	B4	5A	B4	87	B4	5A	B4	87
1x13	1x53	00	3C	00	00	00	48	00	00
1x14	1x54	78	78	28	1E	90	90	30	24
1x15	1x55	A0				A0			
1x16	1x56	02				02			
1x17	1x57	00				00			
1x28	1x58	00	5A	00	87	00	5A	00	87
1x29	1x59	B4	B4	3C	B4	B4	B4	3C	B4
1x2A	1x5A	00	3C	28	00	00	48	30	00
1x2B	1x5B	78	78	50	1E	90	90	60	24
1x2C		00				00			
1x2D		00				00			
1x2E		00				00			
1x2F		00				00			
1x5C		08				08			
1x5D		00				00			
1x5E		00				00			
1x5F		06				06			
1x70		77				77			
1x71		00				00			
1x72		01				01			
1x73		80				80			
1x74		10				16			
1x75		3C				41			
1x76		7C				7C			
1x77		09				4C			
1x78		AA				AA			

Notes 1. Blanks have the same value of 1 CH.

2. All values are Hex format.

For Motion Detector

Address				NTSC	PAL
VIN0	VIN1	VIN2	VIN3		
2x7E				8'h00	8'h00
2x7F				17	17
2x80	2xA0	2xC0	2xE0	07	07
2x81	2xA1	2xC1	2xE1	4A	4A
2x82	2xA2	2xC2	2xE2	07	07
2x83	2xA3	2xC3	2xE3	24	24

REGISTER DESCRIPTION

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x00	DET_FORMAT *			DET_ COLOR *	LOCK_ COLOR *	LOCK_ GAIN *	LOCK_ OFST *	LOCK_ PLL *
1	0x40								
2	0x80								
3	0xC0								

Notes “*” stand for read only register

DET_FORMAT Status of video standard detection for analog input.
- 0 PAL-B/D
- 1 PAL-M
- 2 PAL-N
- 3 PAL-60
- 4 NTSC-M
- 5 NTSC-4.43
- 6 NTSC-N

DET_COLOR Status of color detection for analog input.
- 0 Color is not detected
- 1 Color is detected

LOCK_COLOR Status of locking for color demodulation loop.
- 0 Color demodulation loop is not locked
- 1 Color demodulation loop is locked

LOCK_GAIN Status of locking for AGC loop.
- 0 AGC loop is not locked
- 1 AGC loop is locked

LOCK_OFST Status of locking for clamping loop.
- 0 Claming loop is not locked
- 1 Claming loop is locked

LOCK_PLL Status of locking for horizontal PLL.
- 0 Horizontal PLL is not locked
- 1 Horizontal PLL is locked

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x01	IFMTMAN	IFORMAT			0	1	DET_ NONSTD *	DET_ FLD60 *
1	0x41								
2	0x81								
3	0xC1								

Notes “*” stand for read only register

IFMTMAN — Setting video standard manually with IFORMAT.

0 Detecting video standard of video input automatically (default)

1 Video standard is selected with IFORMAT

IFORMAT — Force to operate in a particular video standard when IFMTMAN = “1” or to free-run in a particular video standard on no-video status when IFMTMAN = “0”.

0 PAL-B/D (default)

1 PAL-M

2 PAL-N

3 PAL-60

4 NTSC-M

5 NTSC-4.43

6 NTSC-N

DET_NONSTD — Status of non-standard video detection.

0 The incoming video source is standard

1 The incoming video source is non-standard

DET_FLD60 — Status of field frequency of incoming video.

0 50Hz field frequency

1 60Hz field frequency

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x02	AGC	PEDEST	1	0	GNTIME		OSTIME	
1	0x42								
2	0x82								
3	0xC2								

AGC — Control the AGC function for active video.
- 0 Disable the AGC (default)
- 1 Enable the AGC

PEDEST — Control pedestal level by 7.5 IRE.
- 0 No pedestal level (0 IRE is ITU-R BT.601 code 16) (default)
- 1 7.5 IRE setup level (7.5 IRE is ITU-R BT.601 code 16)

GNTIME — Control the time constant of gain tracking loop.
- 0 Slower
- 1 Slow (default)
- 2 Fast
- 3 Faster

OSTIME — Control the time constant of offset tracking loop.
- 0 Slower
- 1 Slow (default)
- 2 Fast
- 3 Faster

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	0x07							HDELAY[9:8]	
	1	0x47								
	2	0x87								
	3	0xC7								
	0	0x03	HDELAY[7:0]							
	1	0x43								
	2	0x83								
	3	0xC3								
Y	0	0x07			HDELAY[9:8]					
	1	0x47								
	2	0x87								
	3	0xC7								
	0	0x05	HDELAY[7:0]							
	1	0x45								
	2	0x85								
	3	0xC5								

HDELAY This 10 bit register defines the starting location of horizontal active pixel with 1 pixel unit. The default value is decimal 32.

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	0x07					HACITIVE[9:8]			
	1	0x47								
	2	0x87								
	3	0xC7								
	0	0x04	HACTIVE[7:0]							
	1	0x44								
	2	0x84								
	3	0xC4								
Y	0	0x07	HACTIVE[9:8]							
	1	0x47								
	2	0x87								
	3	0xC7								
	0	0x06	HACTIVE[7:0]							
	1	0x46								
	2	0x86								
	3	0xC6								

HACTIVE This 10 bit register defines the number of horizontal active pixel with 1 pixel unit. The default value is decimal 720.

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x08	0	0	HSWIDTH					
1	0x48								
2	0x88								
3	0xC8								

HSWIDTH This 6 bit register defines the width of horizontal sync output with 1 pixel unit. The default value is decimal 32.

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	0x0D								VDELAY[8]
	1	0x4D								
	2	0x8D								
	3	0xCD								
	0	0x09	VDELAY[7:0]							
	1	0x49								
	2	0x89								
	3	0xC9								
Y	0	0x0D						VDELAY[8]		
	1	0x4D								
	2	0x8D								
	3	0xCD								
	0	0x0B	VDELAY[7:0]							
	1	0x4B								
	2	0x8B								
	3	0xCB								

VDELAY This 9 bit register defines the starting location of vertical active with 1 line unit. The default value is decimal 6.

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	0x0D							VACTIVE[8]	
	1	0x4D								
	2	0x8D								
	3	0xCD								
	0	0x0A	VACTIVE[7:0]							
	1	0x4A								
	2	0x8A								
	3	0xCA								
Y	0	0x0D					VACTIVE[8]			
	1	0x4D								
	2	0x8D								
	3	0xCD								
	0	0x0C	VACTIVE[7:0]							
	1	0x4C								
	2	0x8C								
	3	0xCC								

VACTIVE — This 9 bit register defines the number of vertical active lines with 1 line unit. The default value is decimal 240.

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x0D	HPLLMAN	HPLLTIME						
1	0x4D								
2	0x8D								
3	0xCD								

HPLLMAN — Setting horizontal PLL time constant with HPLLTIME.

- 0 Automatic horizontal tracking mode (default)
- 1 Horizontal PLL time constant is fixed with HPLLTIME

HPLLTIME — Control the time constant of horizontal PLL when HPLLMAN = “1”.

- 0 Slow
- : :
- 4 Typical (default)
- : :
- 7 Fast

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x0E	FLDMODE		VSMODE	FLDPOL	HSPOL	VSPOL	1	0
1	0x4E								
2	0x8E								
3	0xCE								

FLDMODE — Select the field flag generation mode.

- 0 Field flag is detected from incoming video (default)
- 1 Field flag is generated from small accumulator of detected field
- 2 Field flag is generated from medium accumulator of detected field
- 3 Field flag is generated from large accumulator of detected field

VSMODE — Control the VS and field flag timing.

- 0 VS and field flag is aligned with vertical sync (default)
- 1 VS and field flag is aligned with HS

FLDPOL — Select the FLD polarity.

- 0 Odd field is high (default)
- 1 Even field is high

HSPOL — Select the HS polarity.

- 0 Low for sync duration (default)
- 1 High for sync duration

VSPOL — Select the VS polarity.

- 0 Low for sync duration (default)
- 1 High for sync duration

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x0F	HUE							
1	0x4F								
2	0x8F								
3	0xCF								

HUE Control the hue information. The resolution is 1.4° / step.

0 -180°
: :
128 0° (default)
: :
255 180°

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x10	SAT							
1	0x50								
2	0x90								
3	0xD0								

SAT Control the color saturation. The resolution is 0.8% / step.

0 0%
: :
128 100% (default)
: :
255 200%

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x11	CONT							
1	0x51								
2	0x91								
3	0xD1								

CONT Control the contrast. The resolution is 0.8% / step.

0	0%
:	:
128	100% (default)
:	:
255	200%

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x12	BRT							
1	0x52								
2	0x92								
3	0xD2								

BRT Control the brightness. The resolution is 0.2IRE / step.

0	-25IRE
:	:
128	0IRE (default)
:	:
255	25IRE

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x13	IFCOMP		CLPF		ACCTIME		APCTIME	
1	0x53								
2	0x93								
3	0xD3								

IFCOMP — Select the IF-compensation filter mode.

- 0 No compensation (default)
- 1 +1 dB/ MHz
- 2 +2 dB/ MHz
- 3 +3 dB/ MHz

CLPF — Select the Color LPF mode.

- 0 550KHz bandwidth
- 1 750KHz bandwidth (default)
- 2 950KHz bandwidth
- 3 1.1MHz bandwidth

ACCTIME — Control the time constant of auto color control loop.

- 0 Slower
- 1 Slow
- 2 Fast
- 3 Faster (default)

APCTIME — Control the time constant of auto phase control loop.

- 0 Slower
- 1 Slow
- 2 Fast
- 3 Faster (default)

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x14	YPEAK_Y		YPEAK_X		0	0	CKIL	
1	0x54								
2	0x94								
3	0xD4								

YPEAK — Control the luminance peaking for X and Y path.

0 No peaking (default)
1 31.25%
2 62.5%
3 93.75%

CKIL — Control the color killing mode.

0 Auto detection mode (default)
1 Auto detection mode
2 Color is always alive
3 Color is always killed

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x15	VSFLT_Y		VSFLT_X		HSFLT_Y		HSFLT_X	
1	0x55								
2	0x95								
3	0xD5								

VSFLT — Select the vertical anti-aliasing filter mode for X and Y path.

0 Full bandwidth (default)
1 Full bandwidth
2 0.25 Line-rate bandwidth
3 0.18 Line-rate bandwidth

HSFLT — Select the horizontal anti-aliasing filter mode for X and Y path.

0 Full bandwidth (default)
1 2 MHz bandwidth
2 1.5 MHz bandwidth
3 1 MHz bandwidth

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	0x16	YBWI	COMBMD		0	0	0	0	0
	1	0x56								
	2	0x96								
	3	0xD6								
Y	0	0x17								
	1	0x57								
	2	0x97								
	3	0xD7								

YBWI Select the luminance trap filter mode.

0 Narrow bandwidth trap filter mode (default)

1 Wide bandwidth trap filter mode

COMBMD Select the adaptive comb filter mode.

0,1 Adaptive comb filter mode (default)

2 Force trap filter mode

3 Not supported

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	0x18	VSCALE[15:8]							
	1	0x58								
	2	0x98								
	3	0xD8								
	0	0x19	VSCALE[7:0]							
	1	0x59								
	2	0x99								
	3	0xD9								
Y	0	0x1A	VSCALE[15:8]							
	1	0x5A								
	2	0x9A								
	3	0xDA								
	0	0x1B	VSCALE[7:0]							
	1	0x5B								
	2	0x9B								
	3	0xDB								

VSCALE The 16 bit register defines a vertical scaling ratio. The actual vertical scaling ratio is VSCALE/(2^16 – 1). The default value is 0xFFFF.

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	0x1C	HSCALE[15:8]							
	1	0x5C								
	2	0x9C								
	3	0xDC								
	0	0x1D	HSCALE[7:0]							
	1	0x5D								
	2	0x9D								
	3	0xDD								
Y	0	0x1E	HSCALE[15:8]							
	1	0x5E								
	2	0x9E								
	3	0xDE								
	0	0x1F	HSCALE[7:0]							
	1	0x5F								
	2	0x9F								
	3	0xDF								

HSCALE — The 16 bit register defines a horizontal scaling ratio. The actual horizontal scaling ratio is HSCALE/(2^16 – 1). The default value is 0xFFFF.

Path	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	0x20	0	VFLT_MD	VBW		PAL_DLY	ODD_EN	EVEN_EN	1
	1	0x60								
	2	0xA0								
	3	0xE0								
Y	0	0x21								
	1	0x61								
	2	0xA1								
	3	0xE1								

VFLT_MD — Select the additional vertical scaling filter mode.
- 0 Vertical poly-phase mode (default)
- 1 Additional vertical bandwidth reduction mode with VBW bits

VBW — Control the vertical bandwidth when VSFLT_MD = “1”.
- 0 Not Supported (default)
- 1 Not Supported
- 2 Wide
- 3 Narrow

PAL_DLY — Select the PAL delay line mode.
- 0 Vertical scaling mode is selected in chrominance path (default)
- 1 PAL delay line mode is selected in chrominance path

ODD_EN — Control valid signal in ODD field.
- 0 Valid signal is always disabled in ODD field
- 1 Normal operation (default)

EVEN_EN — Control valid signal in EVEN field.
- 0 Valid signal is always disabled in EVEN field
- 1 Normal operation (default)

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x22	BLKEN	BLKCOL	0	LMTOUT	SW_ RESET	ANA_SW	0	
1	0x62								
2	0xA2								
3	0xE2								

BLKEN Control the blank output.

0 Blank color is disabled (default)

1 Blank color is enabled

BLKCOL Select the blank color when BLKEN = “1”.

0 Blue color (default)

1 Black color

LMTOUT Control the range of output level.

0 Output ranges are limited to 2 ~ 254 (default)

1 Output ranges are limited to 16 ~ 239

SW_RESET Reset the system by software except control registers.

This bit is cleared by itself in a few clocks after enabled

0 Normal operation (default)

1 Enable soft reset

ANA_SW Select analog video input using switch.

0 VIN_A channel is selected (default)

1 VIN_B channel is selected

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x23	0	0	0	1	0	0	0	1
1	0x63								
2	0xA3								
3	0xE3								

This is reserved register.

For normal operation, the above value should be set in this register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x37	IRQENA_NOVID				IRQENA_MOTION			

IRQENA_NOVID Interrupt enable for corresponding video-loss detection.
IRQENA_NOVID[3:0] stand for VIN3 to VIN0.
0 Interrupt is disabled (default)
1 Interrupt is enabled

IRQENA_MOTION Interrupt enable for corresponding motion detection.
IRQENA_MOTION [3:0] stand for VIN3 to VIN0.
0 Interrupt is disabled (default)
1 Interrupt is enabled

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x38	IRQCLR_NOVID				IRQCLR_MDBD			

IRQCLR_NOVID Setting “1” to clear interrupt request for corresponding video-loss detection. This bit is cleared by itself in a few clocks after setting “1”.
IRQCLR_NOVID [3:0] stand for VIN3 to VIN0.

IRQCLR_MDBD Setting “1” to clear interrupt request for corresponding motion and blind detection. This bit is cleared by itself in a few clocks after setting “1”.
IRQENA_MD_BD [3:0] stand for VIN3 to VIN0.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x39	DET_NOVID *				DET_MOTION *			

Notes "*" stand for read only register

DET_NOVID Status of video loss detection.
DET_NOVID[3:0] stand for VIN3 to VIN0.
0 Video is alive
1 Video loss is detected

DET_MOTION Status of motion detection.
DET_MOTION[3:0] stand for VIN3 to VIN0.
0 No motion
1 Motion is detected

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3A	IRQENA_BLIND				DET_BLIND *			

Notes "*" stand for read only register

IRQENA_BLIND Interrupt enable for corresponding blind detection.
IRQENA_BLIND[3:0] stand for VIN3 to VIN0.
0 Interrupt is disabled (default)
1 Interrupt is enabled

DET_BLIND Status of blind detection.
DET_BLIND[3:0] stand for VIN3 to VIN0.
0 No blinded video
1 Blind video is detected

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3B	1	0	0	0	0	0	IRQPOL	IRQRPT

IRQPOL Select the IRQ polarity.
0 Active high (default)
1 Active low

IRQRPT Select the IRQ mode.
IRQ pin maintains the state "1" until the interrupt request is cleared (default)
Interrupt request is repeated with 5msec period via IRQ pin when interrupt is not cleared in long time.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3C	U_GAIN							

U_GAIN Adjust gain for U (Cb) component of VIN0 ~ VIN3.
The resolution is 0.8% / step.
0 0%
: :
128 100% (default)
: :
255 200%

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3D	V_GAIN							

V_GAIN Adjust gain for V (Cr) component of VIN0 ~ VIN3.
The resolution is 0.8% / step.
0 0%
: :
128 100% (default)
: :
255 200%

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3E	U_OFF							

U_OFF U (Cb) offset adjustment register of VIN0 ~ VIN3.

The resolution is 0.4% / step.

0	-50%
:	:
128	0% (default)
:	:
255	50%

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3F	V_OFF							

V_OFF V (Cr) offset adjustment register of VIN0 ~ VIN3.

The resolution is 0.4% / step.

0	-50%
:	:
128	0% (default)
:	:
255	50%

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x78	0	0	0	0	ADC_PWDN			

ADC_PWDN Power down the ADC of video input.
ADC_PWDN [3:0] stand for VIN3 to VIN0.
0 Normal (default)
1 Power down

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x79	1	0	0	0	0	0	0	0
0x7A	0	0	0	0	0	0	0	0

This is reserved register.
For normal operation, the above value should be set in this register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7B	FLDOS_ 4Y	FLDOS_ 4X	FLDOS_ 3Y	FLDOS_ 3X	FLDOS_ 2Y	FLDOS_ 2X	FLDOS_ 1Y	FLDOS_ 1X

FLDOS Remove the field offset between ODD and EVEN.
The numbers stand for VIN3 to VIN0 and X and Y stand for X and Y path.
0 Normal operation (default)
1 Remove the field offset between ODD and EVEN field

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7C	0	MPPSET1			0	MPPSET0		

MPPSET1 Output Selection for MPPDEC0[1] ~ MPPDEC3[1] pins.

MPPSET0 Output Selection for MPPDEC0[0] ~ MPPDEC3[0] pins.

For the following 0~5 value, MPPDEC0 ~ MPPDEC3 data comes from VIN0 ~ VIN3 and comes from CH0 ~ CH3 for 6~7 value.

0 Vertical sync (default)
1 Field flag
2 Horizontal sync
3 Vertical valid line
4 Video loss
5 Motion detection
6 Strobe acknowledge of X path
7 Strobe acknowledge of Y path

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7D	0	0	0	0	0	0	0	0

This is reserved register.
For normal operation, the above value should be set in this register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xB8	0	0	0	0	0	0	0	0

This is reserved register.
For normal operation, the above value should be set in this register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xF8	HAV_VALID	CKILCOMB	0	0	C_CORE		Y_H_CORE	

HAV_VALID
Select VALID output mode.
0 Valid data indicator only for active data (default)
1 Valid data indicator for both active data and ITU-R 656 timing codes

CKILCOMB
Control the comb filter on/off whether color is or not.
0 Comb filter is always enabled (default)
1 Comb filter is disabled when color is killed

C_CORE
Coring to reduce the noise in the chrominance.
0 No coring
1 Coring value is within 128 +/- 1 range
2 Coring value is within 128 +/- 2 range (default)
3 Coring value is within 128 +/- 4 range

Y_H_CORE
Coring to reduce the high frequency noise in the luminance.
0 No coring
1 Coring value is within +/- 1 range
2 Coring value is within +/- 2 range (default)
3 Coring value is within +/- 4 range

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xF9	0	CDEL			0	0	0	0

CDEL Adjust the group delay of chrominance relative to luminance.

0 -2.0 pixel
1 -1.5 pixel
2 -1.0 pixel
3 -0.5 pixel
4 0.0 pixel (default)
5 0.5 pixel
6 1.0 pixel
7 1.5 pixel

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFA	0	0	1	1	1	1	0	0
0xFB	0	0	0	1	0	0	0	0
0xFC	1	1	1	1	0	0	0	0
0xFD	0	0	0	0	0	0	0	0

This is reserved register.
For normal operation, the above value should be set in this register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFE	DEV_ID *					REV_ID *		

Notes “*” stand for read only register

DEV_ID The TW2824 product ID code is 00001.

REV_ID The revision number

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x00	SYS_5060	OVERLAY_X	OVERLAY_Y	LINK_LAST	LINK_EN_X	LINK_EN_Y	LINK_NUM	

SYS_5060 Standard format selection for video controller.
- 0 60Hz, 525 line format (default)
- 1 50Hz, 625 line format

OVERLAY_X Control overlay Y path on X path.
- 0 Disable overlay Y path on X path (default)
- 1 Enable overlay Y path on X path

OVERLAY_Y Control overlay X path on Y path.
- 0 Disable overlay X path on Y path (default)
- 1 Enable overlay X path on Y path

LINK_LAST Define last chip of slave in chip-to-chip cascade operation.
- 0 Master or not last of slave chip (default)
- 1 Last of slave chip

LINK_EN Control chip-to-chip cascade connection for X and Y path.
- 0 Disable cascade operation (default)
- 1 Enable cascade operation

LINK_NUM Define number of chip-to-chip cascade stage.
- 0 Master chip (default)
- 1 1st slave chip
- 2 2nd slave chip
- 3 3rd slave chip

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x30	MCLKDEL_Y				MCLKDEL_X			

MCLKDEL Control delay of clock to SDRAM for X and Y path.
The delay can be controlled by 1ns.
The default value is 0.

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x01	0	FRAME_OP	FRAME_FLD	DIS_MODE	HDIV		VDIV	
Y	1x31								

FRAME_OP — Select frame operation mode.

0 Normal operation mode (Default)

1 Frame operation mode

DIS_MODE — Select display mode depending on FRAME_OP.

When FRAME_OP = 0

0 Monitor Display Mode (Default)

1 DVR Display Mode

When FRAME_OP = 1

0 Frame Display Mode

1 DVR Frame Display Mode

FRAME_FLD — Select display field when FRAME_OP = “1”.

0 Odd field display (default)

1 Even field display

HDIV — Horizontal picture size when DIS_MODE = “1”.

0 Full scale size (720 pixels/H) (default)

1 1/2 scale size (360 pixels/H)

2 1/3 scale size (240 pixels/H)

3 1/4 scale size (180 pixels/H)

VDIV — Vertical picture size,

In DVR display mode (FRAME_FLD = “0”, DIS_MODE = “1”)

0 Full scale size (240 lines/V for 60Hz, 288 lines/V for 50Hz) (default)

1 1/2 scale size (120 lines/V for 60Hz, 144 lines/V for 50Hz)

2 1/3 scale size (80 lines/V for 60Hz, 96 lines/V for 50Hz)

3 1/4 scale size (60 lines/V for 60Hz, 72 lines/V for 50Hz)

In DVR frame display mode (FRAME_FLD = “1”, DIS_MODE = “1”)

0 Not allowed (default)

1 Full scale size (240 lines/V for 60Hz, 288 lines/V for 50Hz)

2 2/3 scale size (160 lines/V for 60Hz, 192 lines/V for 50Hz)

3 1/2 scale size (120 lines/V for 60Hz, 144 lines/V for 50Hz)

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x02	0	SAVE_ADDR						
Y	1x32	1							

SAVE_ADDR Define address of SDRAM for saving picture.
Unit Address has 4Mbit Memory Space.

0-3 Reserved for normal operation. Do not use this address.
4-15 Possible address for 64M SDRAM
4-31 Possible address for 128M SDRAM
4-63 Possible address for 256M SDRAM
4-127 Possible address for 512M SDRAM

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x03	RECALL_FLD	0	SAVE_FLD	SAVE_HID	SAVE_REQ			
Y	1x33								

RECALL_FLD Select field or frame data during recall picture.

0 Recall frame data from SDRAM (default)
1 Recall field data from SDRAM

SAVE_FLD Select field or frame data to save.

0 Save frame data to SDRAM (default)
1 Save field data to SDRAM

SAVE_HID Control priority to save picture.

0 Save picture as shown in screen (default)
1 Save picture even though hidden by other picture

SAVE_REQ Request to save for each channel.
SAVE_REQ[3:0] stand for channel 3 to 0

0 None operation (default)
1 Request to start of save picture

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x04	TBLINK	STRB_FLD		DUAL_PAGE	STRB_REQ			
Y	1x34								

TBLINK Control blink period of channel boundary.

0 Blink for every 30 fields (default)

1 Blink for every 60 fields

STRB_FLD Control capturing field for strobe operation.

0 Capture odd field only (default)

1 Capture even field only

2 Capture first field of any field

3 Capture frame

DUAL_PAGE Set dual page mode.

0 Normal strobe operation for each channel (default)

1 Enable dual page operation

STRB_REQ Request strobe operation.

STRB_REQ[3:0] stand for channel 3 to 0

0 None operation (default)

1 Request to start strobe operation

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x05	MUX_MODE	TRIG_MODE	EXT_TRIG	INTR_REQ	INTR_CH			
Y	1x35								

MUX_MODE
Define MUX picture mode.
This bit is fixed to "1" for the TW2824Q and TW2824QS.
0 Switch channel with still picture (default)
1 Switch channel with live picture

TRIG_MODE
Define MUX trigger mode.
0 MUX with external trigger from host (default)
1 MUX with internal trigger

EXT_TRIG
Make trigger when TRIG_MODE = "0".
0 None operation (default)
1 Request to start MUX with external trigger

INTR_REQ
Request interrupt MUX
0 None operation (default)
1 Request to start MUX with interrupt

INTR_CH
Channel number for interrupt MUX.
INTR_CH[3:2] stand for order of linked chips for interrupt MUX.
0 Master chip (default)
1 1st slave chip
2 2nd slave chip
3 3rd slave chip

INTR_CH[1:0] stand for channel number for interrupt MUX.
0 Channel 0 (default)
1 Channel 1
2 Channel 2
3 Channel 3

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x06			QUE_SIZE					
Y	1x36								

QUE_SIZE Define actual used queue size.

0 Queue size = 1 (default)

: :

63 Queue size = 64

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x06	QUE_PERIOD [9:8]							
Y	1x36								
X	1x07	QUE_PERIOD [7:0]							
Y	1x37								

QUE_PERIOD Trigger period for internal trigger mode.

0 Trigger period = 1 field (default)

: :

1023 Trigger period = 1024 fields

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x08	MUX_FLD		QUE_CNT_RST	QUE_POS_RST	QUE_CH			
Y	1x38								

MUX_FLD — Control capturing field for MUX operation.
- 0 Capture odd field only (default)
- 1 Capture even field only
- 2 Capture frame
- 3 Capture frame

INT_CNT_RST — Reset internal field counter to count queue period.
- 0 None operation (default)
- 1 Reset field counter

QUE_POS_RST — Reset queue address.
- 0 None operation (default)
- 1 Reset queue address and restart address

QUE_CH — Channel number to be written in internal queue of QUE_ADDR.

QUE_CH[3:2] stand for order of linked chips for MUX.
- 0 Master chip (default)
- 1 1st slave chip
- 2 2nd slave chip
- 3 3rd slave chip

QUE_CH[1:0] stand for channel number for MUX.
- 0 Channel 0 (default)
- 1 Channel 1
- 2 Channel 2
- 3 Channel 3

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x09	QUE_WR	0	QUE_ADDR					
Y	1x39								

QUE_WR — Control to write internal queue data.

0 None operation (default)

1 Request to start writing QUE_CH in internal queue of QUE_ADDR

QUE_ADDR — Define queue address.

0 1st queue address (default)

: :

63 64th queue address

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x0A	NOVID_MODE		QUE_POS *					
Y	1x3A								

Notes “*” stand for read only register

NOVID_MODE — Channel operation when video loss is detected.

0 Bypass (default)

1 Capture last image

2 Blanked with blank color

3 Capture last image and blink channel boundary

QUE_POS — Information of queue address to be switched next.

0 1st queue address (default)

: :

63 64th queue address

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x0B	0	0	0	0	MUX_OUT_CH *			
Y	1x3B								

Notes “*” stand for read only register

MUX_OUT_CH Information of number for current switched channel.

MUX_OUT_CH[3:2] stand for order of cascaded chips.

0 Master chip
1 1st slave chip
2 2nd slave chip
3 3rd slave chip

MUX_OUT_CH[1:0] stands for number of current channel.

0 Channel 0
1 Channel 1
2 Channel 2
3 Channel 3

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x0C	ZMENA	0	ZMBNDCOL		ZMBNDEN	ZMAREAEN	ZMAREA	
Y	1x3C								

ZMENA — Enable zoom function.

- 0 Disable zoom function (default)
- 1 Enable zoom function

ZMBNDCOL — Define boundary color for zoom area

- 0 0% Black
- 1 25% Gray
- 2 75% Gray (default)
- 3 100% White

ZMBNDEN — Enable boundary of zoom area.

- 0 Disable boundary of zoom area (default)
- 1 Enable boundary of zoom area

ZMAREAEN — Enable mark of zoom area

- 0 Disable mark of zoom area (default)
- 1 Enable mark of zoom area

ZMAREA — Control effect of zoom area.

- 0 10 IRE Bright up for inside of zoom area (default)
- 1 20 IRE Bright up for inside of zoom area
- 2 10 IRE Bright up for outside of zoom area
- 3 20 IRE Bright up for outside of zoom area

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x0D	ZOOMH							
Y	1x3D								

ZOOMH Define horizontal left point of zoom area. 4 pixels/step.

0 Left end value (default)

: :

180 Right end value

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x0E	ZOOMV							
Y	1x3E								

ZOOMV Define vertical top point of zoom area. 2 lines/step.

0 Top end value (default)

: :

120 Bottom end value for 60Hz, 525 lines system

: :

144 Bottom end value for 50Hz, 625 lines system

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x0F	FRZ_FLD		BNDCOL		BGDCOL		BLKCOL	
Y	1x3F								

FRZ_FLD Select image for freeze function or last image capture on video loss.

0 Last image
1 Last image of 1 field before
2 Last image of 2 fields before (default)
3 Last image of 3 fields before

BNDCOL Define boundary color of channel.

0 0% Black
1 25% Gray
2 75% Gray
3 100% White (default)

Channel boundary color is changed according to this value when boundary is blinking.

0 100% White
1 100% White
2 0% Black
3 0% Black (default)

BGDCOL Define background color.

0 0% Black
1 40% Gray (default)
2 75% Gray
3 Blue (100% Amplitude 100% Saturation)

BLKCOL Define color for blanked channel.

0 0% Black
1 40% Gray
2 75% Gray
3 Blue (100% Amplitude 100% Saturation) (default)

<table>
<tr><th>Path</th><th>CH</th><th>Index</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th></tr>
<tr><td rowspan="4">X</td><td>0</td><td>1x10</td><td rowspan="8">CH_EN</td><td rowspan="8">DMCH_EN</td><td rowspan="8">DMCH_PATH</td><td rowspan="8" colspan="2">FUNC_MODE</td><td rowspan="8" colspan="3">DEC_PATH</td></tr>
<tr><td>1</td><td>1x17</td></tr>
<tr><td>2</td><td>1x1E</td></tr>
<tr><td>3</td><td>1x25</td></tr>
<tr><td rowspan="4">Y</td><td>0</td><td>1x40</td></tr>
<tr><td>1</td><td>1x47</td></tr>
<tr><td>2</td><td>1x4E</td></tr>
<tr><td>3</td><td>1x55</td></tr>
</table>

CH_EN Control channel enable.
- 0 Channel disable (default)
- 1 Channel enable

DMCH_EN Control dummy channel enable when corresponding channel is enabled.
- 0 Dummy channel disable (default)
- 1 Dummy channel enable

DMCH_PATH Select real or dummy channel for channel input when dummy channel is enabled.
- 0 Real channel for channel input (default)
- 1 Dummy channel for channel input

FUNC_MODE Select operation mode.
- 0 Live mode (default)
- 1 Strobe mode
- 2-3 Switch mode

DEC_PATH Select video input for each channel.
- 0 Video input from internal video decoder on VIN0 pins (default)
- 1 Video input from internal video decoder on VIN1 pins
- 2 Video input from internal video decoder on VIN2 pins
- 3 Video input from internal video decoder on VIN3 pins
- 4–7 Video input from external video decoder on PBIN pins

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x11	0	FREEZE	MIRROR	ENHANCE	POP_UP	BLANK	BOUND	BLINK
	1	1x18								
	2	1x1F								
	3	1x26								
Y	0	1x41								
	1	1x48								
	2	1x4F								
	3	1x56								

FREEZE — Enable freeze function.
- 0 Normal operation (default)
- 1 Enable freeze function

MIRROR — Enable horizontal mirroring function.
- 0 Normal operation (default)
- 1 Enable horizontal mirroring function

ENHANCE — Enable image enhancement function.
- 0 Normal operation (default)
- 1 Enable image enhancement function

POP_UP — Enable pop-up.
- 0 Disable pop-up (default)
- 1 Enable pop-up

BLANK — Enable Blank.
- 0 Disable blank (default)
- 1 Enable blank

BOUND — Enable channel boundary.
- 0 Disable channel boundary
- 1 Enable channel boundary.

BLINK — Enable boundary blink when boundary is enabled.
- 0 Disable boundary blink (default)
- 1 Enable boundary blink

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x12	RECALL_EN	RECALL_ADDR						
	1	1x19								
	2	1x20								
	3	1x27								
Y	0	1x42								
	1	1x49								
	2	1x50								
	3	1x57								

RECALL_EN — Enable recall function.

0 Disable recall function (default)

1 Enable recall function

RECALL_ADDR — Define address to recall.

0-3 Reserved address. Do not use this value

4-15 Possible address for 64M SDRAM

4-31 Possible address for 128M SDRAM

4-63 Possible address for 256M SDRAM

4-127 Possible address for 512M SDRAM

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x13	PICHL							
	1	1x1A								
	2	1x21								
	3	1x28								
Y	0	1x43								
	1	1x4A								
	2	1x51								
	3	1x58								

PICHL Define horizontal left position of channel region when DIS_MODE = “0”. 1 step is 4 pixels.

0 Left end (default)

: :

180 Right end

Only PICHL[7:6] defines horizontal channel position when DIS_MODE = “1”.

0 1st position of horizontal region defined by HDIV

1 2nd position of horizontal region defined by HDIV

2 3rd position of horizontal region defined by HDIV

3 4th position of horizontal region defined by HDIV

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x14	PICHR							
	1	1x1B								
	2	1x22								
	3	1x29								
Y	0	1x44								
	1	1x4B								
	2	1x52								
	3	1x59								

PICHR Define horizontal right position of channel region when DIS_MODE = “0”. 1 step is 4 pixels.

0 Left end (default)

: :

180 Right end

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x15	PICVT							
	1	1x1C								
	2	1x23								
	3	1x2A								
Y	0	1x45								
	1	1x4C								
	2	1x53								
	3	1x5A								

PICVT

Define vertical top position of channel region.

1 step is 2 lines when DIS_MODE = “0” and FRAME_OP = “0”.

0 Top end (default)

: :

120 Bottom end for 60Hz system

: :

144 Bottom end for 50Hz system

1 step is 4 lines when DIS_MODE = “0” and FRAME_OP = “1”.

0 Odd field top end (default)

: :

60 Odd field bottom end for 60Hz system

: :

72 Odd field bottom end for 50Hz system

: :

120 Even field bottom end for 60Hz system

: :

144 Even field bottom end for 50Hz system

Only PICVT[7:6] defines vertical channel position when DIS_MODE = “1”.

0 1st position of vertical region defined by VDIV

1 2nd position of vertical region defined by VDIV

2 3rd position of vertical region defined by VDIV

3 4th position of vertical region defined by VDIV

Path	CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	0	1x16	PICVB							
	1	1x1D								
	2	1x24								
	3	1x2B								
Y	0	1x46								
	1	1x4D								
	2	1x54								
	3	1x5B								

PICVB Define vertical bottom position of channel region.

1 step is 2 lines when DIS_MODE = “0” and FRAME_OP = “0”.

0 Top end (default)

: :

120 Bottom end for 60Hz system

: :

144 Bottom end for 50Hz system

1 step is 4 lines when DIS_MODE = “0” and FRAME_OP = “1”.

0 Odd field top end (default)

: :

60 Odd field bottom end for 60Hz system

: :

72 Odd field bottom end for 50Hz system

: :

120 Even field bottom end for 60Hz system

: :

144 Even field bottom end for 50Hz system

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x2C	0	0	0	0	0	0	0	0
1x2D	0	0	0	0	0	0	0	0
1x2E	0	0	0	0	0	0	0	0
1x2F	0	0	0	0	0	0	0	0
1x5C	0	0	0	0	1	0	0	0
1x5D	0	0	0	0	0	0	0	0
1x5E	0	0	0	0	0	0	0	0

This is reserved register.
For normal operation, the above value should be set in this register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x5F	MEM_INIT	ENCCLK_Y	ENCCLK_X	0	0	ENCCLKP_Y	ENCCLKP_X	0

MEM_INIT Initialize operation mode of SDRAM.
This is cleared by itself after setting “1”.
0 None operation (default)
1 Request to start initializing operation mode of SDRAM

ENCCLK Control clock frequency of ENC_CLK27 pins for digital video output data.
0 27MHz (default)
1 54MHz

ENCCLKP Control clock phase of ENC_CLK27 pins.
0 Normal (default)
1 Inverted

CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	1x60	DMPICHL							
1	1x64								
2	1x68								
3	1x6C								

DMPICHL — Define horizontal left position of dummy channel region when DIS_MODE = "0". 1 step is 4 pixels.

0 Left end (default)

: :

180 Right end

Only DMPICHL[7:6] defines horizontal channel position when DIS_MODE = "1".

0 1st position of horizontal region defined by HDIV

1 2nd position of horizontal region defined by HDIV

2 3rd position of horizontal region defined by HDIV

3 4th position of horizontal region defined by HDIV

CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	1x61	DMPICHR							
1	1x65								
2	1x69								
3	1x6D								

DMPICHR — Define horizontal right position of dummy channel region when DIS_MODE = "0". 1 step is 4 pixels.

0 Left end (default)

: :

180 Right end

CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	1x62	DMPICVT							
1	1x66								
2	1x6A								
3	1x6E								

DMPICVT

Define vertical top position of dummy channel region.

1 step is 2 lines when DIS_MODE = “0” and FRAME_OP = “0”.

0 Top end (default)

: :

120 Bottom end for 60Hz system

: :

144 Bottom end for 50Hz system

1 step is 4 lines when DIS_MODE = “0” and FRAME_OP = “1”.

0 Odd field top end (default)

: :

60 Odd field bottom end for 60Hz system

: :

72 Odd field bottom end for 50Hz system

: :

120 Even field bottom end for 60Hz system

: :

144 Even field bottom end for 50Hz system

Only DMPICVT[7:6] defines vertical channel position when DIS_MODE = “1”.

0 1st position of vertical region defined by VDIV

1 2nd position of vertical region defined by VDIV

2 3rd position of vertical region defined by VDIV

3 4th position of vertical region defined by VDIV

CH	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	1x63	DMPICVB							
1	1x67								
2	1x6B								
3	1x6F								

DMPICVB — Define vertical bottom position of dummy channel region.

1 step is 2 lines when DIS_MODE = “0” and FRAME_OP = “0”.

0 Top end (default)
: :
120 Bottom end for 60Hz system
: :
144 Bottom end for 50Hz system

1 step is 4 lines when DIS_MODE = “0” and FRAME_OP = ”1”.

0 Odd field top end (default)
: :
60 Odd field bottom end for 60Hz system
: :
72 Odd field bottom end for 50Hz system
: :
120 Even field bottom end for 60Hz system
: :
144 Even field bottom end for 50Hz system

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x70	ENC_IN_X		ENC_IN_Y		CCIR_IN_X		CCIR_IN_Y	

ENC_IN — Select video data for input of video encoder.

0 X path video data without character and mouse pointer overlay (default)
1 X path video data with character and mouse pointer overlay
2 Y path video data without character and mouse pointer overlay
3 Y path video data with character and mouse pointer overlay

CCIR_IN — Select video data for input of ITU-R BT 656 encoder.

0 X path video data without character and mouse pointer overlay (default)
1 X path video data with character and mouse pointer overlay
2 Y path video data without character and mouse pointer overlay
3 Y path video data with character and mouse pointer overlay

For the TW2824MS and TW2824QS,
the selection of X and Y path is controlled by only the ENC_IN_X[1].

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x71	0	DAC_PD_X		DAC_OUT_X	0	DAC_PD_Y		DAC_OUT_Y

DAC_PD

Enable power down for DAC.

0 Normal operation (default)

1 Power down for DAC of VOUTY pin

2 Power down for DAC of VOUTC pin

3 Power down for both DAC of VOUTY and VOUTC pins

DAC_OUT

Define analog video format.

0 S-Video output (default)

1 CVBS output

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x72	0	0	CCIR_OUT_X		0	0	CCIR_OUT_Y	

CCIR_OUT

Define type for ITU-R BT.656 digital output.

The default value is “0” for CCIR_OUT_X, but “1” for CCIR_OUT_Y.

0 X path video data with single output mode (27MHz)

1 Y path video data with single output mode (27MHz)

2 X and Y path video data sequence with dual output mode (54MHz)

3 Y and X path video data sequence with dual output mode (54MHz)

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x73	ENC_ MODE	CCIR_ LMT	ENC_VS	ENC_FLD	CCIR_ FLDPOL	ENC_ HSPOL	ENC_ VSPOL	ENC_ FLDPOL

ENC_MODE — Define operation mode of video encoder.
- 0 Slave mode operation (default)
- 1 Master mode operation

CCIR_LMT — Control the data range of ITU-R BT 656 output.
- 0 Data range is limited to 1 ~ 254 code (default)
- 1 Data range is limited to 16 ~ 235 code

ENC_VS — Define vertical sync detection type.
- 0 Detect vertical sync from VSENC pin (default)
- 1 Detect vertical sync from combination of HSENC and FLDEN pins

ENC_FLD — Define field polarity detection type
- 0 Detect field polarity from FLDENC pin (default)
- 1 Detect field polarity from combination of HSENC and VSENC pins

CCIR_FLDPOL — Invert field polarity of ITU-R BT 656 output.
- 0 Normal (default)
- 1 Inverted

ENC_HSPOL — Control horizontal sync polarity.
- 0 Active low (default)
- 1 Active high

ENC_VSPOL — Control vertical sync polarity.
- 0 Active low (default)
- 1 Active high

ENC_FLDPOL — Control field polarity.
- 0 Even field is high (default)
- 1 Odd field is high

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x74	ENC_VSOFF		ENC_VSDEL					

ENC_VSOFF — Compensate field offset for first active video line.

0 Applied same ENC_VSDEL for odd and even field (default)
1 Applied {ENC_VSDEL+1} for odd and ENC_VSDEL for even field
2 Applied ENC_VSDEL for odd and {ENC_VSDEL +1} for even field
3 Applied ENC_VSDEL for odd and {ENC_VSDEL +2} for even field

ENC_VSDEL — Control vertical delay of active video line from vertical sync by 1 line/step.

0 No delayed
: :
32 32 lines delayed (default)
: :
63 63 lines delayed

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x75	ENC_HSDEL							

ENC_HSDEL — Control horizontal delay of active video pixel from horizontal sync by 2 pixels/step.

0 No delayed
: :
32 64 pixels delayed (default)
: :
255 510 pixels delayed

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x76	ACTIVE_HDEL					ACTIVE_VDEL		

ACTIVE_HDEL Control horizontal delay only for active video with 2 pixels/step.

0 - 30 Pixels delayed

: :

15 0 Pixel delayed (default)

: :

31 + 32 Pixels delayed

ACTIVE_VDEL Control vertical delay only for active video with 1 line/step.

0 - 4 Lines delayed

: :

4 0 Line delayed (default)

: :

7 + 3 Lines delayed

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x77	ENC_FSC		0	0	1	ENC_ PHALT	ENC_ ALTRST	ENC_ PED

ENC_FSC — Set color sub-carrier frequency for video encoder.

0 3.57954545 MHz (default)
1 4.43361875 MHz
2 3.57561149 MHz
3 3.58205625 MHz

ENC_PHALT — Set phase alternation.

0 Disable phase alternation for line-by-line (default)
1 Enable phase alternation for line-by-line

ENC_ALTRST — Reset phase alternation for every 8 fields

0 Disable phase alternation reset for every 8 fields (default)
1 Enable phase alternation reset for every 8 fields

ENC_PED — Set 7.5IRE for pedestal level

0 Disable 7.5 IRE for pedestal level
1 Enable 7.5 IRE for pedestal level (default)

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x78	ENC_CBW_X		ENC_YBW_X		ENC_CBW_Y		ENC_YBW_Y	

ENC_CBW Control chrominance bandwidth of video encoder.

0 0.8 MHz
1 1.15 MHz
2 1.35 MHz (default)
3 Do not use

ENC_YBW Control luminance bandwidth of video encoder.

0 Narrow bandwidth
1 More Narrow bandwidth
2 Wide bandwidth (default)
3 Do not use

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x79	ENC_ BAR_X	ENC_ CKILL_X	ENC_ BAR_Y	ENC_ CKILL_Y	ENC_ VS_READ *	ENC_ FLD_READ *		

Notes “*” stand for read only register

ENC_BAR Enable test pattern output.

0 Normal operation (default)
1 Internal color bar with 100% amplitude 100 % saturation

ENC_CKILL Color killer

0 Normal operation (default)
1 Color is killed

ENC_VS_READ Vertical sync can be read via this register.

ENC_FLD_READ Internal field counter can be read via this register.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x7A	FONT_WR_DATA[27:20]							
1x7B	FONT_WR_DATA[19:12]							
1x7C	FONT_WR_DATA[11:4]							
1x7D	FONT_WR_DATA[3:0]				0	0	0	0

FONT_WR_DATA Font data for 1 line of 1 font.

The default value is 0.

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x7E	0	FONT_WR_INDEX						

FONT_WR_INDEX Define font index.

0 Index 0 (default)

: :

127 Index 127

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x7F	FONT_ REQ_X	FONT_ REQ_Y	FONT_ WR_PAGE	FONT_ WR_FLD	FONT_WR_LINE			

FONT_REQ Request to start writing font to SDRAM.

This bit is cleared by itself after a few clocks.

0 None operation (default)

1 Request to start writing font

FONT_WR_PAGE Define font page to be written.

0 Page 0 (default)

1 Page 1

FONT_WR_FLD Define font field to be written.

0 Odd field (default)

1 Even field

FONT_WR_LINE Define font line to be written.

0 1st Line (default)

: :

15 16th Line

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x80	0	FONT_ RD_PAGE_X	FONT_ RD_FLD_X		0	FONT_ RD_PAGE_Y	FONT_ RD_FLD_Y	

FONT_RD_PAGE Define font page to be displayed.

- 0 Page 0 (default)
- 1 Page 1

FONT_RD_FLD Define font field to be displayed.

- 0 Character is not displayed (default)
- 1 Odd field font is used for both odd and even field
- 2 Even field font is used for both odd and even field
- 3 Both odd and even field font are used for frame display

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x81	0	0	RAMCLR _Y	RAMCLR _X	CLASSEN0 _Y	CLASSEN0 _X	PHIGH	PLOW

RAMCLR Clear display RAM.

This bit is cleared by itself after finishing display RAM clear.

- 0 None operation (default)
- 1 Request to start clearing display RAM

CLASSEN0 Enable class 0 in character mode.

- 0 Disable class 0 (default)
- 1 Enable class 0

PHIGH Select blink time for high.

- 0 0.5 second (default)
- 1 0.75 second

PLOW Select blink time for low.

- 0 0.5 second (default)
- 1 0.75 second

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x82	CHAR_ VSIZE_Y		CHAR_ HSIZE_Y		CHAR_ VSIZE_X		CHAR_ HSIZE_X	

CHAR_VSIZE	Vertical size of displayed character.

0	10 Lines (default)
1	12 Lines
2	14 Lines
3	16 Lines

CHAR_HSIZE	Horizontal size of displayed character.

0	8 Dots (16 Pixels) (default)
1	10 Dots (20 Pixels)
2	12 Dots (24 Pixels)
3	14 Dots (28 Pixels)

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x83	CHAR_VSPC				CHAR_HSPC			
Y	1x85								

CHAR_VSPC	Vertical space between displayed characters.

0	No Space (default)
:	:
15	15 Lines space

CHAR_HSPC	Horizontal space between displayed characters.

0	No space (default)
:	:
15	30 Pixels space

Path	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
X	1x84	CHAR_VDEL				CHAR_HDEL			
Y	1x86								

CHAR_VDEL Vertical offset to first displayed character.

0 No offset (default)

: :

15 15 Lines offset

CHAR_HDEL Horizontal offset to first displayed character.

0 No offset (default)

: :

15 30 Pixels offset

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x87	CHAR_MIX_C				CHAR_MIX_B			

CHAR_MIX_C Control to be mixed with video data in character mode.
CHAR_MIX_C[3:0] stand for class 3 to 0.
0 Disable mix function (default)
1 Enable mix function

CHAR_MIX_B Control to be mixed with video data in bitmap mode.
CHAR_MIX_B[3:0] stand for class 3 to 0.
0 Disable mix function (default)
1 Enable mix function

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x88	CHAR_BLK_C				CHAR_BLK_B			

CHAR_BLK_C Control blink for character mode.
CHAR_BLK_C[3:0] stand for class 3 to 0.
0 Disable blink function (default)
1 Enable blink function

CHAR_BLK_B Control blink for bitmap mode.
CHAR_BLK_B[3:0] stand for class 3 to 0.
0 Disable blink function (default)
1 Enable blink function

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x89	CLASS3COL1_C				CLASS 3COL0_C			
1x8A	CLASS3COL3_C				CLASS 3COL2_C			
1x8B	CLASS3COL1_B				CLASS 3COL0_B			
1x8C	CLASS3COL3_B				CLASS 3COL2_B			
1x8D	CLASS2COL_C				CLASS2COL_B			
1x8E	CLASS1COL_C				CLASS1COL_B			
1x8F	CLASS0COL_C				CLASS0COL_B			

CLASS3COL0_C Color selection 0 of class 3 for character mode
CLASS3COL1_C Color selection 1 of class 3 for character mode
CLASS3COL2_C Color selection 2 of class 3 for character mode
CLASS3COL3_C Color selection 3 of class 3 for character mode
CLASS3COL0_B Color selection 0 of class 3 for bitmap mode
CLASS3COL1_B Color selection 1 of class 3 for bitmap mode
CLASS3COL2_B Color selection 2 of class 3 for bitmap mode
CLASS3COL3_B Color selection 3 of class 3 for bitmap mode
CLASS2COL_C Color selection of class 2 for character mode
CLASS2COL_B Color selection of class 2 for bitmap mode
CLASS1COL_C Color selection of class 1 for character mode
CLASS1COL_B Color selection of class 1 for bitmap mode
CLASS0COL_C Color selection of class 0 for character mode
CLASS0COL_B Color selection of class 0 for bitmap mode

Color selection table

0 White (75% Amplitude 100% Saturation) (default)
1 Yellow (75% Amplitude 100% Saturation)
2 Cyan (75 % Amplitude 100 Saturation)
3 Green (75% Amplitude 100% Saturation)
4 Magenta (75% Amplitude 100% Saturation)
5 Red (75% Amplitude 100% Saturation)
6 Blue (75% Amplitude 100% Saturation)
7 0% Black
8 100% White
9 50% Gray
10 25% Gray
11 Blue (75% Amplitude 75% Saturation)
12 Defined by CLUT0
13 Defined by CLUT1
14 Defined by CLUT2
15 Defined by CLUT3

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x90	CLUT0_Y							
1x91	CLUT0_CB							
1x92	CLUT0_CR							
1x93	CLUT1_Y							
1x94	CLUT1_CB							
1x95	CLUT1_CR							
1x96	CLUT2_Y							
1x97	CLUT2_CB							
1x98	CLUT2_CR							
1x99	CLUT3_Y							
1x9A	CLUT3_CB							
1x9B	CLUT3_CR							

CLUT0_Y	Y component for user defined color 0 (default : 0)
CLUT0_CB	Cb component for user defined color 0 (default : 0)
CLUT0_CR	Cr component for user defined color 0 (default : 0)
CLUT1_Y	Y component for user defined color 1 (default : 0)
CLUT1_CB	Cb component for user defined color 1 (default : 0)
CLUT1_CR	Cr component for user defined color 1 (default : 0)
CLUT2_Y	Y component for user defined color 2 (default : 0)
CLUT2_CB	Cb component for user defined color 2 (default : 0)
CLUT2_CR	Cr component for user defined color 2 (default : 0)
CLUT3_Y	Y component for user defined color 3 (default : 0)
CLUT3_CB	Cb component for user defined color 3 (default : 0)
CLUT3_CR	Cr component for user defined color 3 (default : 0)

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x9C	CHAR_ PATH	0	0	CHAR_VLOC				

CHAR_PATH Select display RAM of X or Y path to write character's attributes.

0 Write into display RAM of X path (default)

1 Write into display RAM of Y path

CHAR_VLOC Define vertical position of displayed character.

0 1st character vertically (default)

: :

28 29th character vertically

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x9D	0	0	CHAR_HLOC					

CHAR_HLOC Define horizontal position of displayed character.

0 1st character horizontally (default)

: :

44 45th character horizontally

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1x9E	0	0	0	0	CHAR_ATTR[11:8]			
	CHAR_ATTR[7:0]							

CHAR_ATTR Character's attributes to be written into display RAM with CHAR_HLOC, CHAR_VLOC and CHAR_PATH.

Each character's attributes consist of 2 bytes so that it should be written in pairs.

CHAR_ATTR has following information.

CHAR_ATTR[11] Mix enable
- 0 Disable mix
- 1 Enable mix with video data

CHAR_ATTR[10] Blink enable
- 0 Disable blink
- 1 Enable blink

CHAR_ATTR[9:8] Color of class3
- 0 CLASS3COL0 in register 1x89~1x8C
- 1 CLASS3COL1 in register 1x89~1x8C
- 2 CLASS3COL2 in register 1x89~1x8C
- 3 CLASS3COL3 in register 1x89~1x8C

CHAR_ATTR[7] Type
- 0 Character type
- 1 Bitmap type

CHAR_ATTR[6:0] Font index
- 0 1st index
- : :
- 127 128th index

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
2x00	CUR_ ON_X	CUR_ ON_Y	CUR_ TYPE	CUR_ SUB	CUR_ BLINK	0		

CUR_ON Enable mouse pointer.
0 Disable mouse pointer (default)
1 Enable mouse pointer

CUR_TYPE Select mouse type
0 Small mouse pointer (default)
1 Large mouse pointer

CUR_SUB Control inside style of mouse pointer.
0 Transparent (default)
1 Filled with white color

CUR_BLINK Enable blink of mouse pointer.
0 Disable blink (default)
1 Enable blink with 0.5 second period

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
2x00							CUR_HP[0]	CUR_VP[0]
2x01	CUR_HP[8:1]							
2x02	CUR_VP[8:1]							

CUR_HP Horizontal location of mouse pointer.
0 0 Pixel position (default)
: :
360 720 Pixels position

CUR_VP Vertical location of mouse pointer.
0 0 Line position (default)
: :
288 288 Line position

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
2x03	BOX_TYPE	BOX_EMP	0	0	BOX_PLNEN			

BOX_TYPE

Select single box type.

0 Flat type (default)

1 3D type

BOX_EMP

Enable emphasis on box plane.

0 Disable emphasis (default)

1 Enable emphasis

BOX_PLNEN

Enable each box plane color.

BOX_PLNEN[3] enables box plane color defined by BOX_PLNCOL3

BOX_PLNEN[2] enables box plane color defined by BOX_PLNCOL2

BOX_PLNEN[1] enables box plane color defined by BOX_PLNCOL1

BOX_PLNEN[0] enables box plane color defined by BOX_PLNCOL0

0 Disable box plane color (default)

1 Enable box plane color

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
2x04	BOX_BNDCOL							

BOX_BNDCOL   Select box boundary color as the following table
The default value is 0.

Boundary		Control Register			Color Description	
		BOX_TYPE	BOX_OBND	BOX_IBND	Register	Color
Outer		0 (Flat Type)	0	0	BOX_ BNDCOL [7:4]	Box off
			0	1		Boundary off
			1	0		0~10 : 0, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100 IRE Gray 11~14 : Selected by BOX_PLNCOL0 ~ BOX_PLNCOL3. 15 : Same as plane color with 20IRE down of luminance
			1	1		
Inner			0	0	BOX_ BNDCOL [3:0]	Box off
			1	0		Same as inner area
			0	1		0~10 : 0, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100 IRE Gray 11~14 : Selected by BOX_PLNCOL0~BOX_PLNCOL3. 15 : Same as plane color with 20IRE up of luminance
			1	1		
Outer	Left & Top	1 (3D Type)	0	0	BOX_ BNDCOL [7:6]	Box off
			0	1		Boundary off
			1	0		0~3 : 90, 80, 70, 60 IRE Gray
			1	1		0~3 : 0, 10, 20, 30 IRE Gray
	Right & Bottom		0	0	BOX_ BNDCOL [5:4]	Box off
			0	1		Boundary off
			1	0		0~3 : 0, 10, 20, 30 IRE Gray
			1	1		0~3 : 90, 80, 70, 60 IRE Gray
Inner	Left & Top		0	0	BOX_ BNDCOL [3:2]	Box off
			0	1		Boundary off
			1	0		Same as inner area
			1	1		0~3 : 30, 40, 50, 60 IRE Gray
	Right & Bottom		0	0	BOX_ BNDCOL [1:0]	Box off
			0	1		Boundary off
			1	0		0~3 : 30, 40, 50, 60 IRE Gray
			1	1		0~3 : 70, 60, 50, 40 IRE Gray

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
2x05	BOX_PLNCOL3				BOX_PLNCOL2			
2x06	BOX_PLNCOL1				BOX_PLNCOL0			

BOX_PLNCOL3 Define box plane color for BOX_PLNSEL = 3

BOX_PLNCOL2 Define box plane color for BOX_PLNSEL = 2

BOX_PLNCOL1 Define box plane color for BOX_PLNSEL = 1

BOX_PLNCOL0 Define box plane color for BOX_PLNSEL = 0

Color selection table

0 White (75% Amplitude 100% Saturation) (default)
1 Yellow (75% Amplitude 100% Saturation)
2 Cyan (75 % Amplitude 100 Saturation)
3 Green (75% Amplitude 100% Saturation)
4 Magenta (75% Amplitude 100% Saturation)
5 Red (75% Amplitude 100% Saturation)
6 Blue (75% Amplitude 100% Saturation)
7 0% Black
8 100% White
9 50% Gray
10 25% Gray
11 Blue (75% Amplitude 75% Saturation)
12 Defined by CLUT0
13 Defined by CLUT1
14 Defined by CLUT2
15 Defined by CLUT3

Box	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x07	BOX_PATH	BOX_OBND	BOX_IBND	BOX_PLNMIX	BOX_PLNSEL			
1	2x0C								
2	2x11								
3	2x16								
4	2x1B								
5	2x20								
6	2x25								
7	2x2A								
8	2x2F								
9	2x34								
10	2x39								
11	2x3E								
12	2x43								
13	2x48								
14	2x4D								
15	2x52								

BOX_PATH — Select path for box to be displayed.
0 X path (default)
1 Y path

BOX_OBND — Enable outer boundary.
Refer to the box boundary color in 2x04.
The default value is 0

BOX_IBND — Enable inner boundary.
Refer to the box boundary color in 2x04.
The default value is 0

BOX_PLNMIX — Enable to mix box plane with video data.
0 Disable to mix (default)
1 Enable to mix

BOX_PLNSEL — Select box plane color.
0 Color defined by BOX_PLNCOL0 and BOX_PLNEN[0] (default)
1 Color defined by BOX_PLNCOL1 and BOX_PLNEN[1]
2 Color defined by BOX_PLNCOL2 and BOX_PLNEN[2]
3 Color defined by BOX_PLNCOL3 and BOX_PLNEN[3]

Box	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x07							BOX_ HL[0]	
1	2x0C								
2	2x11								
3	2x16								
4	2x1B								
5	2x20								
6	2x25								
7	2x2A								
8	2x2F								
9	2x34								
10	2x39								
11	2x3E								
12	2x43								
13	2x48								
14	2x4D								
15	2x52								
0	2x08	BOX_ HL[8:1]							
1	2x0D								
2	2x12								
3	2x17								
4	2x1C								
5	2x21								
6	2x26								
7	2x2B								
8	2x30								
9	2x35								
10	2x3A								
11	2x3F								
12	2x44								
13	2x49								
14	2x4E								
15	2x53								

BOX_HL Define horizontal left location of box.

0 Left end (default)

: :

360 Right end

Box	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x09	BOX_HW							
1	2x0E								
2	2x13								
3	2x18								
4	2x1D								
5	2x22								
6	2x27								
7	2x2C								
8	2x31								
9	2x36								
10	2x3B								
11	2x40								
12	2x45								
13	2x4A								
14	2x4F								
15	2x54								

BOX_HW Define horizontal size of box.

0 0 Pixel width (default)

: :

180 720 Pixels width

Box	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x07								BOX_ VT[0]
1	2x0C								
2	2x11								
3	2x16								
4	2x1B								
5	2x20								
6	2x25								
7	2x2A								
8	2x2F								
9	2x34								
10	2x39								
11	2x3E								
12	2x43								
13	2x48								
14	2x4D								
15	2x52								
0	2x0A	BOX_ VT[8:1]							
1	2x0F								
2	2x14								
3	2x19								
4	2x1E								
5	2x23								
6	2x28								
7	2x2D								
8	2x32								
9	2x37								
10	2x3C								
11	2x41								
12	2x46								
13	2x4B								
14	2x50								
15	2x55								

BOX_VT — Define vertical top location of box.

0	Vertical top (default)
:	:
288	Vertical bottom

Box	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x0B	BOX_VW							
1	2x10								
2	2x15								
3	2x1A								
4	2x1F								
5	2x24								
6	2x29								
7	2x2E								
8	2x33								
9	2x38								
10	2x3D								
11	2x42								
12	2x47								
13	2x4C								
14	2x51								
15	2x56								

BOX_VW	Define vertical size of box.	
	0	0 Lines height (default)
	:	:
	144	288 Lines height

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
2x60	0	0	2DBOX_BNDCOL		2DBOX_PLNCOL			

2DBOX_BNDCOL Define the color of 2D arrayed box boundary

0 0 % Black (default)
1 25% Gray
2 50% Gray
3 75% White

Define the displayed color for cursor cell and motion-detected region

0,1 75% White (default)
2,3 0% Black

2DBOX_PLNCOL Define the color of 2D arrayed box plane.

Color selection table

0 White (75% Amplitude 100% Saturation) (default)
1 Yellow (75% Amplitude 100% Saturation)
2 Cyan (75 % Amplitude 100 Saturation)
3 Green (75% Amplitude 100% Saturation)
4 Magenta (75% Amplitude 100% Saturation)
5 Red (75% Amplitude 100% Saturation)
6 Blue (75% Amplitude 100% Saturation)
7 0% Black
8 100% White
9 50% Gray
10 25% Gray
11 Blue (75% Amplitude 75% Saturation)
12 Defined by CLUT0
13 Defined by CLUT1
14 Defined by CLUT2
15 Defined by CLUT3

2D Box	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	1	2x61			2DBOX_MODE	2DBOX_PATH	2DBOX_MIX	2DBOX_PLNEN	2DBOX_CUREN	2DBOX_BNDEN
1	2	2x68								
2	3	2x6F								
3	4	2x76								

2DBOX_MODE Define operation mode of 2D arrayed box.
0 Table mode (default)
1 Motion display mode

2DBOX_PATH Define path for 2D arrayed box to be displayed.
0 X path (default)
1 Y path

2DBOX_MIX Control to mix 2D arrayed box plane with video data.
0 Disable mix (default)
1 Enable mix

2DBOX_PLNEN Enable plane of 2D arrayed box.
0 Disable plane of 2D arrayed box (default)
1 Enable plane of 2D arrayed box

2DBOX_CUREN Enable cursor cell inside 2D arrayed box.
0 Disable cursor cell (default)
1 Enable cursor cell

2DBOX_BNDEN Enable boundary of 2D arrayed box.
0 Disable boundary (default)
1 Enable boundary

2D Box	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	1	2x61	2DBOX_VT[0]							
1	2	2x68								
2	3	2x6F								
3	4	2x76								
0	1	2x62	2DBOX_VT[8:1]							
1	2	2x69								
2	3	2x70								
3	4	2x77								

2DBOX_VT Define vertical top location of 2D arrayed box.

0 Vertical top end (default)

: :

120 Vertical bottom end for 60Hz system

: :

144 Vertical bottom end for 50Hz system

2D Box	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	1	2x61		2DBOX_HL[0]						
1	2	2x68								
2	3	2x6F								
3	4	2x76								
0	1	2x63	2DBOX_HL[8:1]							
1	2	2x6A								
2	3	2x71								
3	4	2x78								

2DBOX_HL Define horizontal left location of 2D arrayed box.

0 Horizontal left end (default)

: :

360 Horizontal right end

2D Box	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	1	2x64	2DBOX_VW							
1	2	2x6B								
2	3	2x72								
3	4	2x79								

2DBOX_VW Define vertical size of 2D arrayed box.

0 0 Line height (default)

: :

255 255 Lines height

2D Box	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	1	2x65	2DBOX_HW							
1	2	2x6C								
2	3	2x73								
3	4	2x7A								

2DBOX_HW Define horizontal size of 2D arrayed box.

0 0 Pixel width (default)

: :

255 510 Pixels width

2D Box	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	1	2x66	2DBOX_VNUM				2DBOX_HNUM			
1	2	2x6D								
2	3	2x74								
3	4	2x7B								

2DBOX_VNUM Define row number of 2D arrayed box.
For motion display mode, 11 is recommended.
0 1 Row
: :
11 12 Row (default)
: :
15 16 Rows

2DBOX_HNUM Define column number of 2D arrayed box.
For motion display mode, 15 is recommended.
0 1 Column
: :
15 16 Columns (default)

2D Box	VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	1	2x67	2DBOX_CUR_HP				2DBOX_CUR_VP			
1	2	2x6E								
2	3	2x75								
3	4	2x7C								

2DBOX_CUR_HP Define horizontal location of cursor cell within 2DBOX_HNUM.
0 1st Column (default)
: :
15 16th Column

2DBOX_CUR_VP Define vertical location of cursor cell within 2DBOX_VNUM.
0 1st Row (default)
: :
15 16th Row

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
2x7E	MB_DIS				0			

MB_DIS

Disable motion and blind detection.

MB_DIS [3:0] stand for VIN3 to VIN0.

0 Enable motion and blind detection (default)

1 Disable motion and blind detection

Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
2x7F	0		BD_CELSENS		BD_LVSENS			

BD_CELSENS

Define threshold of cell for blind detection.

0 Low threshold (More sensitive) (default)

: :

3 High threshold (Less sensitive)

BD_LVSENS

Define threshold of level for blind detection.

0 Low threshold (More sensitive) (default)

: :

15 High threshold (Less sensitive)

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x80	MASK_ MODE	0	MD_FLD		MD_ALGIN			
1	2xA0								
2	2xC0								
3	2xE0								

MASK_MODE Define mode of MD_MASK register when reading.

0 Reading result of motion detection (default)

1 Reading mask information

MD_FLD Select field for motion detection.

0 Detecting motion for only odd field (default)

1 Detecting motion for only even field

2 Detecting motion for both odd and even field

3 Detecting motion for both odd and even field

MD_ALGIN Adjust horizontal region of motion detection.

0 0 Pixel shift (default)

: :

15 15 Pixels shift

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x81	MD_CELSENS		0	MD_LVSENS				
1	2xA1								
2	2xC1								
3	2xE1								

MD_CELSENS Define threshold of sub-cell number for motion detection.

0 Motion detected for cell if 1 sub-cell has motion (More sensitive) (default)

1 Motion detected for cell if 2 sub-cells have motion

2 Motion detected for cell if 3 sub-cells have motion

3 Motion detected for cell if 4 sub-cells have motion (Less sensitive)

MD_LVSENS Control the level sensitivity of motion detector.

0 More sensitive

: :

8 Middle sensitive (default)

: :

15 Less sensitive

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x82	MD_ REFFLD	0	MD_SPEED					
1	2xA2								
2	2xC2								
3	2xE2								

MD_REFFLD Control the updating time of reference field for motion detection.

0 Update reference field at every field (default)

1 Update reference field according to MD_SPEED

MD_SPEED Control the velocity of motion detector.

Large value is suitable for detection of slow motion.

0 Not supported (default)

1 2 field interval

: :

61 62 field interval

62 Not supported

63 Not supported

VIN	Index	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	2x83	MD_TMPSENS				MD_SPSENS			
1	2xA3								
2	2xC3								
3	2xE3								

MD_TMPSENS Control the temporal sensitivity of motion detector.

0 More Sensitive (default)

: :

15 Less Sensitive

MD_SPSENS Control the spatial sensitivity of motion detector.

0 More Sensitive (default)

: :

15 Less Sensitive

Row	Index				Motion Detection Mask Control for VIN							
	VIN0	VIN1	VIN2	VIN3	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	2x84	2xA4	2xC4	2xE4	MD_MASK[15:8]							
2	2x86	2xA6	2xC6	2xE6								
3	2x88	2xA8	2xC8	2xE8								
4	2x8A	2xAA	2xCA	2xEA								
5	2x8C	2xAC	2xCC	2xEC								
6	2x8E	2xAE	2xCE	2xEE								
7	2x90	2xB0	2xD0	2xF0								
8	2x92	2xB2	2xD2	2xF2								
9	2x94	2xB4	2xD4	2xF4								
10	2x96	2xB6	2xD6	2xF6								
11	2x98	2xB8	2xD8	2xF8								
12	2x9A	2xBA	2xDA	2xFA								
1	2x85	2xA5	2xC5	2xE5	MD_MASK[7:0]							
2	2x87	2xA7	2xC7	2xE7								
3	2x89	2xA9	2xC9	2xE9								
4	2x8B	2xAB	2xCB	2xEB								
5	2x8D	2xAD	2xCD	2xED								
6	2x8F	2xAF	2xCF	2xEF								
7	2x91	2xB1	2xD1	2xF1								
8	2x93	2xB3	2xD3	2xF3								
9	2x95	2xB5	2xD5	2xF5								
10	2x97	2xB7	2xD7	2xF7								
11	2x99	2xB9	2xD9	2xF9								
12	2x9B	2xBB	2xDB	2xFB								

MD_MASK — Motion Mask/Detection Cell for VIN

MD_MASK[15] is right end and MD_MASK[0] is left end of column.

Writing mode

0 Non-masking cell for motion detection (default)

1 Masking cell for motion detection

Reading mode when MASK_MODE = “0”

0 Motion is not detected for cell

1 Motion is detected for cell

Reading mode when MASK_MODE = “1”

0 Non-masked cell

1 Masked cell

Parametric Information

DC Electrical Parameters

Table 9 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VDDADC (measured to VSSADC)	VDD_{ADCM}			3.5	V
VDDDAC (measured to VSSDAC)	VDD_{DACM}			3.5	V
VDDI (measured to VSSI)	VDD_{IM}			3.5	V
VDDO (measured to VSSO)	VDD_{OM}			4.6	V
Voltage on Any Digital Data Pin (See the note below)	-	VSSO–0.5		6.0	V
Analog Input Voltage for ADC	-	VDD_{ADCM}–0.5		VDD_{ADCM}+0.5	V
Analog Input Voltage for DAC		VDD_{DACM}–0.5		VDD_{DACM}+0.5	V
Storage Temperature	T_S	– 65		150	° C
Junction Temperature	T_J	0		125	° C
Vapor Phase Soldering (15 Seconds)	T_{VSOL}			220	° C

NOTE: Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if operate exceeding the rating. The device should be operated under recommended operating condition.

Table 10 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
VDDADC (measured to VSSADC)	VDD_{ADC}	2.25	2.5	2.75	V
VDDDAC (measured to VSSDAC)	VDD_{DAC}	2.25	2.5	2.75	V
VDDI (measured to VSSI)	VDD_I	2.25	2.5	2.75	V
VDDO (measured to VSSO)	VDD_O	3.0	3.3	3.6	V
Maximum $\|VDD_I – VDD_{ADC}\|$				0.3	V
Maximum $\|VDD_I – VDD_{DAC}\|$				0.3	V
Maximum $\|VDD_{ADC} – VDD_{DAC}\|$				0.3	V
Maximum $\|VDD_O – VDD_{ADC}\|$				1.05	V
Maximum $\|VDD_O – VDD_{DAC}\|$				1.05	V
Maximum $\|VDD_O – VDD_I\|$				1.05	V
Analog VIN Amplitude Range (AC coupling required)		0.5	1.0	2.0	V
Ambient Operating Temperature	T_A	0		70	° C

Table 11 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0		5.5	V
Input Low Voltage (TTL)	V_{IL}	-0.3		0.8	V
Input Leakage Current (@V_I=2.5V or 0V)	I_L			±1	µA
Input Capacitance	C_{IN}		6		pF
Digital Outputs					
Output High Voltage	V_{OH}	2.4			V
Output Low Voltage	V_{OL}			0.4	V
High Level Output Current (@V_{OH}=2.4V)	I_{OH}	5.7	11.6	18.6	mA
Low Level Output Current (@V_{OL}=0.4V)	I_{OL}	4.1	6.7	8.2	mA
Tri-state Output Leakage Current (@V_O=2.5V or 0V)	I_{OZ}			±1	µA
Output Capacitance	C_O		6		pF
Analog Pin Input Capacitance	C_A		6		pF

Table 12 Supply Current and Power Dissipation

Parameter	Symbol	Min	Typ	Max	Units
Analog Supply Current (2.5V)	I_{DDA}		200		mA
Digital Internal Supply Current (2.5V)	I_{DDI}		630		mA
Digital I/O Supply Current (3.3V)	I_{DDO}		20		mA
Total Power Dissipation	Pd		2.15		W

AC Electrical Parameters

Table 13 Clock Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Delay from CLK54I to CLK27ENC	1	4.7		12.5	ns
Hold from CLK27ENC (27MHz) to Data	2a	17			ns
Delay from CLK27ENC (27MHz) to Data	2b			21	ns
Hold from CLK54I to Data	3a	8			ns
Delay from CLK54I to Data	3b			12	ns
Setup from PBIN to PBCLK	4a	5			ns
Hold from PBCLK to PBIN	4b	5			ns

Note : Cload = 25pF.

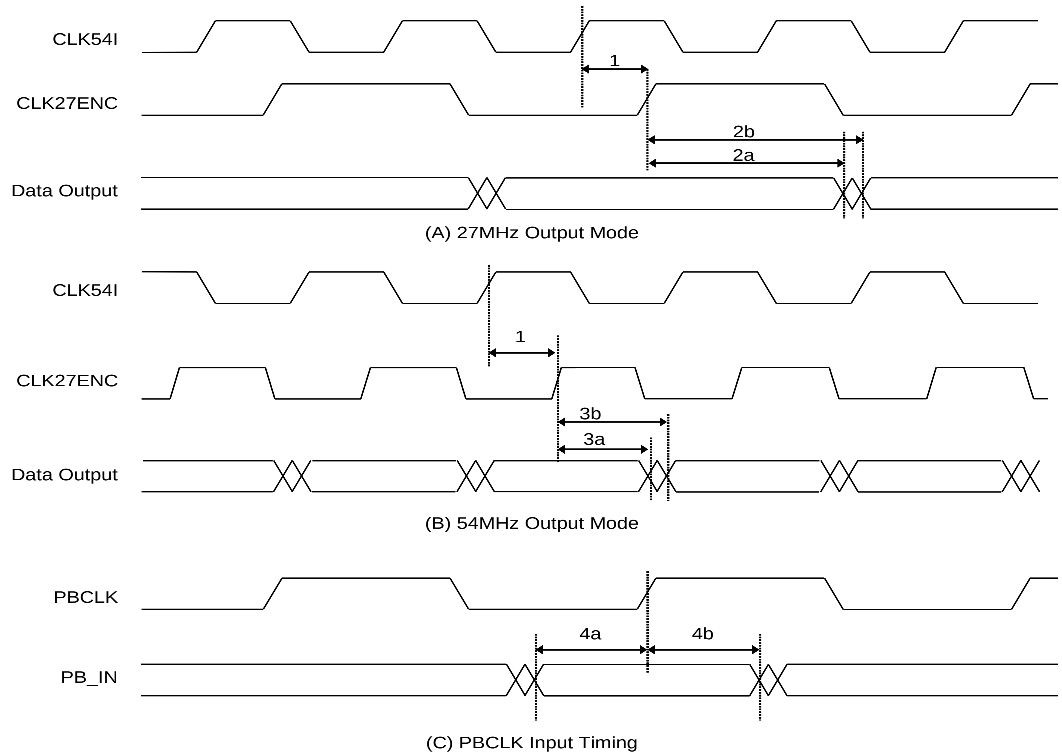


Fig 58 Clock Timing Diagram

Table 14. Serial Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
Bus Free Time between STOP and START	t_{BF}	1.3			us
SDAT setup time	t_{sSDAT}	100			ns
SDAT hold time	t_{hSDAT}	0		0.9	us
Setup time for START condition	t_{sSTA}	0.6			us
Setup time for STOP condition	t_{sSTOP}	0.6			us
Hold time for START condition	t_{hSTA}	0.6			us
Rise time for SCLK and SDAT	t_R			300	ns
Fall time for SCLK and SDAT	t_F			300	ns
Capacitive load for each bus line	C_{BUS}			400	pF
SCLK clock frequency	f_{SCLK}			400	KHz

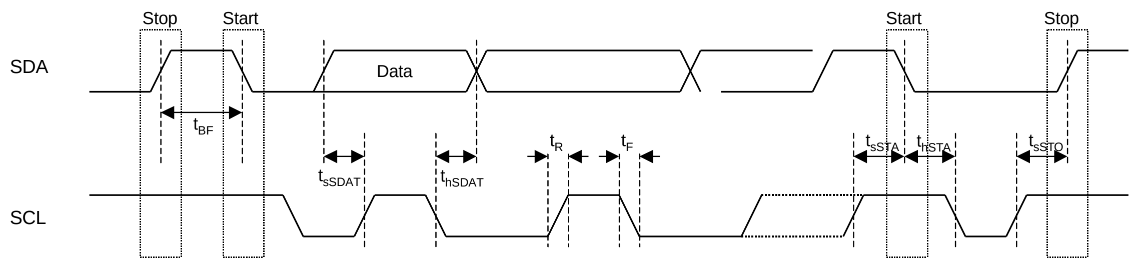


Fig 59. Serial Interface Timing Diagram

Table 15 Parallel Interface Timing Parameter

Parameter	Symbol	Min	Typ	Max	Units
CSB setup until AEN active	Tsu(1)	10			ns
PDATA setup until AEN,WENB active	Tsu(2)	10			ns
AEN, WENB, RENB active pulse width	Tw	40			ns
CSB hold after WENB, RENB inactive	Th(1)	60			ns
PDATA hold after AEN,WENB inactive	Th(2)	20			ns
PDATA delay after RENB active	Td(1)			12	ns
PDATA delay after RENB inactive	Td(2)	60			ns
CSB inactive pulse width	Tcs	60			ns
RENB active delay after AEN inactive RENB active delay after RENB inactive	Trd	60			ns

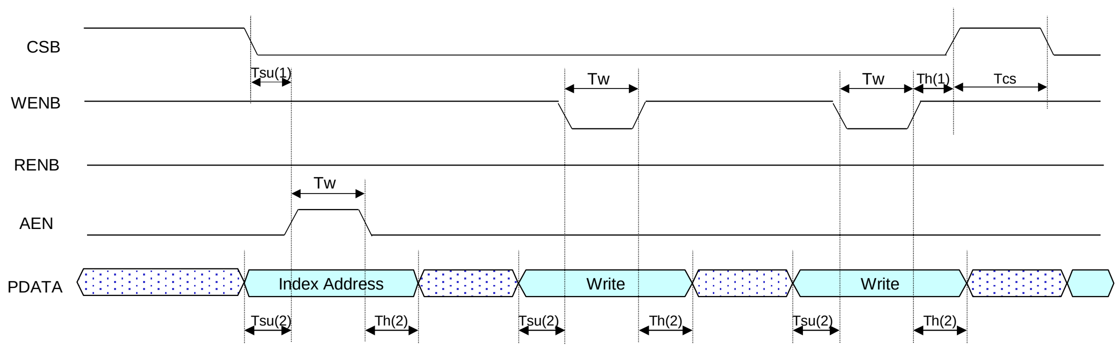


Fig 60 Write timing of parallel interface with auto index increment mode

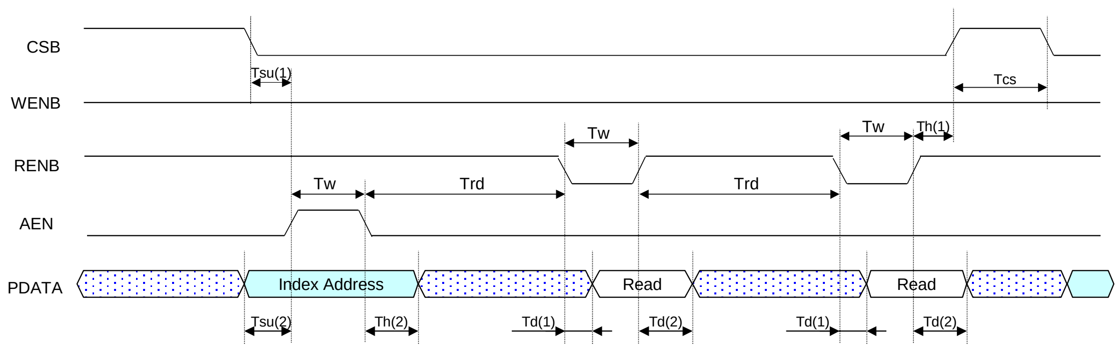


Fig 61 Read timing of parallel interface with auto index increment mode

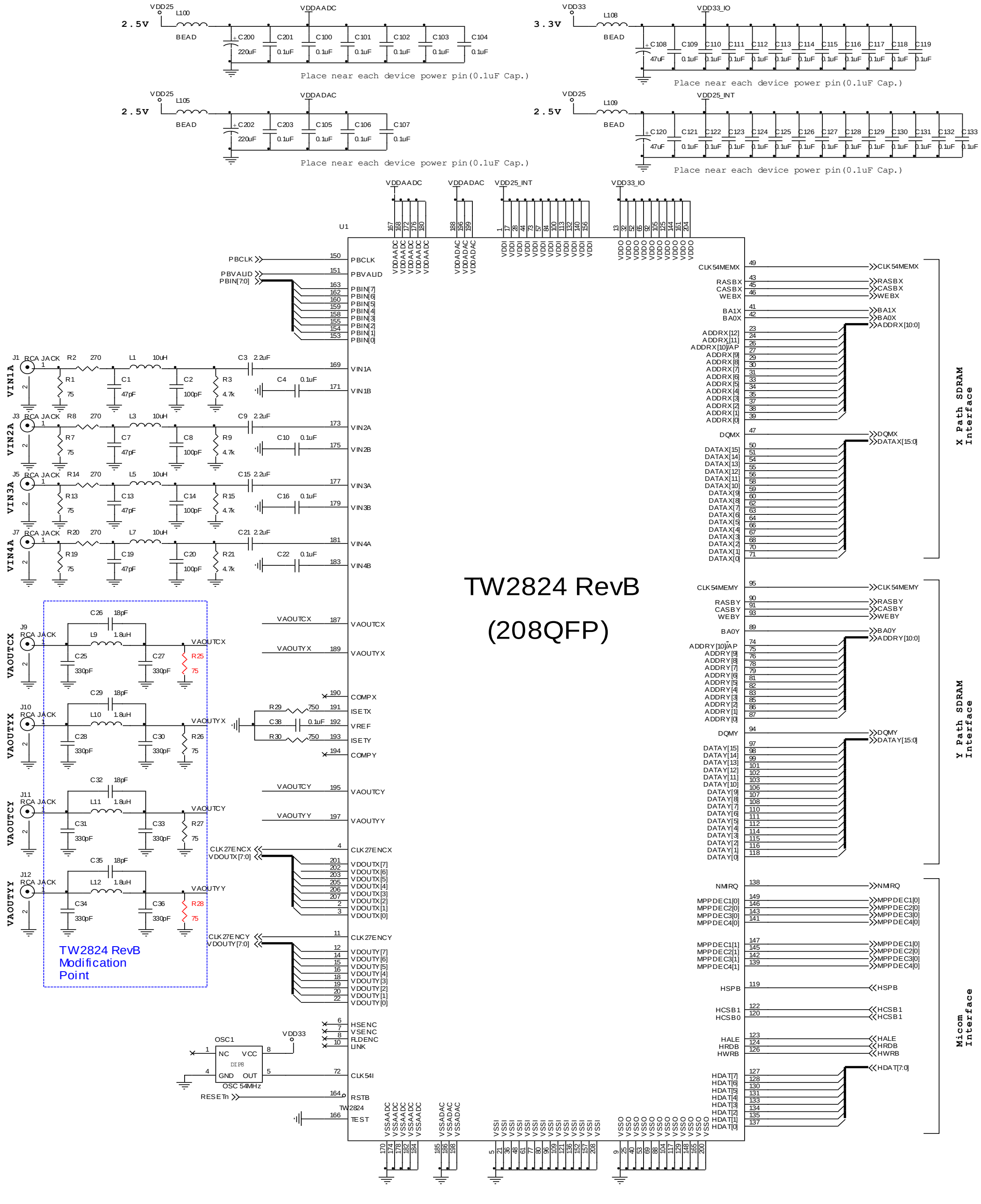
Table 16.Analog Performance Parameter

Parameter	Symbol	Min	Typ	Max	Units
ADC characteristics					
Differential gain	D_{GA}			3	%
Differential phase	D_{pA}			2	deg
Channel Cross-talk	α_{ctA}			-50	dB
DAC characteristic					
Differential gain	D_{GD}			3	%
Differential phase	D_{pD}			2	deg
Channel Cross-talk	α_{ctA}			-50	dB

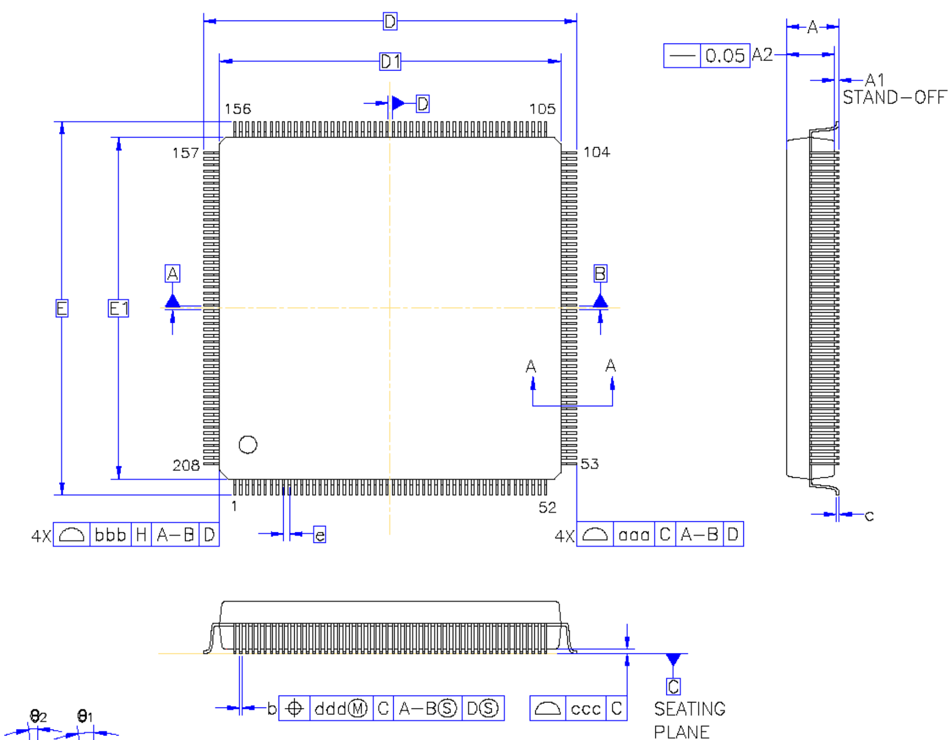
Table 17.Decoder Performance Parameter

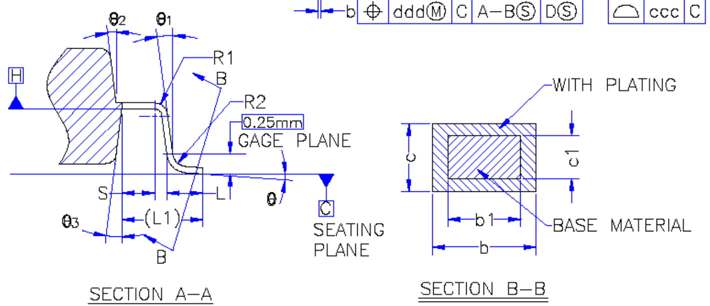
Parameter	Symbol	Min	Typ	Max	Units
Horizontal PLL permissible static deviation	Δf_H			±6	%
Color Sub-carrier PLL lock in range	Δf_{SC}	±800			Hz
Video level tracking range	AGC	-6		18	dB
Color level tracking range	ACC	-6		30	dB
Oscillator Input					
Nominal frequency	f_{OSC}		54		MHz
Permissible frequency deviation	$\Delta f_{OSC}/f_{OSC}$			±100	ppm
Duty cycle	dt_{OSC}			60	%

Application Schematic



Package Dimension





ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.00	—	—	0.157
A1	0.25	0.32	0.40	0.010	0.013	0.016
A2	3.20	3.40	3.60	0.126	0.134	0.142
D	30.60 BASIC			1.205 BASIC		
D1	28.00 BASIC			1.102 BASIC		
E	30.60 BASIC			1.205 BASIC		
E1	28.00 BASIC			1.102 BASIC		
R2	0.08	—	0.25	0.003	—	0.01
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	8°	0°	3.5°	8°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	5°	—	16°	5°	—	16°
$θ_3$	5°	—	16°	5°	—	16°
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.15	0.16	0.004	0.006	0.006
L1	1.30 REF			0.052 REF		
L	0.45	0.60	0.75	0.018	0.024	0.030
S	0.20	—	—	0.008	—	—
b	0.17	—	0.27	0.007	—	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
e	0.50 BSC.			0.020 BSC.		
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES:

1.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.ALLOW PROTRUSION IS 0.25mm PER SIDE.DIMENSIONS D1 AND E1 DO INCLUDE MISMATCH AND ARE DETERMINED AT DATUM PLANE H;

2.DIMENSION b DOES NOT INVLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT;

Revision History

Table 18 Datasheet Revision Histories

Revision	Date	Description	Product Code
FN7738.0	Feb. 2, 2011	Assigned file number FN7738 to datasheet as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. No changes to datasheet content.	

Table 19 List of Revision Point in TW2824 RevB

No.	Issue	TW2824 RevA	TW2824 RevB
1	ADC Linearity	-	Improved ADC linearity more
2	DAC output gain mismatch	The termination resistances are not same among four DACs	Fixed the gain mismatch of DAC output. The termination resistances are same among four DACs.