Device Overview

The 89HPES32T8 is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES32T8 is a 32-lane, 8-port peripheral chip that performs PCI Express packet switching with a feature set optimized for high performance applications such as servers, storage, and communications/networking. It provides connectivity and switching functions between a PCI Express upstream port and up to seven downstream ports and supports switching between downstream ports.

Features

- **High Performance PCI Express Switch**
  - *Thirty-two 2.5 Gbps PCI Express lanes*
  - *Eight switch ports*
  - *Upstream port configurable up to x8*
  - *Downstream ports configurable up to x8*
  - *Low-latency cut-through switch architecture*
  - *Support for Max Payload Size up to 2048 bytes*
  - *One virtual channel*
  - *Eight traffic classes*
  - *PCI Express Base Specification Revision 1.1 compliant*
- **Flexible Architecture with Numerous Configuration Options**
  - *Automatic per port link width negotiation to x8, x4, x2 or x1*
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion on all lanes*
  - *Ability to load device configuration from serial EEPROM*
- **Legacy Support**
  - *PCI compatible INTx emulation*
  - *Bus locking*
- **Highly Integrated Solution**
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates thirty-two 2.5 Gbps embedded SerDes with 8B/10B encoder/decoder (no separate transceivers needed)*
- **Reliability, Availability, and Serviceability (RAS) Features**
  - *Supports ECRC and Advanced Error Reporting*
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O*
  - *Compatible with Hot-Plug I/O expanders used on PC and server motherboards*

Block Diagram

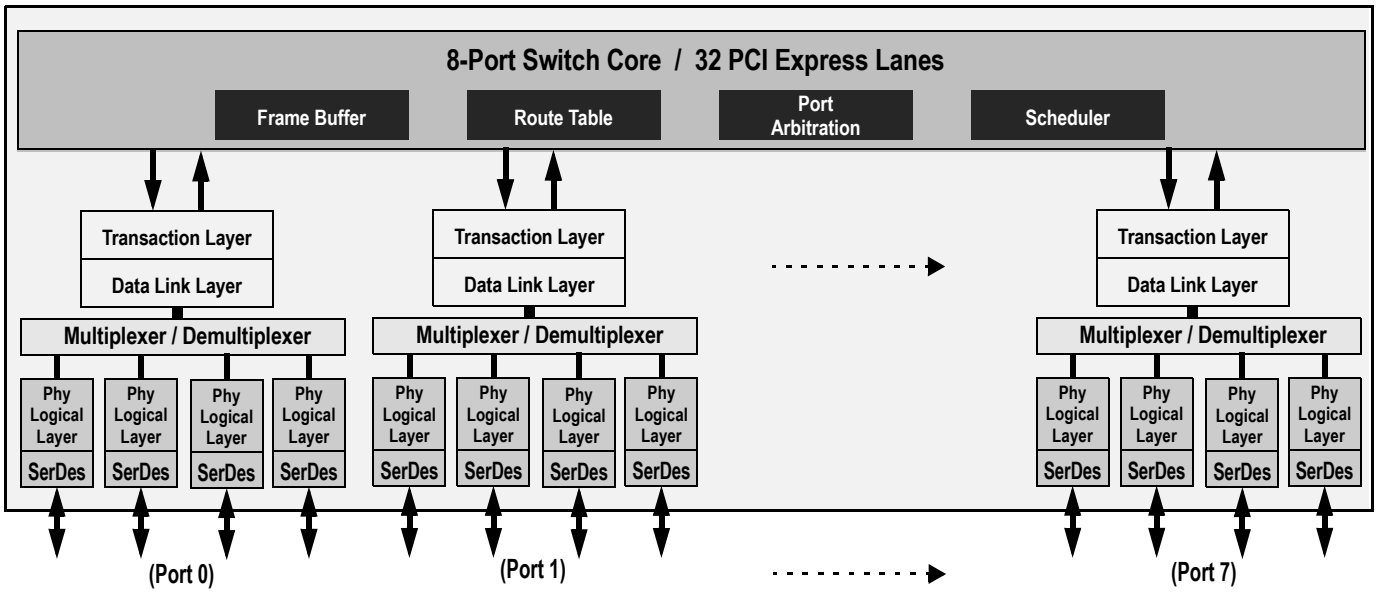


Figure 1 Internal Block Diagram

- **Power Management**
  - *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - *Supports PCI Power Management Interface specification (PCI-PM 1.1)*
    - *Supports device power management states: D0, $D3_{hot}$ and $D3_{cold}$*
  - *Unused SerDes are disabled*
- **Testability and Debug Features**
  - *Ability to read and write any internal register via the SMBus*
- **Sixteen General Purpose Input/Output Pins**
  - *Each pin may be individually configured as an input or output*
  - *Each pin may be individually configured as an interrupt input*
  - *Some pins have selectable alternate functions*
- **Packaged in a 31mm x 31mm 500-ball BGA with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect, the PES32T8 provides the most efficient I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides connectivity for up to 8 ports across 32 integrated serial lanes. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification revision 1.1.

The PES32T8 is based on a flexible and efficient layered architecture. The PCI Express layers consist of SerDes, Physical, Data Link and Transaction layers. The PES32T8 can operate either as a store and forward switch or a cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity.

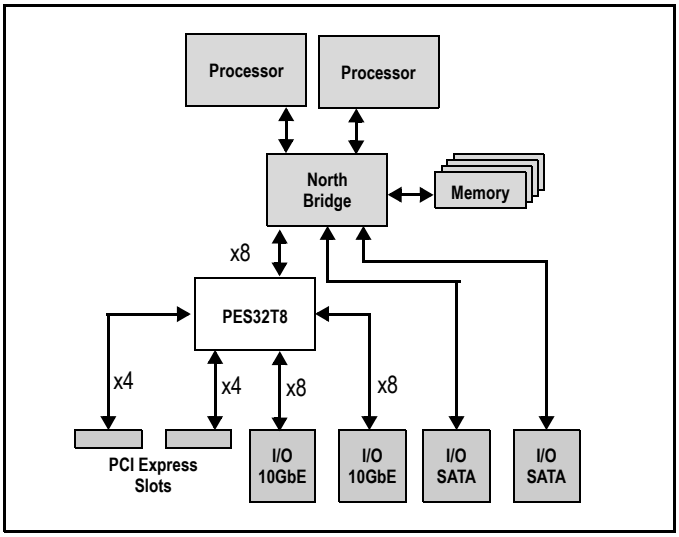


Figure 2 I/O Expansion Application

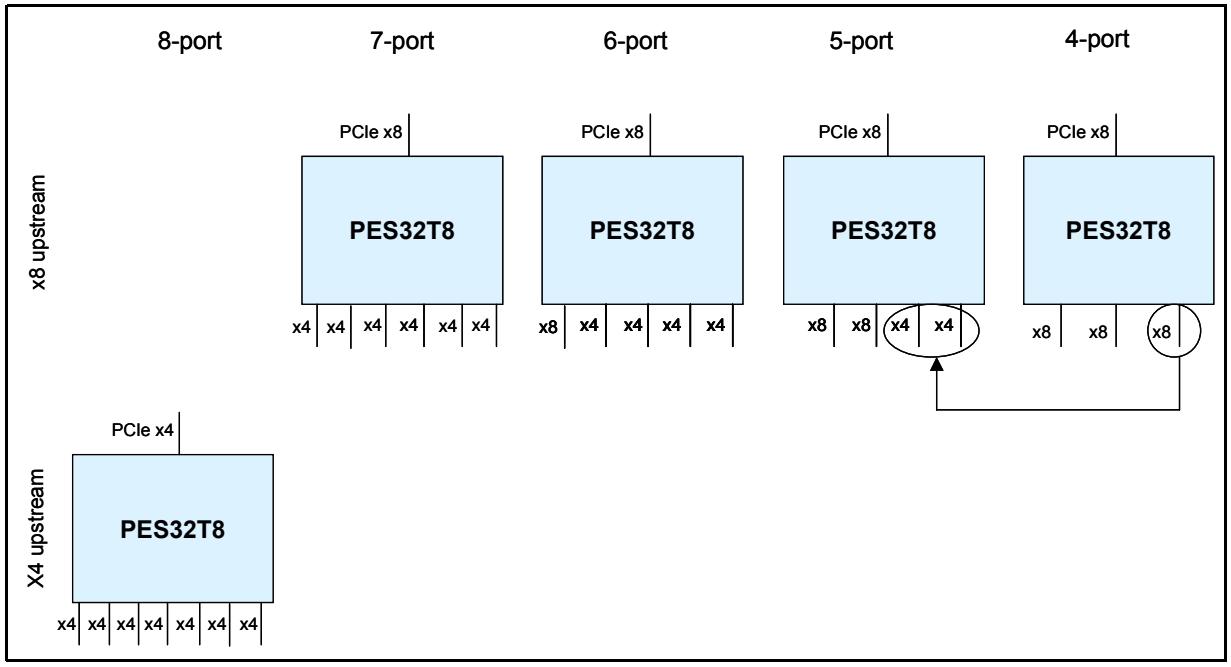


Figure 3 Configuration Options

Note: The configurations in the above diagram show the maximum port widths. The PES32T8 can negotiate to narrower port widths — x4, x2, or x1.

SMBus Interface

The PES32T8 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES32T8, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES32T8 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 4, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 4(a), the master and slave SMBuses are tied together and the PES32T8 acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES32T8 registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES32T8 may be configured to operate in a split configuration as shown in Figure 4(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES32T8 supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

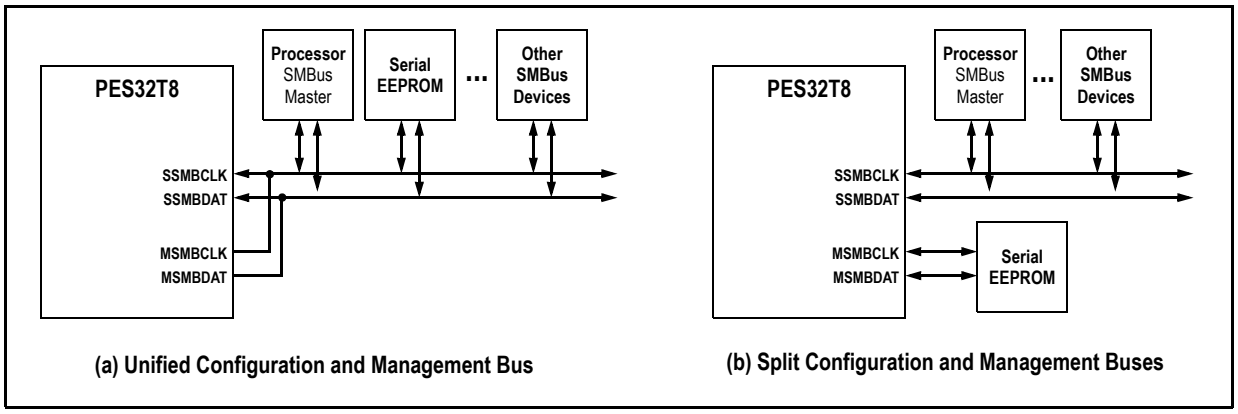


Figure 4 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES32T8 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES32T8 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES32T8 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES32T8. In response to an I/O expander interrupt, the PES32T8 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES32T8 provides 16 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables lists the functions of the pins provided on the PES32T8. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PE0RP[3:0] PE0RN[3:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0. Port 0 is the upstream port.
PE0TP[3:0] PE0TN[3:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0. Port 0 is the upstream port.
PE1RP[3:0] PE1RN[3:0]	I	**PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pairs for port 1. When port 0 is merged with port 1, these signals become port 0 receive pairs for lanes 4 through 7.
PE1TP[3:0] PE1TN[3:0]	O	**PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pairs for port 1. When port 0 is merged with port 1, these signals become port 0 transmit pairs for lanes 4 through 7.
PE2RP[3:0] PE2RN[3:0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE2TP[3:0] PE2TN[3:0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE3RP[3:0] PE3RN[3:0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pairs for port 3. When port 2 is merged with port 3, these signals become port 2 receive pairs for lanes 4 through 7.
PE3TP[3:0] PE3TN[3:0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pairs for port 3. When port 2 is merged with port 3, these signals become port 2 transmit pairs for lanes 4 through 7.
PE4RP[3:0] PE4RN[3:0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pairs for port 4.
PE4TP[3:0] PE4TN[3:0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pairs for port 4.
PE5RP[3:0] PE5RN[3:0]	I	**PCI Express Port 5 Serial Data Receive.** Differential PCI Express receive pairs for port 5. When port 4 is merged with port 5, these signals become port 4 receive pairs for lanes 4 through 7.
PE5TP[3:0] PE5TN[3:0]	O	**PCI Express Port 5 Serial Data Transmit.** Differential PCI Express transmit pairs for port 5. When port 4 is merged with port 5, these signals become port 4 transmit pairs for lanes 4 through 7.
PE6RP[3:0] PE6RN[3:0]	I	**PCI Express Port 6 Serial Data Receive.** Differential PCI Express receive pairs for port 6.
PE6TP[3:0] PE6TN[3:0]	O	**PCI Express Port 6 Serial Data Transmit.** Differential PCI Express transmit pairs for port 6.
PE7RP[3:0] PE7RN[3:0]	I	**PCI Express Port 7 Serial Data Receive.** Differential PCI Express receive pairs for port 7. When port 6 is merged with port 7, these signals become port 6 receive pairs for lanes 4 through 7.

Table 2 PCI Express Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
PE7TP[3:0] PE7TN[3:0]	O	**PCI Express Port 7 Serial Data Transmit.** Differential PCI Express transmit pairs for port 7. When port 6 is merged with port 7, these signals become port 6 transmit pairs for lanes 4 through 7.
PEREFCLKP[2:1] PEREFCLKN[2:1]	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM	I	**PCI Express Reference Clock Mode Select.** This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz

Table 2 PCI Express Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O Expander interrupt 0 input
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN1 Alternate function pin type: Input Alternate function: I/O Expander interrupt 1 input
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: I/O Expander interrupt 2 input
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN3 Alternate function pin type: Input Alternate function: I/O Expander interrupt 3 input
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: Reserved Alternate function pin type: Input Alternate function: Reserved
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output
GPIO[8]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P1RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 1
GPIO[9]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P3RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 3

Table 4 General Purpose I/O Pins (Part 1 of 2)

Signal	Type	Name/Description
GPIO[10]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P5RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 5
GPIO[11]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P6RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 6
GPIO[12]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P7RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 7
GPIO[13]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[14]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[15]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.

Table 4 General Purpose I/O Pins (Part 2 of 2)

Signal	Type	Name/Description
CCLKDS	I	**Common Clock Downstream.** When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port.
CCLKUS	I	**Common Clock Upstream.** When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port.
MSMBSMODE	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
P01MERGEN	I	**Port 0 and 1 Merge.** P01MERGEN is an active low signal. It is pulled low internally via a 251K ohm resistor. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port
P23MERGEN	I	**Port 2 and 3 Merge.** P23MERGEN is an active low signal. It is pulled low internally via a 251K ohm resistor. When this pin is low, port 2 is merged with port 3 to form a single x8 port. The Serdes lanes associated with port 3 become lanes 4 through 7 of port 2. When this pin is high, port 2 and port 3 are not merged, and each operates as a single x4 port.

Table 5 System Pins (Part 1 of 2)

Signal	Type	Name/Description
P45MERGEN	I	**Port 4 and 5 Merge.** P45MERGEN is an active low signal. It is pulled low internally via a 251K ohm resistor. When this pin is low, port 4 is merged with port 5 to form a single x8 port. The Serdes lanes associated with port 5 become lanes 4 through 7 of port 4. When this pin is high, port 4 and port 5 are not merged, and each operates as a single x4 port.
P67MERGEN	I	**Port 6 and 7 Merge.** P67MERGEN is an active low signal. It is pulled low internally via a 251K ohm resistor. When this pin is low, port 6 is merged with port 7 to form a single x8 port. The Serdes lanes associated with port 7 become lanes 4 through 7 of port 6. When this pin is high, port 6 and port 7 are not merged, and each operates as a single x4 port.
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside the PES32T8 and initiates a PCI Express fundamental reset.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, the PES32T8 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the PES32T8 switch operating mode. These pins should be static and not change after the negation of PERSTN. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 - through 0xF Reserved

Table 5 System Pins (Part 2 of 2)

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins

Signal	Type	Name/Description
V_{DD}CORE	I	**Core VDD.** Power supply for core logic.
V_{DD}IO	I	**I/O VDD.** LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power.** PCI Express digital power used by the digital power of the SerDes.
V_{DD}APE	I	**PCI Express Analog Power.** PCI Express analog power used by the PLL and bias generator.
V_{TT}PE	I	**PCI Express Serial Data Transmit Termination Voltage.**
V_{SS}	I	**Ground.**

Table 7 Power and Ground Pins

Pin Characteristics

Note: Some input pads of the PES32T8 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE0RN[3:0]	I	CML	Serial Link		
	PE0RP[3:0]	I				
	PE0TN[3:0]	O				
	PE0TP[3:0]	O				
	PE1RN[3:0]	I				
	PE1RP[3:0]	I				
	PE1TN[3:0]	O				
	PE1TP[3:0]	O				
	PE2RN[3:0]	I				
	PE2RP[3:0]	I				
	PE2TN[3:0]	O				
	PE2TP[3:0]	O				
	PE3RN[3:0]	I				
	PE3RP[3:0]	I				
	PE3TN[3:0]	O				
	PE3TP[3:0]	O				
	PE4RN[3:0]	I				
	PE4RP[3:0]	I				
	PE4TN[3:0]	O				
	PE4TP[3:0]	O				
	PE5RN[3:0]	I				
	PE5RP[3:0]	I				
	PE5TN[3:0]	O				
	PE5TP[3:0]	O				
	PE6RN[3:0]	I				
	PE6RP[3:0]	I				
	PE6TN[3:0]	O				
	PE6TP[3:0]	O				
	PE7RN[3:0]	I				
	PE7RP[3:0]	I				
	PE7TN[3:0]	O				
	PE7TP[3:0]	O				

Table 8 Pin Characteristics (Part 1 of 2)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface (cont.)	PEREFCLKN[2:1]	I	LVPECL/ CML	Diff. Clock Input		Refer to Table 9
	PEREFCLKP[2:1]	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-up	
	MSMBCLK	I/O		STI[2]		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[15:0]	I/O	LVTTL	High Drive	pull-up	
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	P01MERGEN	I			pull-down	
	P23MERGEN	I			pull-down	
	P45MERGEN	I			pull-down	
	P67MERGEN	I			pull-down	
	PERSTN	I				
	RSTHALT	I			pull-down	
	SWMODE[3:0]	I			pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	External pull-down

Table 8 Pin Characteristics (Part 2 of 2)

1. Internal resistor values under typical operating conditions are 54K Ω for pull-up and 251K Ω for pull-down.

2. Schmitt Trigger Input (STI).

Logic Diagram — PES32T8

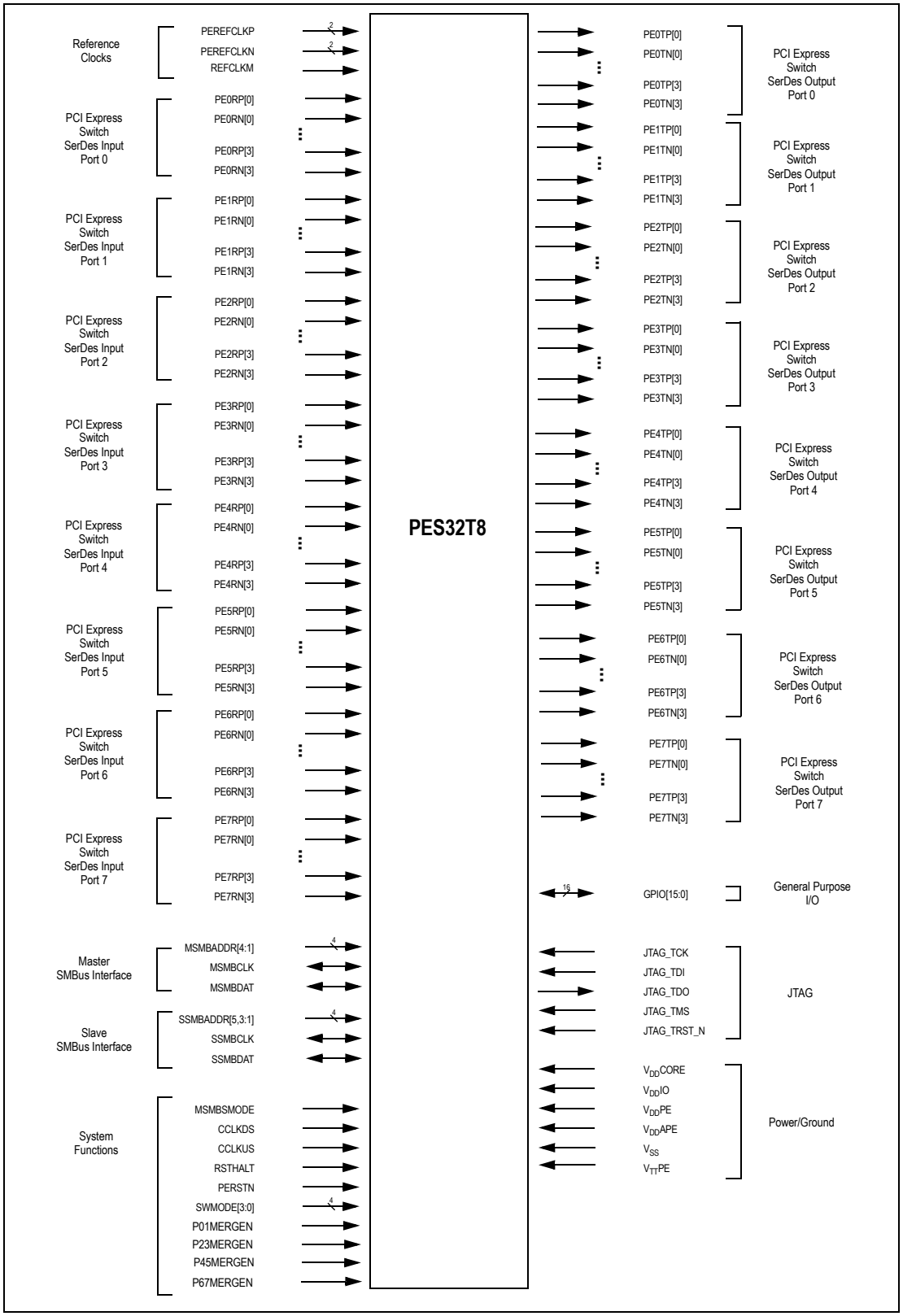


Figure 5 PES32T8 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 14.

Parameter	Description	Min	Typical	Max	Unit
PEREFCLK					
$Refclk_{FREQ}$	Input reference clock frequency range	100		125[1]	MHz
$Refclk_{DC}$[2]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[3]
V_{SW}	Differential input voltage swing[4]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps
R_T	Termination Resistor		110		Ohms

Table 9 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.
2. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
4. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
PCIe Transmit					
UI	Unit Interval	399.88	400	400.12	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.7	.9		UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+ / D- Tx output rise/fall time	50	90		ps
$T_{TX- IDLE-MIN}$	Minimum time in idle	50			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			20	UI
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
PCIe Receive					
UI	Unit Interval	399.88	400	400.12	ps
T_{RX-EYE} (with jitter)	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI
$T_{RX-EYE-MEDIUM TO MAX JITTER}$	Max time between jitter median & max deviation			0.3	UI
$T_{RX-IDLE-DET-DIFF-ENTER TIME}$	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
$T_{RX-SKEW}$	Lane to lane input skew			20	ns

Table 10 PCIe AC Timing Characteristics

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[15:0][1]	Tpw_13b[2]	None	50	—	ns	See Figure 6.

Table 11 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

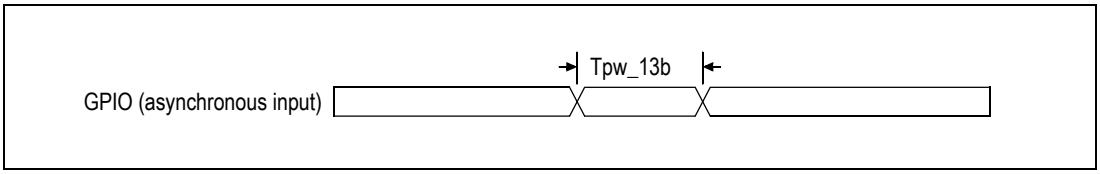


Figure 6 GPIO AC Timing Waveform

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 7.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

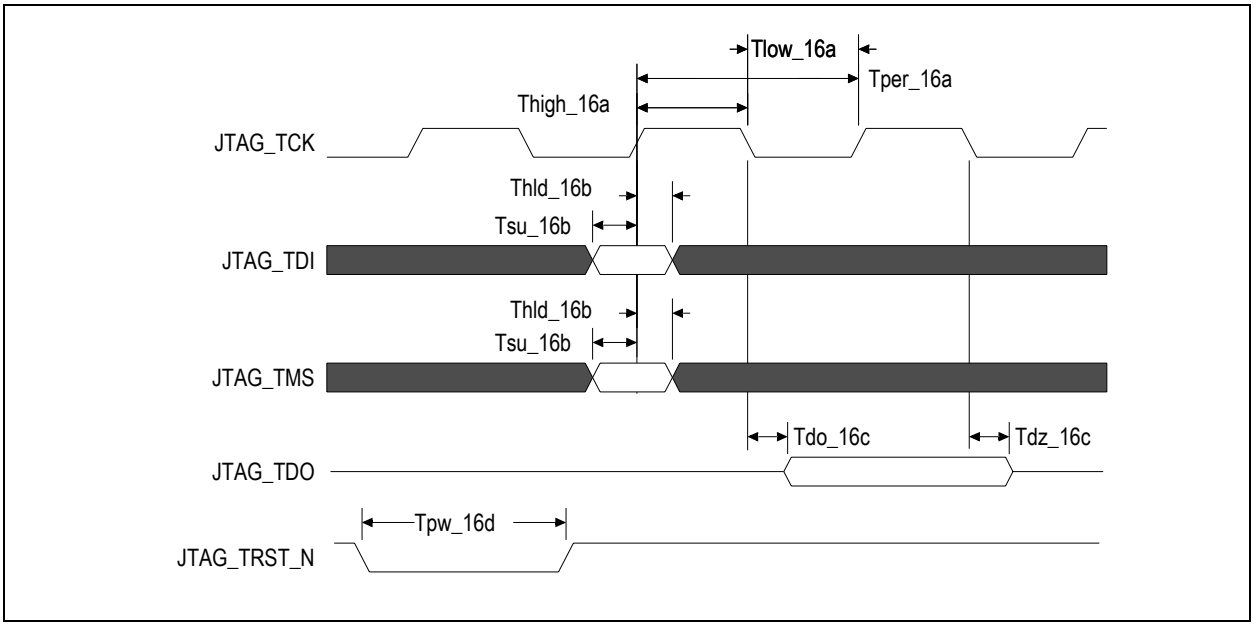


Figure 7 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.0	3.3	3.6	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}APE	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES32T8 Operating Voltages

Power-Up Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES32T8, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels. The power-down sequence must be in the reverse order of the power-up sequence.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient

Table 14 PES32T8 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Digital Supply		PCIe Analog Supply		PCIe Termination Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.5V	Max 1.575V	Typ 3.3V	Max 3.6V	Typ Power	Max Power
8/8/8/4/4 or 8/8/8/8	mA	888	1014	1499	1660	611	627	763	832	1	1	4.1W	5.0W
	Watts	0.89	1.15	1.5	1.83	0.61	0.69	1.14	1.31	0.004	0.004		
8/8/4/4/4	mA	800	973	1284	1471	556	590	613	697	1	1	3.56W	4.4W
	Watts	0.8	1.07	1.28	1.61	0.56	0.65	0.92	1.1	0.003	0.003		

Table 15 PES32T8 Power Consumption

Thermal Considerations

This section describes thermal considerations for the PES32T8 (31mm^2 BXG500 package). The data in Table 16 below contains information that is relevant to the thermal performance of the PES32T8 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum for commercial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	9.3	°C/W	Zero air flow
		7.6	°C/W	1 m/S air flow
		6.8	°C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	6	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.7	°C/W	
P	Power Dissipation of the Device	5.0	Watts	Maximum

Table 16 Thermal Specifications for PES32T8, 31x31 mm BXG500 Package

Note: Parameter $\theta_{JA(eff)}$ is not the *absolute* thermal resistance for the package as defined by JEDEC (JESD-51). Because resistance can vary with the number of board layers, size of the board, and airflow, $\theta_{JA(eff)}$ is the *effective* thermal resistance. The values for effective θ_{JA} given above are based on a 10-layer, standard height, full length (4.3"x12.2") PCIe add-in card.

Heat Sink

Table 17 lists heat sink requirements for the PES32T8 under three common usage scenarios. As shown in this table, a heat sink is not required in most cases.

Air Flow	Board Size	Board Layers	Heat Sink Requirement
Zero	4.3"x6.6" (PCIe standard height, half length form factor)	10 or more	No heat sink required
Zero	3.9"x6.2" (ExpressModule form factor)	14 or more	No heat sink required
1 m/S or more	Any	Any	No heat sink required

Table 17 Heat Sink Requirements Based on Air Flow and Board Characteristics

Thermal Usage Examples

The junction-to-ambient thermal resistance is a measure of a device's ability to dissipate heat from the die to its surroundings in the absence of a heat sink. The general formula to determine θ_{JA} is:

$$\theta_{JA} = (T_J - T_A)/P$$

Thermal reliability of a device is generally assured when the actual value of T_J in the specific system environment being considered is less than the maximum T_J specified for the device. Using an ambient temperature of 70°C and assuming a system with 1m/S airflow, the actual value of T_J is:

$$T_{J(actual)} = T_A + P * \theta_{JA(eff)} = 70^oC + 5.0W * 7.6W/^oC = 108^oC$$

The actual T_J of 108°C is well below the maximum T_J of 125°C specified for the device (shown in Table 16). Therefore, no heat sink is needed in this scenario. The formula is also useful from a system design perspective. It can be used to determine if a heat sink should be added to the device based on some desired value of T_J. For example, if for reliability purposes the desired T_J is 100°C, then the maximum allowable T_A is:

$$T_{A(allowed)} = T_{J(desired)} - (P * \theta_{JA(effective)})$$
$$T_{A(allowed)} = 100^oC - (5.0W * 7.6W/^oC) = 100^oC - 38^oC = 62^oC$$

An appropriate level of increased air flow and/or a heat sink can be added to achieve this lower ambient temperature. Please contact ssdhelp@idt.com for further assistance.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	**PCIe Transmit**						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	
	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
	PCIe Receive						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	

Table 18 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}IO$ + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}IO$ + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	$V_{DD}I/O$ (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	$V_{DD}I/O$ (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	$V_{DD}I/O$ (max)

Table 18 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1.

Package Pinout — 500-BGA Signal Pinout for PES32T8

The following table lists the pin numbers and signal names for the PES32T8 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B5	V_{SS}		C9	V_{SS}		D13	V_{SS}	
A2	V_{DD}CORE		B6	V_{SS}		C10	V_{DD}PE		D14	PE6RN03	
A3	V_{SS}		B7	V_{DD}APE		C11	V_{TT}PE		D15	V_{SS}	
A4	V_{DD}CORE		B8	PE6TP00		C12	V_{DD}PE		D16	PE7RN00	
A5	V_{SS}		B9	V_{SS}		C13	V_{SS}		D17	V_{SS}	
A6	V_{DD}CORE		B10	PE6TP01		C14	V_{DD}PE		D18	PE7RN01	
A7	V_{SS}		B11	V_{DD}APE		C15	V_{TT}PE		D19	V_{SS}	
A8	PE6TN00		B12	PE6TP02		C16	V_{DD}PE		D20	PE7RN02	
A9	V_{DD}APE		B13	V_{SS}		C17	V_{SS}		D21	V_{SS}	
A10	PE6TN01		B14	PE6TP03		C18	V_{DD}PE		D22	PE7RN03	
A11	V_{SS}		B15	V_{DD}APE		C19	V_{TT}PE		D23	V_{SS}	
A12	PE6TN02		B16	PE7TP00		C20	V_{DD}PE		D24	MSMBSMODE	
A13	V_{SS}		B17	V_{SS}		C21	V_{SS}		D25	GPIO_15	
A14	PE6TN03		B18	PE7TP01		C22	V_{DD}PE		D26	GPIO_11	1
A15	V_{SS}		B19	V_{DD}APE		C23	V_{SS}		D27	V_{SS}	
A16	PE7TN00		B20	PE7TP02		C24	REFCLKM		D28	V_{DD}CORE	
A17	V_{SS}		B21	V_{SS}		C25	V_{SS}		D29	V_{SS}	
A18	PE7TN01		B22	PE7TP03		C26	GPIO_12	1	D30	V_{DD}CORE	
A19	V_{SS}		B23	V_{SS}		C27	GPIO_09	1	E1	V_{SS}	
A20	PE7TN02		B24	V_{SS}		C28	V_{DD}CORE		E2	V_{DD}CORE	
A21	V_{DD}APE		B25	V_{DD}CORE		C29	V_{SS}		E3	P01MERGEN	
A22	PE7TN03		B26	GPIO_14		C30	V_{SS}		E4	P23MERGEN	
A23	V_{SS}		B27	V_{SS}		D1	V_{DD}CORE		E5	P45MERGEN	
A24	V_{DD}APE		B28	V_{SS}		D2	V_{DD}IO		E6	P67MERGEN	
A25	V_{DD}IO		B29	V_{DD}CORE		D3	V_{SS}		E7	V_{SS}	
A26	V_{SS}		B30	V_{SS}		D4	V_{DD}IO		E8	PE6RP00	
A27	V_{DD}IO		C1	V_{SS}		D5	V_{SS}		E9	V_{SS}	
A28	V_{DD}IO		C2	V_{DD}CORE		D6	V_{DD}IO		E10	PE6RP01	
A29	V_{DD}CORE		C3	V_{SS}		D7	V_{SS}		E11	V_{DD}CORE	
A30	V_{SS}		C4	V_{DD}CORE		D8	PE6RN00		E12	PE6RP02	
B1	V_{SS}		C5	V_{SS}		D9	V_{SS}		E13	V_{SS}	
B2	V_{DD}CORE		C6	V_{DD}CORE		D10	PE6RN01		E14	PE6RP03	
B3	V_{SS}		C7	V_{TT}PE		D11	V_{SS}		E15	V_{DD}CORE	
B4	V_{DD}CORE		C8	V_{DD}PE		D12	PE6RN02		E16	PE7RP00	

Table 19 PES32T8 500-pin Signal Pin-Out (Part 1 of 4)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
E17	V_{SS}		H4	V_{SS}		M1	V_{SS}		R28	V_{DD}PE	
E18	PE7RP01		H5	V_{DD}CORE		M2	V_{DD}APE		R29	PE4TP03	
E19	V_{DD}CORE		H26	V_{SS}		M3	V_{TT}PE		R30	PE4TN03	
E20	PE7RP02		H27	V_{SS}		M4	V_{SS}		T1	V_{SS}	
E21	V_{SS}		H28	V_{TT}PE		M5	V_{DD}CORE		T2	V_{DD}APE	
E22	PE7RP03		H29	V_{DD}APE		M26	V_{DD}CORE		T3	V_{TT}PE	
E23	V_{SS}		H30	V_{SS}		M27	V_{SS}		T4	V_{SS}	
E24	V_{DD}CORE		J1	PE3TN03		M28	V_{TT}PE		T5	V_{DD}CORE	
E25	GPIO_13		J2	PE3TP03		M29	V_{DD}APE		T26	V_{DD}CORE	
E26	GPIO_10	1	J3	V_{DD}PE		M30	V_{SS}		T27	V_{SS}	
E27	GPIO_08	1	J4	PE3RN03		N1	PE3TN01		T28	V_{TT}PE	
E28	V_{SS}		J5	PE3RP03		N2	PE3TP01		T29	V_{DD}APE	
E29	V_{DD}IO		J26	PE4RP00		N3	V_{DD}PE		T30	V_{SS}	
E30	V_{SS}		J27	PE4RN00		N4	PE3RN01		U1	PE2TN03	
F1	PEREFCLKN1		J28	V_{DD}PE		N5	PE3RP01		U2	PE2TP03	
F2	V_{SS}		J29	PE4TP00		N26	PE4RP02		U3	V_{DD}PE	
F3	V_{DD}CORE		J30	PE4TN00		N27	PE4RN02		U4	PE2RN03	
F4	V_{SS}		K1	V_{DD}APE		N28	V_{DD}PE		U5	PE2RP03	
F5	V_{DD}IO		K2	V_{SS}		N29	PE4TP02		U26	PE5RP00	
F26	V_{SS}		K3	V_{SS}		N30	PE4TN02		U27	PE5RN00	
F27	V_{DD}CORE		K4	V_{SS}		P1	V_{SS}		U28	V_{DD}PE	
F28	V_{DD}CORE		K5	V_{SS}		P2	V_{SS}		U29	PE5TP00	
F29	V_{SS}		K26	V_{SS}		P3	V_{SS}		U30	PE5TN00	
F30	PEREFCLKP2		K27	V_{SS}		P4	V_{SS}		V1	V_{SS}	
G1	PEREFCLKP1		K28	V_{SS}		P5	V_{SS}		V2	V_{SS}	
G2	V_{SS}		K29	V_{SS}		P26	V_{SS}		V3	V_{SS}	
G3	V_{SS}		K30	V_{DD}APE		P27	V_{SS}		V4	V_{SS}	
G4	V_{SS}		L1	PE3TN02		P28	V_{SS}		V5	V_{SS}	
G5	V_{SS}		L2	PE3TP02		P29	V_{SS}		V26	V_{SS}	
G26	V_{SS}		L3	V_{DD}PE		P30	V_{SS}		V27	V_{SS}	
G27	V_{SS}		L4	PE3RN02		R1	PE3TN00		V28	V_{SS}	
G28	V_{SS}		L5	PE3RP02		R2	PE3TP00		V29	V_{SS}	
G29	V_{SS}		L26	PE4RP01		R3	V_{DD}PE		V30	V_{SS}	
G30	PEREFCLKN2		L27	PE4RN01		R4	PE3RN00		W1	PE2TN02	
H1	V_{SS}		L28	V_{DD}PE		R5	PE3RP00		W2	PE2TP02	
H2	V_{DD}APE		L29	PE4TP01		R26	PE4RP03		W3	V_{DD}PE	
H3	V_{TT}PE		L30	PE4TN01		R27	PE4RN03		W4	PE2RN02	

Table 19 PES32T8 500-pin Signal Pin-Out (Part 2 of 4)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
W5	PE2RP02		AC2	PE2TP00		AF9	PE1RP03		AG16	V_{SS}	
W26	PE5RP01		AC3	V_{DD}PE		AF10	V_{SS}		AG17	PE0RN03	
W27	PE5RN01		AC4	PE2RN00		AF11	PE1RP02		AG18	V_{SS}	
W28	V_{DD}PE		AC5	PE2RP00		AF12	V_{DD}CORE		AG19	PE0RN02	
W29	PE5TP01		AC26	PE5RP03		AF13	PE1RP01		AG20	V_{SS}	
W30	PE5TN01		AC27	PE5RN03		AF14	V_{SS}		AG21	PE0RN01	
Y1	V_{SS}		AC28	V_{DD}PE		AF15	PE1RP00		AG22	V_{SS}	
Y2	V_{DD}APE		AC29	PE5TP03		AF16	V_{DD}CORE		AG23	PE0RN00	
Y3	V_{TT}PE		AC30	PE5TN03		AF17	PE0RP03		AG24	V_{SS}	
Y4	V_{SS}		AD1	V_{SS}		AF18	V_{SS}		AG25	SWMODE_3	
Y5	V_{DD}CORE		AD2	V_{DD}APE		AF19	PE0RP02		AG26	V_{SS}	
Y26	V_{DD}CORE		AD3	V_{DD}IO		AF20	V_{DD}CORE		AG27	GPIO_04	1
Y27	V_{SS}		AD4	V_{DD}IO		AF21	PE0RP01		AG28	V_{DD}CORE	
Y28	V_{TT}PE		AD5	JTAG_TCK		AF22	V_{SS}		AG29	V_{SS}	
Y29	V_{DD}APE		AD26	GPIO_07	1	AF23	PE0RP00		AG30	V_{DD}CORE	
Y30	V_{SS}		AD27	V_{SS}		AF24	CCLKDS		AH1	V_{DD}CORE	
AA1	PE2TN01		AD28	V_{SS}		AF25	SWMODE_2		AH2	V_{SS}	
AA2	PE2TP01		AD29	V_{DD}APE		AF26	GPIO_00	1	AH3	JTAG_TMS	
AA3	V_{DD}PE		AD30	V_{SS}		AF27	GPIO_05	1	AH4	MSMBADDR_3	
AA4	PE2RN01		AE1	V_{DD}CORE		AF28	V_{SS}		AH5	MSMBDAT	
AA5	PE2RP01		AE2	V_{SS}		AF29	V_{DD}IO		AH6	SSMBADDR_3	
AA26	PE5RP02		AE3	V_{SS}		AF30	V_{SS}		AH7	CCLKUS	
AA27	PE5RN02		AE4	JTAG_TDI		AG1	V_{SS}		AH8	V_{DD}PE	
AA28	V_{DD}PE		AE5	JTAG_TRST_N		AG2	V_{DD}CORE		AH9	V_{DD}PE	
AA29	PE5TP02		AE26	GPIO_03	1	AG3	JTAG_TDO		AH10	V_{SS}	
AA30	PE5TN02		AE27	GPIO_06		AG4	MSMBADDR_2		AH11	V_{DD}PE	
AB1	V_{DD}APE		AE28	V_{DD}IO		AG5	V_{SS}		AH12	V_{TT}PE	
AB2	V_{SS}		AE29	V_{SS}		AG6	SSMBADDR_2		AH13	V_{DD}PE	
AB3	V_{SS}		AE30	V_{DD}CORE		AG7	SSMBDAT		AH14	V_{SS}	
AB4	V_{SS}		AF1	V_{SS}		AG8	V_{SS}		AH15	V_{DD}PE	
AB5	V_{SS}		AF2	V_{DD}CORE		AG9	PE1RN03		AH16	V_{TT}PE	
AB26	V_{SS}		AF3	V_{SS}		AG10	V_{SS}		AH17	V_{DD}PE	
AB27	V_{SS}		AF4	MSMBADDR_1		AG11	PE1RN02		AH18	V_{SS}	
AB28	V_{SS}		AF5	MSMBADDR_4		AG12	V_{SS}		AH19	V_{DD}PE	
AB29	V_{SS}		AF6	SSMBADDR_1		AG13	PE1RN01		AH20	V_{TT}PE	
AB30	V_{DD}APE		AF7	SSMBCLK		AG14	V_{SS}		AH21	V_{DD}PE	
AC1	PE2TN00		AF8	V_{SS}		AG15	PE1RN00		AH22	V_{SS}	

Table 19 PES32T8 500-pin Signal Pin-Out (Part 3 of 4)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
AH23	V_{DD}PE		AJ10	V_{SS}		AJ27	GPIO_01	1	AK14	V_{SS}	
AH24	V_{TT}PE		AJ11	PE1TP02		AJ28	V_{SS}		AK15	PE1TN00	
AH25	SWMODE_1		AJ12	V_{DD}APE		AJ29	V_{DD}CORE		AK16	V_{SS}	
AH26	RSTHALT		AJ13	PE1TP01		AJ30	V_{SS}		AK17	PE0TN03	
AH27	GPIO_02	1	AJ14	V_{SS}		AK1	V_{SS}		AK18	V_{SS}	
AH28	V_{DD}CORE		AJ15	PE1TP00		AK2	V_{DD}CORE		AK19	PE0TN02	
AH29	V_{SS}		AJ16	V_{DD}APE		AK3	V_{SS}		AK20	V_{SS}	
AH30	V_{DD}CORE		AJ17	PE0TP03		AK4	V_{DD}CORE		AK21	PE0TN01	
AJ1	V_{SS}		AJ18	V_{SS}		AK5	V_{SS}		AK22	V_{DD}APE	
AJ2	V_{DD}IO		AJ19	PE0TP02		AK6	V_{DD}CORE		AK23	PE0TN00	
AJ3	V_{SS}		AJ20	V_{DD}APE		AK7	V_{SS}		AK24	V_{SS}	
AJ4	MSMBCLK		AJ21	PE0TP01		AK8	V_{DD}APE		AK25	V_{DD}IO	
AJ5	V_{DD}IO		AJ22	V_{SS}		AK9	PE1TN03		AK26	V_{SS}	
AJ6	SSMBADDR_5		AJ23	PE0TP00		AK10	V_{DD}APE		AK27	V_{DD}IO	
AJ7	V_{SS}		AJ24	V_{DD}APE		AK11	PE1TN02		AK28	V_{SS}	
AJ8	V_{DD}CORE		AJ25	SWMODE_0		AK12	V_{SS}		AK29	V_{DD}CORE	
AJ9	PE1TP03		AJ26	PERSTN		AK13	PE1TN01		AK30	V_{SS}	

Table 19 PES32T8 500-pin Signal Pin-Out (Part 4 of 4)

Alternate Signal Functions

Pin	GPIO	Alternate	Pin	GPIO	Alternate
AF26	GPIO_00	P2RSTN	AD26	GPIO_07	GPEN
AJ27	GPIO_01	P4RSTN	E27	GPIO_08	P1RSTN
AH27	GPIO_02	IOEXPINTN0	C27	GPIO_09	P3RSTN
AE26	GPIO_03	IOEXPINTN1	E26	GPIO_10	P5RSTN
AG27	GPIO_04	IOEXPINTN2	D26	GPIO_11	P6RSTN
AF27	GPIO_05	IOEXPINTN3	C26	GPIO_12	P7RSTN

Table 20 PES32T8 Alternate Signal Functions

Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}IO	V_{DD}PE	V_{DD}PE	V_{DD}APE	V_{TT}PE
A2	Y26	A25	C8	AH17	A9	C7
A4	AE1	A27	C10	AH19	A21	C11
A6	AE30	A28	C12	AH21	A24	C15
A29	AF2	D2	C14	AH23	B7	C19
B2	AF12	D4	C16		B11	H3
B4	AF16	D6	C18		B15	H28
B25	AF20	E29	C20		B19	M3
B29	AG2	F5	C22		H2	M28
C2	AG28	AD3	J3		H29	T3
C4	AG30	AD4	J28		K1	T28
C6	AH1	AE28	L3		K30	Y3
C28	AH28	AF29	L28		M2	Y28
D1	AH30	AJ2	N3		M29	AH12
D28	AJ8	AJ5	N28		T2	AH16
D30	AJ29	AK25	R3		T29	AH20
E2	AK2	AK27	R28		Y2	AH24
E11	AK4		U3		Y29	
E15	AK6		U28		AB1	
E19	AK29		W3		AB30	
E24			W28		AD2	
F3			AA3		AD29	
F27			AA28		AJ12	
F28			AC3		AJ16	
H5			AC28		AJ20	
M5			AH8		AJ24	
M26			AH9		AK8	
T5			AH11		AK10	
T26			AH13		AK22	
Y5			AH15			

Table 21 PES32T8 Power Pins

Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	C17	F26	P4	AB27	AG26
A3	C21	F29	P5	AB28	AG29
A5	C23	G2	P26	AB29	AH2
A7	C25	G3	P27	AD1	AH10
A11	C29	G4	P28	AD27	AH14
A13	C30	G5	P29	AD28	AH18
A15	D3	G26	P30	AD30	AH22
A17	D5	G27	T1	AE2	AH29
A19	D7	G28	T4	AE3	AJ1
A23	D9	G29	T27	AE29	AJ3
A26	D11	H1	T30	AF1	AJ7
A30	D13	H4	V1	AF3	AJ10
B1	D15	H26	V2	AF8	AJ14
B3	D17	H27	V3	AF10	AJ18
B5	D19	H30	V4	AF14	AJ22
B6	D21	K2	V5	AF18	AJ28
B9	D23	K3	V26	AF22	AJ30
B13	D27	K4	V27	AF28	AK1
B17	D29	K5	V28	AF30	AK3
B21	E1	K26	V29	AG1	AK5
B23	E7	K27	V30	AG5	AK7
B24	E9	K28	Y1	AG8	AK12
B27	E13	K29	Y4	AG10	AK14
B28	E17	M1	Y27	AG12	AK16
B30	E21	M4	Y30	AG14	AK18
C1	E23	M27	AB2	AG16	AK20
C3	E28	M30	AB3	AG18	AK24
C5	E30	P1	AB4	AG20	AK26
C9	F2	P2	AB5	AG22	AK28
C13	F4	P3	AB26	AG24	AK30

Table 22 PES32T8 Ground Pins

Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	AF24	System
CCLKUS	I	AH7	
GPIO_00	I/O	AF26	General Purpose I/O
GPIO_01	I/O	AJ27	
GPIO_02	I/O	AH27	
GPIO_03	I/O	AE26	
GPIO_04	I/O	AG27	
GPIO_05	I/O	AF27	
GPIO_06	I/O	AE27	
GPIO_07	I/O	AD26	
GPIO_08	I/O	E27	
GPIO_09	I/O	C27	
GPIO_10	I/O	E26	
GPIO_11	I/O	D26	
GPIO_12	I/O	C26	
GPIO_13	I/O	E25	
GPIO_14	I/O	B26	
GPIO_15	I/O	D25	
JTAG_TCK	I	AD5	Test
JTAG_TDI	I	AE4	
JTAG_TDO	O	AG3	
JTAG_TMS	I	AH3	
JTAG_TRST_N	I	AE5	
MSMBADDR_1	I	AF4	SMBus Interface
MSMBADDR_2	I	AG4	
MSMBADDR_3	I	AH4	
MSMBADDR_4	I	AF5	
MSMBCLK	I/O	AJ4	
MSMBDAT	I/O	AH5	
MSMBSMODE	I	D24	System
P01MERGEN	I	E3	
P23MERGEN	I	E4	
P45MERGEN	I	E5	
P67MERGEN	I	E6	

Table 23 89PES32T8 Alphabetical Signal List (Part 1 of 6)

Signal Name	I/O Type	Location	Signal Category
PE0RN00	I	AG23	PCI Express
PE0RN01	I	AG21	
PE0RN02	I	AG19	
PE0RN03	I	AG17	
PE0RP00	I	AF23	
PE0RP01	I	AF21	
PE0RP02	I	AF19	
PE0RP03	I	AF17	
PE0TN00	O	AK23	
PE0TN01	O	AK21	
PE0TN02	O	AK19	
PE0TN03	O	AK17	
PE0TP00	O	AJ23	
PE0TP01	O	AJ21	
PE0TP02	O	AJ19	
PE0TP03	O	AJ17	
PE1RN00	I	AG15	
PE1RN01	I	AG13	
PE1RN02	I	AG11	
PE1RN03	I	AG9	
PE1RP00	I	AF15	
PE1RP01	I	AF13	
PE1RP02	I	AF11	
PE1RP03	I	AF9	
PE1TN00	O	AK15	
PE1TN01	O	AK13	
PE1TN02	O	AK11	
PE1TN03	O	AK9	
PE1TP00	O	AJ15	
PE1TP01	O	AJ13	
PE1TP02	O	AJ11	
PE1TP03	O	AJ9	
PE2RN00	I	AC4	
PE2RN01	I	AA4	
PE2RN02	I	W4	
PE2RN03	I	U4	

Table 23 89PES32T8 Alphabetical Signal List (Part 2 of 6)

Signal Name	I/O Type	Location	Signal Category
PE2RP00	I	AC5	PCI Express (cont.)
PE2RP01	I	AA5	
PE2RP02	I	W5	
PE2RP03	I	U5	
PE2TN00	O	AC1	
PE2TN01	O	AA1	
PE2TN02	O	W1	
PE2TN03	O	U1	
PE2TP00	O	AC2	
PE2TP01	O	AA2	
PE2TP02	O	W2	
PE2TP03	O	U2	
PE3RN00	I	R4	
PE3RN01	I	N4	
PE3RN02	I	L4	
PE3RN03	I	J4	
PE3RP00	I	R5	
PE3RP01	I	N5	
PE3RP02	I	L5	
PE3RP03	I	J5	
PE3TN00	O	R1	
PE3TN01	O	N1	
PE3TN02	O	L1	
PE3TN03	O	J1	
PE3TP00	O	R2	
PE3TP01	O	N2	
PE3TP02	O	L2	
PE3TP03	O	J2	
PE4RN00	I	J27	
PE4RN01	I	L27	
PE4RN02	I	N27	
PE4RN03	I	R27	
PE4RP00	I	J26	
PE4RP01	I	L26	
PE4RP02	I	N26	
PE4RP03	I	R26	

Table 23 89PES32T8 Alphabetical Signal List (Part 3 of 6)

Signal Name	I/O Type	Location	Signal Category
PE4TN00	O	J30	PCI Express (cont.)
PE4TN01	O	L30	
PE4TN02	O	N30	
PE4TN03	O	R30	
PE4TP00	O	J29	
PE4TP01	O	L29	
PE4TP02	O	N29	
PE4TP03	O	R29	
PE5RN00	I	U27	
PE5RN01	I	W27	
PE5RN02	I	AA27	
PE5RN03	I	AC27	
PE5RP00	I	U26	
PE5RP01	I	W26	
PE5RP02	I	AA26	
PE5RP03	I	AC26	
PE5TN00	O	U30	
PE5TN01	O	W30	
PE5TN02	O	AA30	
PE5TN03	O	AC30	
PE5TP00	O	U29	
PE5TP01	O	W29	
PE5TP02	O	AA29	
PE5TP03	O	AC29	
PE6RN00	I	D8	
PE6RN01	I	D10	
PE6RN02	I	D12	
PE6RN03	I	D14	
PE6RP00		E8	
PE6RP01	II	E10	
PE6RP02	I	E12	
PE6RP03	I	E14	
PE6TN00	O	A8	
PE6TN01	O	A10	
PE6TN02	O	A12	
PE6TN03	O	A14	

Table 23 89PES32T8 Alphabetical Signal List (Part 4 of 6)

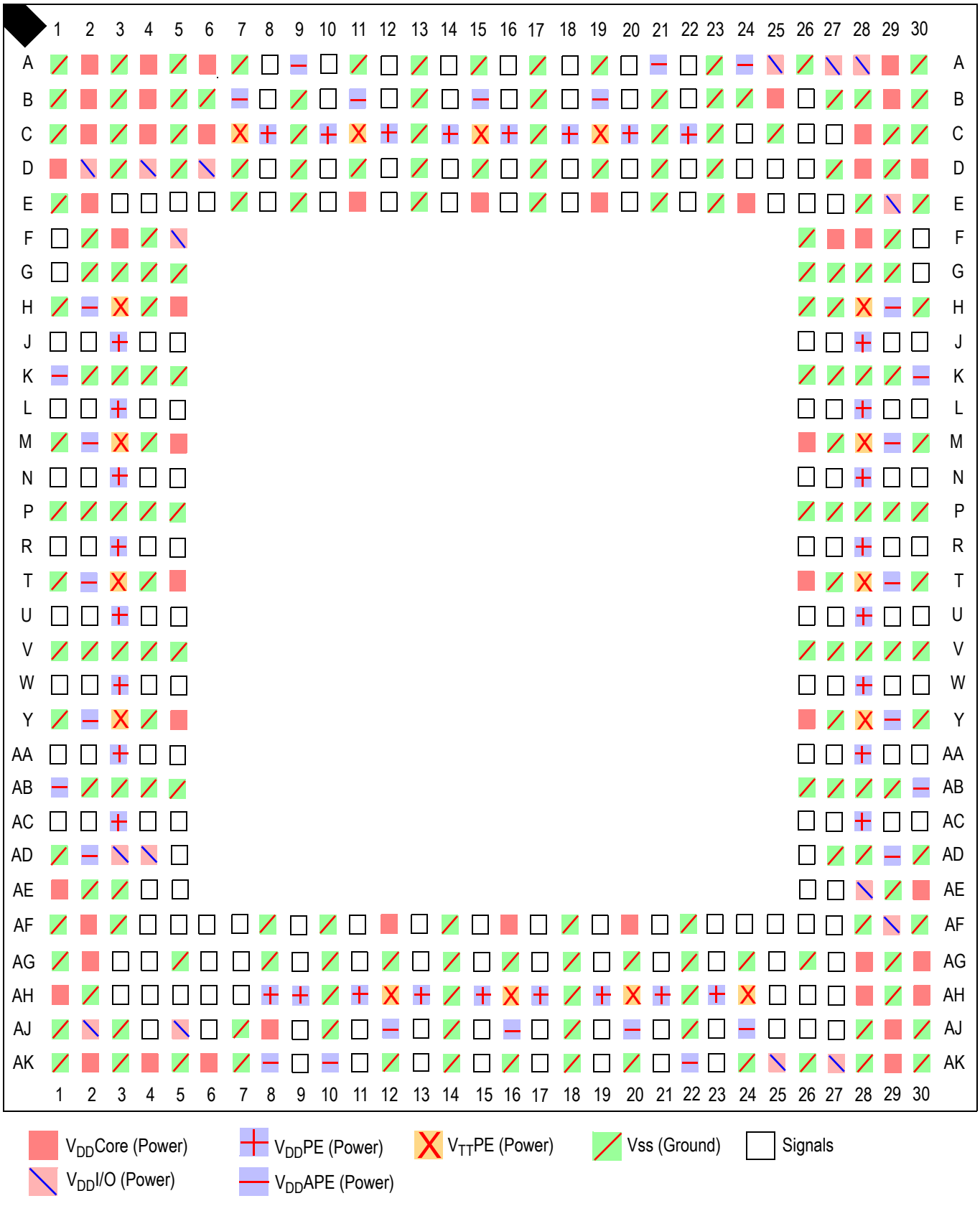
Signal Name	I/O Type	Location	Signal Category
PE6TP00	O	B8	PCI Express (cont.)
PE6TP01	O	B10	
PE6TP02	O	B12	
PE6TP03	O	B14	
PE7RN00	I	D16	
PE7RN01	I	D18	
PE7RN02	I	D20	
PE7RN03	I	D22	
PE7RP00	I	E16	
PE7RP01	I	E18	
PE7RP02	I	E20	
PE7RP03	I	E22	
PE7TN00	O	A16	
PE7TN01	O	A18	
PE7TN02	O	A20	
PE7TN03	O	A22	
PE7TP00	O	B16	
PE7TP01	O	B18	
PE7TP02	O	B20	
PE7TP03	O	B22	
PEREFCLKN1	I	F1	
PEREFCLKN2	I	G30	
PEREFCLKP1	I	G1	
PEREFCLKP2	I	F30	
PERSTN	I	AJ26	System
REFCLKM	I	C24	PCI Express
RSTHALT	I	AH26	System
SSMBADDR_1	I	AF6	SMBus Interface
SSMBADDR_2	I	AG6	
SSMBADDR_3	I	AH6	
SSMBADDR_5	I	AJ6	
SSMBCLK	I/0	AF7	
SSMBDAT	I/O	AG7	

Table 23 89PES32T8 Alphabetical Signal List (Part 5 of 6)

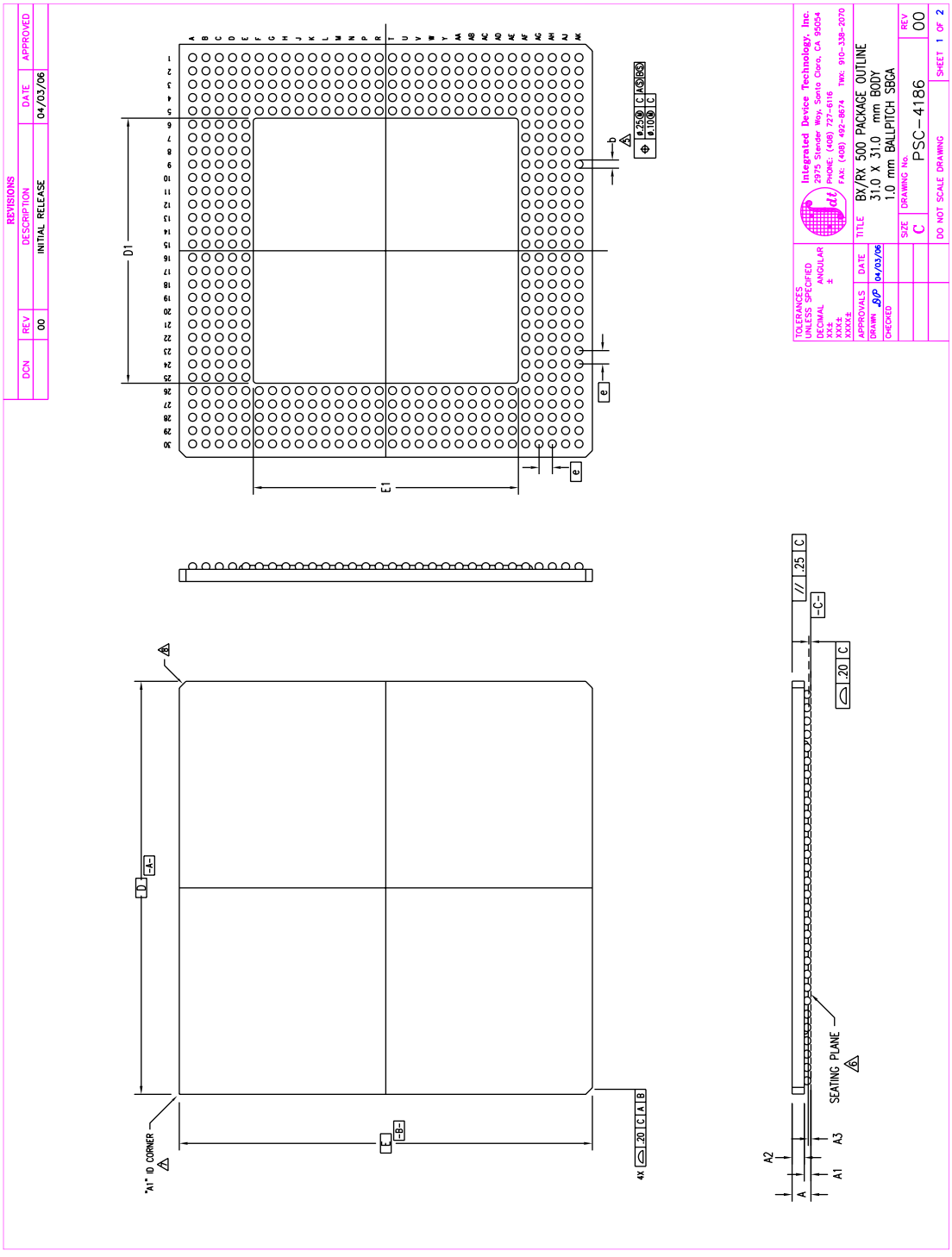
Signal Name	I/O Type	Location	Signal Category
SWMODE_0	I	AJ25	System
SWMODE_1	I	AH25	
SWMODE_2	I	AF25	
SWMODE_3	I	AG25	
V_{DD}CORE, V_{DD}APE, V_{DD}IO, V_{DD}PE, V_{TT}PE	See Table 21 for a listing of power pins.		
V_{SS}	See Table 22 for a listing of ground pins.		

Table 23 89PES32T8 Alphabetical Signal List (Part 6 of 6)

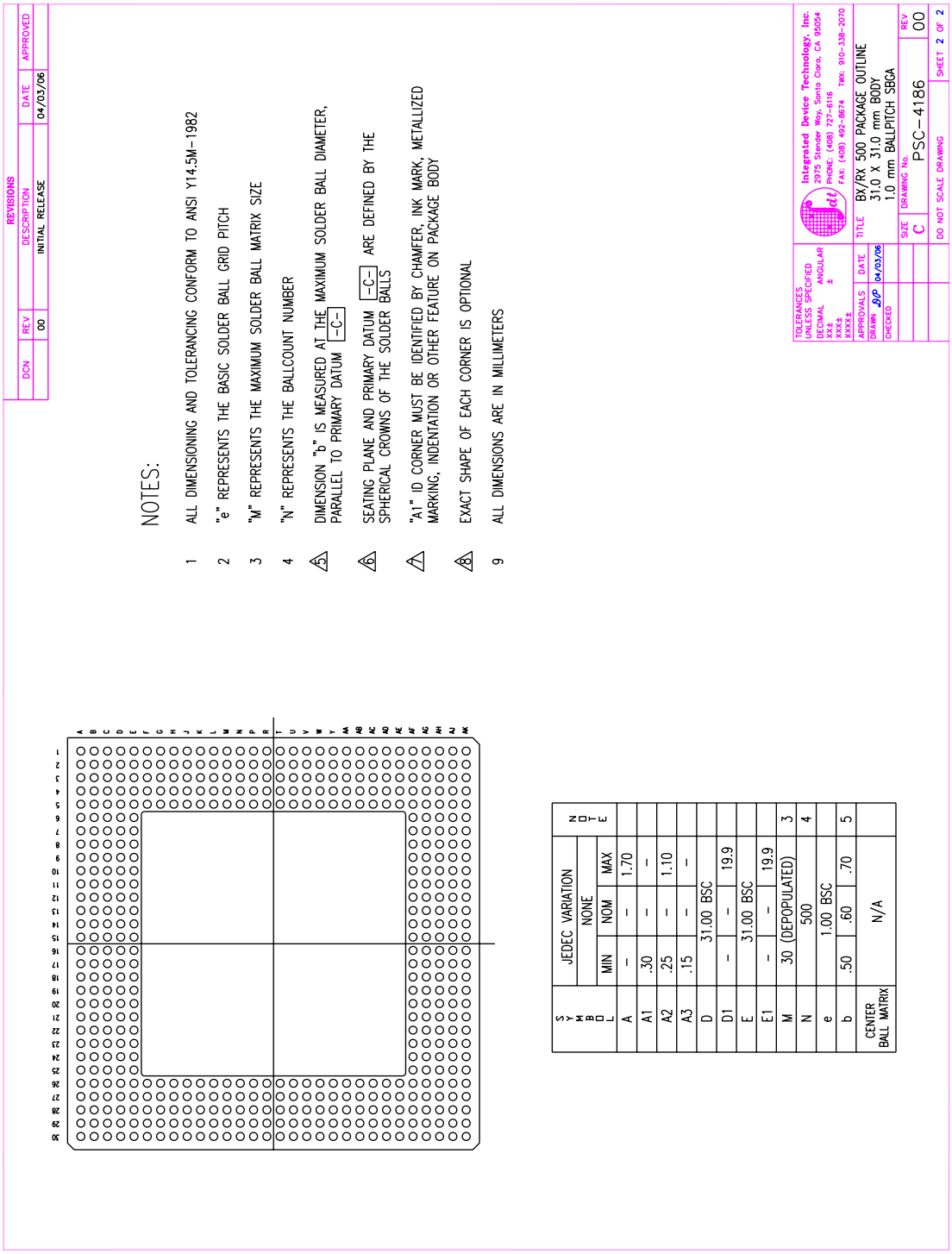
PES32T8 Pinout — Top View



PES32T8 Package Drawing — 500-Pin BX500/BXG500



PES32T8 Package Drawing — Page Two



REVISIONS

DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	04/03/06	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE
4. "N" REPRESENTS THE BALLCOUNT NUMBER
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-
6. SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
7. "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. ALL DIMENSIONS ARE IN MILLIMETERS

SYMBOL	JEDEC VARIATION NONE			NOTE
	MIN	NOM	MAX	
A	–	–	1.70	
A1	.30	–	–	
A2	.25	–	1.10	
A3	.15	–	–	
D	31.00 BSC			
D1	–	–	19.9	
E	31.00 BSC			
E1	–	–	19.9	
M	30 (DEPOPULATED)			3
N	500			4
e	1.00 BSC			
b	.50	.60	.70	5
CENTER BALL MATRIX	N/A			

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±
APPROVALS DATE
DRAWN JVP 04/03/06
CHECKED

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

TITLE BX/RX 500 PACKAGE OUTLINE
31.0 X 31.0 mm BODY
1.0 mm BALLPITCH SBGA

SIZE C | DRAWING No. PSC-4186 | REV 00

DO NOT SCALE DRAWING | SHEET 2 OF 2

Revision History

February 8, 2007: Initial publication.

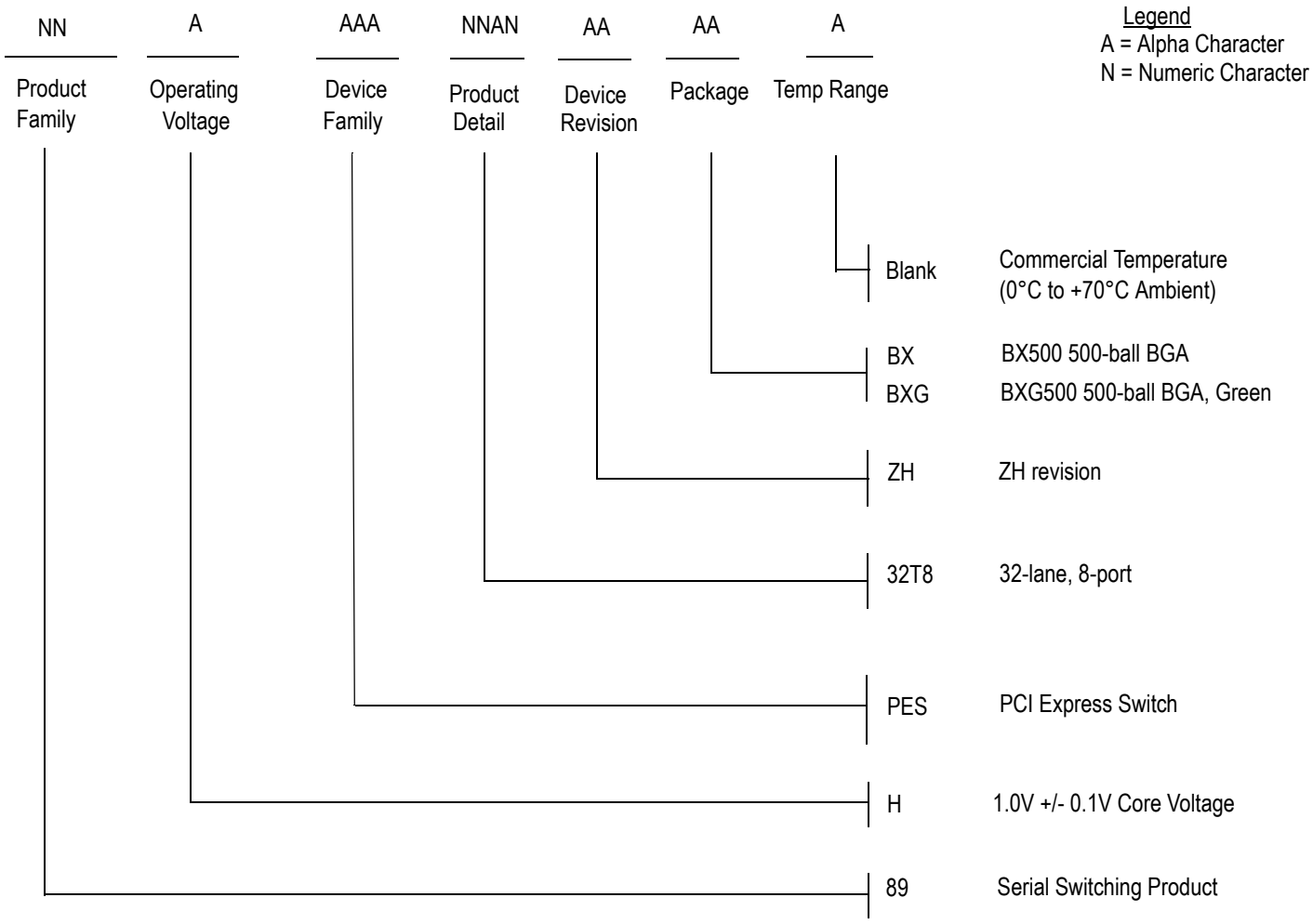
April 4, 2007: In Table 3, revised description for MSMBCLK signal.

May 30, 2007: Changed device revision in Ordering Information from ZD to ZH.

November 14, 2007: Added new parameter, Termination Resistor, to Table 9, Input Clock Requirements.

March 25, 2008: Added θ_{JB} and θ_{JC} parameters to Table 16, Thermal Specifications.

Ordering Information



Valid Combinations

89HPES32T8ZHBX	500-ball BGA package, Commercial Temperature
89HPES32T8ZHBXG	500-ball Green BGA package, Commercial Temperature

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(Rev.1.0 Mar 2020)

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