MPM3509B

36V, 0.6A Module, Synchronous, Step-Down Converter with an Integrated Inductor, AEC-Q100 Qualified

DESCRIPTION

The MPM3509B is a synchronous, rectified, step-down converter power module with built-in power MOSFETs, inductors, and capacitors. The MPM3509B offers a very compact solution and requires only four external components to achieve 0.6A of continuous output current with excellent load and line regulation over a wide input supply range. The MPM3509B operates with a 400kHz switching frequency to achieve a fast load transient response.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MPM3509B eliminates design and manufacturing risks while dramatically improving time-to-market.

The MPM3509B is available in a space-saving QFN-17 (3mmx5mmx1.6mm) package.

FEATURES

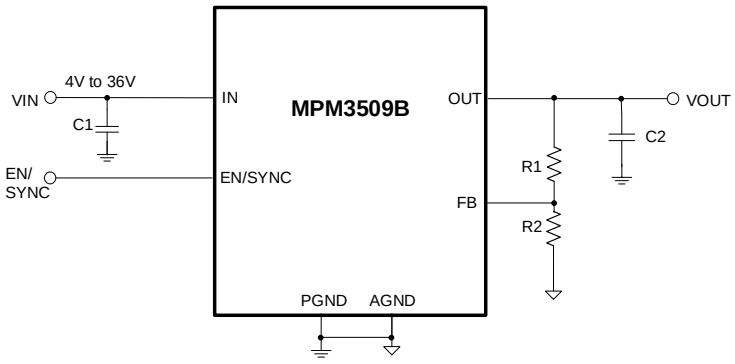
- Complete Switch-Mode Power Supply
- Wide 4V to 36V Operating Input Range
- 0.6A Continuous Load Current
- 90mΩ/50mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Fixed 400kHz Switching Frequency
- 410kHz to 2.2MHz Frequency Sync
- Forced Continuous Conduction Mode (FCCM)
- Power Good (PG) Indicator
- Over-Current Protection (OCP) with Valley-Current Detection and Hiccup Mode
- Thermal Shutdown
- Output Adjustable from 0.807V
- CISPR25 Class 5 Compliant
- Available in a QFN-17 (3mmx5mmx1.6mm) Package
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Automotive Telematics
- Medical and Imaging Equipment
- Distributed Power Systems

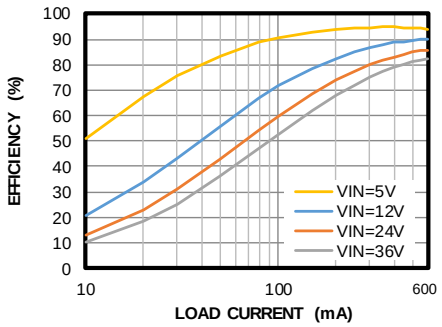
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TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 3.3V



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPM3509BGQVE-AEC1***	QFN-17 (3mmx5mmx1.6mm)	*See Below*	*3*

* For Tape & Reel, add suffix –Z (e.g. MPM3509BGQVE-AEC1–Z).

** Moisture Sensitivity Level Rating.

*** Wettable Flank.

TOP MARKING

MPYW

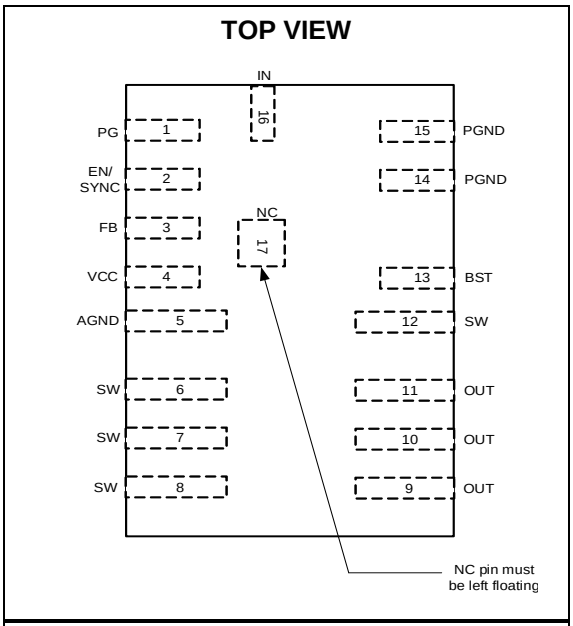
3509

BLLL

EEM

MP: MPS prefix
Y: Year code
W: Week code
3509B: Part number
LLL: Lot number
E: Package suffix
E: Wettable flank
M: Module

PACKAGE REFERENCE



QFN-17 (3mmx5mmx1.6mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	PG	**Power good indicator.** PG is an open-drain structure.
2	EN/ SYNC	**Enable/sync.** Pull EN/SYNC above the specified threshold (1.45V) to enable the MPM3509B. Float EN/SYNC or pull it below the specified threshold (1V) to disable the MPM3509B. Apply an external clock to EN/SYNC to change the switching frequency.
3	FB	**Feedback.** To set the output voltage, connect FB to the tap of an external resistor divider from the output to AGND. The feedback threshold voltage is 0.807V. The frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV. This prevents current limit runaway during a short-circuit fault. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
4	VCC	**Internal 4.9V LDO output.** An internal circuit integrates the LDO output capacitor, so VCC does not require an external capacitor.
5	AGND	**Analog ground.** Reference ground of the logic circuit. AGND is connected to PGND internally. Do not add external connections to PGND.
6, 7, 8, 12	SW	**Switch output.** The SW pins are not required to be connected. However, it is recommended to place a large copper plane on pin 6, pin 7, and pin 8 to improve heat sinking.
9, 10, 11	OUT	**Power output.** Connect the load to OUT. An output capacitor is required.
13	BST	**Bootstrap.** The bootstrap capacitor is integrated internally. BST does not require external connections.
14, 15	PGND	**Power ground.** PGND is the reference ground of the power device, and requires careful consideration while designing the PCB layout. For the best results, connect PGND with copper pours and vias.
16	IN	**Supply voltage.** IN supplies power to the internal MOSFET and regulator. The MPM3509B operates from a 4V to 36V input rail. A low-ESR, low-inductance capacitor is required to decouple the input rail. Place the input capacitor very close to IN, and connect it with wide PCB traces and multiple vias.
17	NC	**No connection.** NC must be left floating.

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +40V
V_{SW}, V_{OUT} ..... -0.3V to V_{IN} + 0.3V
V_{BST} ..... V_{SW} + 6V
All other pins ..... -0.3V to +6V (2)
Continuous power dissipation (T_A = 25°C) (3) (5) 3.9W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Electrostatic Discharge (ESD rating)

Human body model (HBM) ..... ±2kV
Charged device model (CDM)..... ±750V

Recommended Operating Conditions

Supply voltage (V_{IN}) ..... 4V to 36V
Output voltage (V_{OUT}) ..... 0.807V to V_{IN} x D_{MAX}
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-17 (3mmx5mmx1.6mm)		
JESD51-7 (4)	46	10 °C/W
EVM3509B-QV-00A (5)	32	1.6 °C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) For details on EN/SYNC's absolute maximum rating, see the EN/SYNC section on page 16.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on JESD51-7, 4-layer PCB.
5) Measured on MPS standard EVB, 6.4cmx6.4cm, 2-oz. thick copper, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{IN}	$V_{EN/SYNC}$ = 0V			8	μA
Quiescent supply current	I_Q	$V_{EN/SYNC}$ = 2V, V_{FB} = 1V, no switching		0.7	1	mA
HS switch on resistance	$HS_{RDS(ON)}$	V_{BST-SW} = 5V		90	165	mΩ
LS switch on resistance	$LS_{RDS(ON)}$	V_{CC} = 5V		50	105	mΩ
Inductor DC resistance	L_{DCR}			165		mΩ
Switch leakage	SW_{LKG}	$V_{EN/SYNC}$ = 0V, V_{SW} = 12V			2	μA
Current limit (6)	I_{LIMIT}	40% duty cycle	3.0	5.0	7.0	A
Low-side valley current limit			1.5	2.5	3.5	A
Reverse current limit			1.2	3		A
Oscillator frequency	f_{SW}	V_{FB} = 700mV	300	400	500	kHz
Foldback frequency during soft start (6)	f_{FB}	V_{FB} = 200mV		125		kHz
Maximum duty cycle	D_{MAX}	V_{FB} = 700mV	92	95		%
Minimum on time (6)	t_{ON_MIN}			40		ns
Feedback voltage	V_{FB}	T_J = 25°C	795	807	819	mV
		T_J = -40°C to +125°C	790	807	827	mV
Feedback current	I_{FB}	V_{FB} = 820mV		10	50	nA
EN/SYNC rising threshold	V_{EN_RISING}		1.2	1.45	1.7	V
EN/SYNC falling threshold	$V_{EN_FALLING}$		0.8	1	1.3	V
EN/SYNC input current	I_{EN}	$V_{EN/SYNC}$ = 2V		5	10	μA
EN/SYNC turn-off delay	EN_{TD_OFF}			3		μs
EN/SYNC frequency range			410		2200	kHz
V_{IN} under-voltage lockout rising threshold	$INUV_{VTH}$		3	3.5	3.8	V
V_{IN} under-voltage lockout threshold hysteresis	$INUV_{HYS}$			330		mV
PG rising threshold	PG_{VTH_HI}		0.83	0.88	0.93	V_{FB}
PG falling threshold	PG_{VTH_LO}		0.78	0.83	0.88	V_{FB}
PG rising delay	PG_{TD_RISING}		40	90	160	μs
PG falling delay	$PG_{TD_FALLING}$		30	55	95	μs
PG sink current capability	V_{PG}	Sink 4mA			0.4	V
PG leakage current	I_{PG_LEAK}				100	nA
VCC regulator	V_{CC}		4.6	4.9	5.2	V
VCC load regulation		I_{CC} = 5mA		1.5	4	%
Soft-start time	t_{SS}	V_{OUT} from 10% to 90%	0.4	1.7	3	ms
Thermal shutdown (6)				170		°C
Thermal hysteresis (6)				20		°C

Note:

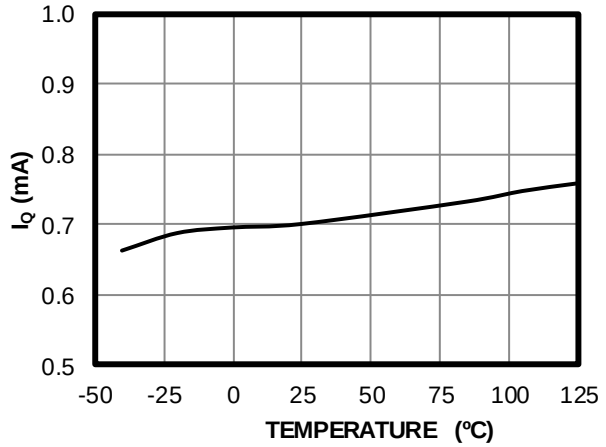
6) Derived from the bench characterization. Not tested in production.

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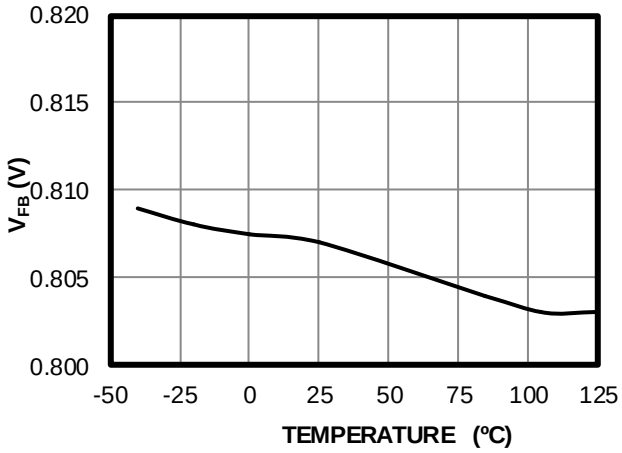
TYPICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C to +125°C, unless otherwise noted.

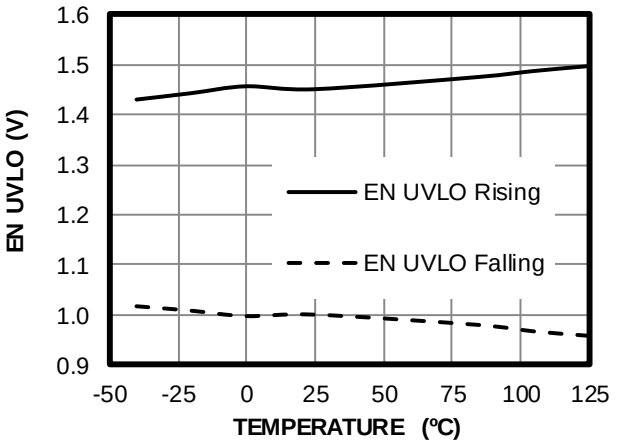
I_Q vs. Temperature



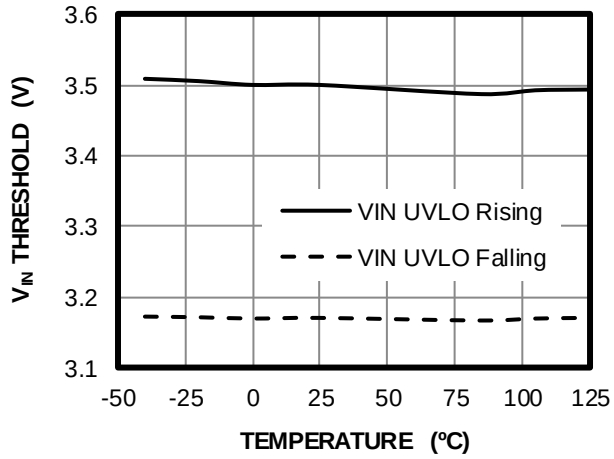
V_{FB} vs. Temperature



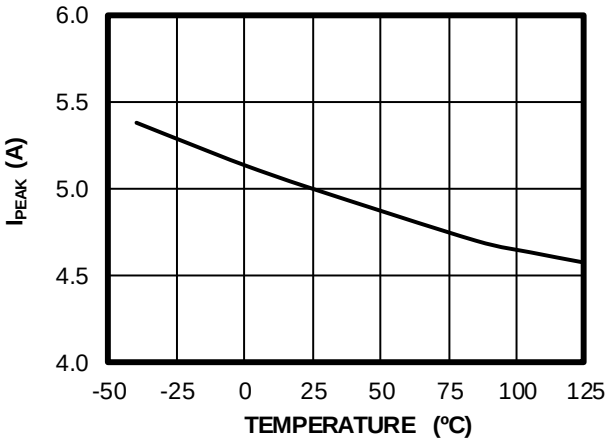
EN UVLO Threshold vs. Temperature



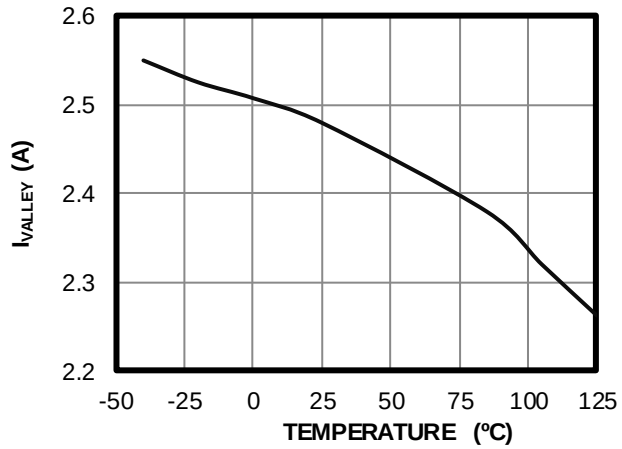
V_{IN} Threshold vs. Temperature



Peak Current Limit vs. Temperature



Valley Current Limit vs. Temperature

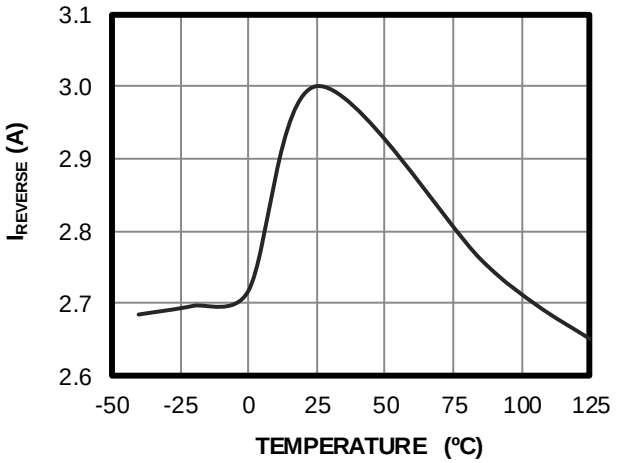


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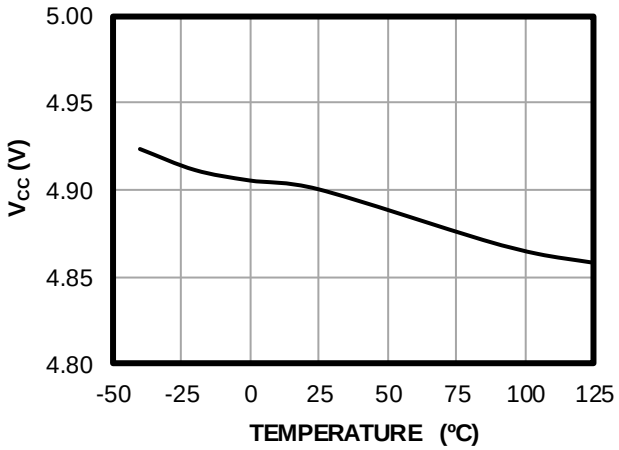
TYPICAL CHARACTERISTICS *(continued)*

V_{IN}=12V, T_J=-40°C to +125°C, unless otherwise noted.

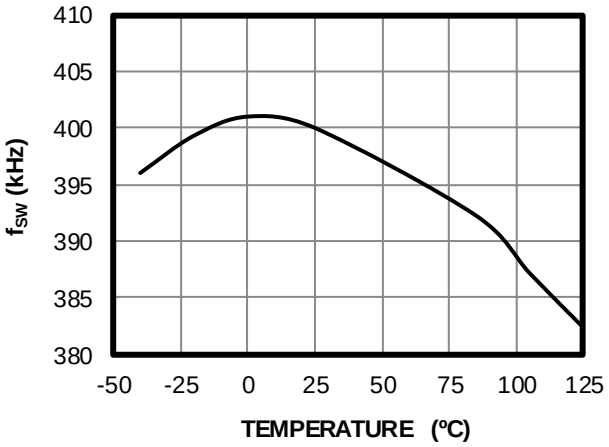
Reverse Current Limit vs. Temperature



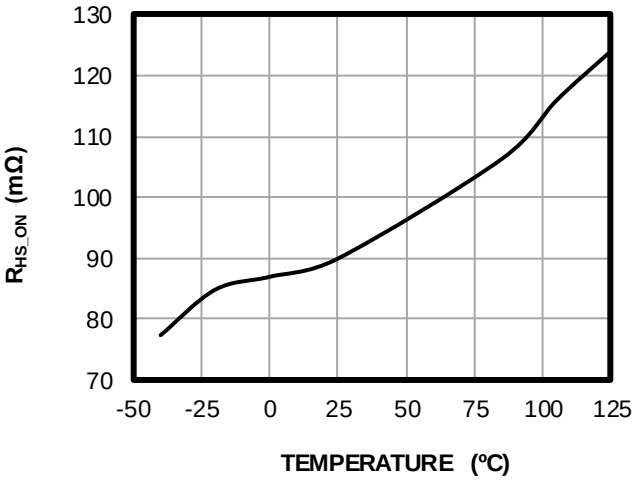
V_{CC} vs. Temperature



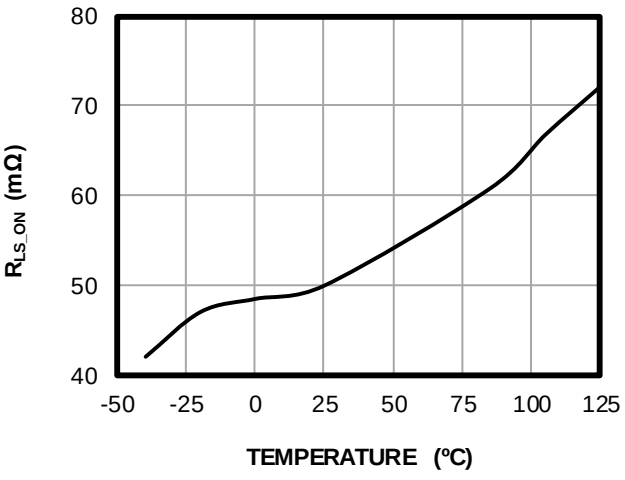
f_{SW} vs. Temperature



R_{HS_ON} vs. Temperature



R_{LS_ON} vs. Temperature



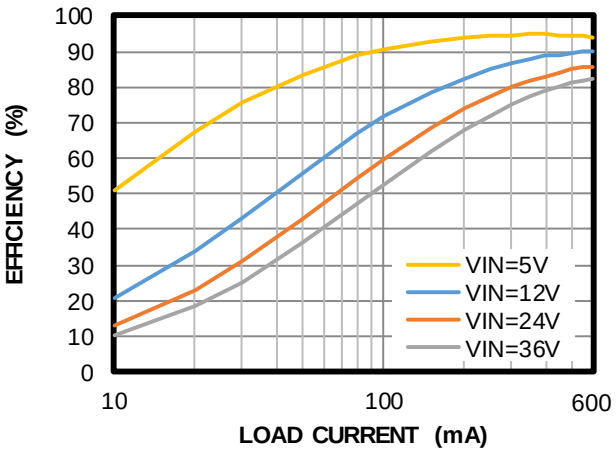
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

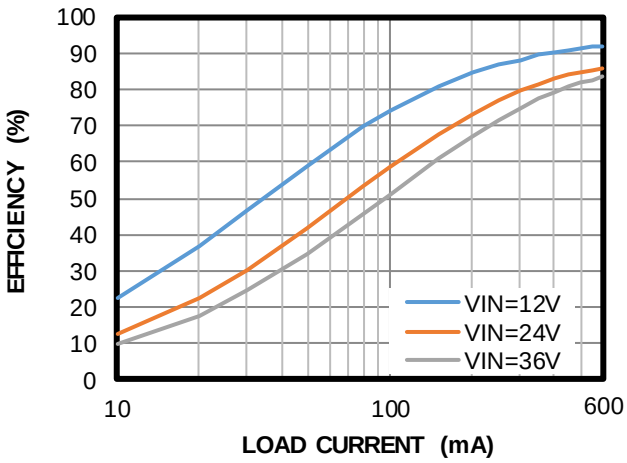
Efficiency vs. Load Current

V_{OUT} = 3.3V



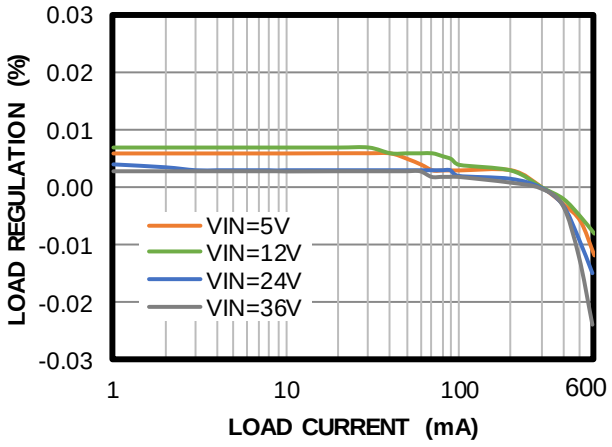
Efficiency vs. Load Current

V_{OUT} = 5V



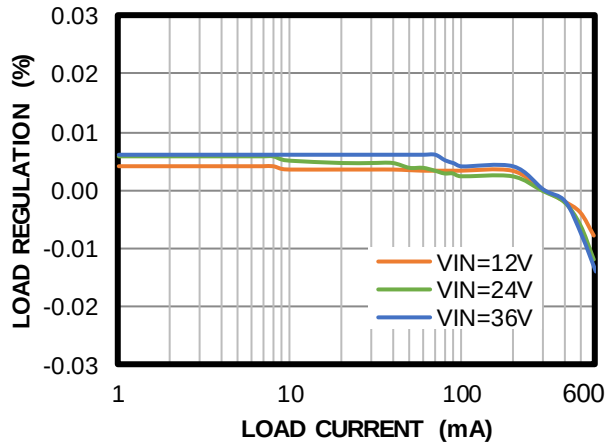
Load Regulation

V_{OUT} = 3.3V

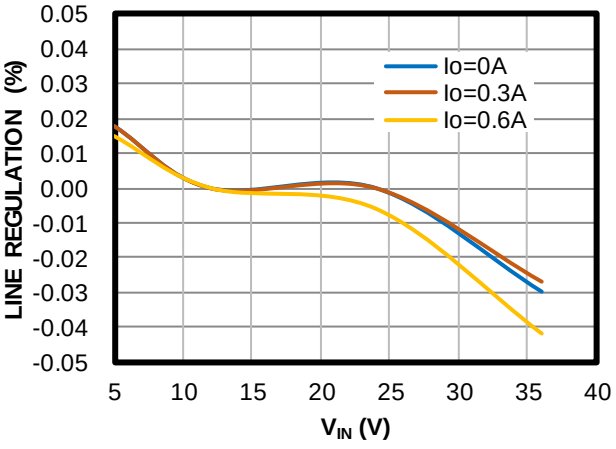


Load Regulation

V_{OUT} = 5V



Line Regulation

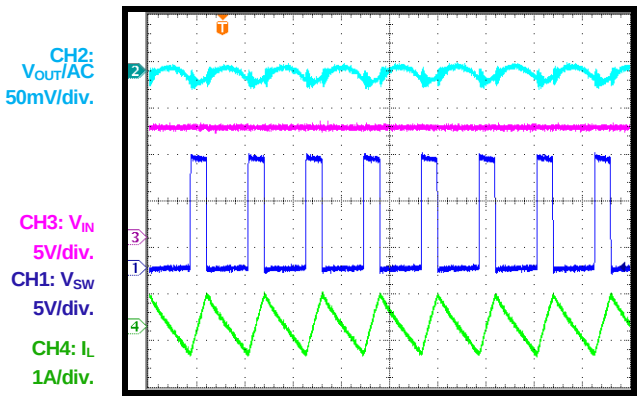


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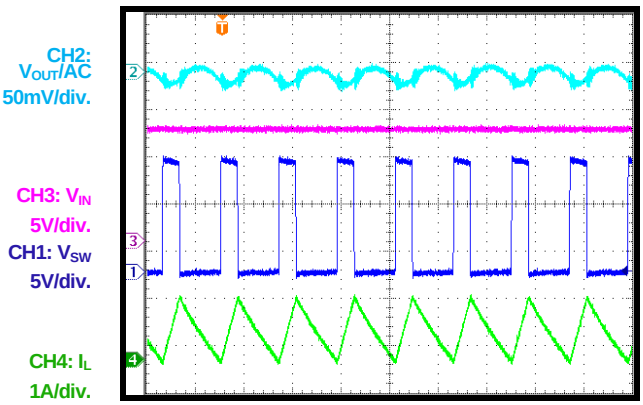
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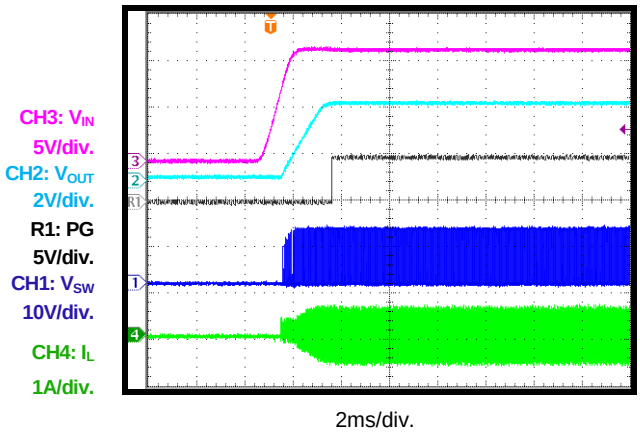
Steady State
I_{OUT} = 0A



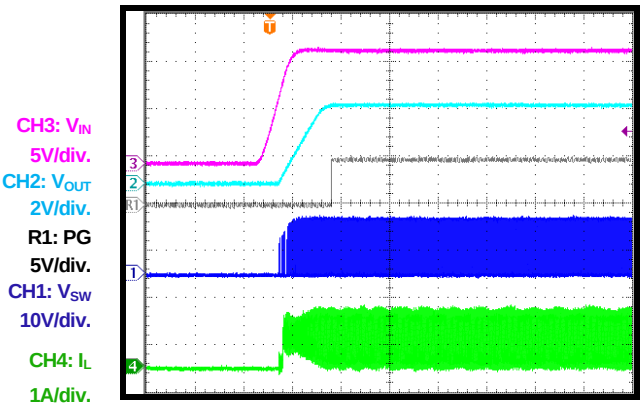
Steady State
I_{OUT} = 0.6A



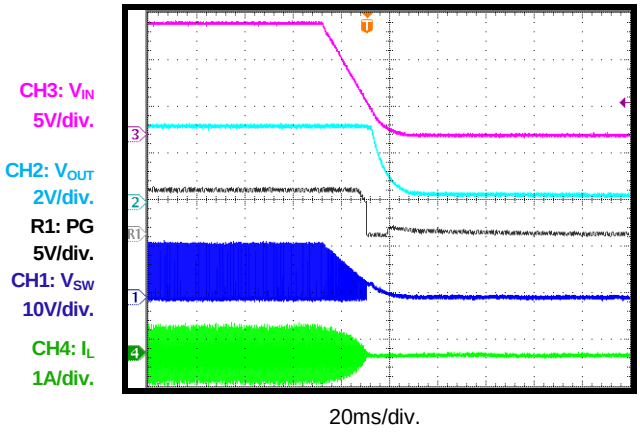
Start-Up through VIN
I_{OUT} = 0A



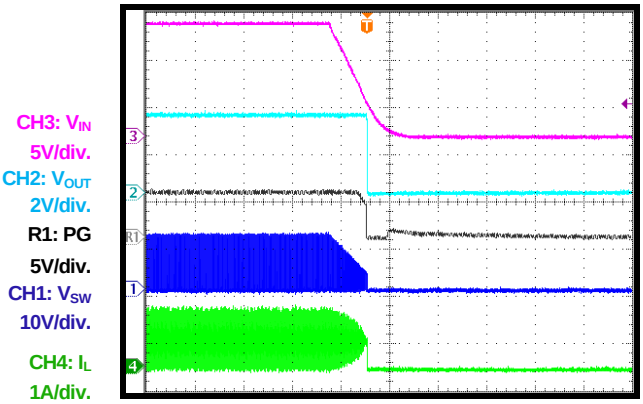
Start-Up through VIN
I_{OUT} = 0.6A



Shutdown through VIN
I_{OUT} = 0A



Shutdown through VIN
I_{OUT} = 0.6A



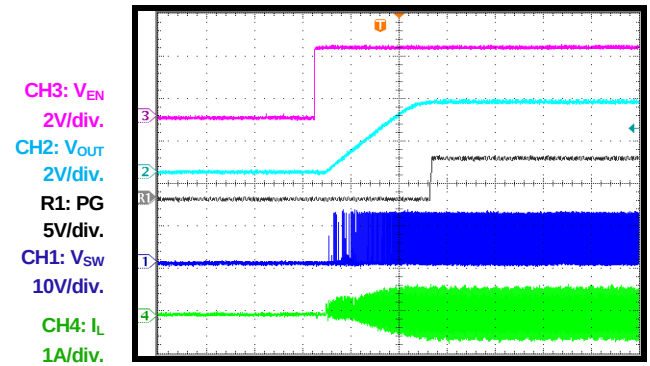
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

Start-Up through EN

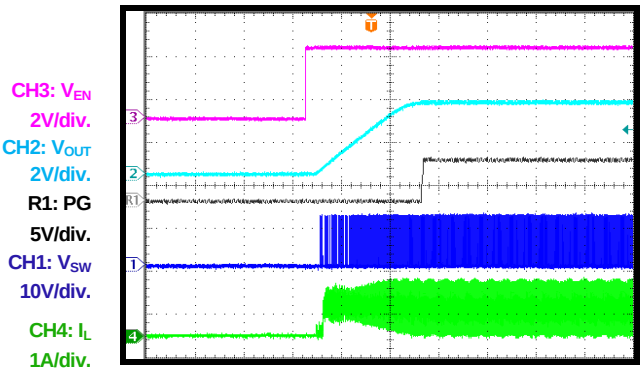
I_{OUT} = 0A



1ms/div.

Start-Up through EN

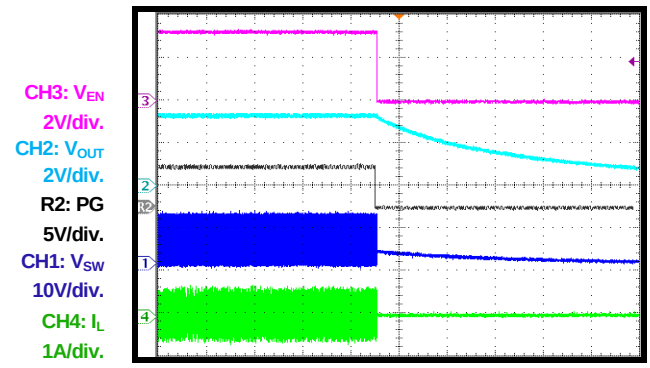
I_{OUT} = 0.6A



1ms/div.

Shutdown through EN

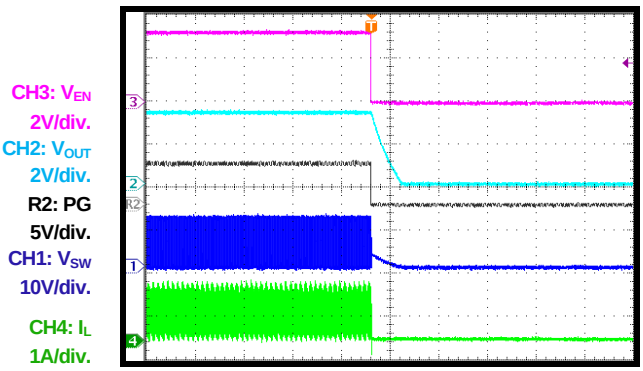
I_{OUT} = 0A



1s/div.

Shutdown through EN

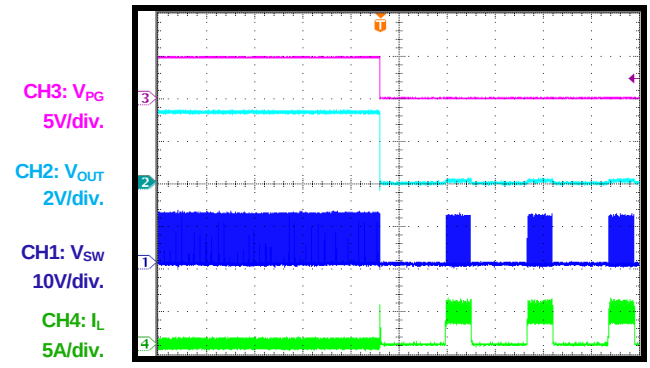
I_{OUT} = 0.6A



400µs/div.

SCP Entry

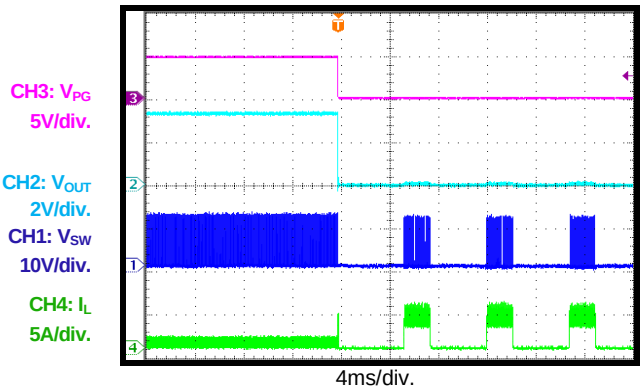
I_{OUT} = 0A



4ms/div.

SCP Entry

I_{OUT} = 0.6A



4ms/div.

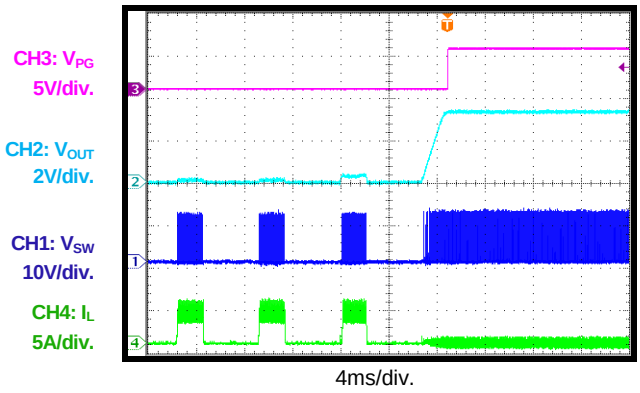
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

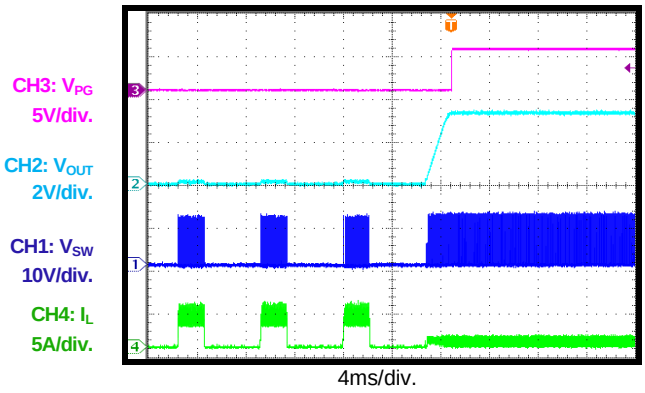
SCP Recovery

I_{OUT} = 0A



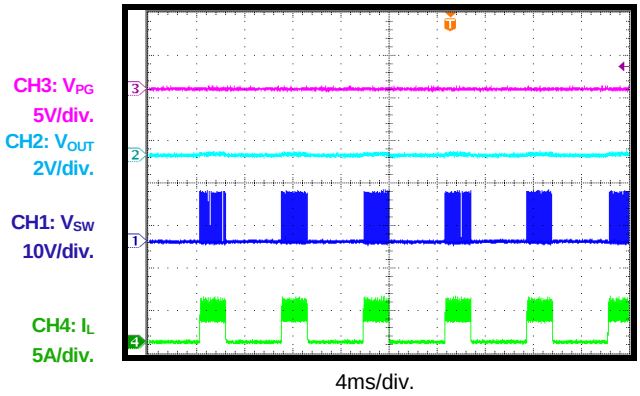
SCP Recovery

I_{OUT} = 0.6A



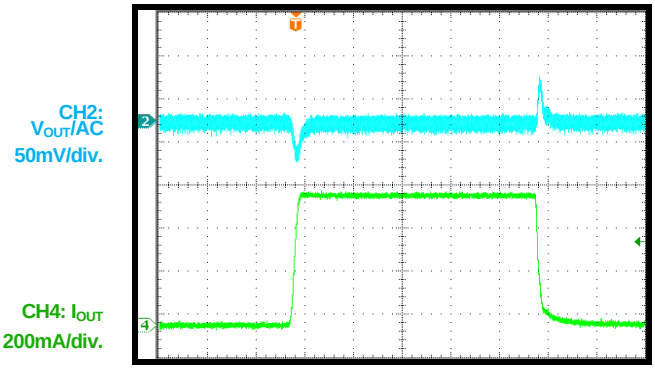
SCP Steady

I_{OUT} = 0.6A



Load Transient

I_{OUT} = 0A to 0.6A



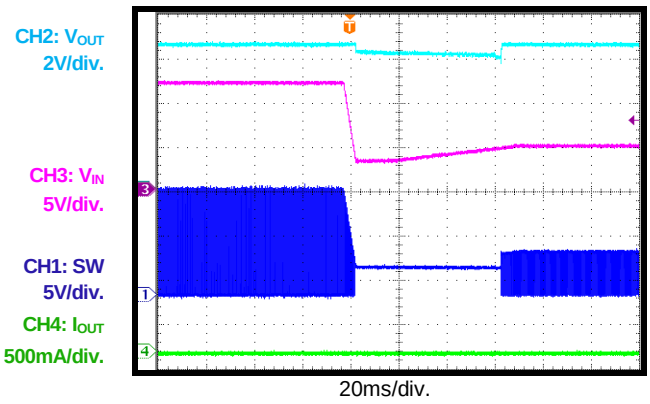
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

Cold Crank

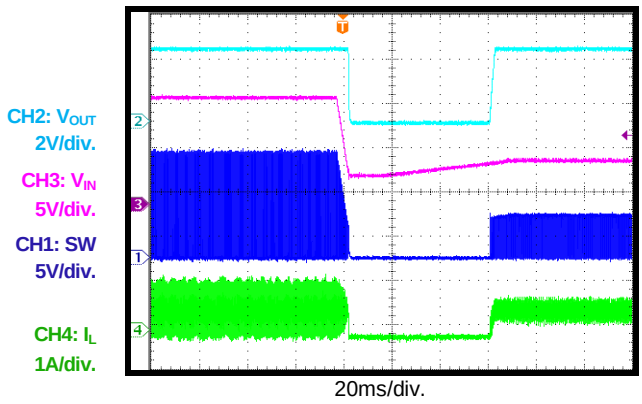
V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 0A



20ms/div.

Cold Crank

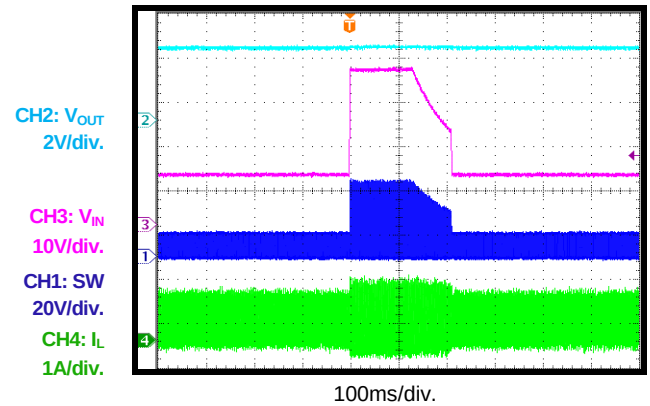
V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 0.6A



20ms/div.

Load Dump

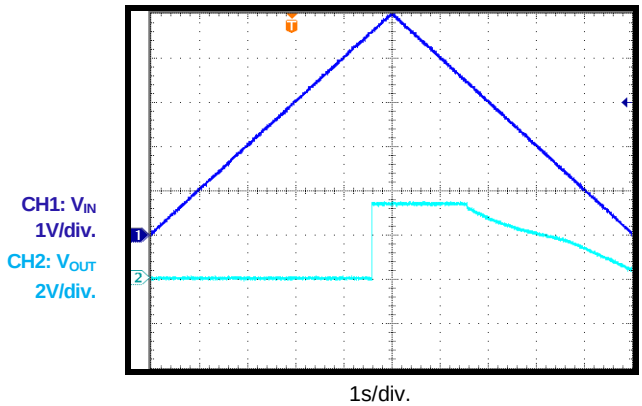
V_{IN} = 12V to 36V to 12V, I_{OUT} = 0.6A



100ms/div.

VIN Ramp Up and Down

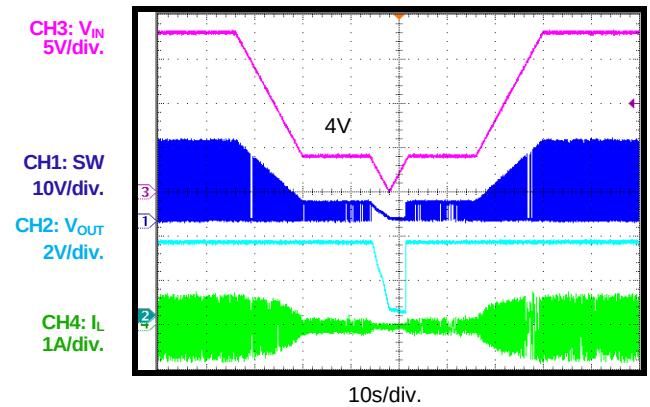
V_{IN} = 0V to 5V to 0V, I_{OUT} = 0A



1s/div.

VIN Ramp Down and Up

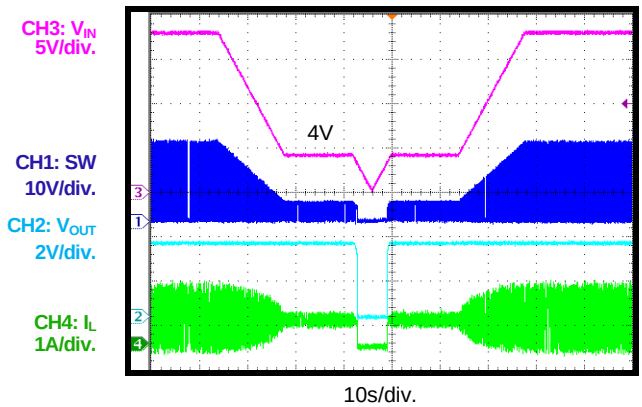
I_{OUT} = 0A



10s/div.

VIN Ramp Down and Up

I_{OUT} = 0.6A



10s/div.

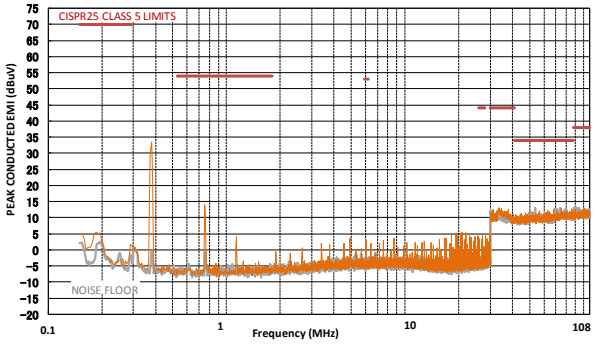
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 400kHz, T_A = 25°C, with EMI filters, unless otherwise noted. (7)

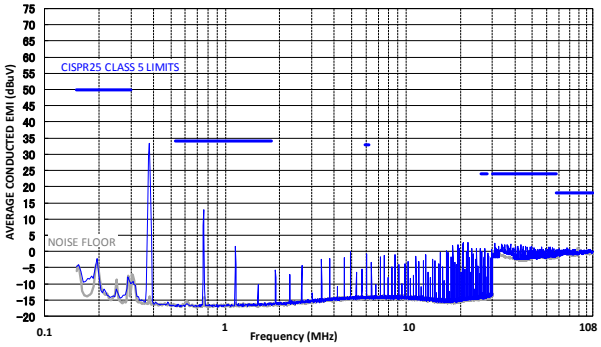
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 108MHz



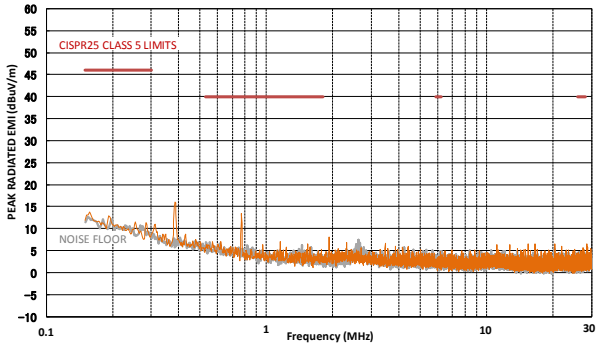
CISPR25 Class 5 Average Radiated Emissions

150kHz to 108MHz



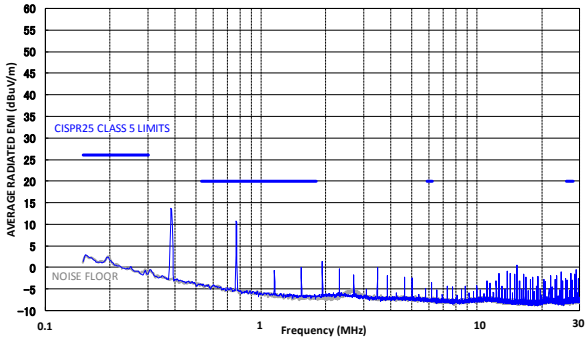
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



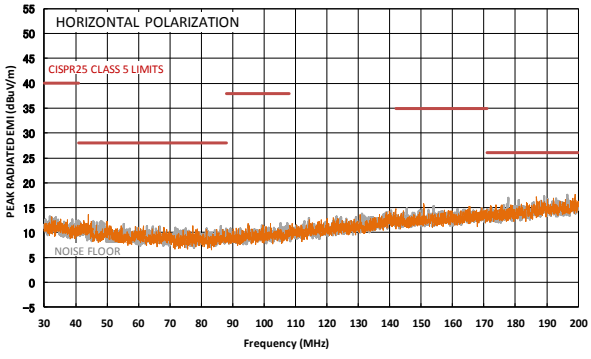
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



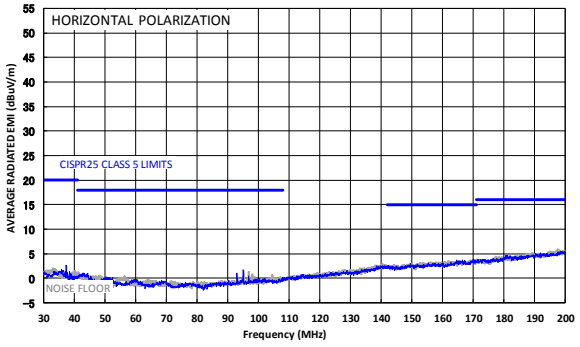
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz



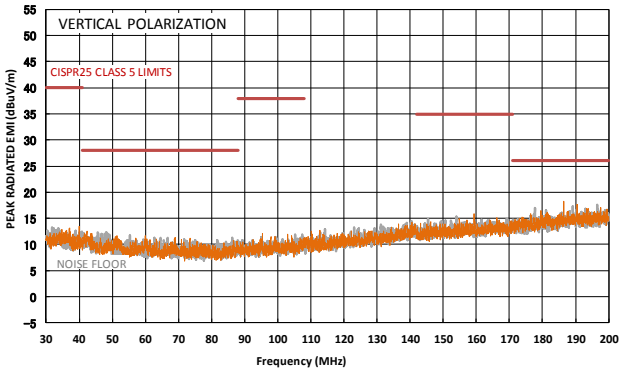
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 400kHz, T_A = 25°C, with EMI filters, unless otherwise noted. (7)

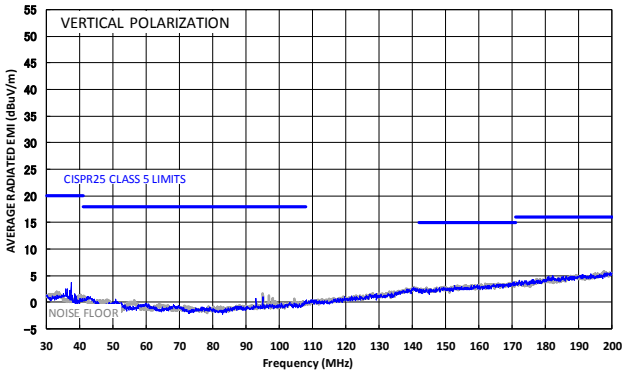
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



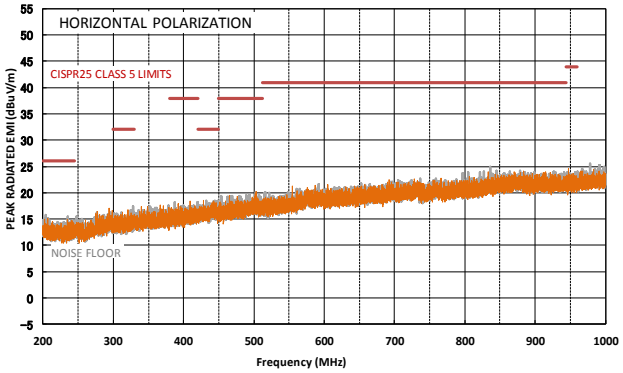
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



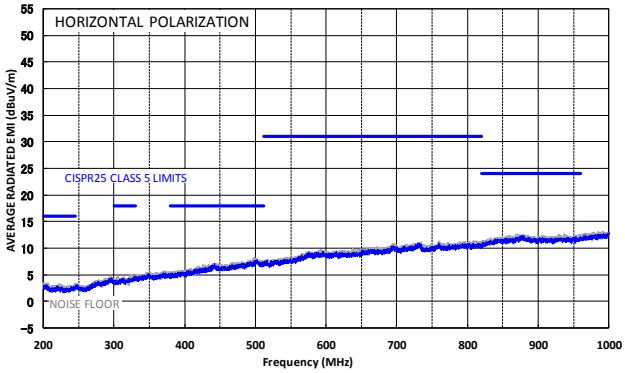
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



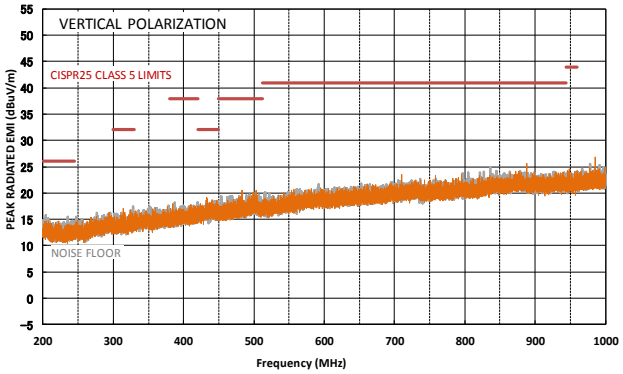
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



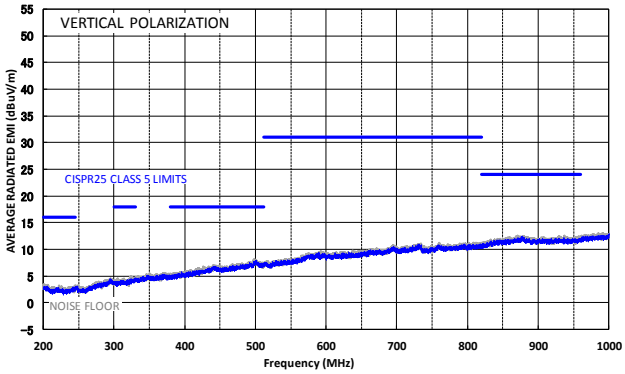
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



Note:

7) The EMC test results are based on the typical application circuit in Figure 11 on page 23. The results are tested on the EVM3509B-QV-00A.

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FUNCTIONAL BLOCK DIAGRAM

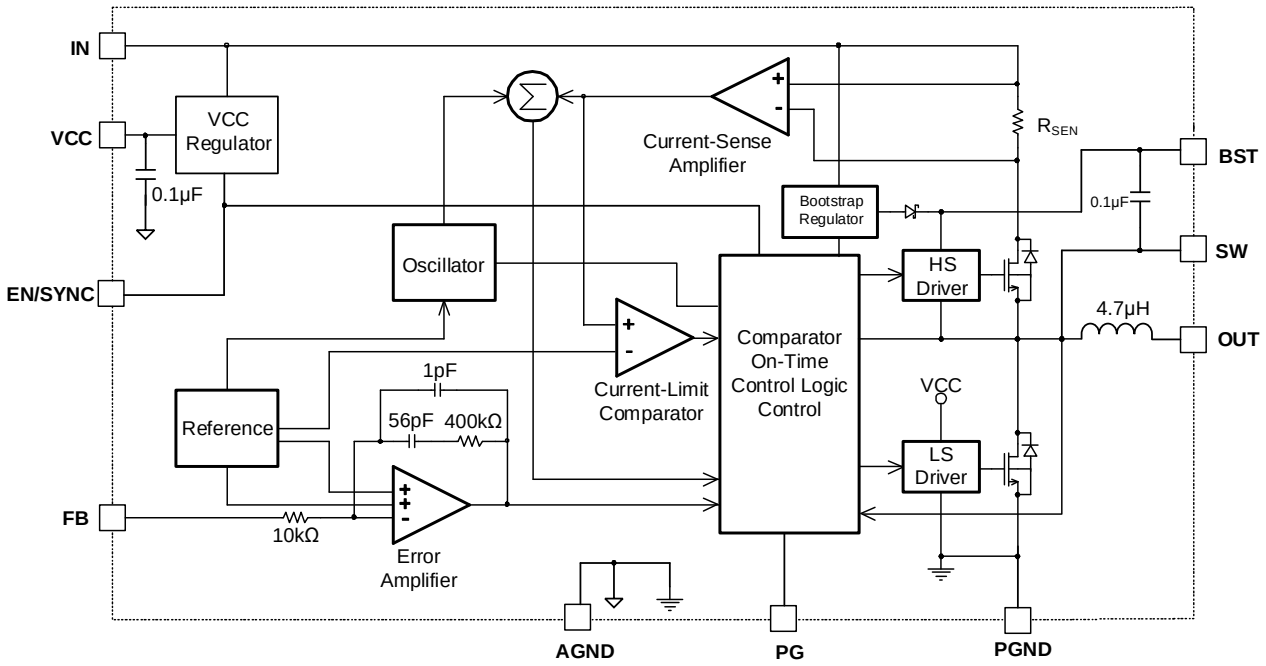


Figure 1: Functional Block Diagram

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OPERATION

The MPM3509B is a high-frequency, synchronous, rectified, step-down, switch-mode converter power module with built-in power MOSFETs, an integrated inductor, and two capacitors. The MPM3509B offers a very compact solution that achieves 0.6A of continuous output current with excellent load and line regulation across a 4V to 36V input supply range.

The MPM3509B operates in fixed-frequency, peak current control mode to regulate the output voltage. An internal clock initiates a pulse-width modulation (PWM) cycle. The integrated high-side power MOSFET (HS-FET) turns on, and remains on until the current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle begins. If the current in the power MOSFET does not reach the value set by V_{COMP} within 95% of one PWM period, the power MOSFET is forced off.

Internal Regulator

A 4.9V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 4.9V, the output of the regulator is in full regulation. When V_{IN} drops below 4.9V, the output decreases. The MPM3509B integrates an internal decoupling capacitor, so an external VCC output capacitor is not required.

Forced Continuous Conduction Mode (FCCM) Operation

The MPM3509B uses forced continuous conduction mode (FCCM) to ensure that the part works with a fixed frequency from a no-load to a full-load range. The advantage of FCCM is the controllable frequency and lower output ripple under light-load conditions.

Error Amplifier (EA)

The error amplifier compares the FB voltage to the internal 0.807V reference (V_{REF}) and outputs a current proportional to the difference between the two values. The output current then charges or discharges the internal compensation network to form V_{COMP}, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies control loop design.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 3.5V, and its falling threshold is about 3.17V.

EN/SYNC

EN/SYNC is a control pin that turns the regulator on and off. Drive EN/SYNC high to turn on the regulator; drive EN/SYNC low to turn off the regulator. An internal 500kΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

EN/SYNC is clamped internally using a 6.5V series Zener diode (see Figure 2). Connecting the EN/SYNC input to V_{IN} through a pull-up resistor limits the EN/SYNC input current below 100μA. For example, with 12V connected to VIN, $R_{PULLUP} \geq (12V - 6.5V) \div 100\mu A = 55k\Omega$.

Connecting EN/SYNC to a voltage source directly without a pull-up resistor requires limiting the amplitude of the voltage source below 6V to prevent damage to the Zener diode.

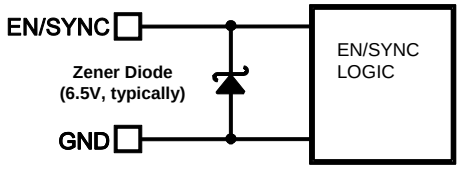


Figure 2: 6.5V Zener Diode Connection

Connect an external clock with a range of 410kHz to 2.2MHz to synchronize the internal clock rising edge to the external clock rising edge. The pulse wide of the external clock signal should be below 1.7us, and the off time of external clock signal should be below 1.9μs.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start (V_{SS}) voltage that ramps up from 0V to 4.9V. When V_{SS} is below V_{REF}, the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is set to 1.7ms internally.

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Over-Current Protection (OCP) and Hiccup

The MPM3509B has cycle-by-cycle peak current limit protection and valley current detection protection. The inductor current is monitored during the HS-FET on state. If the inductor current exceeds the current limit value set by the COMP high-clamp voltage, the HS-FET turns off immediately. The low-side MOSFET (LS-FET) then turns on to discharge the energy, and the inductor current decreases. The HS-FET remains off unless the inductor valley current drops below the valley current limit, even if the internal clock pulses high.

If the inductor current does not drop below the valley current limit when the internal clock pulses high, the HS-FET misses the clock, and the switching frequency decreases to half the nominal value. Both the peak and valley current limits assist in keeping the inductor current from running away during an overload or short-circuit condition.

If the output voltage drops below the under-voltage (UV) threshold (typically 50% below V_{REF}), the MPM3509B enters hiccup mode to periodically restart the part. Simultaneously, the peak current limit is reached.

This protection mode is useful when the output is dead-shorted to ground, and greatly reduces the average short-circuit current to alleviate thermal issues and protect the regulator. The MPM3509B exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the die temperatures exceed 170°C, the device stops switching. When the temperature drops below its lower threshold (typically 150°C), the power supply resumes operation.

Floating Driver and Bootstrap Charging

An internal bootstrap capacitor powers the floating power MOSFET driver. A dedicated internal regulator charges and regulates the bootstrap capacitor voltage to about 5V (see Figure 3). When the voltage between the BST and SW nodes drops below the regulation voltage, a PMOS pass transistor that is connected from V_{IN} to BST turns on. The charging current path is from VIN to BST to SW. The external circuit should provide enough voltage headroom to facilitate charging. As long as V_{IN} exceeds SW significantly, the bootstrap capacitor remains charged. When the HS-FET is on, V_{IN} is about equal to V_{SW}, so the bootstrap capacitor cannot charge. When the LS-FET is on, V_{IN} - V_{SW} reaches its maximum value for fast charging. When there is no inductor current, V_{SW} is equal to V_{OUT}, so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor. The floating driver has its own under-voltage lockout (UVLO) protection, with a rising threshold of 2.2V and hysteresis of 150mV.

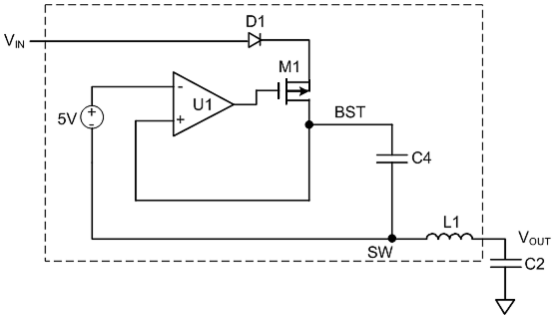


Figure 3: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If V_{IN} exceeds its thresholds, the MPM3509B starts up. The reference block starts first, generating a stable reference voltage and current. Then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: V_{IN} going low, EN/SYNC going low, and thermal shutdown. During shutdown, the signaling path is first blocked to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application Circuits section on page 21). The feedback resistor (R1) sets the feedback loop bandwidth with the internal compensation capacitor. Choose R1 to be about 75kΩ when V_{OUT} exceeds 1V. R2 can then be calculated with Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.807V} - 1} \quad (1)$$

Figure 4 shows the feedback network.

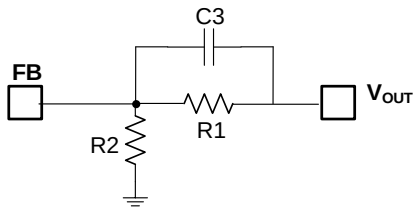


Figure 4: Feedback Network

Table 1 lists recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.8	75	61
2.5	75	35.7
3.3	75	24.3
5	75	14.3

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For the most applications, use a 4.7µF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating.

The RMS current in the input capacitor can be estimated with Equation (2):

$$I_{C1} = I_{LOAD} x \sqrt{\frac{V_{OUT}}{V_{IN}} x \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (2)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (3):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (3)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} x C1} x \frac{V_{OUT}}{V_{IN}} x \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} x L_1} x \left(1 - \frac{V_{OUT}}{V_{IN}}\right) x \left(R_{ESR} + \frac{1}{8 x f_{SW} x C2}\right) \quad (5)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple.

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For simplification, the output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8xf_{SW}^2xL_1xC2}x\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW}xL_1}x\left(1-\frac{V_{OUT}}{V_{IN}}\right)xR_{ESR} \quad (7)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPM3509B can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator under the following conditions:

- V_{OUT} is 5V or 3.3V
- The duty cycle (D) exceeds 65%. D can be estimated with Equation (9):

$$D = \frac{V_{OUT}}{V_{IN}} \quad (9)$$

In these cases, add an external BST diode from VCC to BST (see Figure 5).

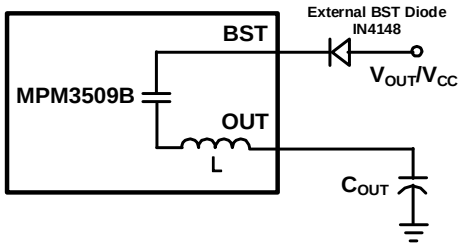


Figure 5: Optional External Bootstrap Diode Added to Enhance Efficiency

The recommended external BST diode is IN4148.

Design Example

Table 2 lists a design example following the application guidelines for the specifications below.

Table 2: Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	0.6A

See the Typical Performance Characteristics section on page 8 for more details. For additional device applications, refer to the related evaluation board datasheet.

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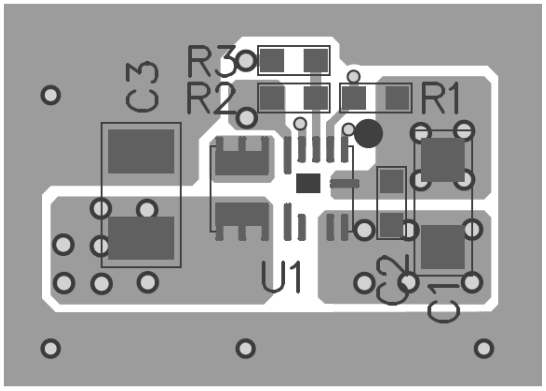
PCB Layout Guidelines [8]

Efficient PCB layout, especially input capacitor placement, is critical for stable operation. For the best results, refer to Figure 6 and follow the guidelines below:

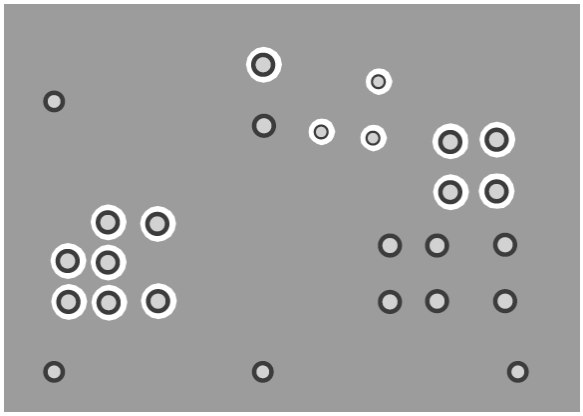
1. Connect a large ground plane directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
2. Ensure that the high-current paths at GND and IN have short, direct, and wide traces.
3. Place the ceramic input capacitor close to IN and PGND.
4. Keep the connection between the input capacitor and IN as short and wide as possible.
5. Place the external feedback resistors next to FB.
6. Keep the feedback network away from the switching node.

Note:

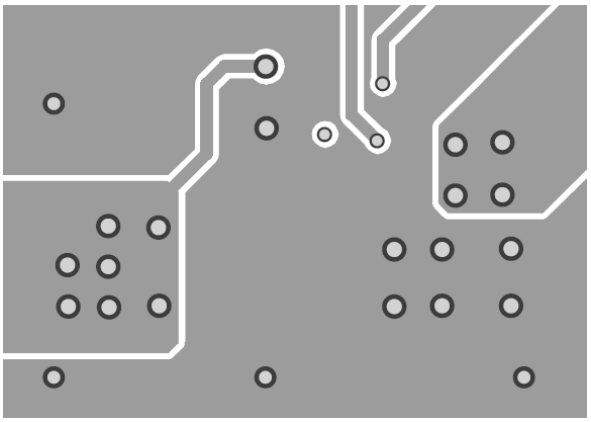
8) The recommended layout is based on Figure 6.



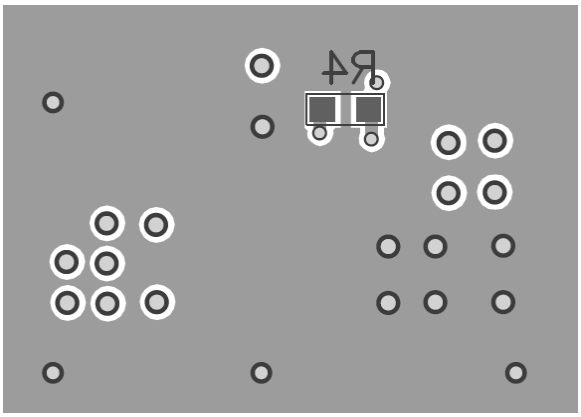
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 6: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

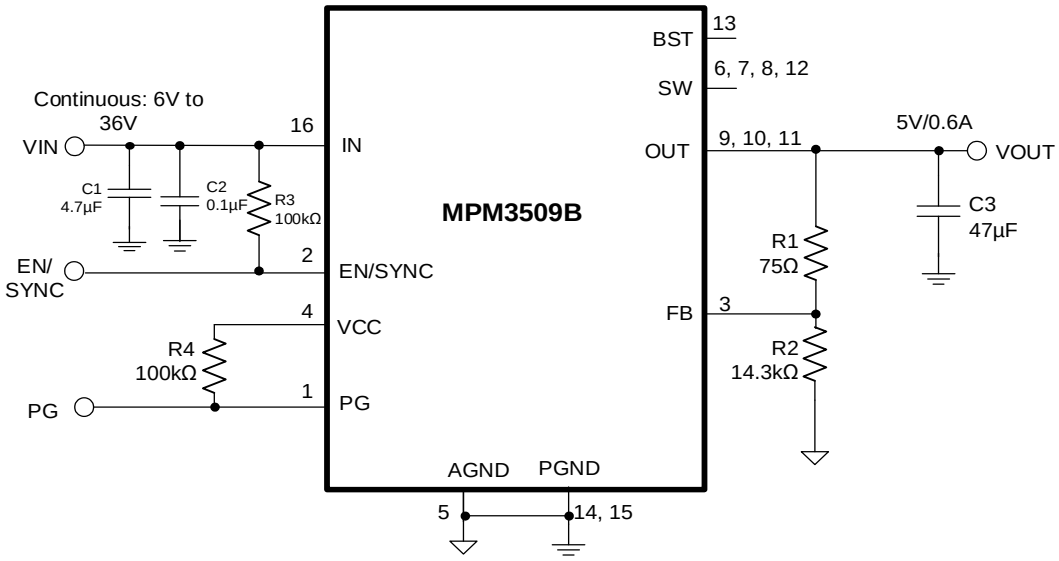


Figure 7: V_{OUT} = 5V, I_{OUT} = 0.6A

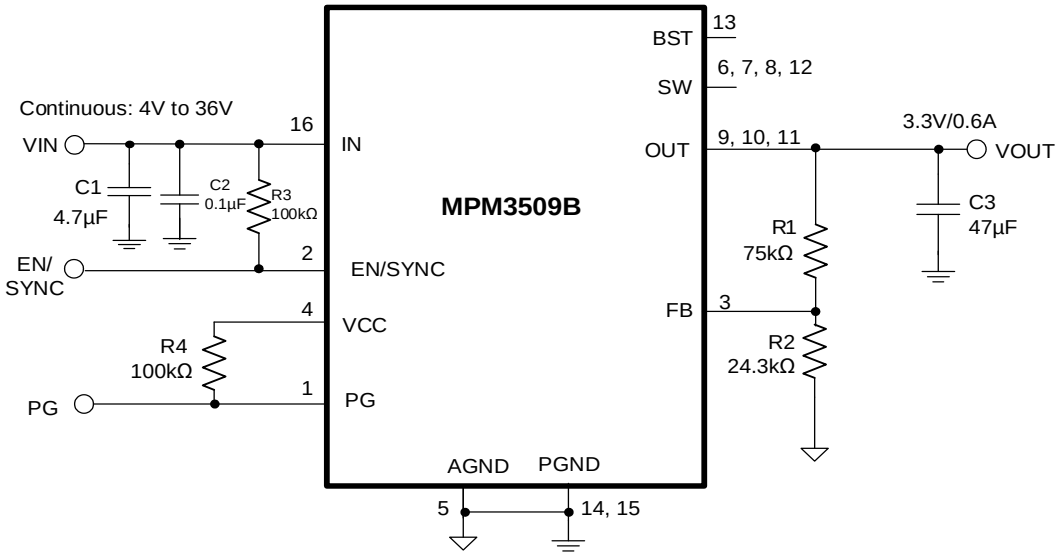


Figure 8: V_{OUT} = 3.3V, I_{OUT} = 0.6A

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TYPICAL APPLICATION CIRCUITS *(continued)*

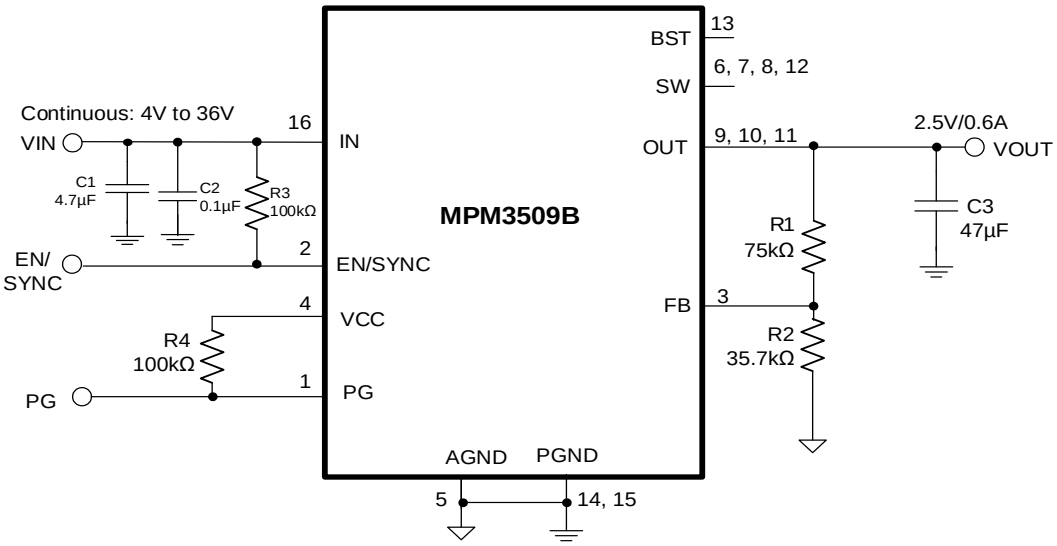


Figure 9: V_{OUT} = 2.5V, I_{OUT} = 0.6A

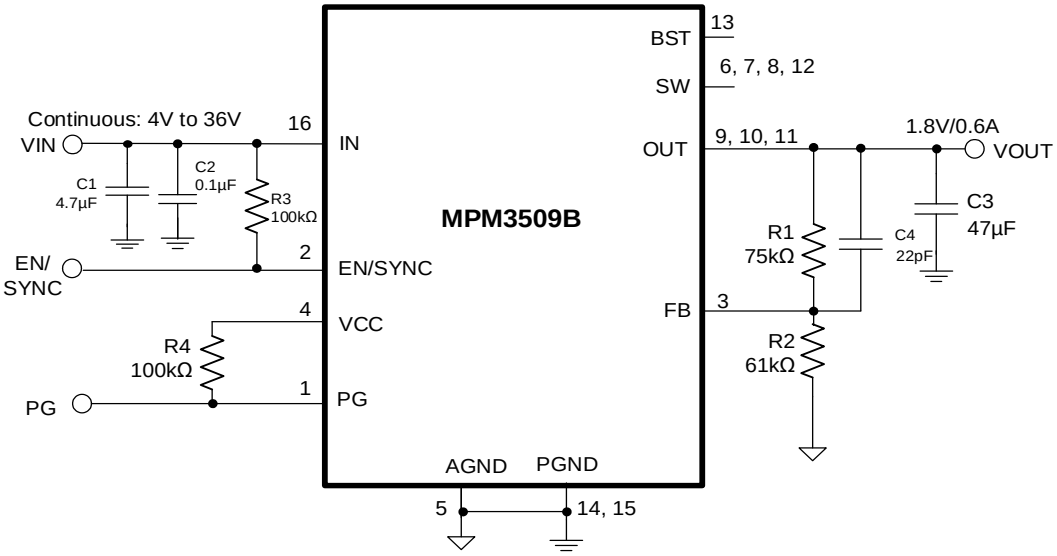


Figure 10: V_{OUT} = 1.8V, I_{OUT} = 0.6A

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TYPICAL APPLICATION CIRCUITS *(continued)*

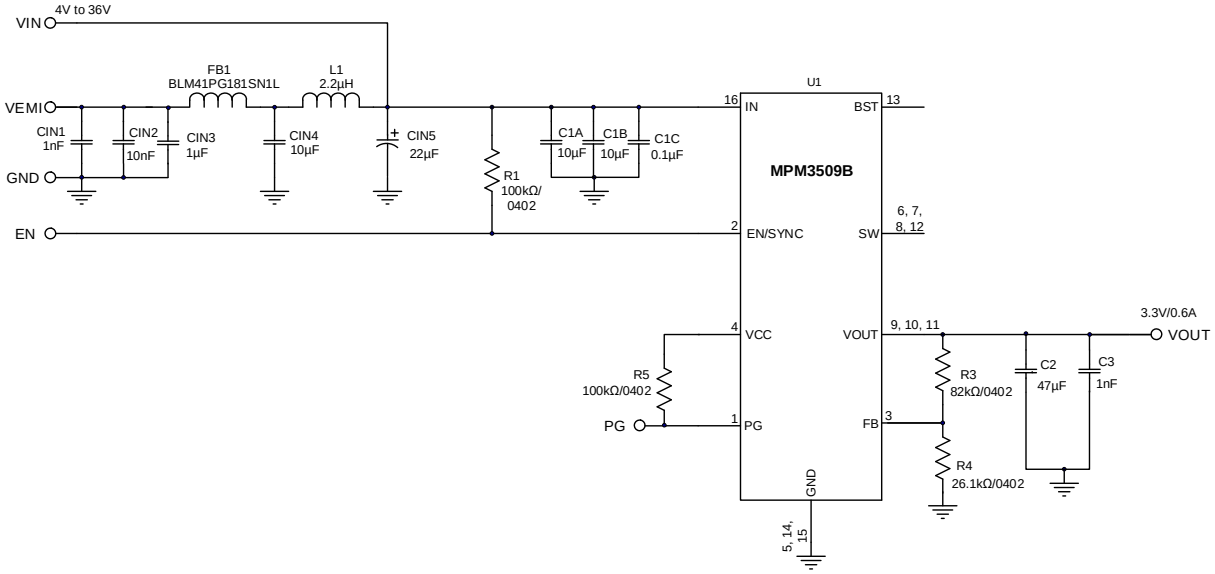
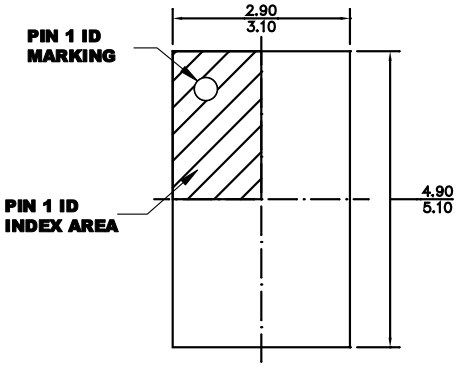


Figure 11: V_{OUT} = 3.3V, I_{OUT} = 0.6A with EMI Filter

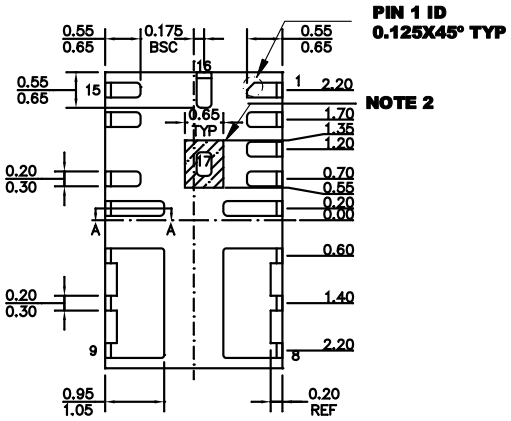
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PACKAGE INFORMATION

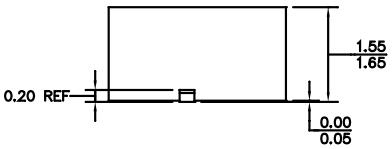
QFN-17 (3mmx5mmx1.6mm)
Wettable Flank



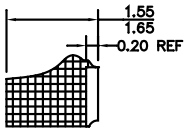
TOP VIEW



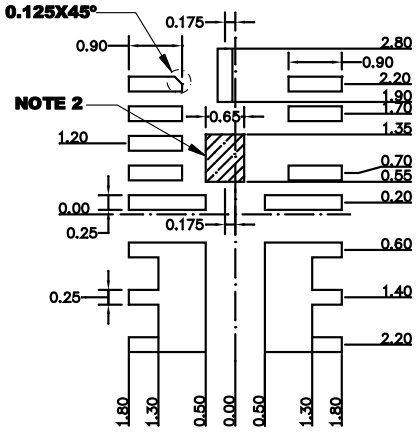
BOTTOM VIEW



SIDE VIEW



SECTION A-A



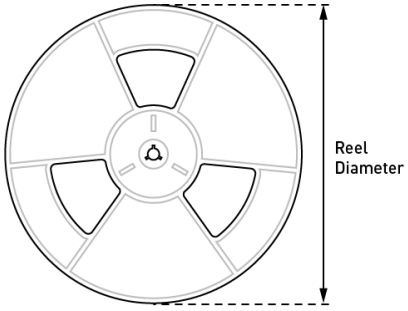
RECOMMENDED LAND PATTERN

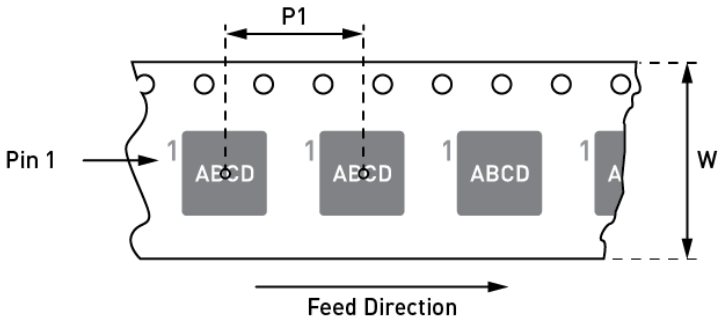
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) THE SHADED AREA IS THE KEEP-OUT ZONE. DO NOT ELECTRONICALLY OR MECHNICALLY CONNECT A PCB METAL TRACE OR VIA TO THIS AREA.
3) THE LEAD SIDE IS WETTABLE.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION





Part Number	Package Description	Quantity/Reel	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3509BGQVE-AEC1–Z	QFN-17 (3mmx5mmx1.6mm)	2500	13in	12mm	8mm

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Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	5/28/2020	Initial Release	-

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