Bipolar Hall Latch

High Precision Hall Effect Latch for Consumer Applications

TLV4961-3TA
TLV4961-3TB

SP001274776
SP001283606

TLV4961-3T

Data Sheet

Revision 1.2, 2019-12-20

Sense & Control

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1 Product description

1.1 Overview

Characteristic	Supply Voltage	Supply Current	Sensitivity	Interface	Temperature
Bipolar Hall Effect Latch	3.0 V ~ 26 V	1.6 mA	B_{OP}: 7.5 mT B_{RP}: -7.5 mT	Open Drain Output	-40°C to 125°C

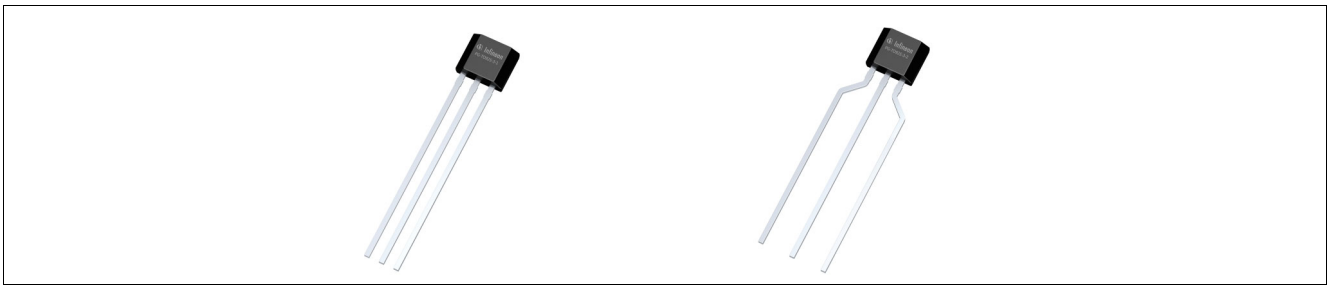


Figure 1 TLV4961-3T in the TO92S-3-1 and TO92S-3-2 package

1.2 Features

- 3.0 V to 26 V operating supply voltage
- Operation from unregulated power supply
- Output overcurrent and overtemperature protection
- Active error compensation
- High stability of magnetic thresholds
- High ESD performance
- Leaded, halogen-free package TO92S-3-1 for TLV4961-3TA, TO92S-3-2 for TLV4961-3TB

For automotive applications please refer to the Infineon TLE Hall Switches/Latches series.

Table 1 Ordering information

Product name	Product type	Ordering code	Package
TLV4961-3TA	Bipolar Hall Latch	SP001274776	TO92S-3-1 (Bulk)
TLV4961-3TB	Bipolar Hall Latch	SP001283606	TO92S-3-2 (Ammo pack)

1) Only the package is halogen-free.

1.3 Target applications

Target applications for the TLV496x Hall Latch family are all applications which require a high precision Hall Latch with an operating temperature range from -40°C to 125°C.

The magnetic behavior as a latch and switching thresholds of typical ±7.5 mT make the device especially suited for the use with a pole wheel for index counting applications, for rotor position detection as in brushless DC motor commutation and for white goods or open/closing detection.

2 Functional description

2.1 General

The TLV4961-3T is an integrated Hall effect latch designed specifically for highly accurate applications with superior supply voltage capability and temperature stability of the magnetic thresholds.

2.2 Pin configuration (top view)

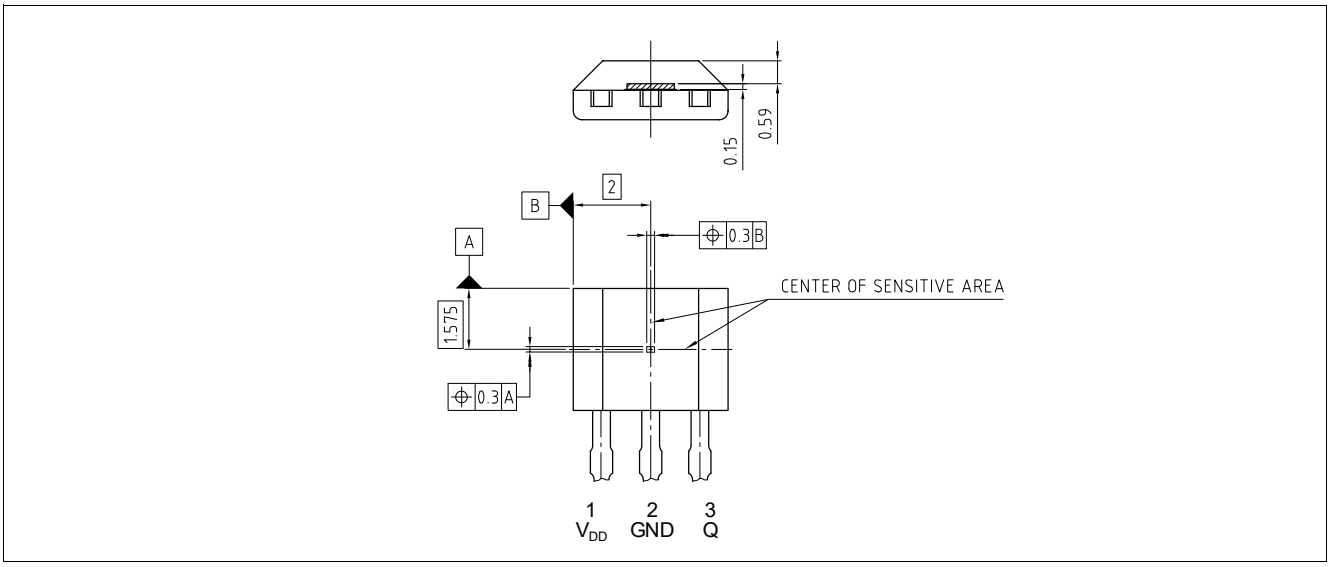


Figure 2 Pin configuration and center of sensitive area

2.3 Pin description

Table 2 Pin description

Pin no.	Symbol	Function
1	VDD	Supply voltage
2	GND	Ground
3	Q	Output

2.4 Block diagram

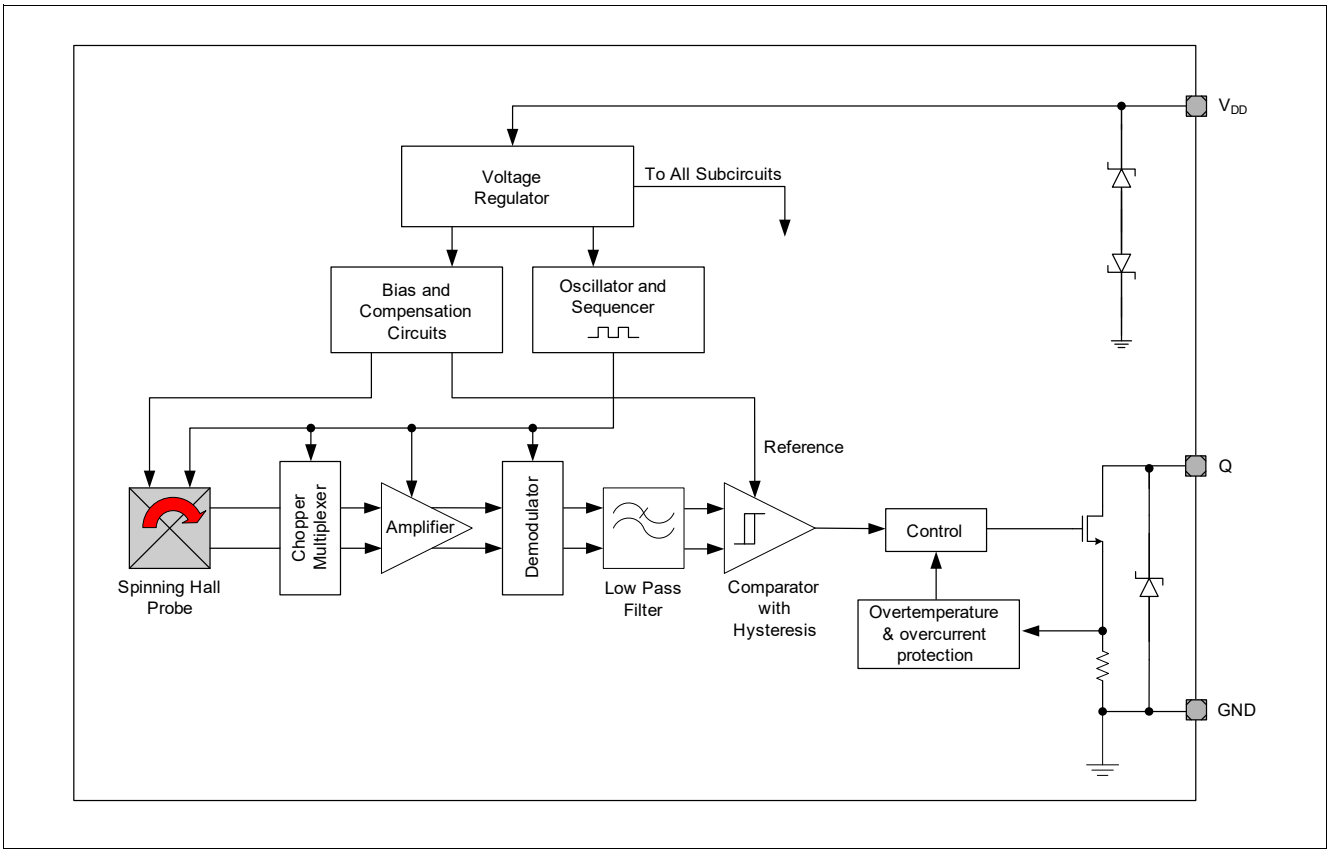


Figure 3 Functional block diagram TLV4961-3T

2.5 Functional block description

The chopped Hall IC switch comprises a Hall probe, bias generator, compensation circuits, oscillator and output transistor.

The bias generator provides currents for the Hall probe and the active circuits. Compensation circuits stabilize the temperature behavior and reduce influence of technology variations.

The active error compensation (chopping technique) rejects offsets in the signal path and the influence of mechanical stress to the Hall probe caused by molding and soldering processes and other thermal stress in the package. The chopped measurement principle together with the threshold generator and the comparator ensures highly accurate and temperature stable magnetic thresholds.

The output transistor has an integrated overcurrent and overtemperature protection.

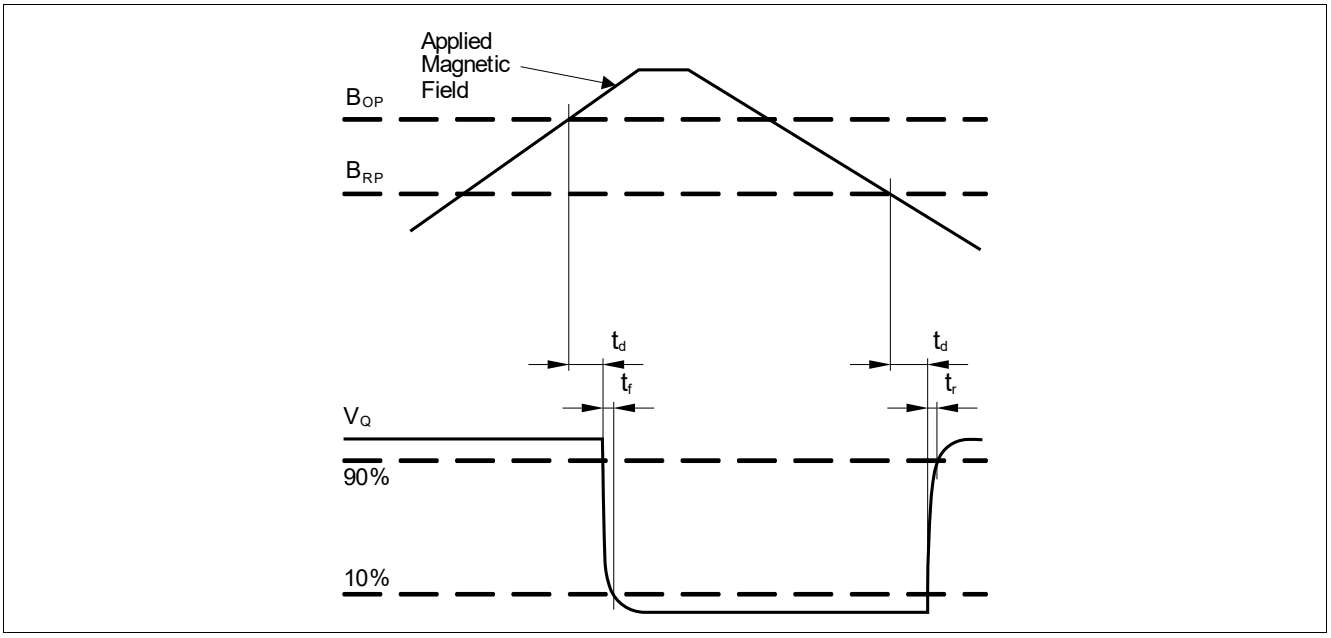


Figure 4 Timing diagram TLV4961-3T

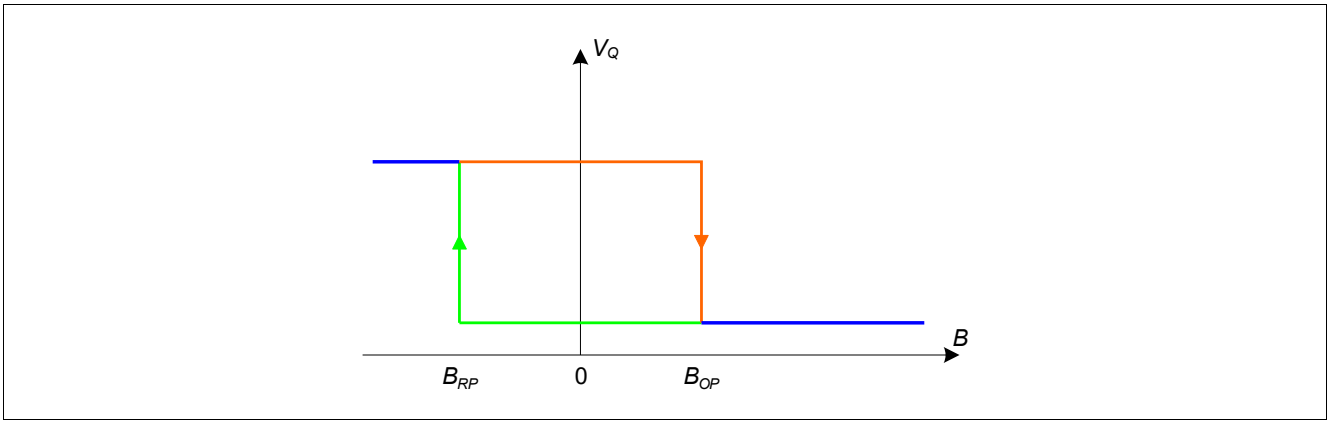


Figure 5 Output signal TLV4961-3T

2.6 Default start-up behavior

The magnetic thresholds exhibit a hysteresis $B_{HYS} = B_{OP} - B_{RP}$. In case of a power-on with a magnetic field B within hysteresis ($B_{OP} > B > B_{RP}$) the output of the sensor is set to the pull up voltage level (V_Q) per default. After the first crossing of B_{OP} or B_{RP} of the magnetic field the internal decision logic is set to the corresponding magnetic input value.

V_{DDA} is the internal supply voltage which is following the external supply voltage V_{DD}.

This means for $B > B_{OP}$ the output is switching, for $B < B_{RP}$ and $B_{OP} > B > B_{RP}$ the output stays at V_Q.

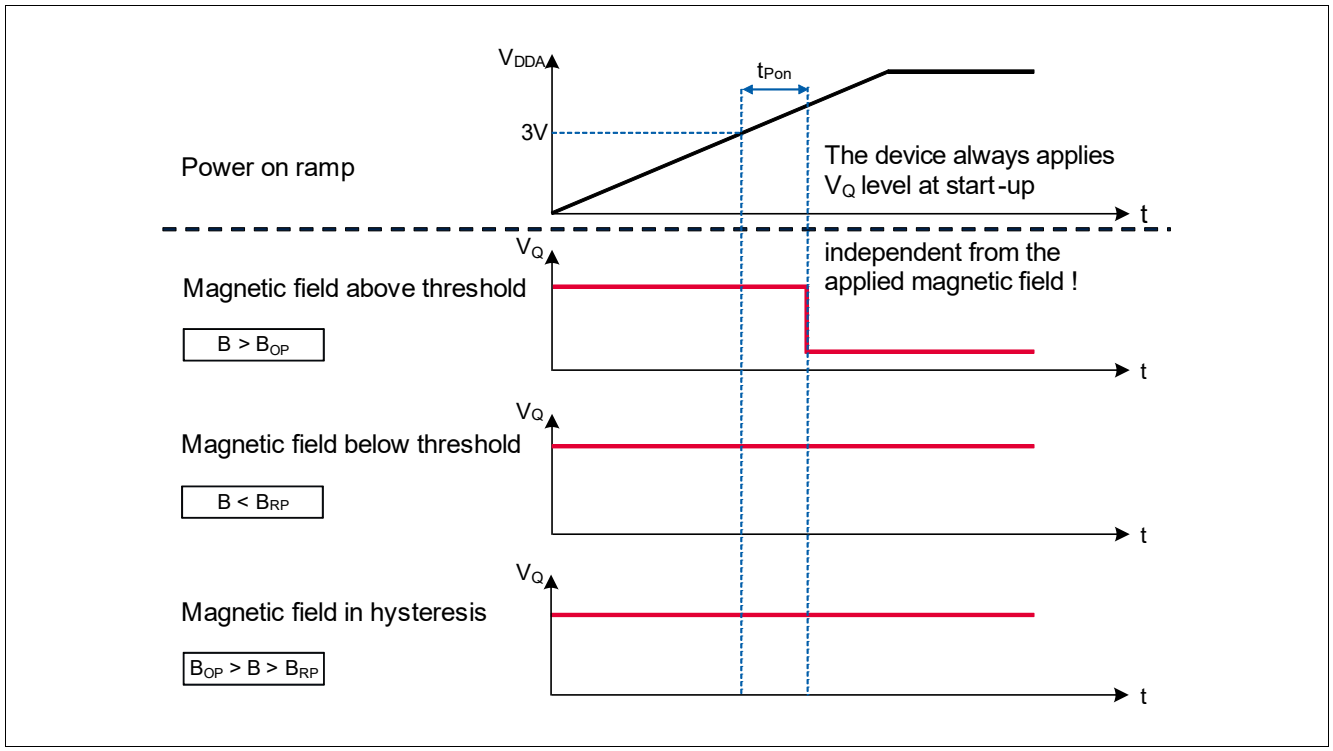


Figure 6 Start-up behavior of the TLV4961-3T

3 Specification

3.1 Application circuit

The following **Figure 7** shows the basic option of an application circuit. Only a pull-up resistor R_Q is necessary. The resistor R_Q has to be in a dimension to match the applied V_S to keep I_Q limited to the operating range of maximum 25 mA.

e.g.: V_S = 12 V; I_Q = 12 V/1200 Ω = 10 mA

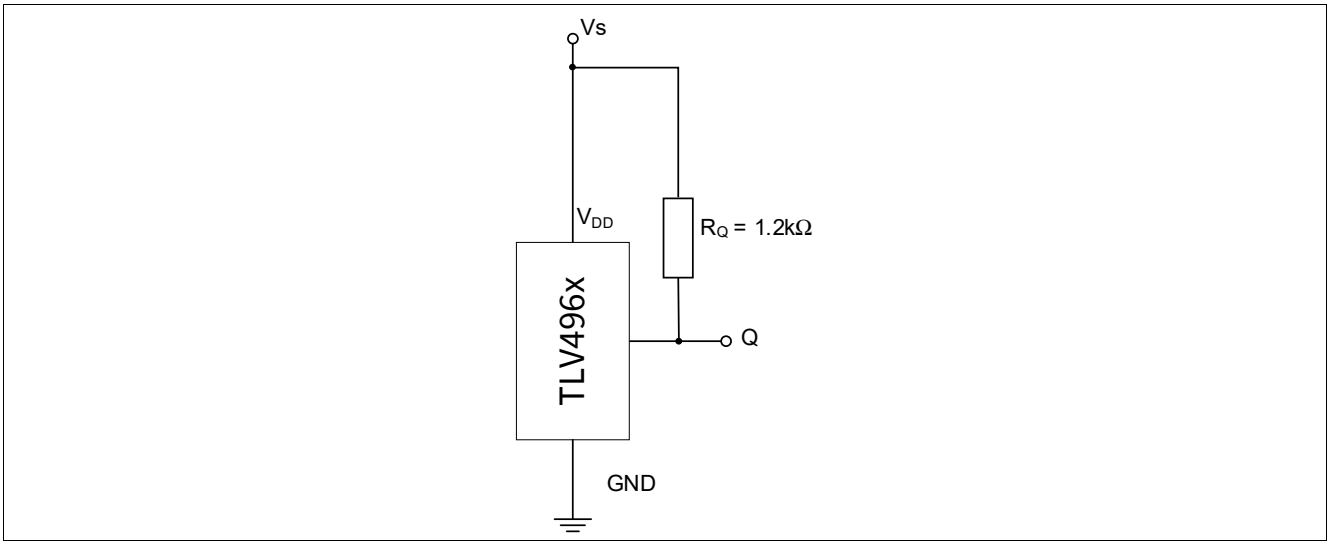


Figure 7 Basic application circuit #1: only pull-up resistor is necessary

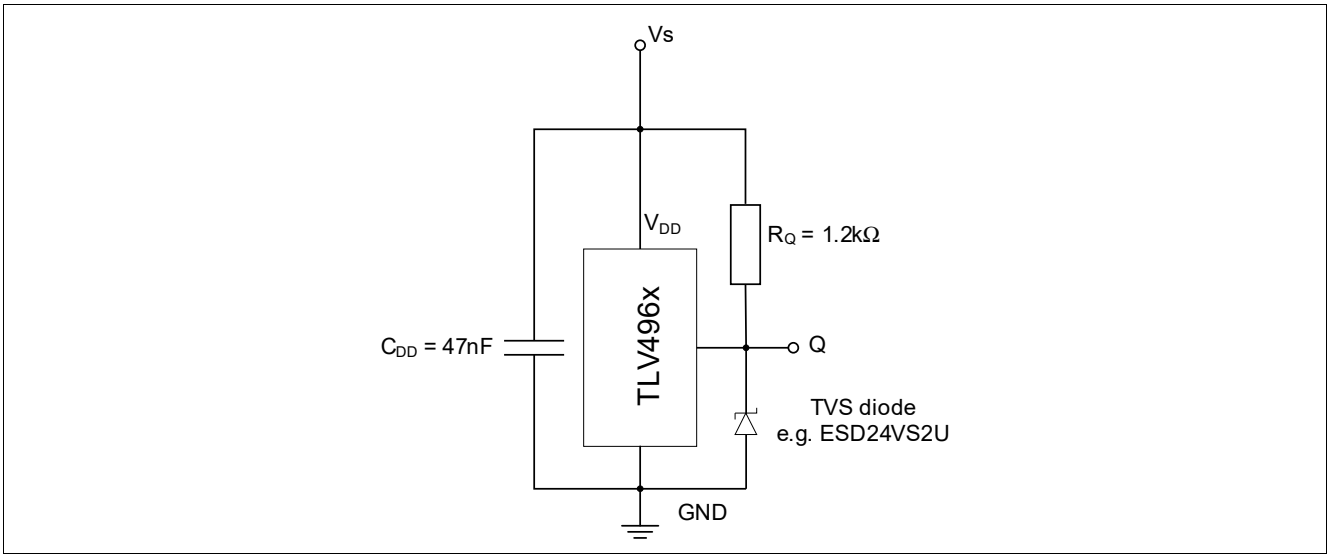


Figure 8 Enhanced application circuit #2: for extended ESD robustness

With an additional capacitor C_{DD} and a transient voltage suppression (TVS) diode an extended ESD robustness on system level is achieved (**Figure 8**).

3.2 Absolute maximum ratings

Table 3 Absolute maximum rating parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage[1)]	V_{DD}	3	–	26	V	–
Output voltage	V_Q	-0.5	–	26	V	–
Reverse output current	I_Q	-70	–	–	mA	–
Junction temperature[1)]	T_J	-40	–	150	°C	–
Storage temperature	T_S	-40	–	150	°C	–
Thermal resistance Junction ambient	R_{thJA}	–	–	250	K/W	for TO92S-3-1, TO92S-3-2 (2s2p)

1) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Calculation of the dissipated power P_{DIS} and junction temperature T_J of the chip (TO92S example):
e.g. for: V_{DD} = 12 V, I_S = 2.5 mA, V_{QSAT} = 0.5 V, I_Q = 20 mA
Power dissipation: P_{DIS} = 12 V x 2.5 mA + 0.5 V x 20 mA = 30 mW + 10 mW = 40 mW
Temperature $\Delta T = R_{thJA} \times P_{DIS}$ = 250 K/W x 40 mW = 10 K
For T_A = 50°C: $T_J = T_A + \Delta T$ = 50°C + 10 K = 60°C

Table 4 ESD protection[1] (T_A = 25°C)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
ESD voltage (HBM)[2]	V_{ESD}	-4	–	4	kV	R = 1.5 kΩ, C = 100 pF
ESD voltage (CDM)[3]	V_{ESD}	-1	–	1	kV	–

1) Characterization of ESD is carried out on a sample basis, not subject to production test.
2) Human Body Model (HBM) tests according to ANSI/ESDA/JEDEC JS-001.
3) Charge device model (CDM) tests according to JESD22-C101.

3.3 Operating range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLV4961-3T.

All parameters specified in the following sections refer to these operating conditions unless otherwise mentioned.

The maximum tested magnetic field is 600 mT.

Table 5 Operating conditions parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	3.0	–	26[1]	V	–
Output voltage	V_Q	3.0	–	26	V	–
Operation temperature	T_A	-40	–	125	°C	R_{thJA} ≤ 250 K/W
Output current	I_Q	0	–	25	mA	–

1) Latch-up test with factor 1.5 is not covered. Please see max ratings also.

3.4 Electrical and magnetic characteristics

Product characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production and correspond to V_{DD} = 12 V and T_A = 25°C. The below listed specification is valid in combination with the application circuit shown in **Figure 7** and **Figure 8**.

Table 6 General electrical characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply current	I_S	1.1	1.6	2.5	mA	–
Output current limitation	I_{QLIMIT}	30	56	70	mA	internally limited and thermal shutdown
Output fall time[1)]	t_f	0.17	0.4	1	µs	1.2 kΩ / 50 pF, see **Figure 4**
Output rise time[1)]	t_r	0.4	0.5	1	µs	1.2 kΩ / 50 pF, see **Figure 4**
Delay time[1)2)]	t_d	12	15	30	µs	see **Figure 4**
Power-on time[1)3)]	t_{PON}	–	80	150	µs	V_{DD} = 3 V, $B \le B_{RP}$ - 0.5 mT or $B \ge B_{OP}$ + 0.5 mT

1) Not subject to production test, verified by design/characterization.
2) Systematic delay between magnetic threshold reached and output switching.
3) Time from applying V_{DD} = 3.0 V to the sensor until the output is valid.

Table 7 Magnetic characteristics

Parameter	Symbol	T (°C)	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Operating point	B_{OP}	-40	5.2	8.4	11.5	mT	–
		25	4.6	7.5	10.4		
		125	3.6	6.2	8.7		
Release point	B_{RP}	-40	-11.5	-8.4	-5.2	mT	–
		25	-10.4	-7.5	-4.6		
		125	-8.7	-6.2	-3.6		
Hysteresis	B_{HYS}	-40	12.4	16.8	22.9	mT	–
		25	11.2	15.0	20.8		
		125	9.2	12.3	17.4		
Temperature compensation of magnetic thresholds[1)]	T_C	–	–	-1800	–	ppm/K	–

1) Not subject to production test, verified by design/characterization.

Field direction definition

Positive magnetic fields are defined with the south pole of the magnet to the branded side of package.

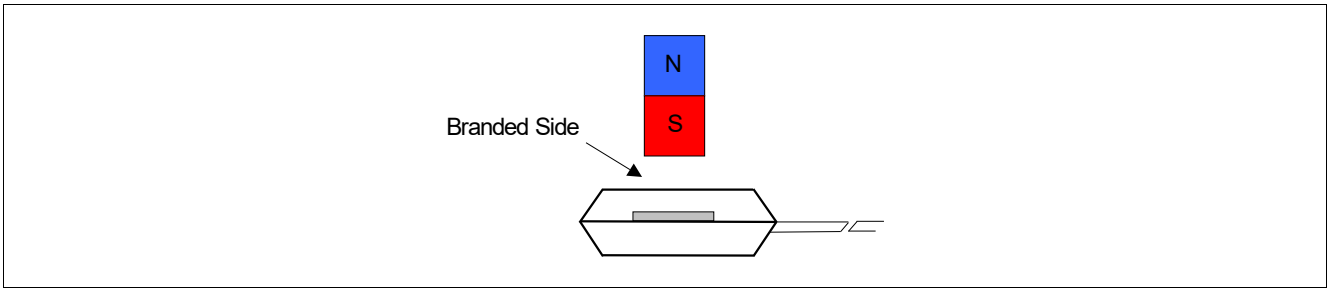


Figure 9 Definition of magnetic field direction TO92S-3-1, TO92S-3-2

4 Package information

The TLV4961-3TA is available in Bulk packing with TO92S-3-1-package.

The TLV4961-3TB is available in AMMO packing with TO92S-3-2-package.

4.1 Package outline

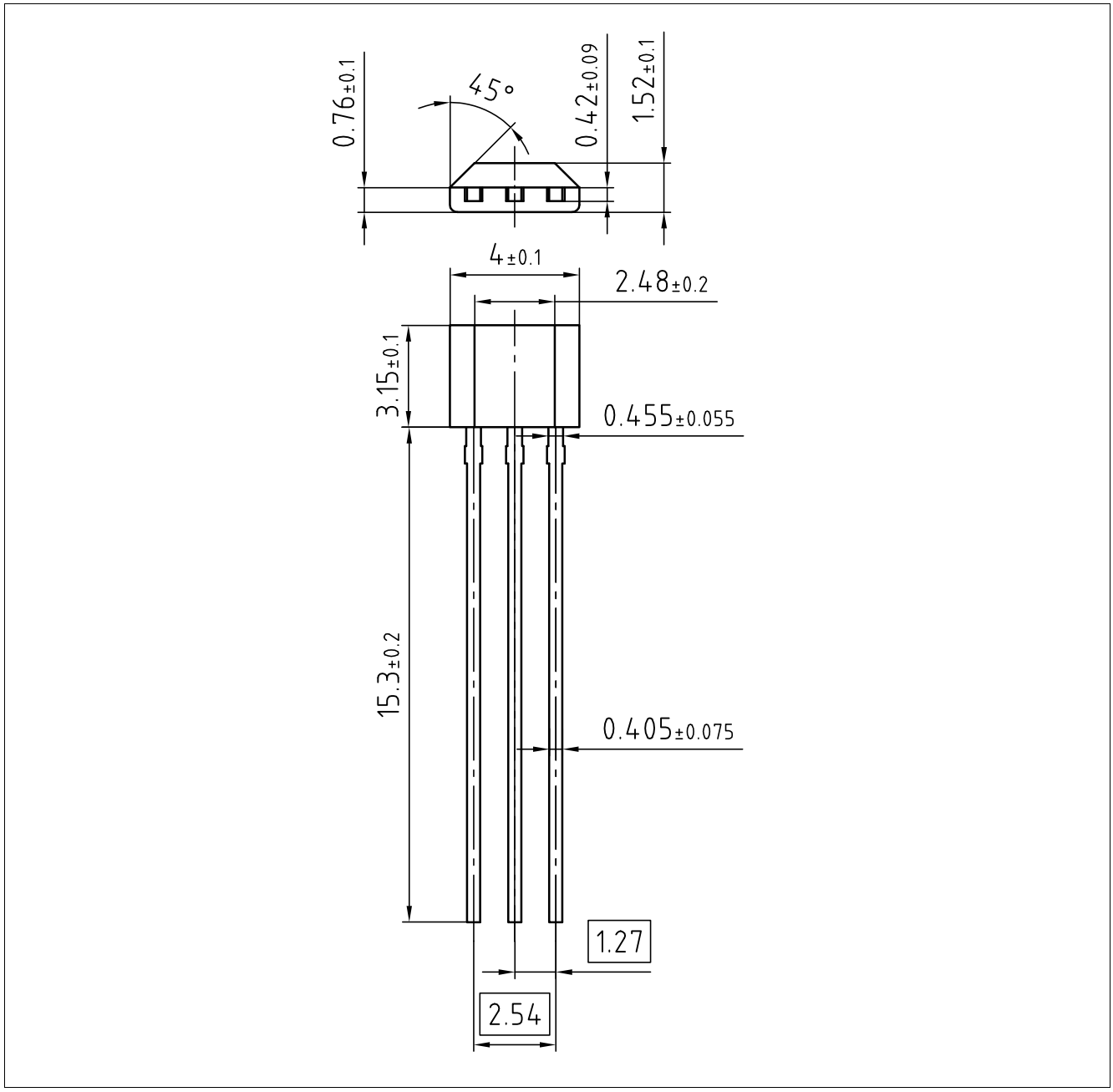


Figure 10 Package outline TLV4961-3TA: TO92S-3-1 (all dimensions in mm)

Package information

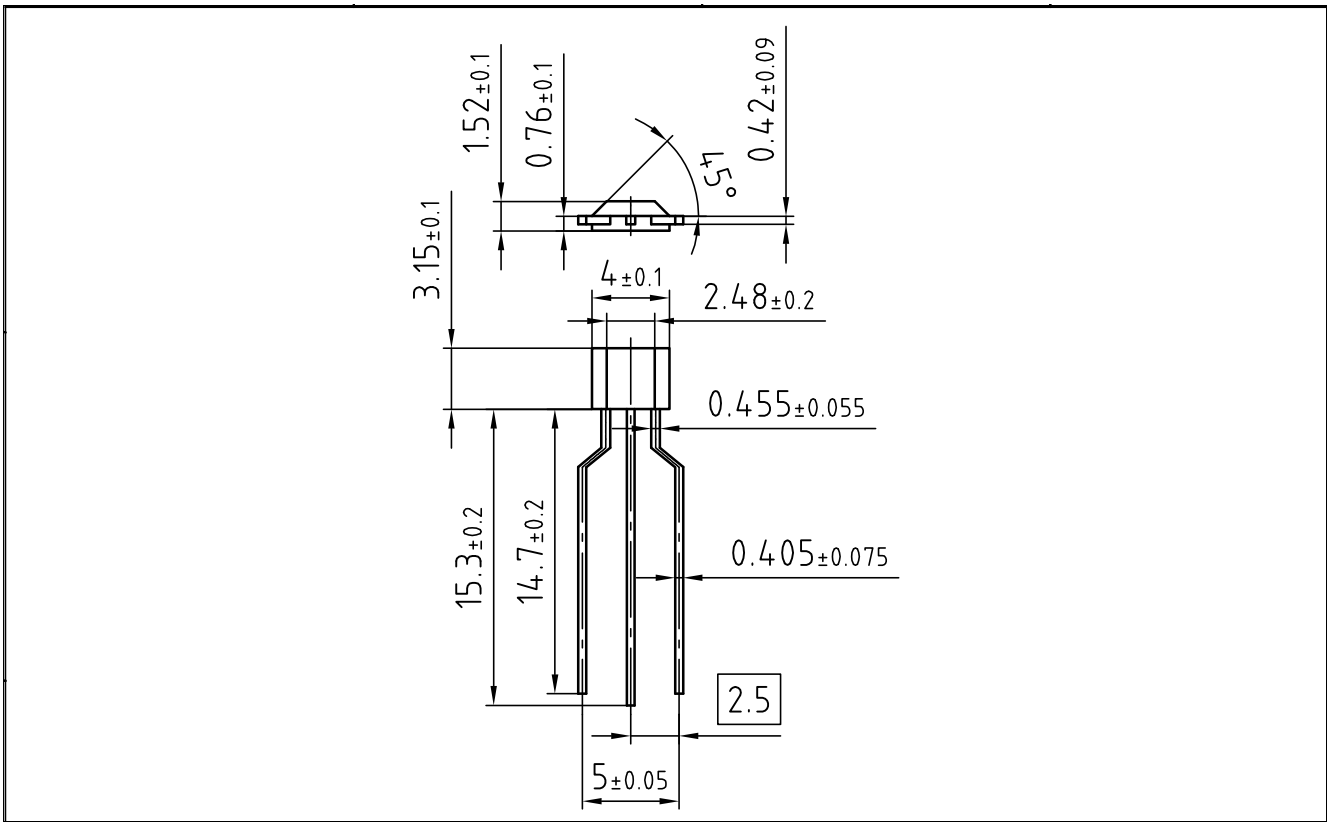


Figure 11 Package outline TLV4961-3TB: TO92S-3-2 (all dimensions in mm)

4.2 Packing information

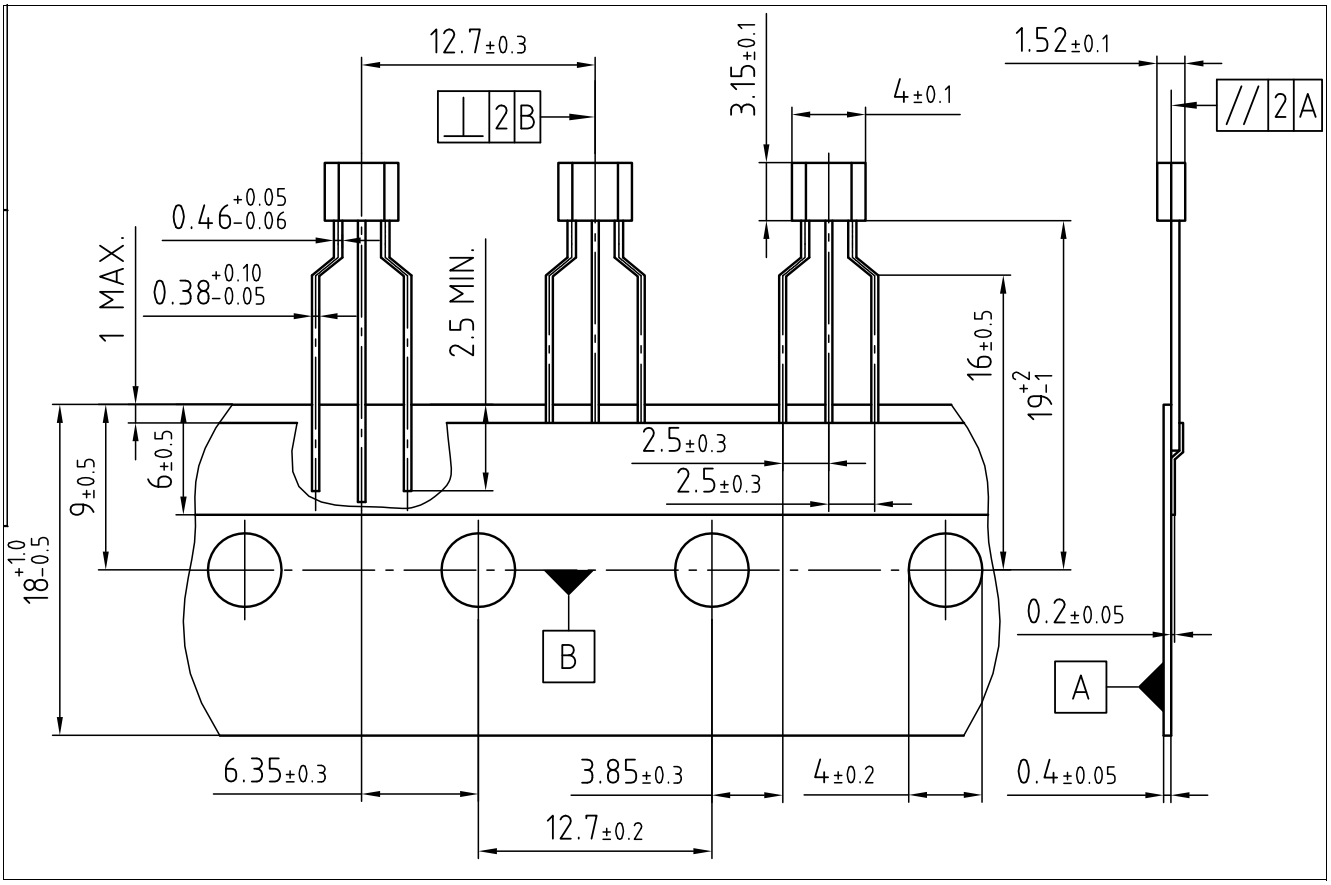


Figure 12 Packing information

4.3 Distance between chip and package

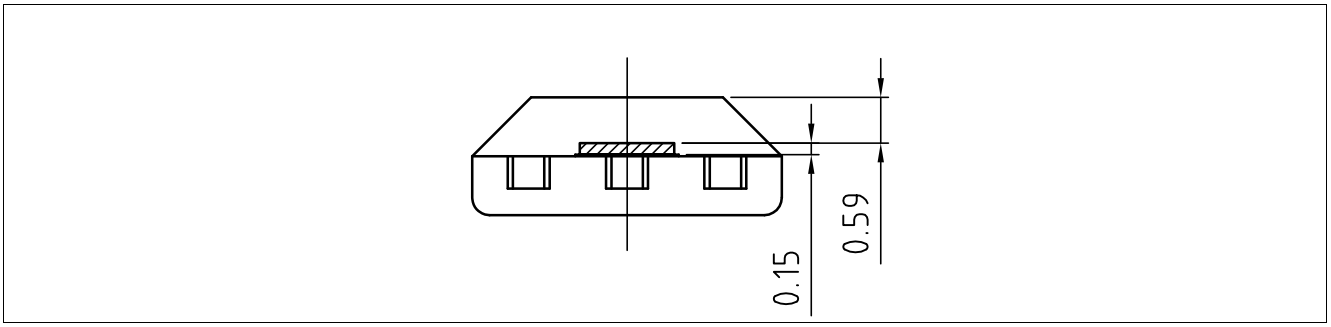


Figure 13 Distance between chip and package

4.4 Package marking

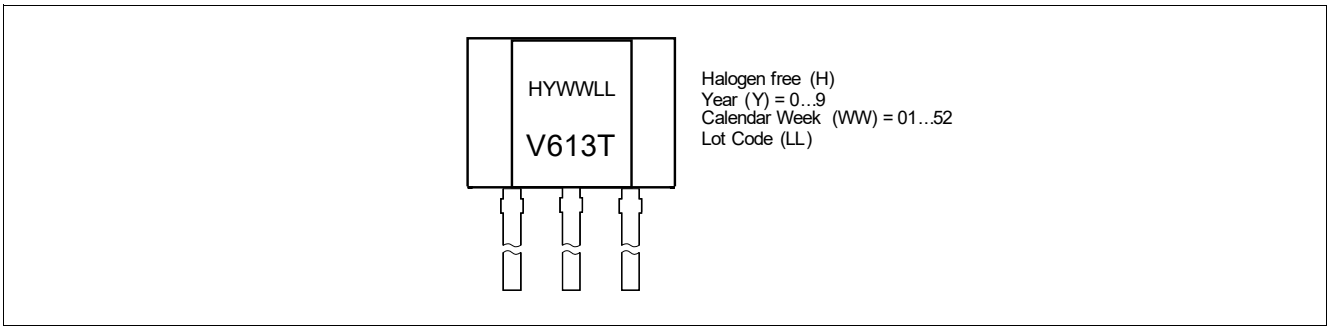


Figure 14 Marking of TLV4961-3T

5 Revision history

Revision	Date	Changes
Revision 1.2	2019-12-20	Updated text and figure in **Chapter 2.6** Updated standards in **Table 4** Added maximum tested magnetic field in **Chapter 3.3** Editorial changes
Revision 1.0	2015-05-18	Initial release

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