MPM3822C

2.75 - 6V, 2A, Ultra-Small and Ultra-Low Noise Power Module

DESCRIPTION

The MPM3822C is a synchronous, step-down, power module with an integrated inductor. The MPM3822C achieves 2A of continuous output current from a 2.75V to 6V input voltage range with excellent load and line regulation. The MPM3822C works in forced continuous conduction mode (CCM) and has a voltage ripple less than 10mV with one output capacitor, making it suitable for optical modules, FGPA, ASIC, and other applications requiring low ripple noise. The output voltage can be regulated as low as 0.6V. Only FB resistors, input capacitors, and output capacitors are needed to complete the design.

The constant-on-time control (COT) scheme provides fast transient response, high efficiency, and easy loop stabilization.

Full protection features include cycle-by-cycle current limiting and thermal shutdown.

The MPM3822C requires a minimal number of readily available, standard, external components and is available in an ultra-small QFN-18 (2.5mmx3.5mmx1.6mm) package.

FEATURES

- Wide 2.75V to 6V Operating Input Range
- Adjustable Output from 0.6V
- Low Radiated Emissions (EMI) Complies with EN55022 Class B Standard
- Up to 2A Continuous Output Current
- 100% Duty Cycle in Dropout
- Forced Continuous Conduction Mode (CCM)
- Enable (EN) and Power Good (PG) for Power Sequencing
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Only Four External Components Requires
- Available in a QFN-18 (2.5mmx3.5mmx 1.6mm) Package

APPLICATIONS

- FPGA, ASIC, DSP Power
- Optical Modules
- LDO Replacements
- Power for Portable Products
- Storage (SSD/HDD)
- Space-Limited Applications

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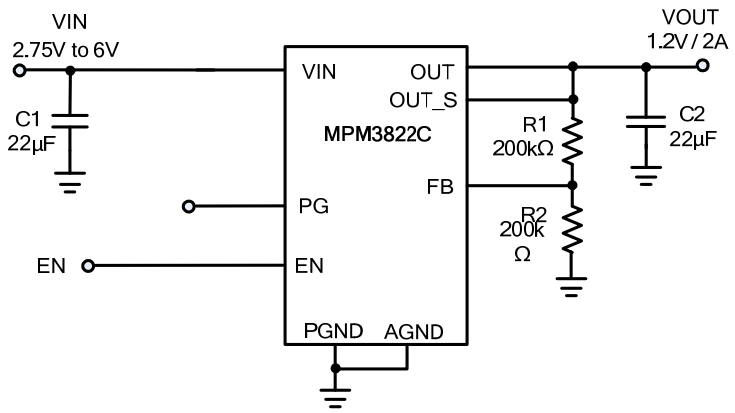
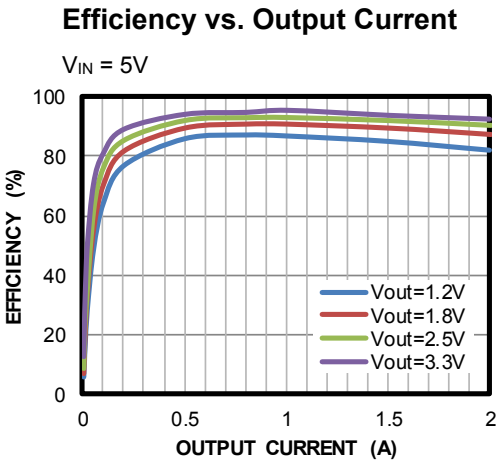
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM3822CGRH	QFN-18 (2.5mmx3.5mmx1.6mm)	*See Below*

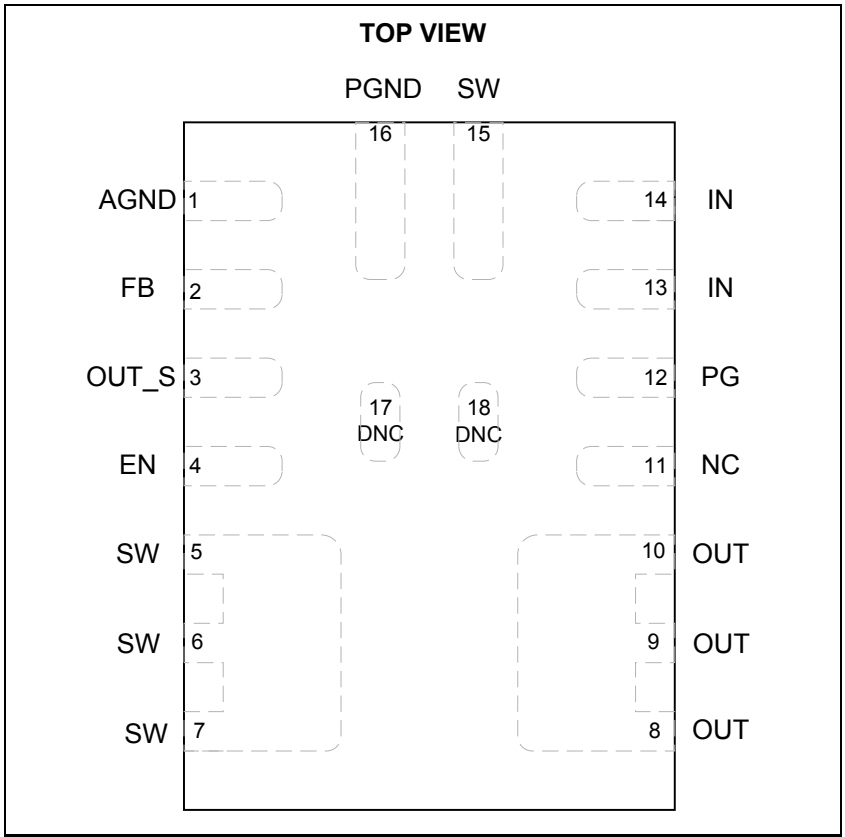
* For Tape & Reel, add suffix –Z (e.g.: MPM3822CGRH–Z).

TOP MARKING

BFV
YWW
LLL

BFV: Product code of MPM3822CGRH
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-18 (2.5mmx3.5mmx1.6mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	AGND	**Analog ground for the internal control circuit.**
2	FB	**Feedback.** Use an external resistor divider from the output to GND tapped to FB to set the output voltage.
3	OUT_S	**Output voltage sense.**
4	EN	**On/off control.**
5 - 7, 15	SW	**Switch output.**
8 - 10	OUT	**Power output.**
11	NC	**No connection.** Float NC or connect NC to GND.
12	PG	**Power good indicator.** The output of PG is an open drain with an internal pull-up resistor to IN. PG is pulled up to IN when the FB voltage is within 10% of the regulation level; otherwise, PG is low.
13, 14	IN	**Supply voltage to internal control circuitry.**
16	PGND	**Power ground.**
17,18	DNC	**No connection.** Leave DNC floating.

ABSOLUTE MAXIMUM RATINGS (1)

V_{SW} ..... -0.3V (-5V for <10ns) to 6.5V (10V for <10ns)
All other pins ..... -0.3V to +6.5V
Junction temperature ..... 150°C
Lead temperature..... 260°C
Continuous power dissipation (T_A = +25°C) (2)(4)
QFN-18 ..... 3W
Storage temperature .....-65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.75V to 6V
Operating junction temp. (T_J)....-40°C to +150°C

Thermal Resistance	θ_{JA}	θ_{JC}	
EVM3822C-RH-00A (4)	42	13	°C/W
JESD51-7 (5)	50	12	°C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EVM3822C-RH-00A, 2-layer PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback voltage	V_{FB}	2.75V ≤ V_{IN} ≤ 6V	591	600	609	mV
Feedback current	I_{FB}	V_{FB} = 0.6V		10		nA
Inductor L value	L	Inductance value at 1MHz		1		μH
Dropout resistance	R_{DR}	100% on duty		130		mΩ
Switch leakage		V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V and 6V, T_J = 25°C		0	2	μA
P-FET peak current limit			2.8	5.6		A
N-FET valley current limit (6)				1.5		A
On time	T_{ON}	V_{IN} = 5V, V_{OUT} = 1.2V		185		ns
		V_{IN} = 3.6V, V_{OUT} = 1.2V		250		
Switching frequency	F_s	V_{OUT} = 1.2V, I_{LOAD} = 1A		1150		kHz
Minimum off time	$T_{MIN-OFF}$			230		ns
Minimum on time (6)	T_{MIN-On}			80		ns
Soft-start time (6)	T_{SS-ON}			1.3		ms
Soft-stop time	T_{SS-OFF}			1.7		ms
Power good upper trip threshold		FB voltage in respect to the regulation		+10		%
Power good lower trip threshold				-10		%
Power good delay				100		μs
Power good sink current capability	V_{PG_LO}	Sink 1mA			0.4	V
Power good logic high voltage	V_{PG_HI}	V_{IN} = 5V, V_{FB} = 0.6V	4			V
Power good internal pull-up resistor	R_{PG}			440		kΩ
Under-voltage lockout threshold rising			2.3	2.5	2.75	V
Under-voltage lockout threshold hysteresis				400		mV
EN input logic low voltage					0.3	V
EN input logic high voltage			1.2			V
EN input current		V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		μA
Supply current (shutdown)		V_{EN} = 0V, T_J = 25°C		0	1	μA
Supply current (quiescent)		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 3.6V		500		μA
Thermal shutdown (7)				160		°C
Thermal hysteresis (7)				30		°C

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Converter System (6)						
Output voltage range			0.6		6	V
Recommended input capacitance	C_{IN1}	V_{IN} = 3.6V, V_{OUT} = 1.2V, I_{OUT} = 2A	4.7	22		µF
Output capacitance	C_{OUT1}	V_{IN} = 3.6V, V_{OUT} = 1.2V, I_{OUT} = 2A	10	22	100	µF
Output ripple		V_{IN} = 3.6V, V_{OUT} = 1.2V, C_{OUT} = 22µF, I_{OUT} = 2A		5		mV
Efficiency		V_{IN} = 3.6V, V_{OUT} = 1.2V, I_{OUT} = 2A		82		%
Load transient peak-to-peak voltage	V_{P2P1}	V_{IN} = 3.6V, V_{OUT} = 1.2V, C_{OUT} = 22µF, I_{OUT} = 0 to 2A @ 1A/µs			100	mV

NOTES:
6) Derived from engineering sample test, not tested in production.
7) Derived from characterization test, not tested in production.

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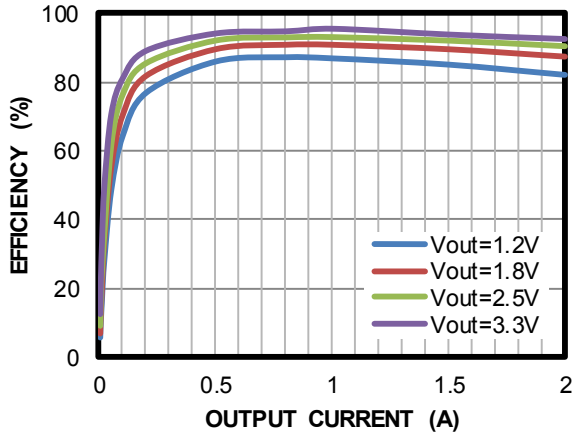
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

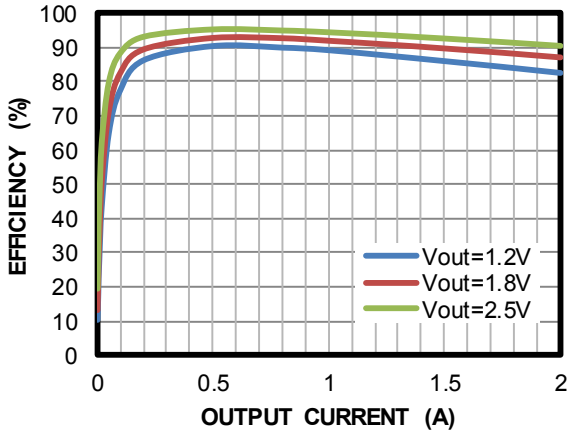
Efficiency vs. Output Current

V_{IN} = 5V

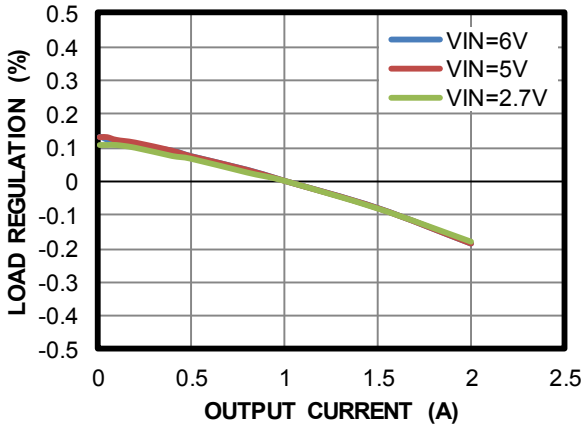


Efficiency vs. Output Current

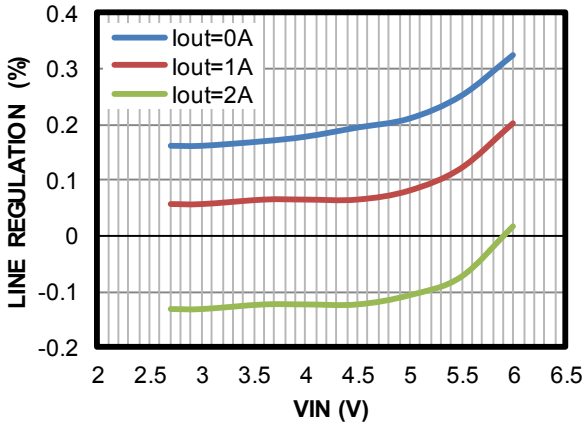
V_{IN} = 3.6V



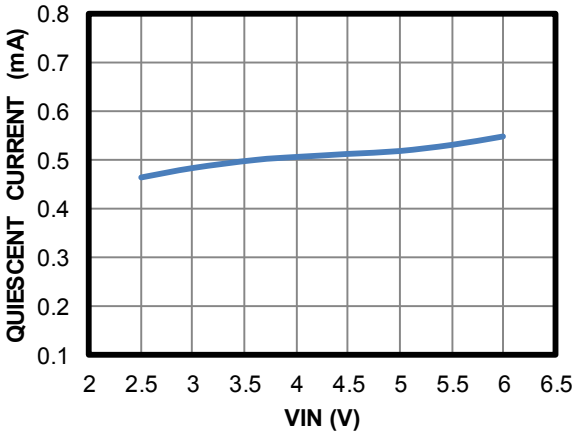
Load Regulation vs. Output Current



Line Regulation vs. V_{IN}

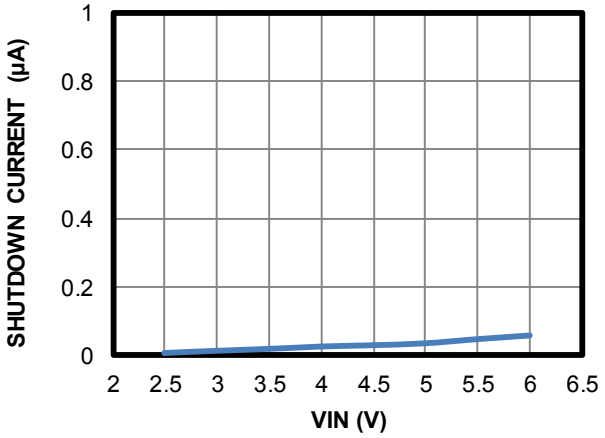


Quiescent Current vs. V_{IN}



Shutdown Current vs. V_{IN}

V_{IN} = 5V



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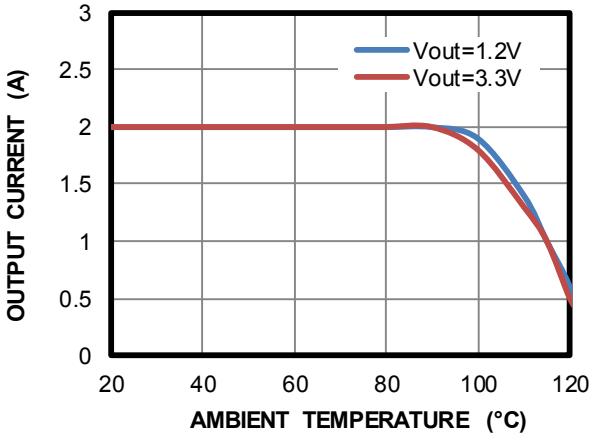
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

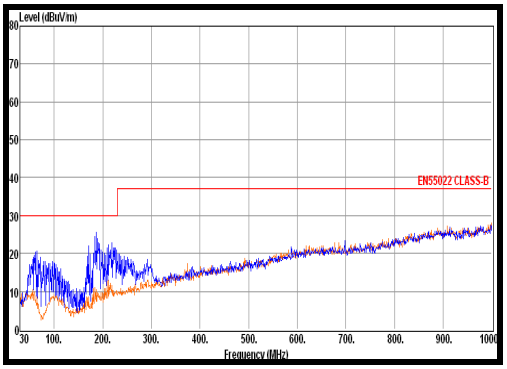
Output Current vs. Ambient Temperature

T_J < 125°C

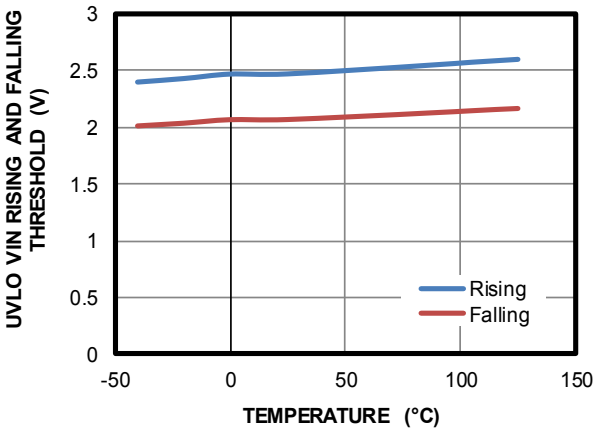


Radiated Emission

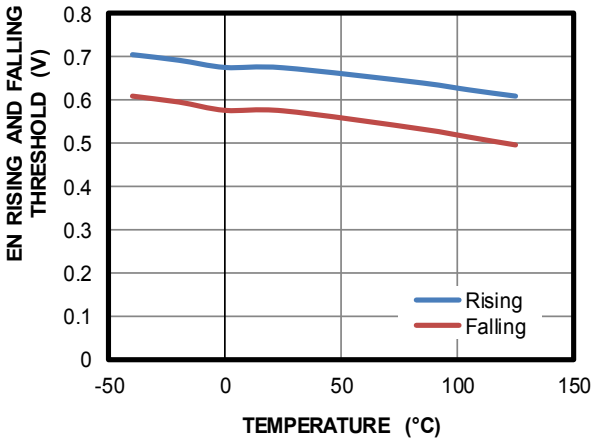
I_{OUT} = 2A, tested on EVM3822C-RH-00A



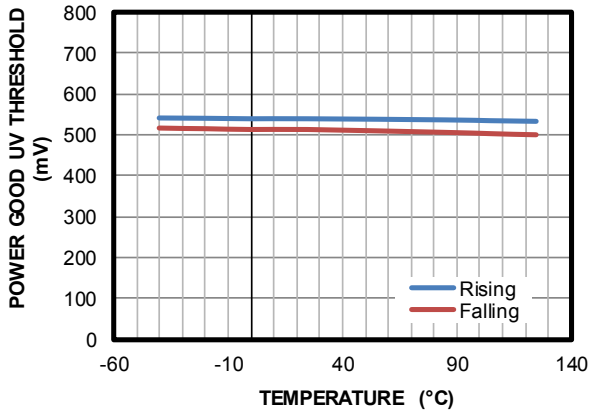
UVLO V_{IN} Rising and Falling Threshold vs. Temperature



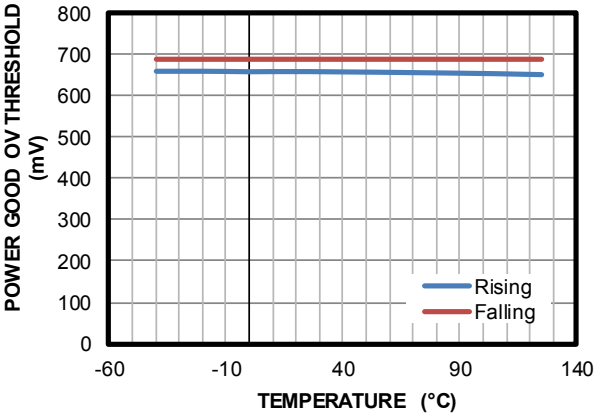
EN Rising and Falling Threshold vs. Temperature



Power Good UV Threshold vs. Temperature



Power Good OV Threshold vs. Temperature



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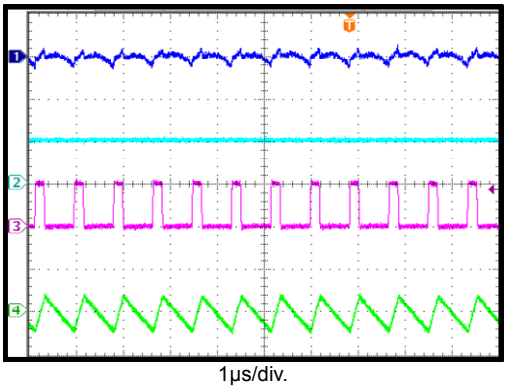
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{OUT} = 1.2V, Co = 22µF, T_A = 25°C, unless otherwise noted.

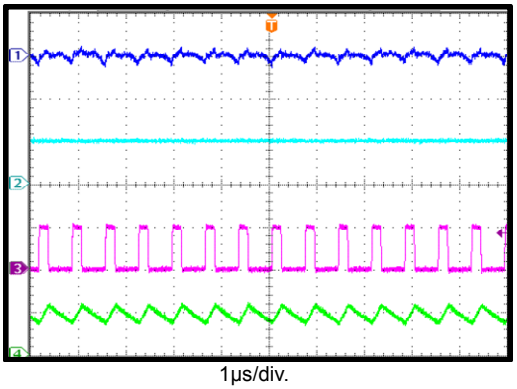
Steady State

I_{OUT} = 0A



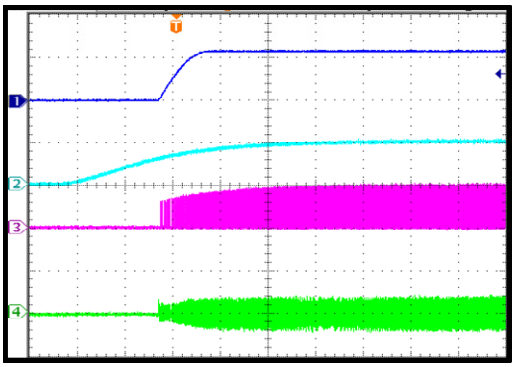
Steady State

I_{OUT} = 2A



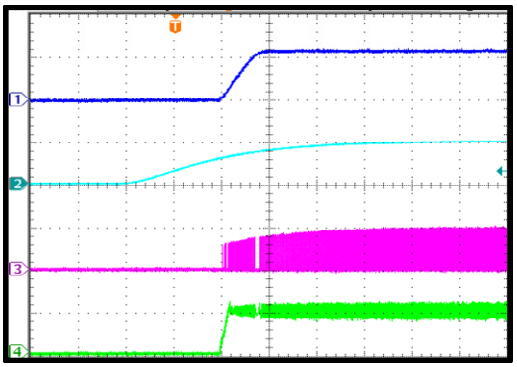
V_{IN} Start-Up

I_{OUT} = 0A



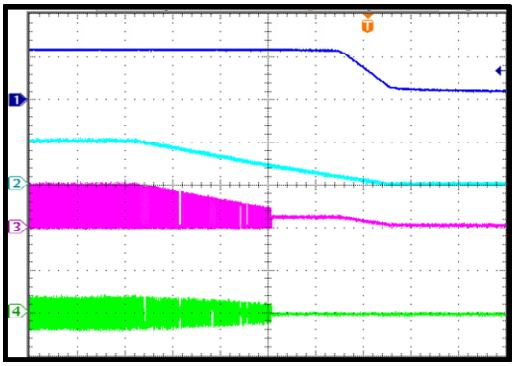
V_{IN} Start-Up

I_{OUT} = 2A



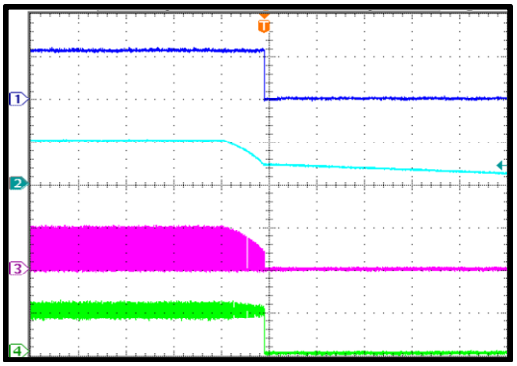
V_{IN} Shutdown

I_{OUT} = 0A



V_{IN} Shutdown

I_{OUT} = 2A



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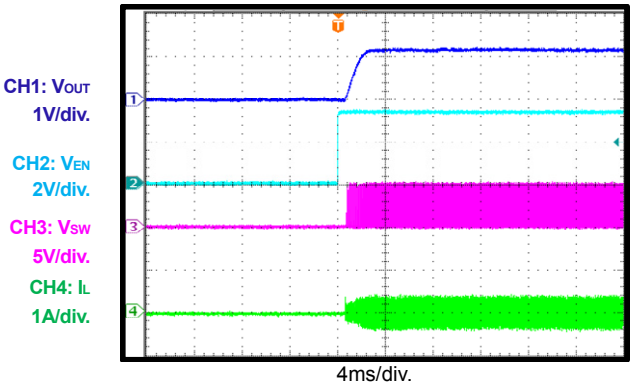
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{OUT} = 1.2V, Co = 22µF, T_A = 25°C, unless otherwise noted.

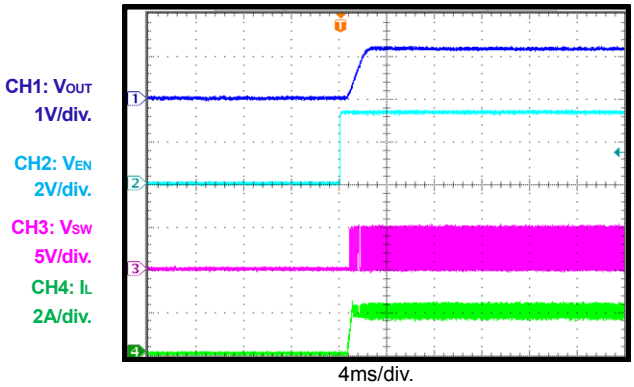
EN On

I_{OUT} = 0A



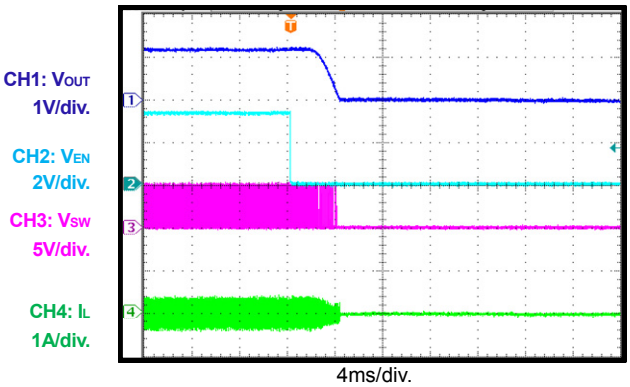
EN On

I_{OUT} = 2A



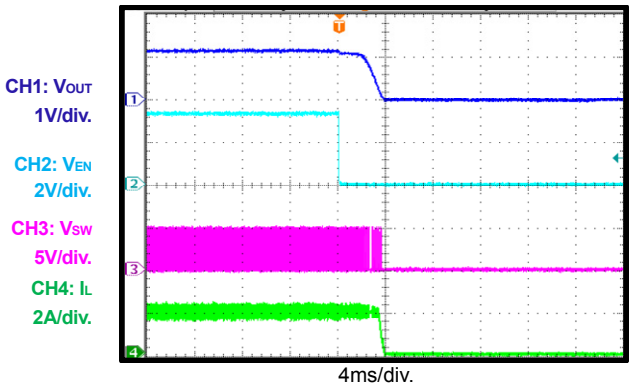
EN Off

I_{OUT} = 0A



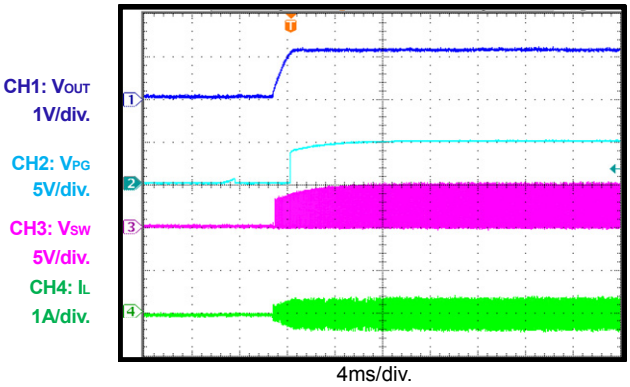
EN Off

I_{OUT} = 2A



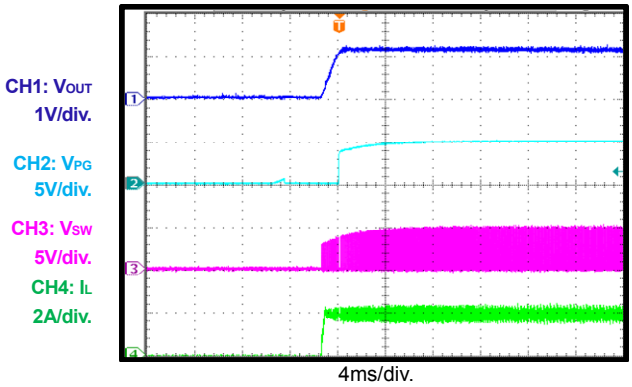
Power Good On

I_{OUT} = 0A



Power Good On

I_{OUT} = 2A



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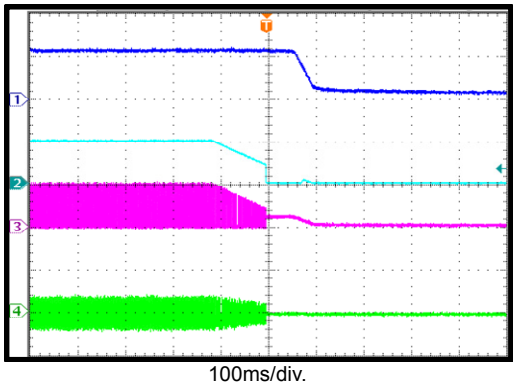
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{OUT} = 1.2V, Co = 22µF, T_A = 25°C, unless otherwise noted.

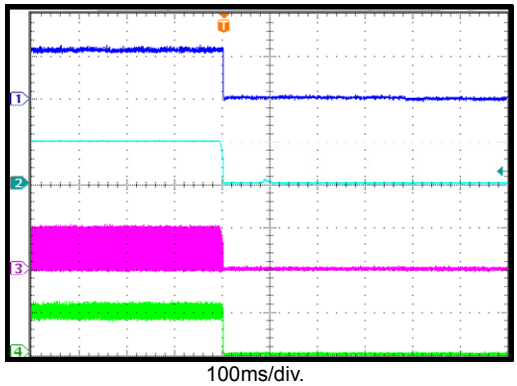
Power Good Off

I_{OUT} = 0A



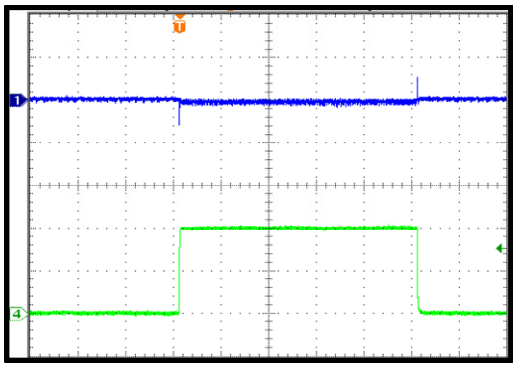
Power Good Off

I_{OUT} = 2A



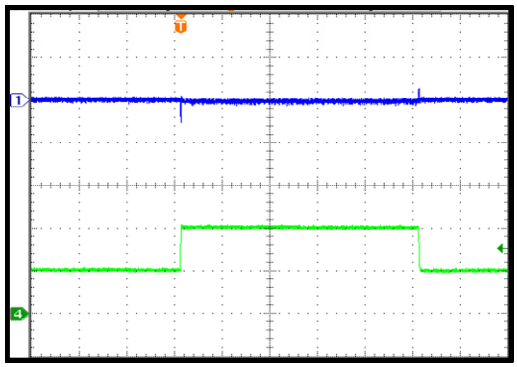
Load Transient

I_{OUT} = 0 - 2A, 2.5A/µs

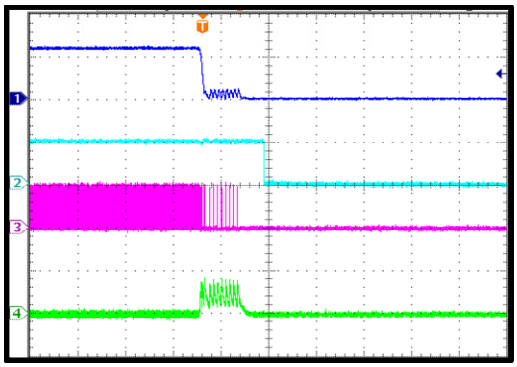


Load Transient

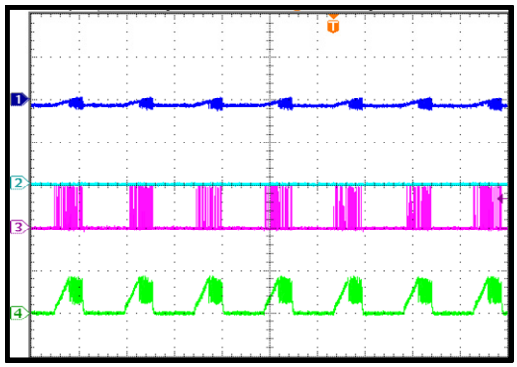
I_{OUT} = 1 - 2A, 2.5A/µs



Short Entry



Short Steady State



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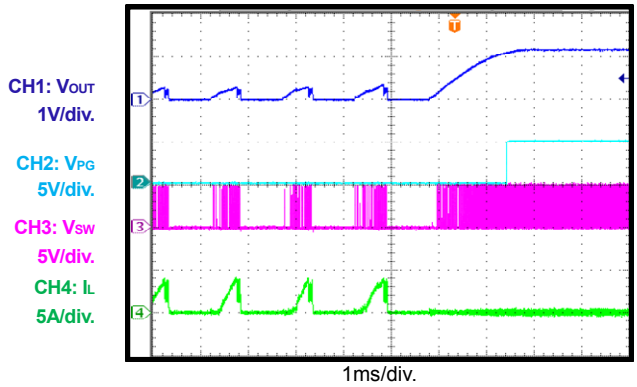
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{OUT} = 1.2V, Co = 22µF, T_A = 25°C, unless otherwise noted.

Short Recovery

I_{OUT} = 0A



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BLOCK DIAGRAM

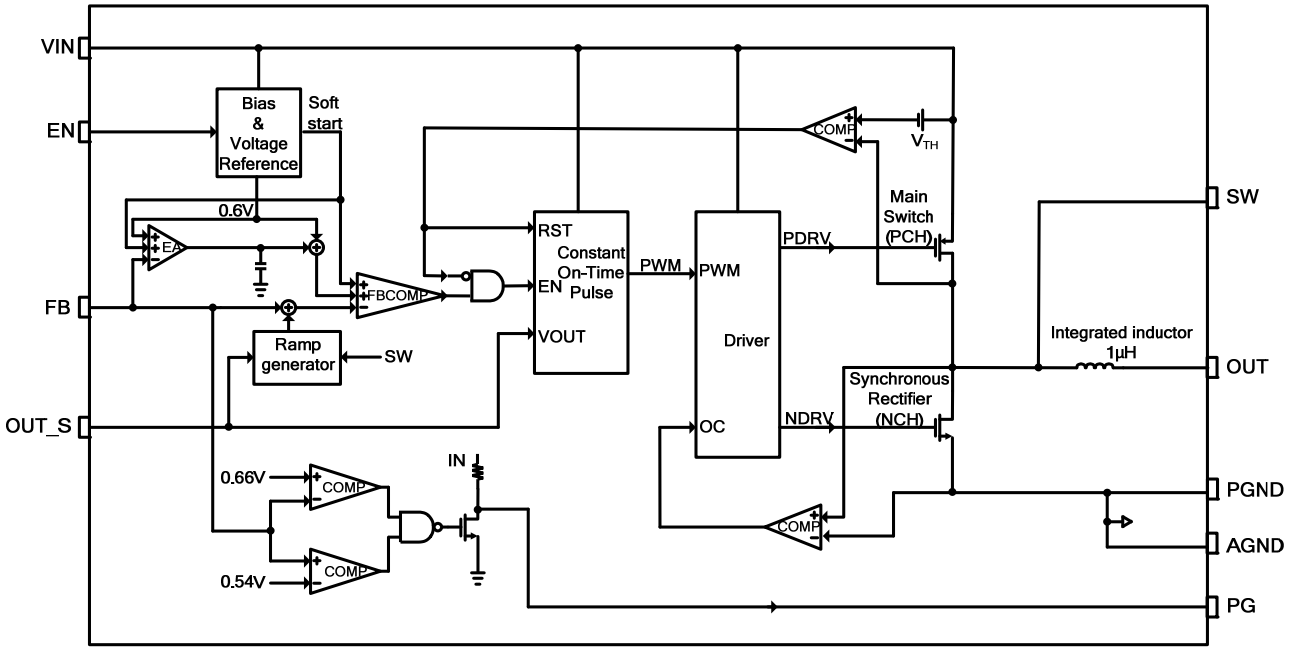

Figure 1: Functional Block Diagram

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OPERATION

The MPM3822C comes in a small surface-mounted QFN-18 (2.5mmx3.5mmx1.6mm) package. The MPM3822C's integrated inductor simplifies the schematic and layout design. Only FB resistors, input capacitors, and output capacitors are needed to complete the design. The MPM3822C uses constant-on-time (COT) control with input voltage feed-forward to stabilize the switching frequency over the full input range.

Constant-On-Time Control (COT)

Compared to fixed-frequency pulse-width modulation (PWM) control, COT control offers the advantage of a simpler control loop and faster transient response. By using input voltage feed-forward, the MPM3822C maintains a nearly constant switching frequency across the input and output voltage ranges. The on time of the switching pulse can be estimated with Equation (1):

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.833\mu s \quad (1)$$

To prevent inductor current runaway during the load transition, the MPM3822C fixes the minimum off time at 230ns. This minimum off-time limit does not affect operation during steady state.

Forced PWM Operation

The MPM3822C works in continuous current mode (CCM) to achieve a smaller V_{OUT} ripple, load regulation, and load transient in the full load range.

Enable (EN)

If the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 2.5V), the MPM3822C can be enabled by pulling EN above 1.2V. Leave EN floating or pull EN down to ground to disable the MPM3822C. There is an internal 1MΩ resistor from EN to ground.

Soft Start/Stop

The MPM3822C has a built-in soft start that ramps up the output voltage at a controlled slew rate to prevent overshoots during start-up. The soft-start time is about 1.3ms, typically.

When disabled, the MPM3822C ramps down the internal reference, so the load can discharge the output linearly. The soft-stop time is 1.7ms, typically.

Power Good Indicator (PG)

The MPM3822C has an open drain with a 440kΩ pull-up resistor pin for power good indication (PG). When FB is within ±10% of the regulation voltage (0.6V), PG is pulled up to IN by the internal resistor. If the FB voltage is out of the ±10% window, PG is pulled down to ground by an internal MOSFET. The MOSFET has a maximum $R_{DS(ON)}$ of less than 100Ω.

Current Limit

The MPM3822C high-side switch has a typical 5.6A current limit, and the low-side switch has a 1.5A current limit. When the high-side switch reaches its current limit, the high-side is turned off, and the low-side is turned on. When the current drops to the valley current-limit threshold, the MPM3822C turns on the high-side again. If the high-side reaches the peak current limit and the low-side reaches the valley current limit in every cycle for 100µs, the MPM3822C remains at the hiccup threshold until the current decreases. This prevents the inductor current from continuing to build and damaging components.

Short Circuit and Recovery

If the output voltage is shorted to GND, the current limit is triggered. If the current limit is triggered every cycle for 100µs, the MPM3822C enters hiccup mode and disables the output power stage. The MPM3822C discharges the soft-start capacitor, and then attempts to soft start again automatically. If the short-circuit condition still remains after the soft start ends, the MPM3822C repeats this operation cycle until the short circuit is removed and the output rises back to the regulation level.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage. The feedback resistor (R1) cannot be too large or too small considering the trade-off for stability and dynamics. There is no strict requirement for the feedback resistor. R2 can be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1} \quad (2)$$

The feedback circuit is shown in Figure 2.

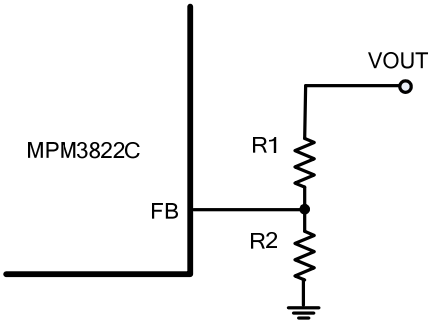

Figure 2: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current while maintaining the DC input voltage. For optimal performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22μF capacitor is sufficient

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (i.e.: 0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Output Capacitor

An output capacitor (C2) is required to maintain the DC output voltage.

Low ESR ceramic capacitors can be used to keep the output ripple low. Generally, a 22μF output ceramic capacitor is sufficient for most applications. In higher output voltage conditions, a 47μF capacitor may be required for a stable system.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

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When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (7)$$

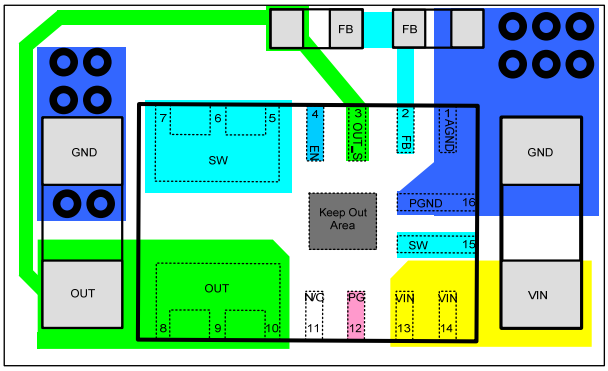
Where L1 is a 1μH integrated inductor.

The characteristics of the output capacitor affect the stability of the regulation system.

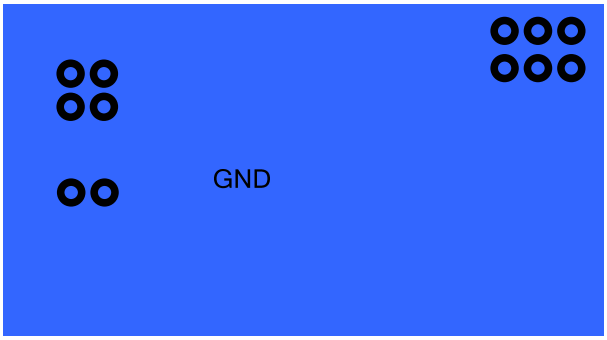
PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation, especially for the high switching converter. If the layout is not done carefully, the regulator could show poor line or load regulation or stability issues. For best results, refer to Figure 3 and follow the guidelines below.

1. Place the 0805 size ceramic input capacitor as close to the IC pins as possible.
2. Connect the two ends of the ceramic capacitor to VIN and PGND directly.
3. Add copper to SW for power dissipation.
4. Place the external feedback resistor next to FB.



Top Layer



Bottom Layer

Figure 3: Recommended Layout

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TYPICAL APPLICATION CIRCUITS

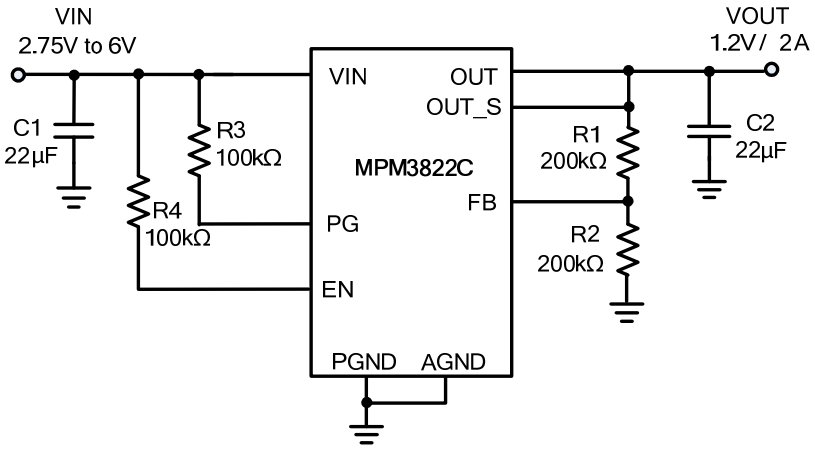

Figure 4: Typical Application Circuits for MPM3822C

NOTE: VIN < 3.3V applications may require additional input capacitors.

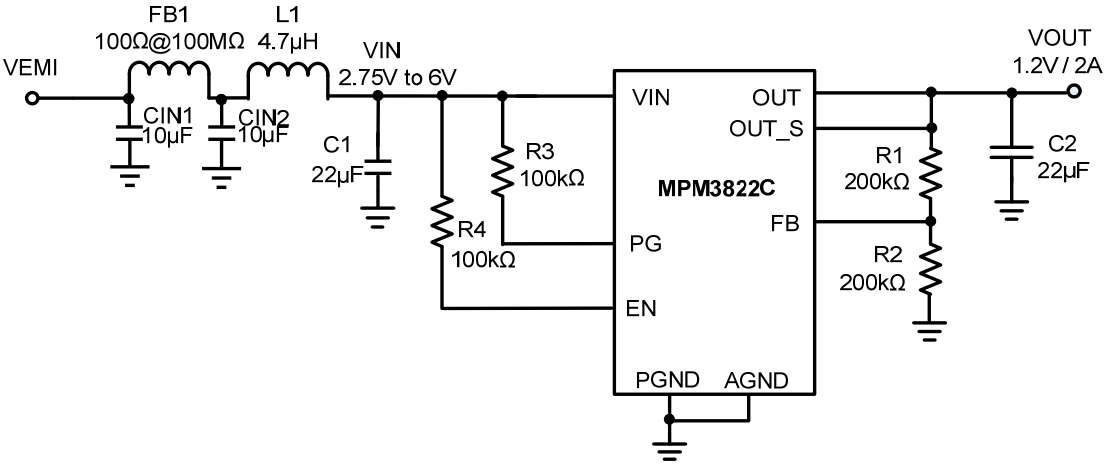

Figure 5: EMI Test Circuits for the MPM3822C

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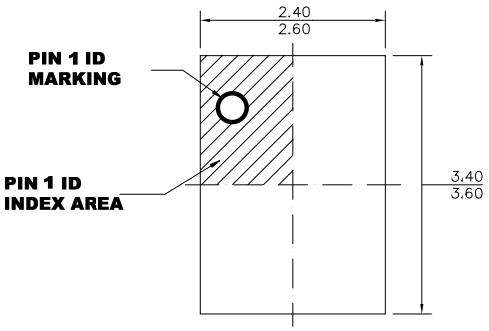
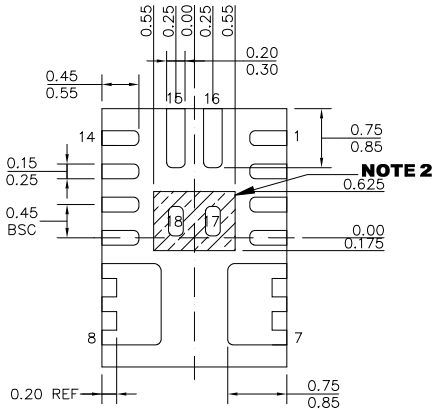
PACKAGE INFORMATION

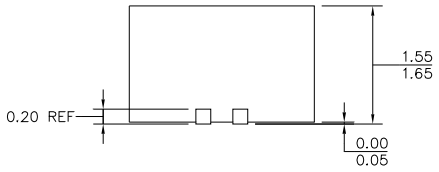
QFN-18 (2.5mmx3.5mmx1.6mm)



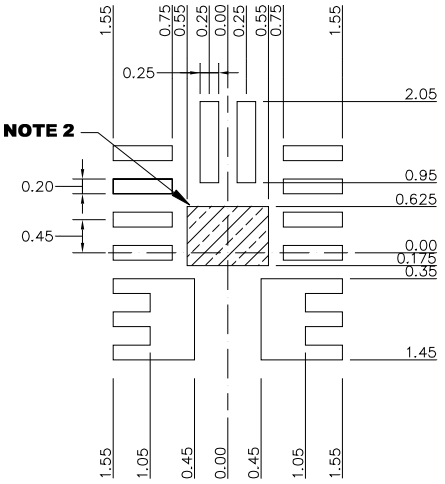
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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