Migrating from MX30LF2G18AC to MX30LF2G28AD

1. Introduction

This application note is a guide for migrating Macronix NAND device from the MX30LF2G18AC to the MX30LF2G28AD. The document does not provide detailed information on the individual devices, but highlights the major similarities and differences between them. The comparison covers the general features, performance, command codes and other differences.

The information in this document is based on datasheets listed in Section 8. Newer versions of the datasheets may override the contents of this document.

2. General Features

Feature differences are highlighted in ***Bold Italic*** type in the table.

Table 2-1. Key Features Comparison

Part Name	MX30LF2G18AC	MX30LF2G28***AD***
Voltage	2.7V-3.6V	2.7V-3.6V
Bus Width	x8	x8
Operating Temperature	-40°C to 85°C	***-40˚C to 85˚C***
Interface	ONFI 1.0 Compliant	ONFI 1.0 Compliant
Page Size	(2K+64)B	(***2K+128***)B
Block Size	(128K+4K)B	***(128K+8K)***B
ECC Requirement	4bit/528B	8bit/***544***B
Cache Read/ Cache Program	ONFI Standard	ONFI Standard
OTP	30 Pages	30 Pages
Unique ID	ONFI Standard	ONFI Standard ***(PUF type)***[note]
Block Protection	PT pin & BP Bits	PT pin & BP Bits
Randomizer	N/A	***Supported***
Special Read for Data Recovery	N/A	***Supported***
Guaranteed Good Blocks at Shipping	Block#0	***Block#0-7***
Data Retention	10 Years	10 Years
Endurance	100K Cycles	***60***K Cycles
Package	48TSOP (12x20mm) 63-VFBGA (9x11mm)	48TSOP (12x20mm) 63-VFBGA (9x11mm)

3. Electrical Performance

The key performance specifications are similar for the two devices. Performance differences are highlighted in Bold Italic type in **Table 3-1**.

Table 3-1. Key Performance Comparison

Part Name		MX30LF2G18AC			MX30LF2G28*AD*		
Performance		Min.	Typ.	Max.	Min.	Typ.	Max.
Access Time	Random (tR)	-	-	25us	-	-	25us
	Cache Read Busy time	-	3.5us	25us	-	***4.5us***	25us
	Sequential	20ns	-	-	20ns	-	-
Program Time	Page Program	-	300us	600us	-	***320us***	***700us***
	Cache Program Busy time	-	5us	600us	-	5us	***700us***
Erase Time	Block	-	1ms	3.5ms	-	***4ms***	***6ms***
Current Consumption	Standby (TTL)	-	-	1mA	-	-	1mA
	Standby (CMOS)	-	10uA	50uA	-	10uA	50uA
	Active Read	-	15mA	30mA	-	***20mA***	30mA
	Active Program	-	15mA	30mA	-	***20mA***	30mA
	Active Erase	-	15mA	30mA	-	***20mA***	30mA
	Power-up Current (Including POR Current)	-	-	50mA	-	-	50mA
	Input Leakage	-	-	+/- 10uA	-	-	+/- 10uA
	Output Leakage	-	-	+/- 10uA	-	-	+/- 10uA
Partial-Page Programs	NOP	-	-	4 cycles	-	-	4 cycles

4. Command Set

The command set is the same for the two devices (**Table 4-1 Command Set**).

Table 4-1. Command Set

Part Name	MX30LF2G18AC		MX30LF2G28*AD*	
Command Description	1st Command Cycle	2nd Command Cycle	1st Command Cycle	2nd Command Cycle
Read	00h	30h	00h	30h
Random Data Input	85h	-	85h	-
Random Read Data Output	05h	E0h	05h	E0h
Cache Read Random	00h	31h	00h	31h
Cache Read Sequential	31h	-	31h	-
Cache Read End	3Fh	-	3Fh	-
Read ID	90h	-	90h	-
Parameter Page Read (ONFI)	ECh	-	ECh	-
Read Unique ID (ONFI)	EDh	-	EDh	-
Get Features (ONFI)	EEh	-	EEh	-
Set Features (ONFI)	EFh	-	EFh	-
Reset	FFh	-	FFh	-
Page Program	80h	10h	80h	10h
Cache Program (Start)	80h	15h	80h	15h
Cache Program (End)	80h	10h	80h	10h
Block Erase	60h	D0h	60h	D0h
Status Read	70h	-	70h	-
Status Enhanced Read (ONFI)	78h	-	78h	-
Block Protection Status Read	7Ah	-	7Ah	-
Two-plane Program (ONFI)	80h-11h-80h-10h		80h-11h-80h-10h	
Two-plane Cache Program - Start/Cont.(ONFI)	80h-11h-80h-15h		80h-11h-80h-15h	
Two-plane Cache Program - End (ONFI)	80h-11h-80h-10h		80h-11h-80h-10h	
Two-plane Block Erase (ONFI)	60h-D1h-60h-D0h		60h-D1h-60h-D0h	
Two-plane Program (Traditional)	80h-11h-81h-10h		80h-11h-81h-10h	
Two-plane Cache Program- Start/Cont. (Traditional)	80h-11h-81h-15h		80h-11h-81h-15h	
Two-plane Cache Program- End (Traditional)	80h-11h-81h-10h		80h-11h-81h-10h	
Two-plane Block Erase (Traditional)	60h-60h-D0h		60h-60h-D0h	

5. Status Register Comparison

Status Register bit functions are the same (**Table 5-1 Status Register Comparison**). Please refer to the Macronix datasheet for additional details.

Table 5-1. Status Register Comparison

Part Name	MX30LF2G18AC	MX30LF2G28*AD*
SR[0]	Program/Cache program(page N)/ Erase Pass or Fail	Program/Cache program(page N)/ Erase Pass or Fail
SR[1]	Cache Program (page N-1) Pass or Fail	Cache Program (page N-1) Pass or Fail
SR[2]	Not Used	Not Used
SR[3]	Not Used	Not Used
SR[4]	Not Used	Not Used
SR[5]	Ready/Busy for Internal Controller Program/Erase/Read Operation	Ready/Busy for Internal Controller Program/Erase/Read Operation
SR[6]	Ready/Busy	Ready/Busy
SR[7]	Write Protect	Write Protect

6. Package Pin Definition

The package physical dimensions and pin definitions of the MX30LF2G18AC and the MX30LF2G28AD are identical in 48-TSOP and 63-VFBGA.

7. Device Identification

The Device ID lengths of the MX30LF2G18AC and the MX30LF2G28AD differ by one byte. The ID of the MX30LF2G18AC begins with a one-byte Manufacturer Code followed by a four-byte Device ID. The ID of the MX30LF2G28AD begins with a one-byte Manufacturer Code followed by a five-byte Device ID. The ID codes of the MX30LF2G18AC and the MX30LF2G28AD are identical for the first three bytes, but different for the 4th and 5th byte which indicates differences in spare size and ECC requirement. The extended 6th byte of MX30LF2G28AD is for device generation (**Table 7-1 Device Identification**).

Table 7-1. Device Identification

Part Name		MX30LF2G18AC	MX30LF2G28*AD*
ID Code		C2h/DAh/90h/***95h/06h***	C2h/DAh/90h/***91h/07h/03h***
ID Definition	1st Byte	Manufacturer ID	Manufacturer ID
	2nd Byte	Device ID	Device ID
	3rd Byte	Number of Die per CE	Number of Die per CE
		Cell Structure	Cell Structure
		Number of Concurrently Programmed Pages	Number of Concurrently Programmed Pages
		nterleaved operations between Multiple die	Interleaved Programming between multiple devices
		Cache program	Cache program
	4th Byte	Page Size (2KB, bit1=0 & bit0=1)	Page Size (2KB, bit1=0 & bit0=1)
		Spare Area Size (16-byte per 512-byte), bit2=1	Spare Area Size ***(32-byte*** per 512-byte), ***bit2=0***
		Sequential Read Cycle Time (bit7, bit3=1,0)	Sequential Read Cycle Time (bit7, bit3=1,0)
		Block Size (128KB excluding spare area, bit5=0 & bit4=1)	Block Size (128KB excluding spare area, bit5=0 & bit4=1)
		Organization	Organization
	5th Byte	ECC level requirement, ***4-bit ECC required (bit 1:0=10b)***	ECC level requirement, ***8-bit ECC required (bit 1:0=11b)***
		Number of Planes per CE	Number of Planes per CE
		Plane Size	Plane Size
		Reserved	Reserved
	6th Byte	N/A	***Device Generation***

8. References

Table 8-1 shows the datasheet versions used for comparison in this application note. For the most current, detailed specification, please visit Macronix website or contact sales.

Table 8-1. Datasheet Versions

Datasheet	Location	Date Issued	Revision
MX30LF2G18AC	Website	Jan. 2017	Rev. 1.4
MX30LF2G28AD	Website	Dec. 2019	Rev. 1.0

9. Summary

The Macronix MX30LF2G18AC and MX30LF2G28AD NAND flash share the same basic Read, Program, and Erase commands and have the same package dimension and pin-outs. However, migrating to the MX30LF2G28AD may require firmware modifications to accommodate differences in spare size and ECC Requirement. The implementation of wear leveling is required from host system software for high program/erase application on the 60K P/E endurance cycle of MX30LF2G28AD.

10. Part Number Cross-Reference

Table 10-1. Part Number Cross Reference

Bus Width	Voltage	Package	Part Number	Part Number
x8	3V	48-TSOP	MX30LF2G18AC-TI	MX30LF2G28AD-TI
x8	3V	64-VFBGA	MX30LF2G18AC-XKI	MX30LF2G28AD-XKI

11. Revision History

Table 11-1. Revision History

Revision No.	Description	Page	Date
REV. 1	Initial Release	ALL	Aug. 14, 2019
REV. 2	1. Updated Table 3-1. Key Performance Comparison 2. Removed Deep Power Down descriptions	P2 P1-3	December 27, 2019

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