MPQ2167A

6V, 6A, Frequency-Configurable Synchoronous Buck Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ2167A is a frequency-configurable (300kHz to 2.2MHz), synchronous step-down converter. It can achieve up to 6A of continuous output current with peak current control for excellent transient response and efficiency performance. The MPQ2167A operates from a 2.7V to 6.0V input range and generates an output voltage as low as 0.606V. It is ideal for a wide range of applications, including automotive infotainment, clusters, and telematics, as well as portable instruments.

The MPQ2167A integrates a 35mΩ high-side switch and a 25mΩ synchronous rectifier for high efficiency without an external Schottky diode.

The MPQ2167A can be configured for either advanced asynchronous mode (AAM) or forced continuous conduction mode (FCCM) at light-load. AAM provides high efficiency by reducing switching losses at light load, while FCCM has a controllable frequency and a lower output ripple.

The MPQ2167A offers standard features, including soft start, external SYNC clock, enable control, and a power good indicator. In addition, the MPQ2167A provides over-current protection (OCP) with valley current detection to avoid current runaway, short-circuit protection (SCP), reliable over-voltage protection (OVP), and auto-recovery thermal protection.

With internal compensation, the MPQ2167A requires a minimal number of readily available, standard external components, and is available in a QFN-14 (3mmx3mm) package.

FEATURES

- 2.7V to 6.0V Operating Input Voltage Range
- Adjustable Output from 0.606V
- Up to 6A Continuous Output Current
- High-Efficiency Synchronous Mode Control
- 35mΩ and 25mΩ Internal Power MOSFET
- Configurable Frequency Up to 2.2MHz
- External SYNC Clock Up to 2.2MHz
- 42μA Quiescent Current
- Low-Shutdown Mode Current
- 100% Duty Cycle Operation
- Internal Compensation Mode
- Selectable AAM or FCCM Operation
- External Soft Start
- Remote EN Control
- Power Good Indicator
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP)
- V_{IN} Under-Voltage Lockout (UVLO)
- V_{OUT} Over-Voltage Protection (OVP)
- Thermal Shutdown
- Available in a QFN-14 (3mmx3mm) Package
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade-1

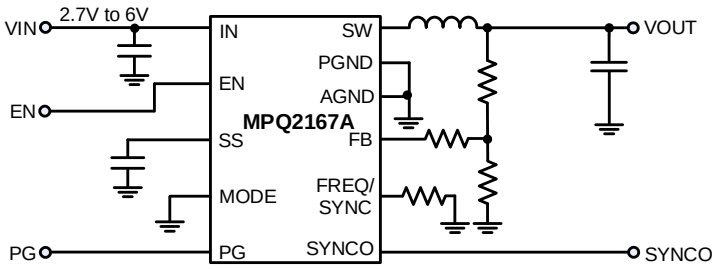
APPLICATIONS

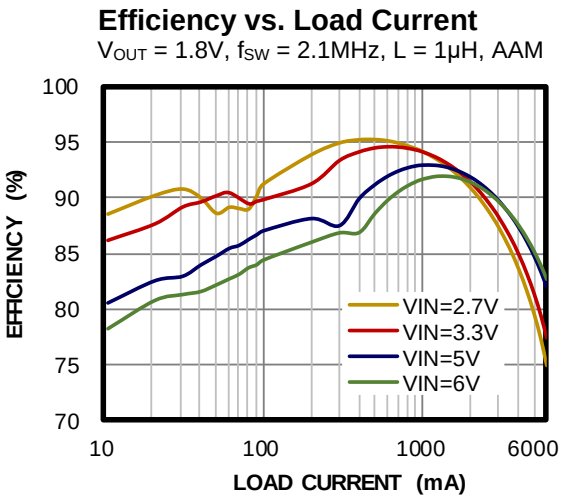
- Automotive Infotainment
- Automotive Clusters
- Automotive Telematics
- Portable Instruments
- Industrial Supplies
- Battery-Powered Devices

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TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2167AGQE-AEC1***	QFN-14 (3mmx3mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MPQ2167AGQE-AEC1–Z).
** Moisture Sensitivity Level Rating
*** Wettable Flank

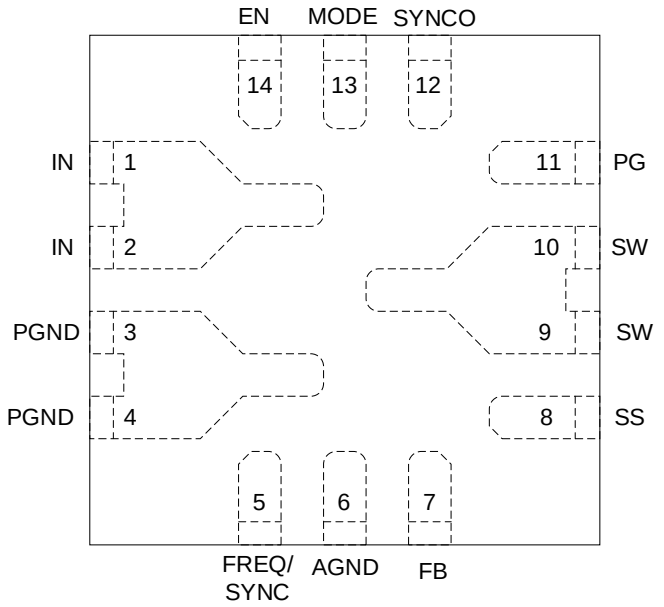
TOP MARKING

BHLY
LLL

BHL: Product code of MPQ2167AGQE-AEC1
Y: Year code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-14 (3mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 2	IN	**Input supply.** IN supplies all power to the converter. To reduce switching spikes, place a decoupling capacitor to ground, as close as possible to the IC.
3, 4	PGND	**Power ground.** Connect to larger copper areas on the negative terminals of the input and output capacitors.
5	FREQ/ SYNC	**Configurable switching frequency and synchronization input.** Connect a resistor to GND to set the switching frequency. The switching frequency can be synchronized via this pin using an external clock.
6	AGND	**Analog ground.** Ground for internal logic and signal circuit.
7	FB	**Feedback point.** Negative input of the error amplifier. To set the regulation voltage, connect FB to the tap of an external resistor divider between the output and GND. In addition, the power good (PG) and under-voltage lockout (UVLO) circuits use FB to monitor the output voltage.
8	SS	**Soft start.** To externally set the soft-start time, place a capacitor from SS to GND. Float this pin to activate the internal default 1ms soft-start setting.
9, 10	SW	**Switch output.** Connect SW internally to the high-side and low-side power switches. Connect SW externally to the output inductor.
11	PG	**Power good indicator.** The PG output is an open drain that connects to VIN via an internal pull-up resistor. PG is pulled up to V_{IN} when the FB voltage is within 15% of the regulation level. If the FB voltage is out of that regulation range, it drops down.
12	SYNCO	**Synchronization output.** Outputs a 180° out-of-phase clock to the other devices.
13	MODE	**Mode selection.** Connect to logic high or input voltage (V_{IN}) for FCCM. Connect to logic low or ground for AAM. Do not leave MODE floating.
14	EN	**Enable input.** Drive EN high to turn on the device. Ground or float EN to disable the device.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... +6.5V
V_{SW}..... - 0.3V (-3V for < 10ns) to 6.5V (7.0V for < 10ns)
All other pins .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2) 2.1W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Electrostatic Discharge (ESD) Rating

Human body model (HBM) .....±2kV
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions

Continuous supply voltage (V_{IN}).....2.7V to 6.0V
Output voltage (V_{OUT}).....0.606V to V_{IN}
Load current range .....0A to 6A
Operating junction temp (T_J)…….
……...-40°C to +125°C (3)

Thermal Resistance θ_{JA} θ_{JC}

QFN-14 (3mmx3mm)		
JESD51-7 (4)	60	12 °C/W
EV2167A-Q-00A (5)	39	6.2 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the module will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device may be able to support an operating junction temperature above 125°C. Contact MPS for details.
4) Measured on JESD51-7, 4-layer PCB.
5) Measured on standard EVB, 6.35cmx6.35cm, 2oz. thick copper, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.6V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply and UVLO						
Quiescent supply current	I_Q	Mode = AAM, V_{EN} = 2V, no load, R_{FREQ} = 1MΩ, T_J = 25°C		42	50	μA
		T_J = -40°C to +125°C			120	
Shutdown current	I_{SD}	Mode = AAM, V_{EN} = 0V, T_J = 25°C		0	1	μA
		T_J = -40°C to +125°C			20	
V_{IN} UVLO rising threshold	$INUV_{Vth-R}$		2.3	2.5	2.7	V
V_{IN} UVLO falling threshold	$INUV_{Vth-F}$		2	2.15	2.3	V
V_{IN} UVLO hysteresis threshold	$INUV_{HYS}$			350		mV
Output and Regulation						
Regulated FB voltage	V_{FB}	T_J = 25°C	0.596	0.606	0.616	V
		T_J = -40°C to +125°C	0.591		0.621	V
FB input current	I_{FB}	V_{FB} = 0.63V		10	100	nA
Output discharge resistor	$R_{DISCHARGE}$		50	100	150	Ω
Switches and Frequency						
High-side switch on resistance	R_{DSON-P}	V_{IN} = 5V, I_{OUT} = 200mA		35	70	mΩ
Low-side switch on resistance	R_{DSON-N}	V_{IN} = 5V, I_{OUT} = 200mA		25	70	mΩ
High-side SW leakage current	$I_{HSW-LKG}$	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 6V, T_J = 25°C		0	1	μA
		T_J = -40°C to +125°C			30	
Low-side SW leakage current	$I_{LSW-LKG}$	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V, T_J = 25°C		0	1	μA
		T_J = -40°C to +125°C			10	
Switching frequency	f_{SW}	R_{FREQ} = 499kΩ	380	450	520	kHz
		R_{FREQ} = 75kΩ	1800	2100	2400	
SYNC frequency range	f_{SYNC}		0.3		2.2	MHz
SYNC high-voltage threshold	$V_{SYNC-HIGH}$	V_{IN} = 2.7V (6)	1.5			V
		V_{IN} = 3.6V	1.8			
		V_{IN} = 6V (6)	3.2			
SYNC low-voltage threshold	$V_{SYNC-LOW}$	V_{IN} = 2.7V (6)			0.8	V
		V_{IN} = 3.6V			1.1	
		V_{IN} = 6V (6)			1.6	
Maximum duty cycle	D_{MAX}			100		%
Minimum on time (6)	t_{ON-MIN}			50		ns
Minimum off time (6)	$t_{OFF-MIN}$			95		ns
PG						
PG sink current capacity	$V_{PG-SINK}$	Sink 1mA			300	mV
PG logic high voltage	$V_{PG-HIGH}$	V_{IN} = 5V	4.5			V
PG delay time	$t_{PG-DELAY}$	V_{OUT} rising edge	40	100	180	μs
		V_{OUT} falling edge	5	20	30	μs
PG upper rising threshold	PG_{UP_R}	As a percentage of V_{FB}	108	115	122	%
PG upper hysteresis	PG_{UP_HYS}	As a percentage of V_{FB}		5		%
PG lower rising threshold	PG_{LOW_R}	As a percentage of V_{FB}	80	85	90	%
PG lower hysteresis	PG_{LOW_HYS}	As a percentage of V_{FB}		5		%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.6V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
EN						
EN input rising threshold	$V_{EN-RISING}$		1.2			V
EN input falling threshold	$V_{EN-FALLING}$				0.4	V
EN input current	I_{EN}	V_{EN} = 2V		2	5	µA
		V_{EN} = 0V		0	0.5	µA
Mode and Soft Start						
MODE pin rising threshold	$V_{MODE-FCCM}$	Into FCCM	1.2			V
MODE pin falling threshold	$V_{MODE-AAM}$	Into AAM			0.4	V
Mode input leakage current	I_{MODE}	Pulled up to 6V			1	µA
Soft-start charging current	I_{SS}	V_{SS} = 0V	2	4	6	µA
Default soft-start time	$t_{SS-DEFAULT}$			1		ms
Protections						
Peak current limit	$I_{PEAK-LIMIT}$	Sourcing, duty cycle = 40%	7	9	11	A
Valley current limit	$I_{VALLEY-LIMIT}$			7		A
OCP timer (6)	t_{OCP}			100		µs
Zero-cross threshold	I_{ZCD}			100		mA
Output over-voltage limit	OV_{LIMIT}	As a percentage of V_{FB}		115		%
Thermal shutdown (6)	T_{SD}	Temperature rising		170		°C
Thermal shutdown hysteresis (6)	T_{SD-SYS}			25		°C

Note:

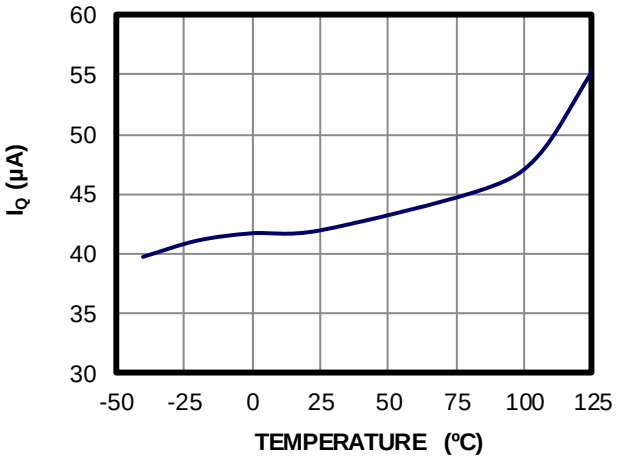
6) Not tested in production. Guaranteed by design and characterization.

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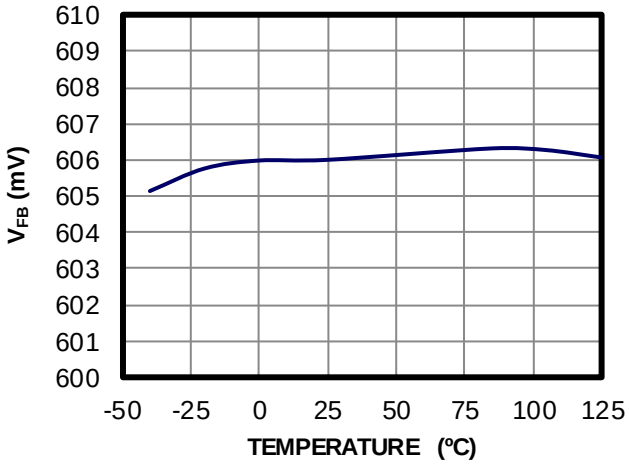
TYPICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = 25°C, unless otherwise noted.

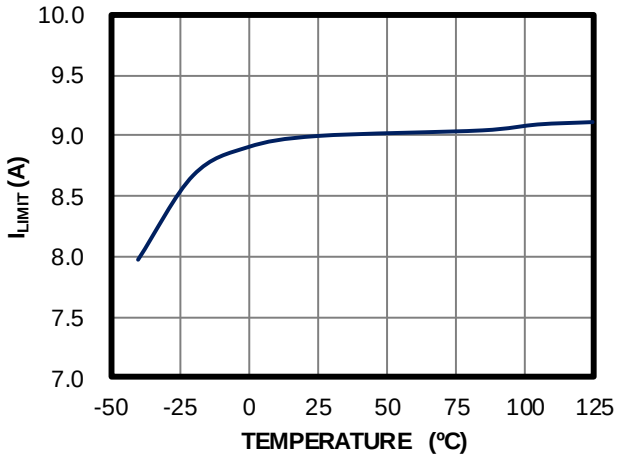
Quiescent Current vs. Temperature



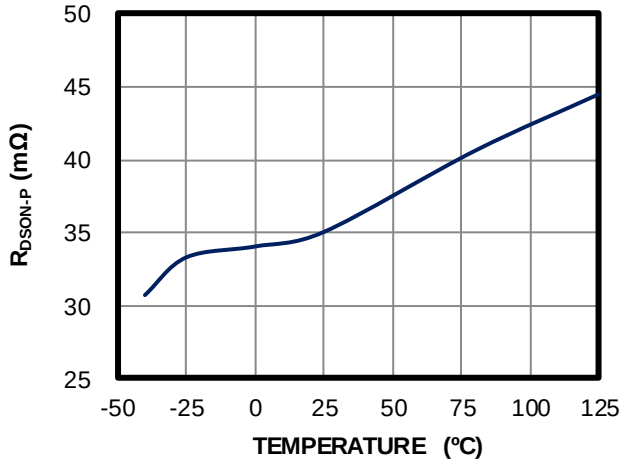
Feedback Voltage vs. Temperature



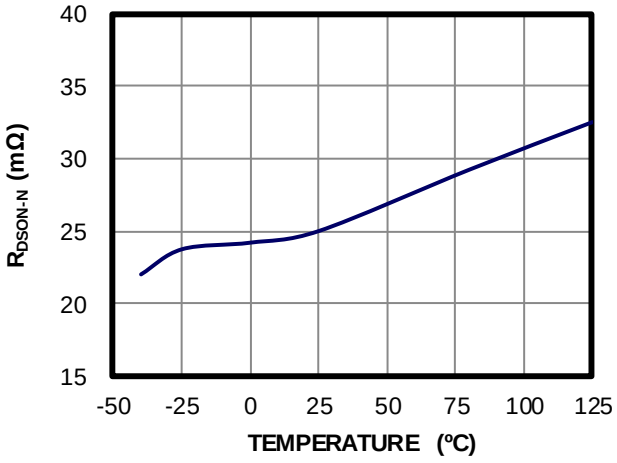
Peak Current Limit vs. Temperature



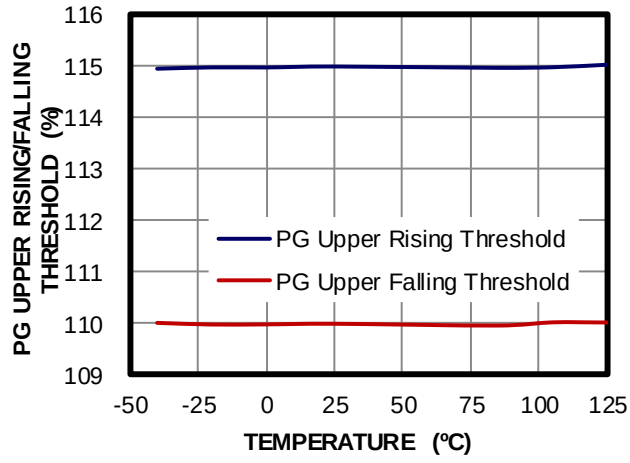
High-Side Switch On Resistance vs. Temperature



Low-Side Switch On Resistance vs. Temperature



PG Upper Rising/Falling Threshold vs. Temperature

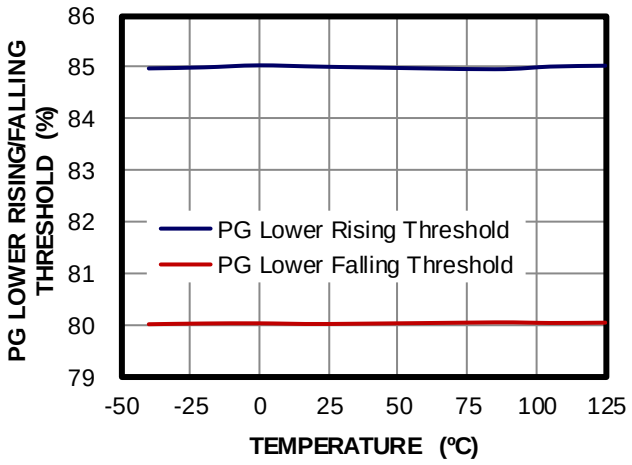


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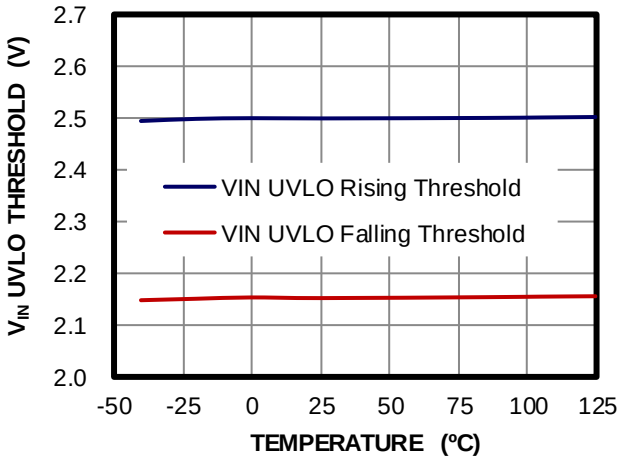
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = 25°C, unless otherwise noted.

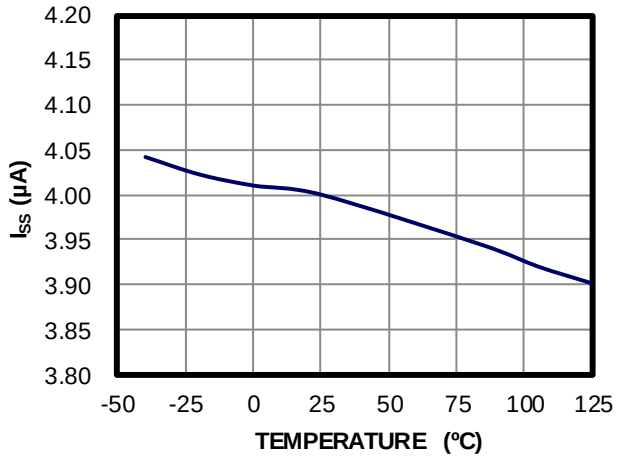
PG Lower Rising/Falling Threshold vs. Temperature



V_{IN} UVLO Threshold vs. Temperature



Soft-Start Current vs. Temperature

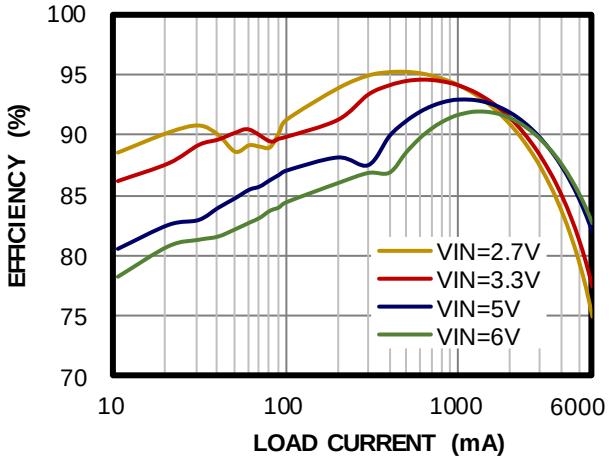


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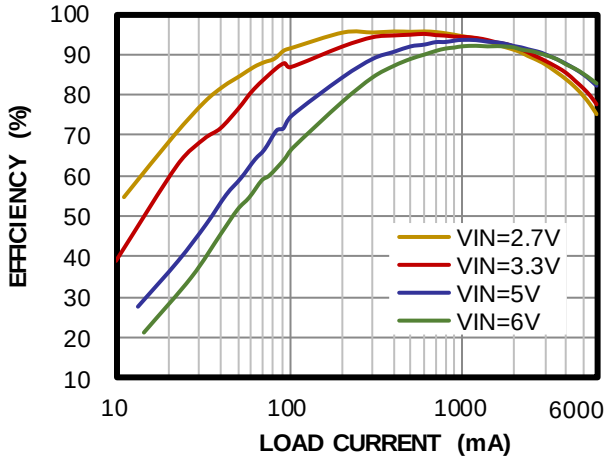
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

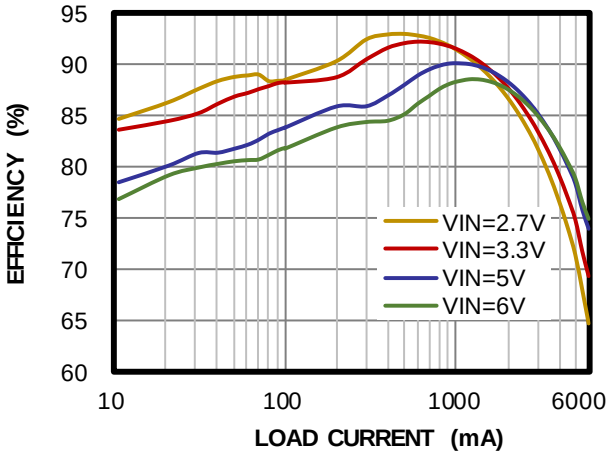
Efficiency vs. Load Current
V_{OUT} = 1.8V, AAM



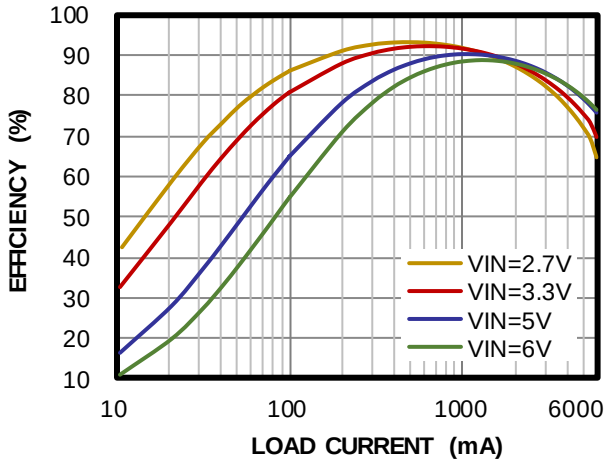
Efficiency vs. Load Current
V_{OUT} = 1.8V, FCCM



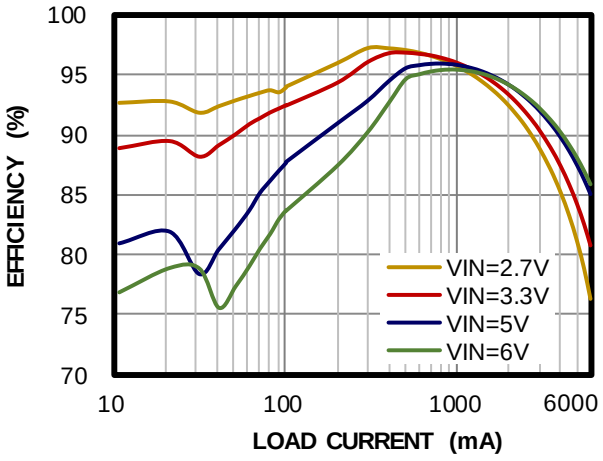
Efficiency vs. Load Current
V_{OUT} = 1.2V, AAM



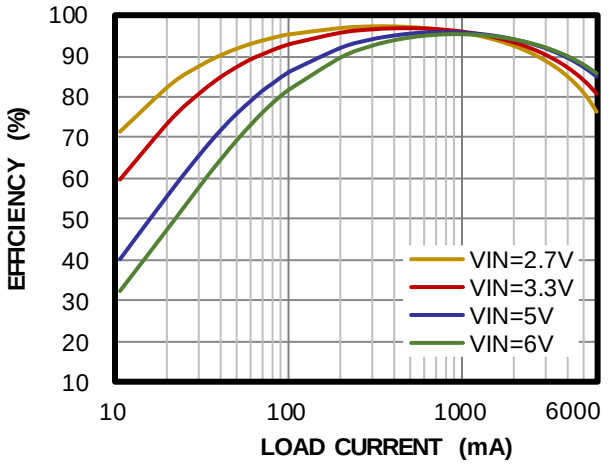
Efficiency vs. Load Current
V_{OUT} = 1.2V, FCCM



Efficiency vs. Load Current
V_{OUT} = 1.8V, f_{SW} = 450kHz, L = 4.7µH, AAM



Efficiency vs. Load Current
V_{OUT} = 1.8V, f_{SW} = 450kHz, L = 4.7µH, FCCM



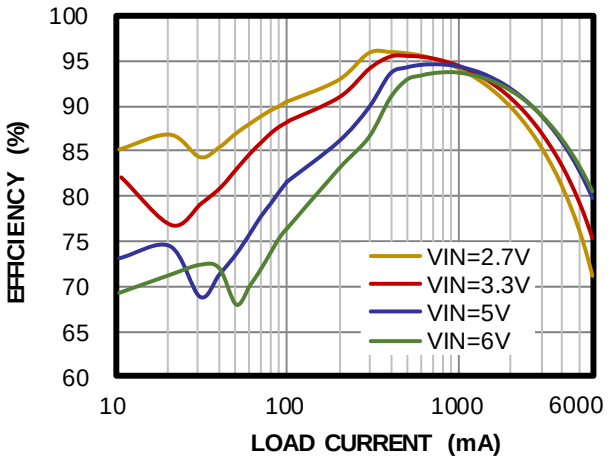
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

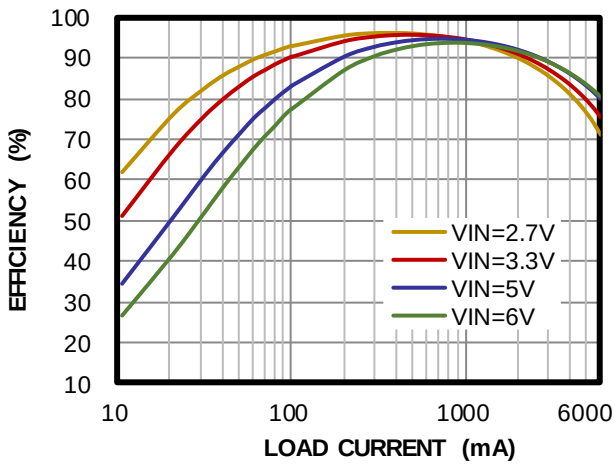
Efficiency vs. Load Current

V_{OUT} = 1.2V, f_{SW} = 450kHz, L = 4.7µH, AAM



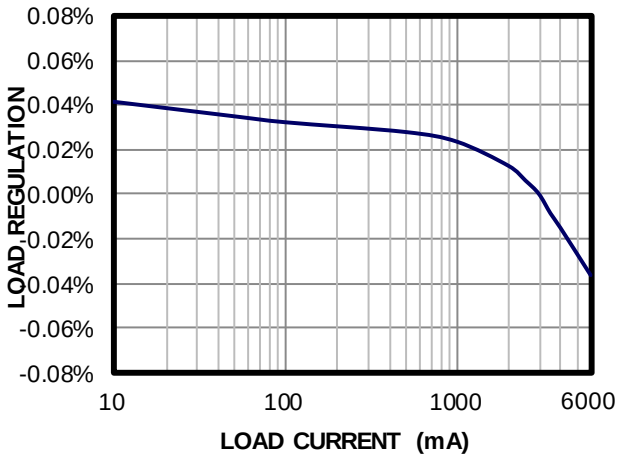
Efficiency vs. Load Current

V_{OUT} = 1.2V, f_{SW} = 450kHz, L = 4.7µH, FCCM



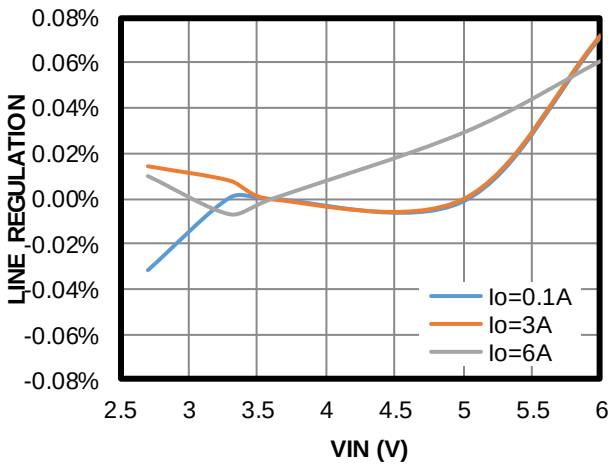
Load Regulation

V_{OUT} = 1.8V, AAM

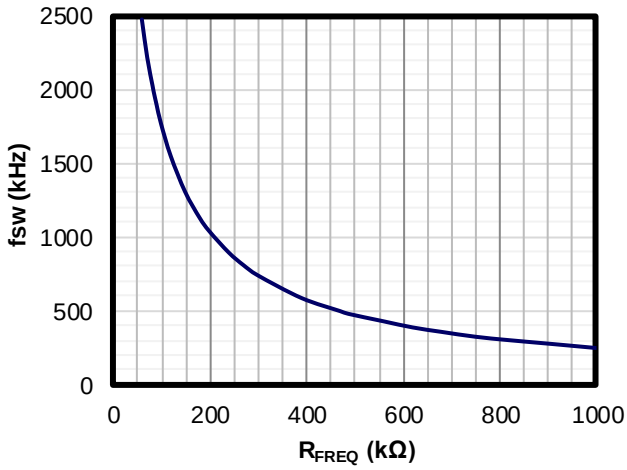


Line Regulation

V_{OUT} = 1.8V, AAM



Switching Frequency vs. Frequency Resistor

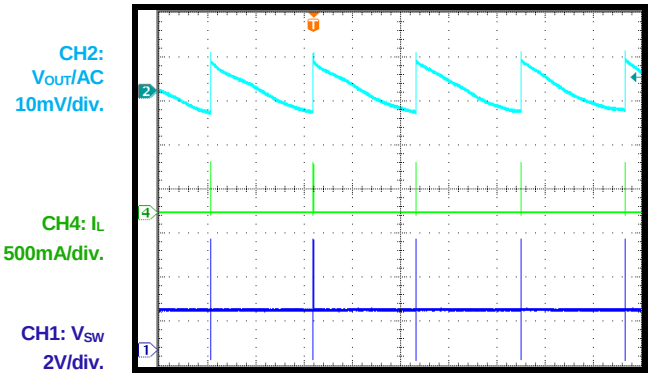


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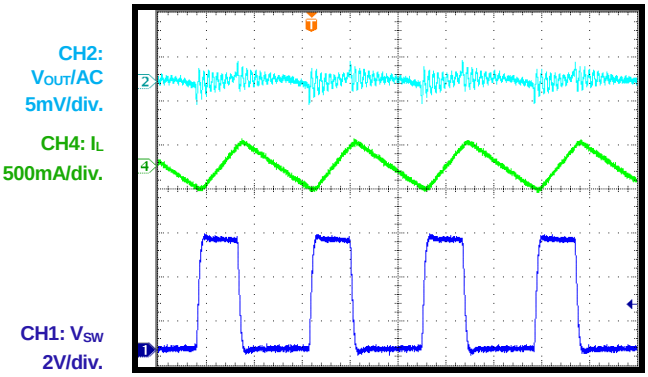
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

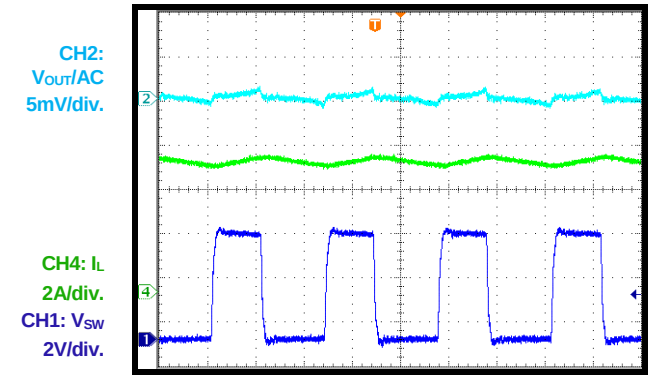
Steady State
I_{OUT} = 0A, AAM



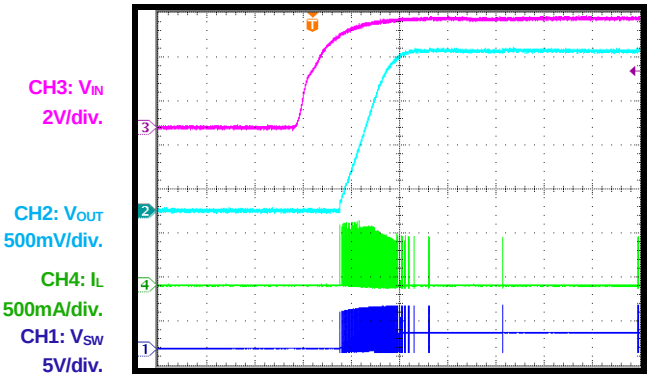
Steady State
I_{OUT} = 0A, CCM



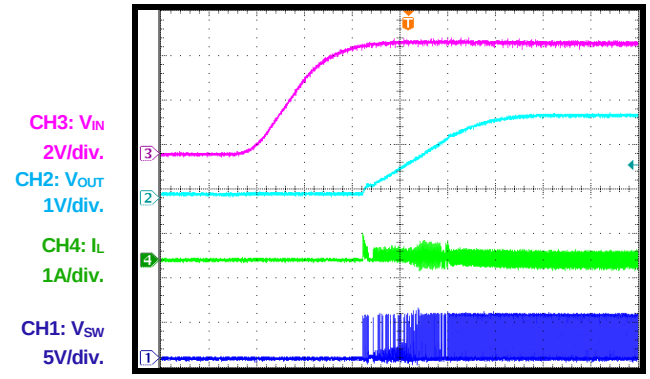
Steady State
I_{OUT} = 6A



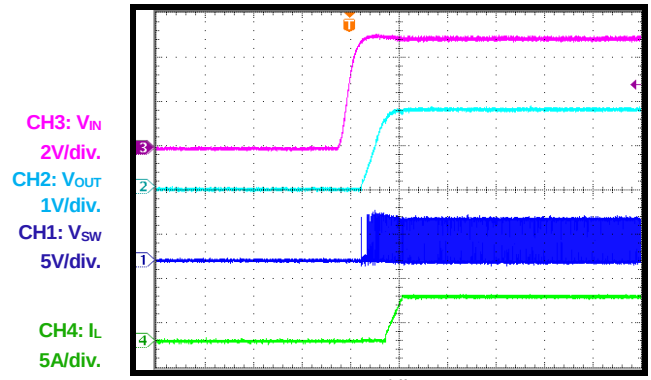
Start-Up through VIN
I_{OUT} = 0A, AAM



Start-Up through VIN
I_{OUT} = 0A, CCM



Start-Up through VIN
I_{OUT} = 6A



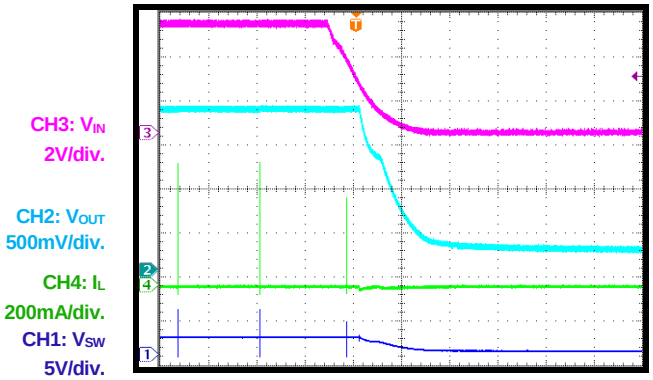
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

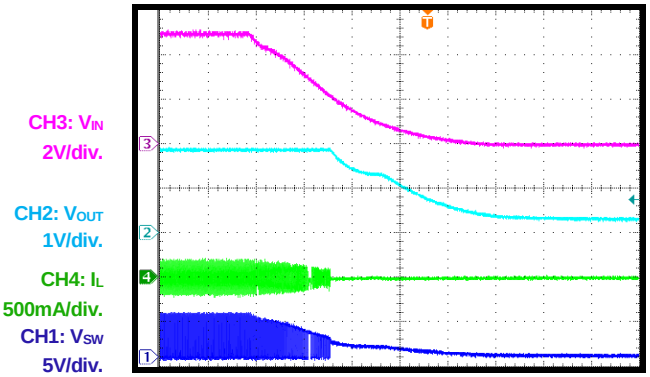
Shutdown through VIN

I_{OUT} = 0A, AAM



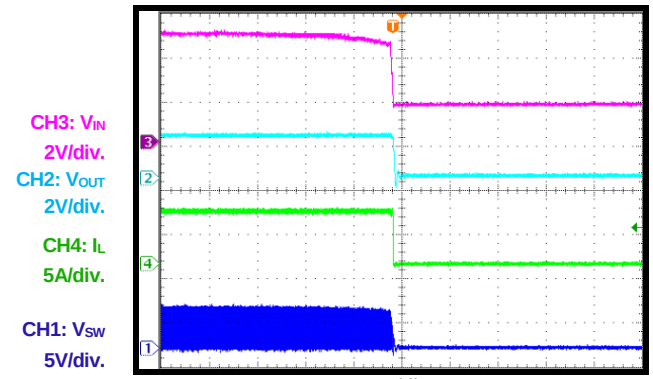
Shutdown through VIN

I_{OUT} = 0A, CCM



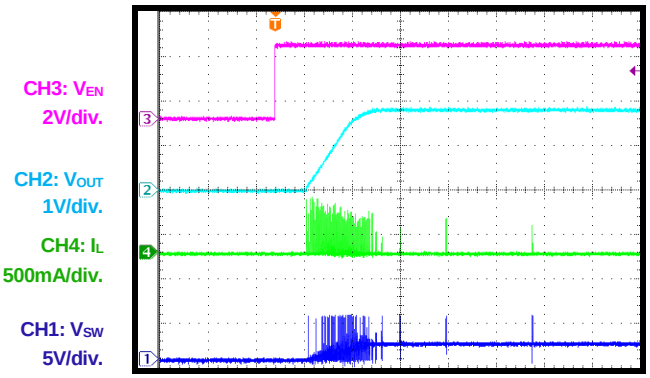
Shutdown through VIN

I_{OUT} = 6A



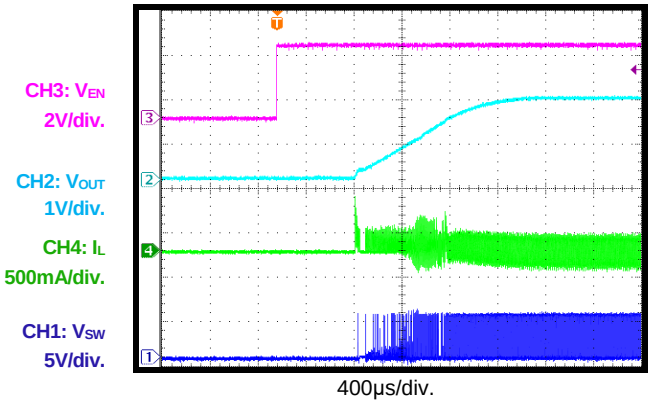
Start-Up through EN

I_{OUT} = 0A, AAM



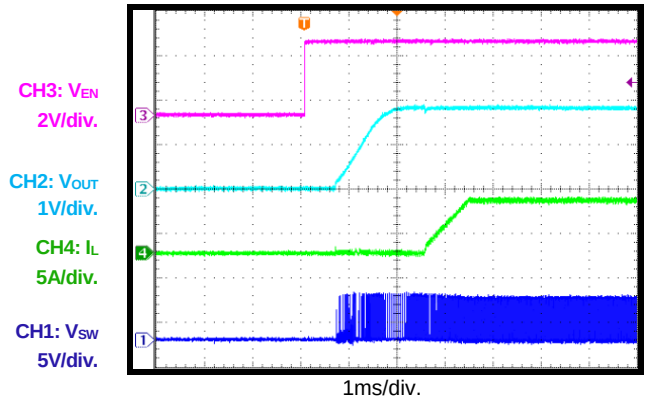
Start-Up through EN

I_{OUT} = 0A, CCM



Start-Up through EN

I_{OUT} = 6A



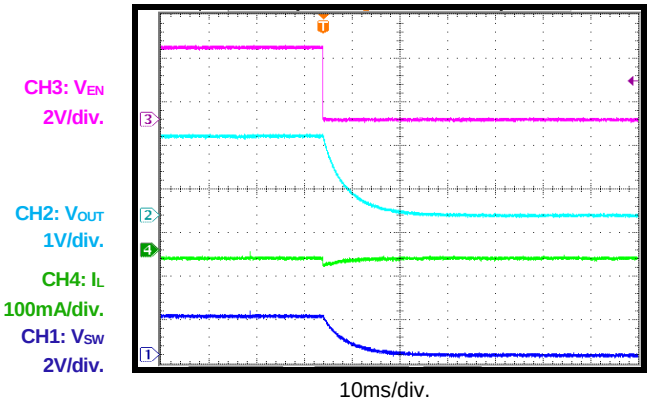
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

Shutdown through EN

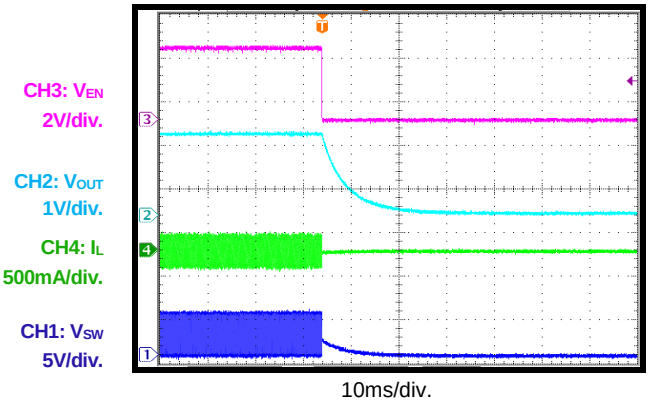
I_{OUT} = 0A, AAM



10ms/div.

Shutdown through EN

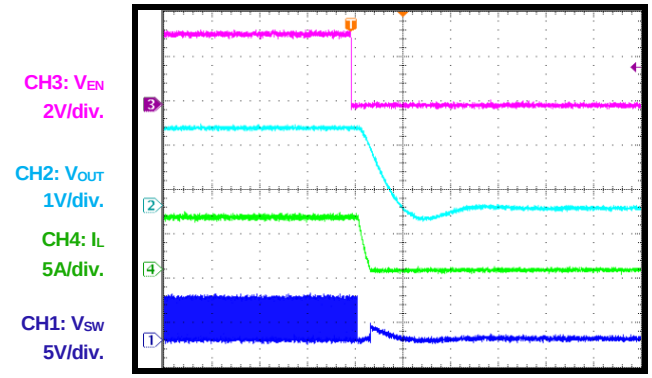
I_{OUT} = 0A, CCM



10ms/div.

Shutdown through EN

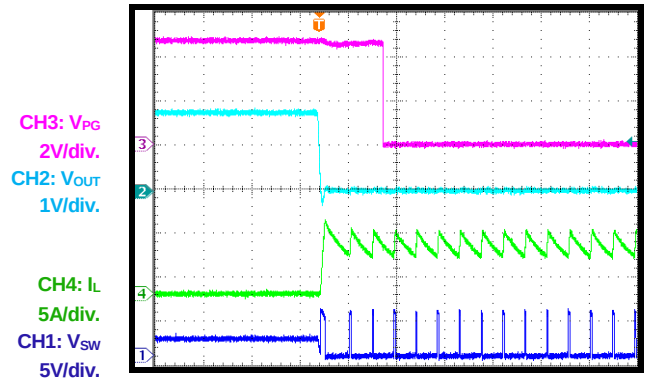
I_{OUT} = 6A



20µs/div.

SCP Entry

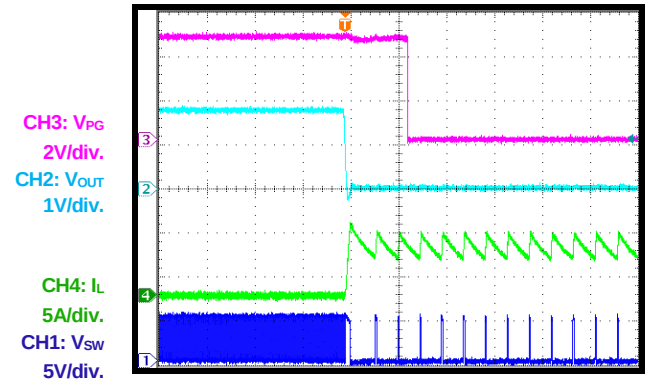
I_{OUT} = 0A, AAM



20µs/div.

SCP Entry

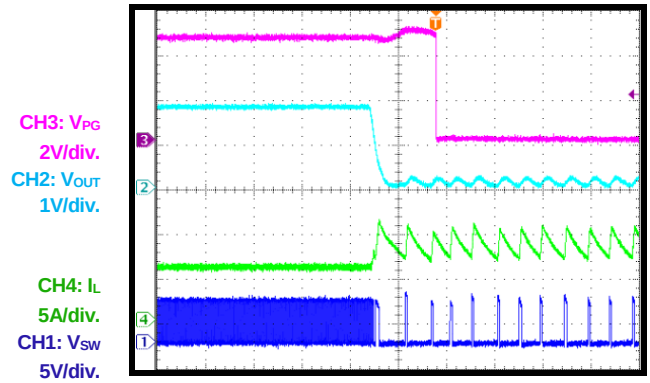
I_{OUT} = 0A, CCM



20µs/div.

SCP Entry

I_{OUT} = 6A



20µs/div.

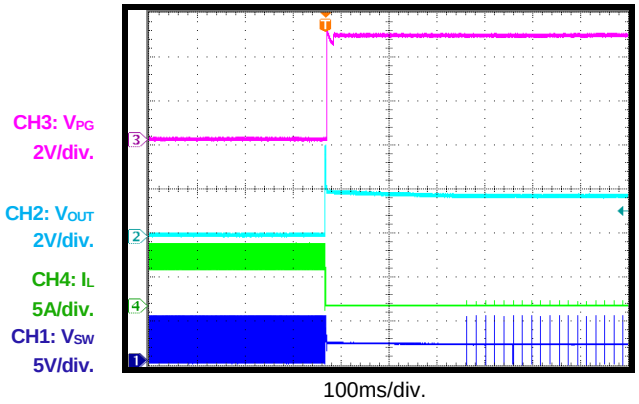
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

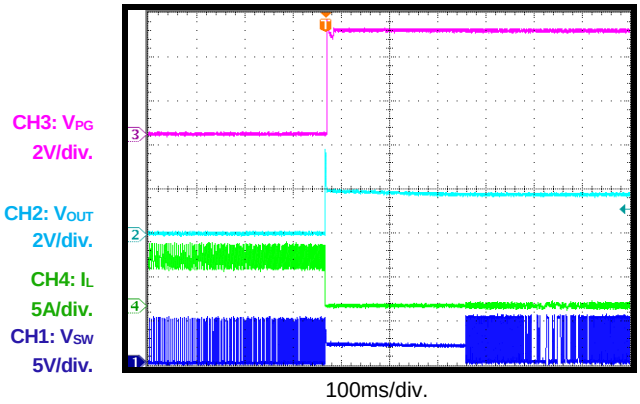
SCP Recovery

I_{OUT} = 0A, AAM



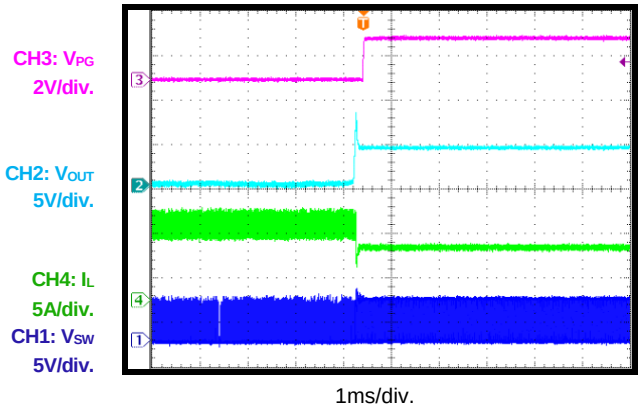
SCP Recovery

I_{OUT} = 0A, CCM



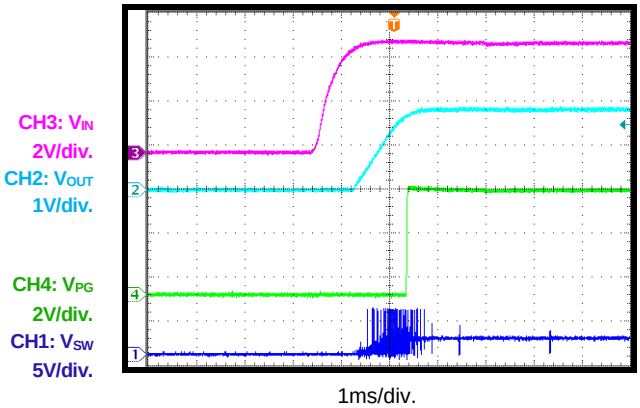
SCP Recovery

I_{OUT} = 6A



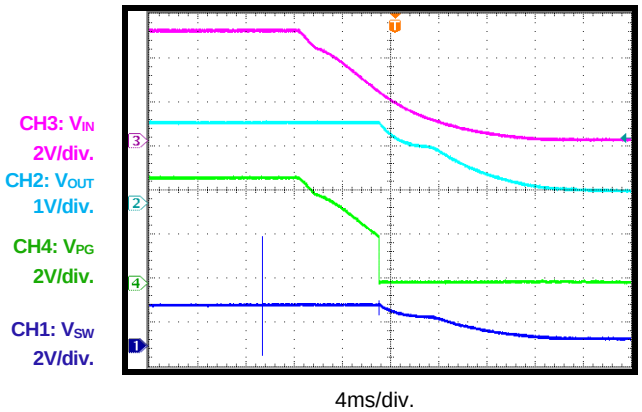
PG Start-Up through V_{IN}

I_{OUT} = 0A, AAM



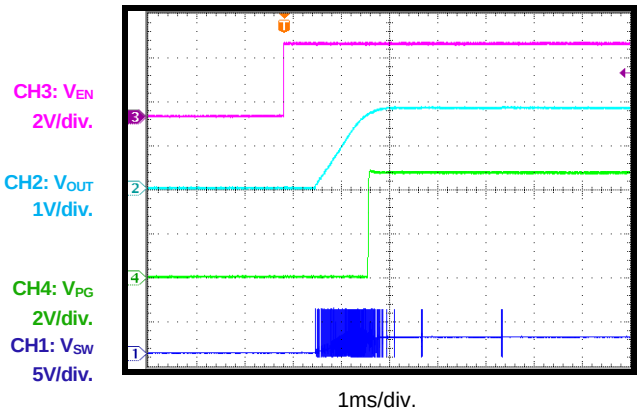
PG Shutdown through V_{IN}

I_{OUT} = 0A, AAM



PG Start-Up through EN

I_{OUT} = 0A, AAM



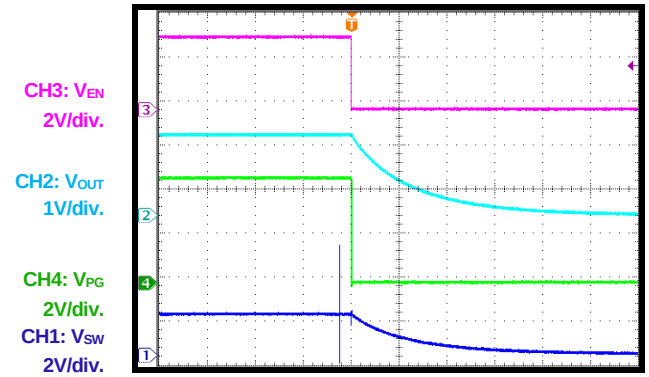
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

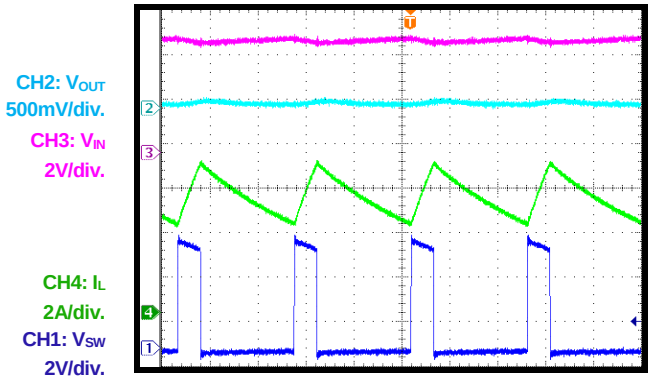
V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

PG Shutdown through EN

I_{OUT} = 0A, AAM

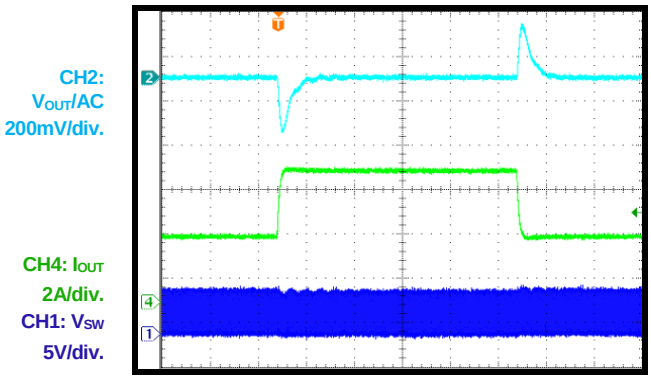


SCP Steady State



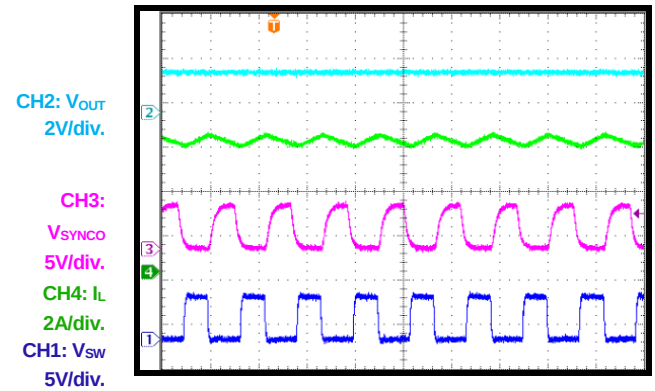
Load Transient

I_{OUT} = 3A to 6A, 1.6A/µs



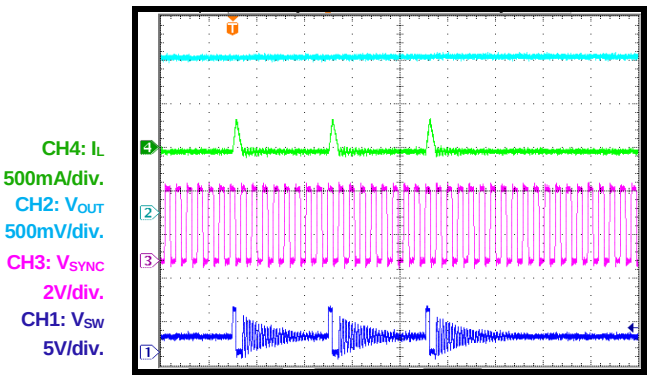
SYNCO

I_{OUT} = 6A



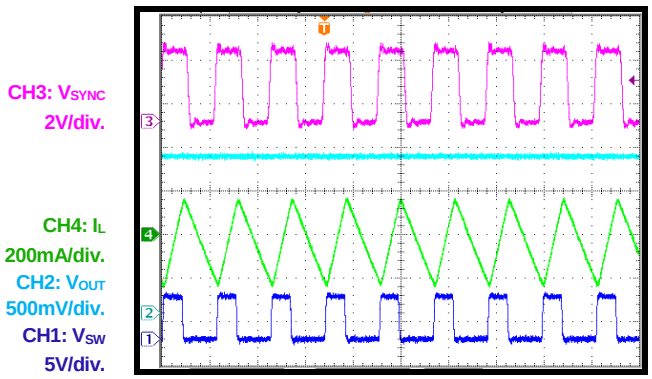
SYNCIN

I_{OUT} = 0A, AAM, SYNC clock = 2.2MHz



SYNCIN

I_{OUT} = 0A, FCCM, SYNC clock = 2.2MHz



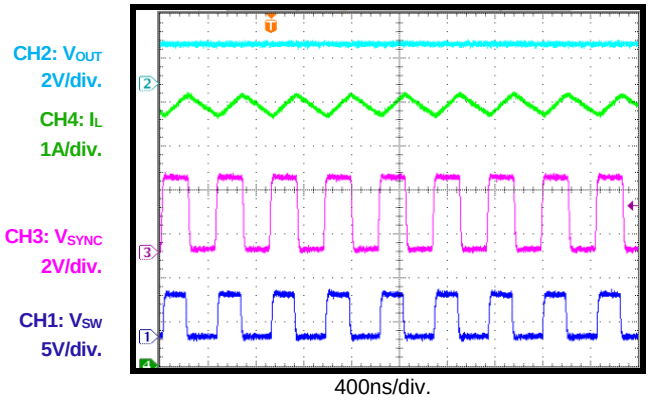
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

SYNCIN

I_{OUT} = 6A, SYNC clock = 2.2MHz



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FUNCTIONAL BLOCK DIAGRAM

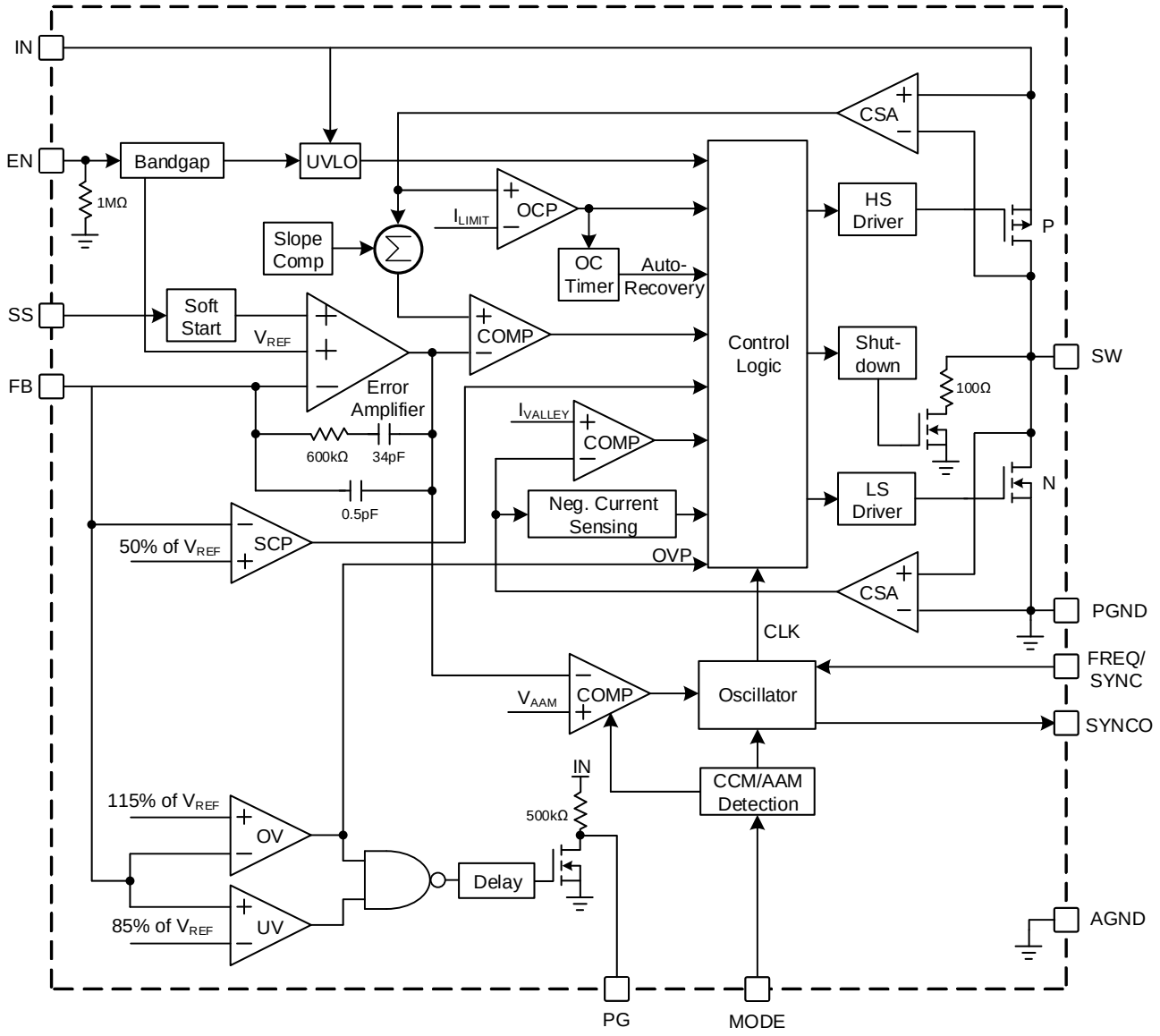


Figure 1: Functional Block Diagram

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OPERATION

The MPQ2167A is a fully integrated, synchronous, rectified, step-down, non-isolated switch-mode converter. It uses peak current mode control with internal compensation for faster transient response and cycle-by-cycle current limit.

Figure 1 shows the block diagram of the device. The MPQ2167A is available with a 2.7V to 6.0V input supply range, and can achieve a 6A continuous output current with excellent load and line regulation across an ambient temperature range of -40°C to +125°C. The output voltage can be regulated as low as 0.606V.

The MPQ2167A is optimized for low-voltage portable applications where efficiency and small size are critical. It can operate with up to a 2.2MHz switching frequency, which enables the use of a smaller inductor while still providing excellent efficiency. It also allows for high power conversion efficiency under light-load conditions with advanced asynchronous mode (AAM).

Forced Continuous Conduction Mode (FCCM)

Pulling MODE high (>1.2V) forces the converter into forced continuous conduction mode (FCCM). In FCCM, the MPQ2167A operates in fixed-frequency, peak current control mode to regulate the output voltage, regardless of the output current.

An internal clock initiates an FCCM cycle. At the rising edge of the clock, the high-side switch (HS-FET) turns on, and the inductor current rises linearly to provide energy to the load. The HS-FET remains on until its current reaches the COMP voltage (V_{COMP}), which is the output of the internal error amplifier. V_{COMP} depends on the difference between the output feedback voltage and the internal high-precision reference. V_{COMP} determines how much energy should be transferred to the load. A higher load current results in a higher V_{COMP}.

When the HS-FET is off, the low-side switch (LS-FET) turns on immediately and remains on until the next clock starts. During this time, the inductor current flows through the LS-FET. To avoid shoot-through, a dead time is inserted to avoid the HS-FET and LS-FET turning on simultaneously. For each turn-on/off period in a switching cycle, the HS-FET remains on or off for a certain time limit.

Advanced Asynchronous Mode (AAM)

Pulling MODE low (<0.4V) forces the converter into light-load advanced asynchronous mode (AAM). There is an internally fixed AAM threshold voltage (V_{AAM}). Under light-load conditions, the value of V_{COMP} is low. If V_{COMP} exceeds V_{AAM}, the MPQ2167A first enters discontinuous conduction mode (DCM) with a fixed frequency, as long as the inductor current approaches 0A.

If the load decreases further, or there is no load and V_{COMP} drops below V_{AAM}, the internal clock is blocked, and the MPQ2167A skips some pulses. During this time, V_{FB} is below V_{REF}, so V_{COMP} ramps up until it exceeds V_{AAM}. Then the internal clock is reset, and the crossover time is used as a benchmark for the next clock. This control scheme helps achieve high efficiency by scaling down the frequency to reduce the switching and gate driver losses.

As the output current increases from a light-load condition, V_{COMP} becomes larger, and the switching frequency increases. If the output current exceeds the critical level while V_{COMP} exceeds V_{AAM}, the MPQ2167A resumes fixed-frequency control, which is the same as FCCM (see Figure 2).

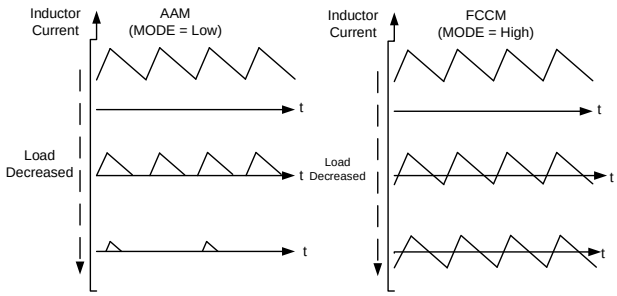


Figure 2 : AAM and FCCM

Enable (EN)

The MPQ2167A can be enabled or disabled via a remote EN signal that is referenced to ground. The remote EN control operates with positive logic that is compatible with popular logic devices. Positive logic implies that when the input voltage exceeds the under-voltage lockout (UVLO) threshold (typically 2.5V), the converter is enabled by pulling EN above 1.2V. Float or ground the EN pin to

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disable the MPQ2167A. There is an internal 1MΩ resistor from EN to ground.

Oscillator and SYNC Function

The oscillating frequency of the MPQ2167A can be configured via an external frequency resistor. The frequency resistor should be located between FREQ and GND, as close to the device as possible. Select the R_{FREQ} value following the Switching Frequency vs. R_{FREQ} curve in the Typical Performance Characteristics section on page 10.

The FREQ pin can also synchronize the internal oscillator rising edge to an external clock falling edge. The amplitude of the SYNC clock drives the internal logic (to determine the proper amplitude, see the Electrical Characteristics section on page 5). The recommended external SYNC frequency is between 300kHz and 2.2MHz.

There is no pulse width requirement. However, there is always parasitic capacitance on the pad, so if the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in application. Add the external SYNC clock (300kHz to 2.2MHz) before the device starts up, and keep the clock until the device is off. During this operation, constant high, constant low, or high/low transitions are not allowed on the SYNC signal.

The MPQ2167A also has SYNCO pin, which can output a 180° phase-shift clock. This signal can be used to synchronize other devices to operate at the same operation frequency but the opposite phase, which reduces the total input current ripple.

Soft-Start and Output Discharge

The MPQ2167A has soft start (SS). To avoid overshoot at start-up, soft start ramps up the output voltage at a controlled slew rate when EN goes high.

When soft start begins, an internal current source charges the external SS capacitor. When the SS voltage (V_{SS}) falls below the internal reference (V_{REF}), V_{SS} overrides V_{REF} as the error amplifier reference. When V_{SS} exceeds V_{REF}, V_{REF} acts as the reference. After soft start finishes, the MPQ2167A enters steady state. SS can be used for tracking and sequencing.

The SS time set by the external SS capacitor can be calculated with Equation (1):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (1)$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (0.606V), and I_{SS} is the internal 4μA SS charge current.

When SS is floating, the SS time is 1ms after the internal setting. If the MPQ2167A is disabled or experiencing an input shutdown, the device discharges the output voltage to GND through an internal 100Ω resistor that is in parallel with the LS-FET.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} (which means the output has a pre-biased voltage) at start-up, the HS-FET and LS-FET remain off until V_{SS} exceeds V_{FB}.

100% Duty Cycle

The MPQ2167A can operate with 100% duty cycle, which can extend the battery life. When the input voltage is too low to regulate the output, the device turns the HS-FET completely on to achieve maximum output voltage.

Power Good Indicator

The MPQ2167A has power good (PG) indication. PG is the open drain of the MOSFET. In the presence of an input voltage, the MOSFET turns on, and PG is pulled to GND before soft start is ready. When the output voltage is within a ±15% window of the rated voltage set by FB, PG is pulled up to V_{IN} by an internal resistor after a delay. If V_{FB} moves outside the ±15% range with a hysteresis, the device pulls PG low to indicate an output failure status.

Over-Current Protection (OCP)

The MPQ2167A has 9A cycle-by-cycle peak current limit control. The inductor current is monitored while the HS-FET is on. Once the inductor current reaches the current limit, the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy, and the inductor current decreases. The HS-FET does not turn on again until the inductor is below a certain current threshold, called the valley current limit. This operation prevents the inductor current from running away and possibly damaging the components.

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When the valley current limit is triggered, the OCP timer starts immediately. The OCP timer is set at 100µs. If the valley current limit is reached within this 100µs time frame during each cycle, short-circuit protection (SCP) is triggered.

Short-Circuit Protection (SCP)

When a short circuit occurs, the MPQ2167A immediately reaches its current limit. Meanwhile, the output voltage drops until V_{FB} is below 50% of V_{REF} (0.606V). The the device considers this an output dead short, and triggers short-circuit protection (SCP) immediately.

In SCP, the inductor current is monitored while the HS-FET is on. Once the inductor current reaches the current limit, the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy, and the inductor current drops. The HS-FET does not turn on again until the inductor drops below a certain current threshold, called the valley current limit. The device repeats this operation until the short circuit disappears, and the output returns to the regulation level. This protection mode prevents the inductor current from running away and possibly damaging the components.

Over-Voltage Protection (OVP)

The MPQ2167A monitors the output voltage through FB to detect output over-voltage (OV) conditions. If V_{FB} that exceeds 115% of V_{REF} (0.606V), OVP is triggered, and the LS-FET turns on to discharge V_{OUT} until the inductor current drops to 0A. Meanwhile, the HS-FET remains off. Then the LS-FET shuts off, and the output is discharged through the internal 100Ω resistor (in parallel with the LS-FET). The controller does not begin to switch until the output is within regulation.

Under-Voltage Lockout Protection (UVLO)

The MPQ2167A has input under-voltage lockout protection (UVLO) to ensure reliable output power. Assuming EN is active, the MPQ2167A is powered on when the input voltage exceeds the UVLO rising threshold. The device is powered off when the input voltage drops below the UVLO falling threshold. This function prevents the device from operating at an insufficient voltage. It is a non-latch protection.

Thermal Shutdown

The MPQ2167A employs thermal protection by internally monitoring the IC temperature. This function prevents the chip from operating at exceedingly high temperatures. If the junction temperature exceeds the threshold value (typically 170°C), it shuts down the whole chip. This is a non-latch protection. There is a 25°C hysteresis. Once the junction temperature drops to about 145°C, the device resumes normal operation by initiating a soft start.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank start-up errors. If the soft-start block is enabled, it first holds its SS output low to ensure the rest of the circuitries are ready, and then slowly ramps up.

Three events can shut down the chip: EN going low, V_{IN} under-voltage lockout (UVLO), and thermal shutdown. During shutdown, the signaling path is blocked first to avoid any fault triggers. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to FB sets the output voltage (see Figure 3). The feedback resistor (R4) must account for both stability and dynamic response, so it cannot be too large or too small. R4 is estimated to be 100kΩ. R5 is then given using Equation (2):

$$R5 = \frac{R4}{\frac{V_{OUT}}{0.606} - 1} \quad (2)$$

Using a T-type feedback network is highly recommended (see Figure 3).

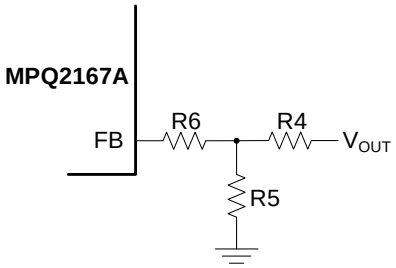


Figure 3: Feedback Network

The R6 and R4 values set the loop bandwidth. Generally, a higher R6 + R4 value results in lower bandwidth. To ensure loop stability, it is strongly recommended to limit the bandwidth at about 10% of the switching frequency (f_{SW}).

Table 1 lists the recommended feedback divider resistor values for common output voltages. Check the loop analysis before using in application. Change the resistance of R_T for loop stability if necessary.

Table 1: Resistor Values for Typical V_{OUT}

V_{OUT} (V)	R6 (kΩ)	R4 (kΩ)	R5 (kΩ)
1.2	100	100 (1%)	100 (1%)
1.5	100	100 (1%)	66.5 (1%)
1.8	100	100 (1%)	49.9 (1%)
2.5	100	100 (1%)	31.6 (1%)
3.3	100	100 (1%)	22.1 (1%)

Selecting the Inductor

The inductor must supply constant current to the output load while being driven by the switching input voltage. For a default 2.1MHz application, a 0.47µH to 1.5µH inductor is recommended. For the highest efficiency, chose an inductor with a DC resistance below 15mΩ. When setting the frequency or SYNC function, the inductance may need to be increased with the frequency decreasing. A larger-value inductor results in less ripple current and a lower output ripple voltage. However, larger-value inductors are physically larger, and have a higher series resistance and/or lower saturation current.

A good rule to determine the inductor value is to make the inductor ripple current approximately 30% of the maximum load current. Ensure that the peak inductor current is below the device peak current limit. The inductance value can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. Do not use other capacitor types, such Y5V and Z5U, because they lose too much capacitance with frequency, temperature, and bias voltage.

Place the input capacitors as close to IN as possible. For most applications, a 22µF capacitor is sufficient. For applications with higher output voltage, use a 47µF capacitor to improve system stability. To get a small solution size, it is better to choose a proper package size capacitor with a rating voltage compliant to the input spec.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple

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current rating. The rating should exceed the converter's maximum input ripple current. The input ripple current can be calculated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, estimated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor whose RMS current rating that is greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, use a small, high-quality ceramic capacitor (0.1μF) placed as close to the IC as possible. The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system design, choose an input capacitor that meets the specification.

The input voltage ripple caused by capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

The output capacitor maintains the output DC voltage. Low-ESR ceramic capacitors are recommended for their small size and ability to keep the output voltage ripple low. Electrolytic and polymer capacitors may also be used.

The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (9)$$

Where R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

When choosing the output capacitance, consider the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, the energy stored in the inductor is transferred to C_{OUT}, which causes its voltage to rise. To achieve a proper overshoot relative to the regulated voltage, the output capacitance can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times ((V_{OUTMAX} / V_{OUT})^2 - 1)} \quad (12)$$

Where V_{OUTMAX} / V_{OUT} is the maximum allowable overshoot.

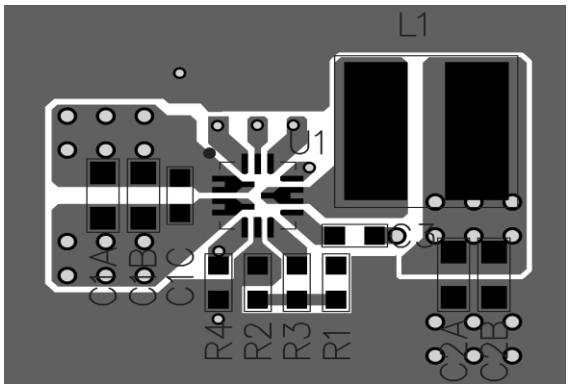
After calculating the capacitance required for both the ripple and overshoot, choose the larger of the calculated values. The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ2167A can be optimized for a wide range of capacitance and ESR values.

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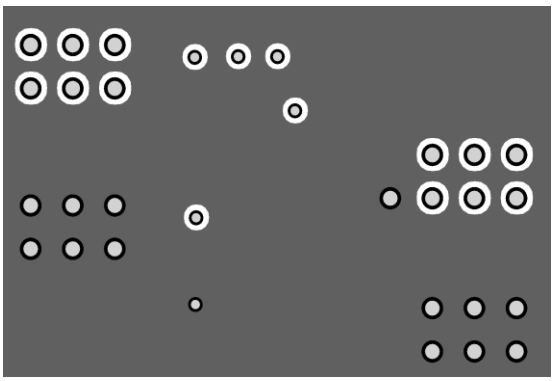
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 4 and follow the guidelines below:

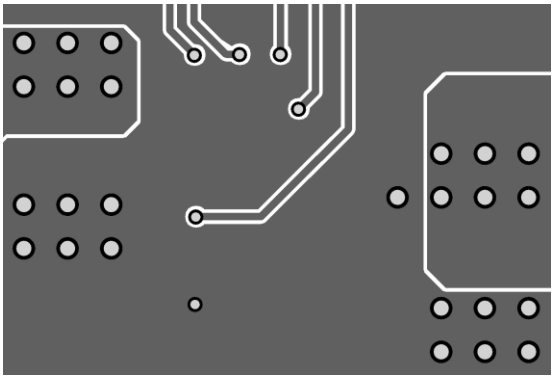
1. Place high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place input capacitors as close to IN as possible to minimize high-frequency noise.
3. Place the feedback resistor divider as close as possible to FB.
4. Route the FB trace away from the switching (SW) node.
5. Connect the bottom IN and SW pads to a large copper area to improve thermal performance.
6. Use large copper areas for power planes (IN, SW, OUT, and GND) to minimize conduction loss and thermal stress.
7. Use multiple vias to connect the power planes to the internal layers.



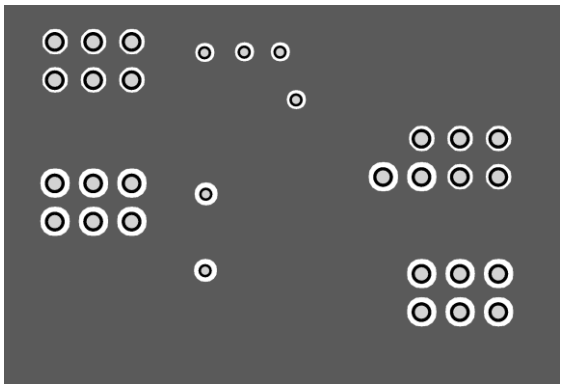
Top and Top Silk Layer



Inner Layer 1



Inner Layer 2



Bottom and Bottom Silk Layer

Figure 4: Recommended PCB Layout (7)

Note:

7) The recommended PCB layout is based on the circuit in Figure 5.

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TYPICAL APPLICATION CIRCUITS

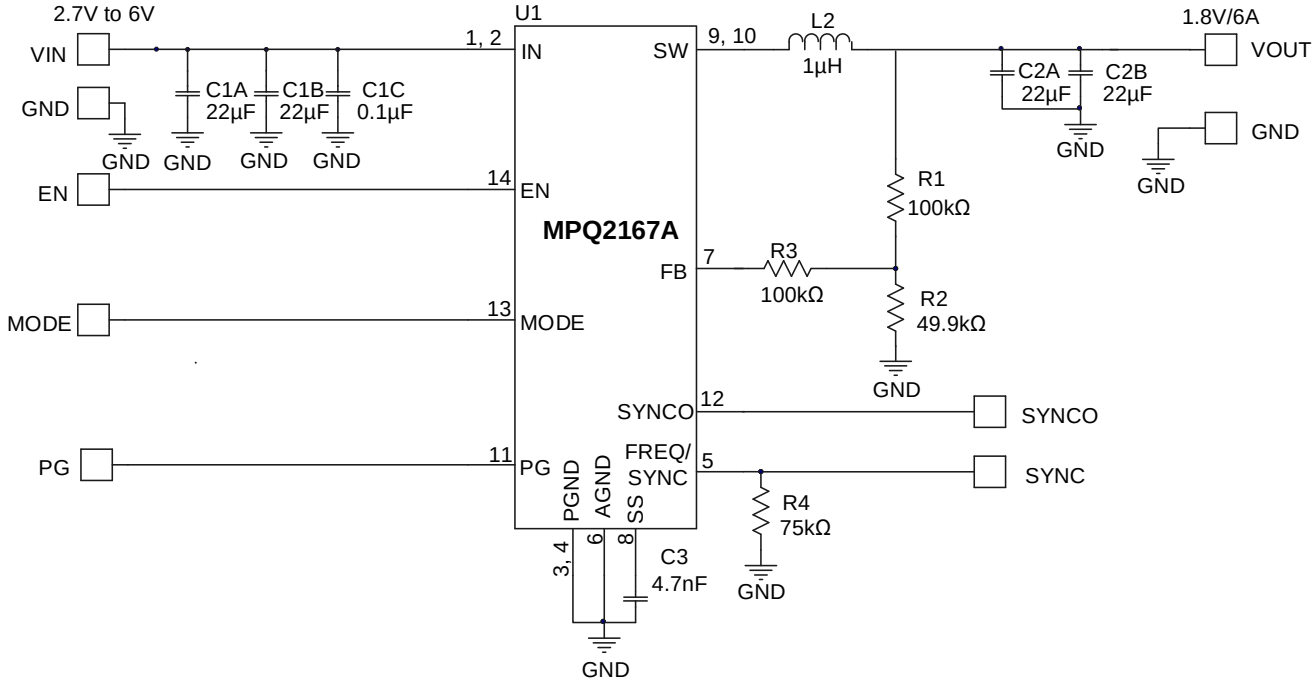


Figure 5: V_{OUT} = 1.8V, I_{OUT} = 6A Application Circuit

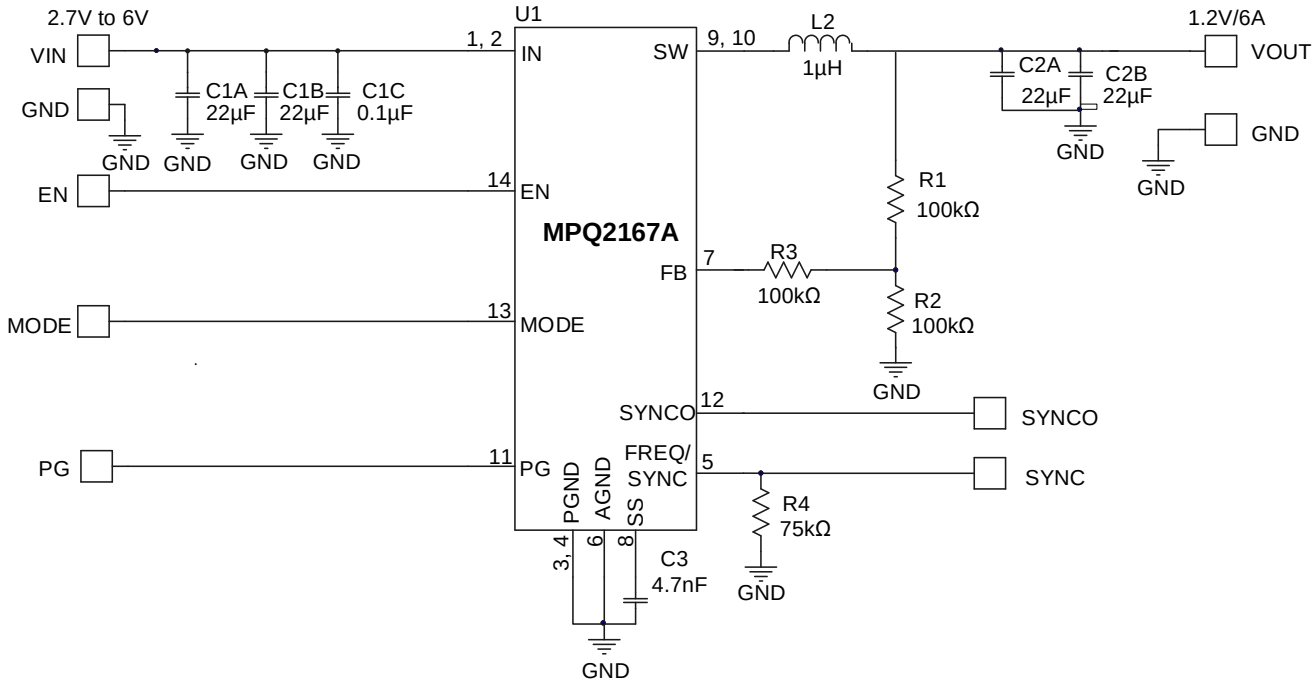
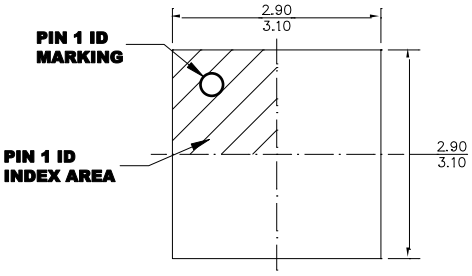


Figure 6: V_{OUT} = 1.2V, I_{OUT} = 6A Application Circuit

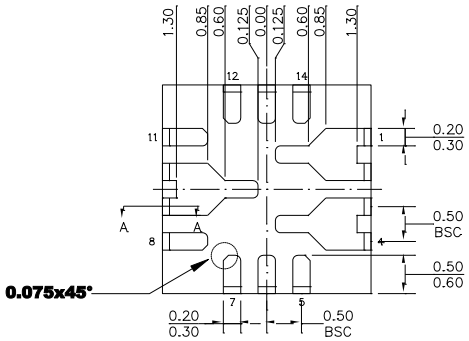
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PACKAGE INFORMATION

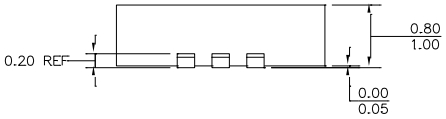
QFN-14 (3mmx3mm)
Wettable Flank



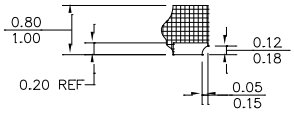
TOP VIEW



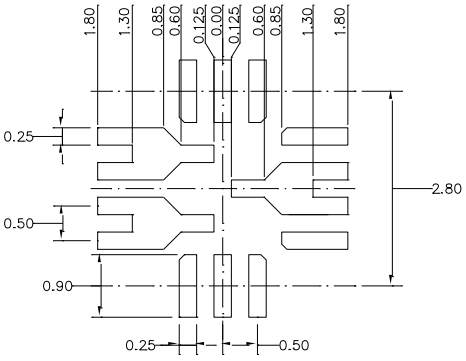
BOTTOM VIEW



SIDE VIEW



SECTION A-A



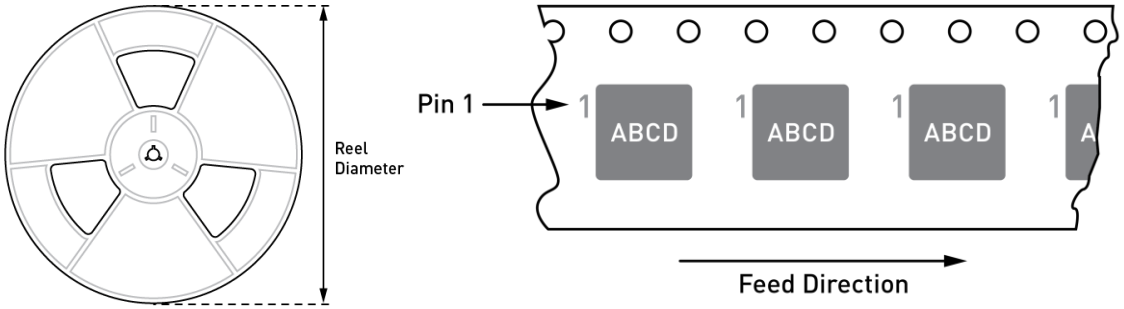
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2167AGQE-AEC1–Z	QFN-14 (3mmx3mm)	5000	13in	12mm	8mm

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