ispClock™5300S Family

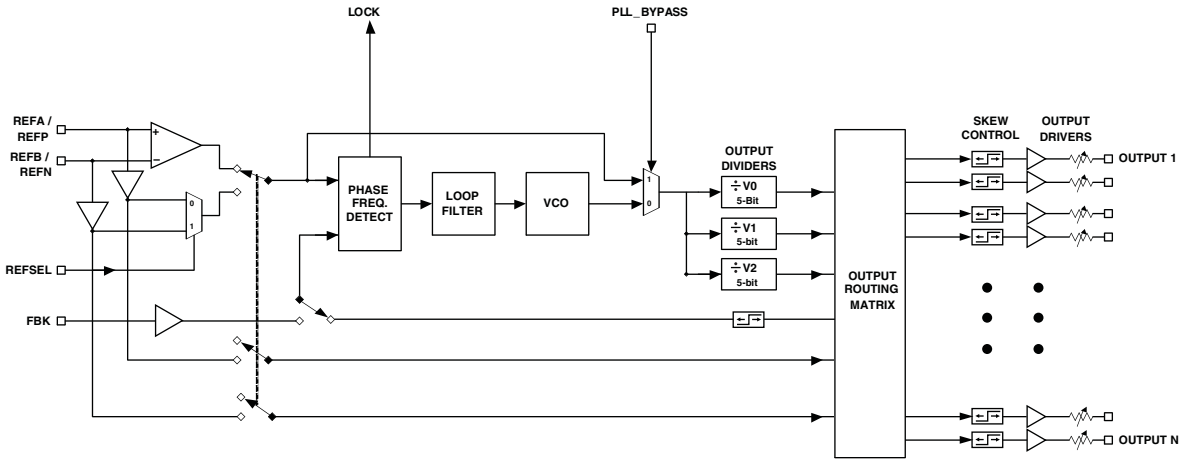
In-System Programmable, Zero-Delay Universal Fan-Out Buffer, Single-Ended

October 2007 **Preliminary Data Sheet DS1010**

Features

- **Four Operating Configurations**
  - Zero delay buffer
  - Zero delay and non-zero delay buffer
  - Dual non-zero delay buffer
  - Non-zero delay buffer with output divider
- **8MHz to 267MHz Input/Output Operation**
- **Low Output to Output Skew (<100ps)**
- **Low Jitter Peak-to-Peak (< 70 ps)**
- **Up to 20 Programmable Fan-out Buffers**
  - Programmable single-ended output standards and individual enable controls
    - LVTTL, LVCMOS, HSTL, eHSTL, SSTL
  - Programmable output impedance
    - 40 to 70Ω in 5Ω increments
  - Programmable slew rate
  - Up to 10 banks with individual V_{CCO} and GND
    - 1.5V, 1.8V, 2.5V, 3.3V
- **Fully Integrated High-Performance PLL**
  - Programmable lock detect
  - Three “Power of 2” output dividers (5-bit)
  - Programmable on-chip loop filter
  - Compatible with spread spectrum clocks
  - Internal/external feedback
- **Precision Programmable Phase Adjustment (Skew) Per Output**
  - 8 settings; minimum step size 156ps
    - Locked to VCO frequency
  - Up to +/- 5ns skew range
  - Coarse and fine adjustment modes
- **Up to Three Clock Frequency Domains**
- **Flexible Clock Reference and External Feedback Inputs**
  - Programmable single-ended or differential input reference standards
    - LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, Differential HSTL, Differential SSTL
  - Clock A/B selection multiplexer
  - Programmable Feedback Standards
    - LVTTL, LVCMOS, SSTL, HSTL
  - Programmable termination
- **All Inputs and Outputs are Hot Socket Compliant**
- **Full JTAG Boundary Scan Test In-System Programming Support**
- **Exceptional Power Supply Noise Immunity**
- **Commercial (0 to 70°C) and Industrial (-40 to 85°C) Temperature Ranges**
- **48-pin and 64-pin TQFP Packages**
- **Applications**
  - Circuit board common clock distribution
  - PLL-based frequency generation
  - High fan-out clock buffer
  - Zero-delay clock buffer

ispClock5300S Family Functional Diagram



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General Description

The ispClock5300S is an in-system-programmable zero delay universal fan-out buffer for use in clock distribution applications. The ispClock5312S, the first member of the ispClock5300S family, provides up to 12 single-ended ultra low skew outputs. Each pair of outputs may be independently configured to support separate I/O standards (LVTTL, LVCMOS -3.3V, 2.5V, 1.8, SSTL, HSTL) and output frequency. In addition, each output provides independent programmable control of termination, slew-rate, and timing skew. All configuration information is stored on-chip in non-volatile $E^2CMOS^®$ memory.

The ispClock5300S devices provide extremely low propagation delay (zero-delay) from input to output using the on-chip low jitter high-performance PLL. A set of three programmable 5-bit counters can be used to generate three frequencies derived from the PLL clock. These counters are programmable in powers of 2 only (1, 2, 4, 8, 16, 32). The clock output from any of the V-dividers can then be routed to any clock output pin through the output routing matrix. The output routing matrix, in addition, also enables routing of reference clock inputs directly to any output.

The ispClock5300S device can be configured to operate in four modes: zero delay buffer mode, dual non-zero delay buffer mode, non-zero delay buffer mode with output dividers, and combined zero-delay and non-zero delay buffer mode.

The core functions of all members of the ispClock5300S family are identical. Table 1 summarizes the ispClock5300S device family.

Table 1. ispClock5300S Family

Device	Number of Programmable Clock Inputs	Number of Programmable Single-Ended Outputs
ispClock5320S	1 Differential, 2 Single-Ended	20
ispClock5316S	1 Differential, 2 Single-Ended	16
ispClock5312S	1 Differential, 2 Single-Ended	12
ispClock5308S	1 Differential, 2 Single-Ended	8
ispClock5304S	1 Differential, 2 Single-Ended	4

Figure 1. ispClock5304S Functional Block Diagram

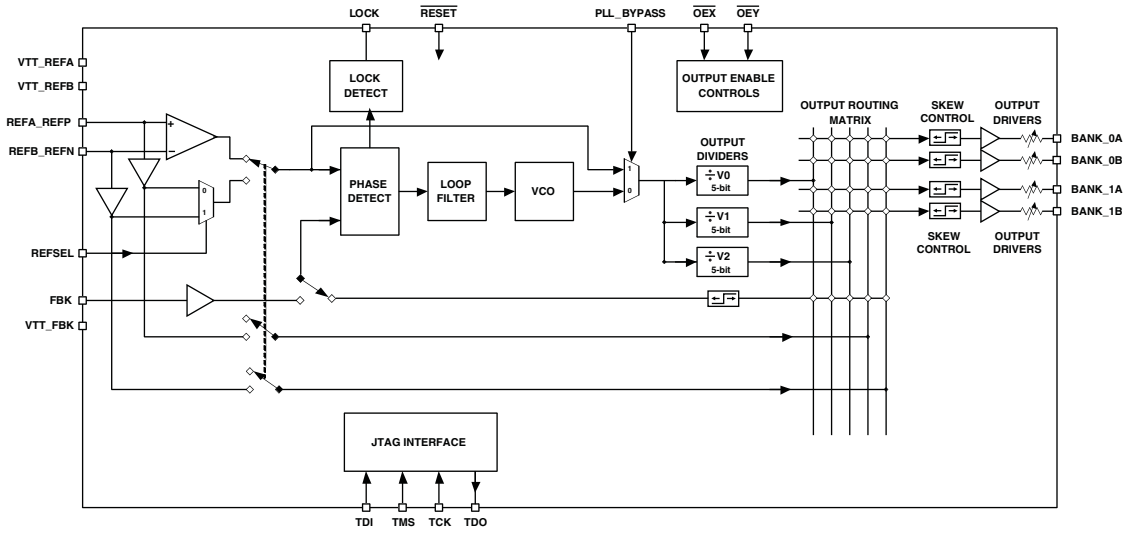


Figure 2. ispClock5308S Functional Block Diagram

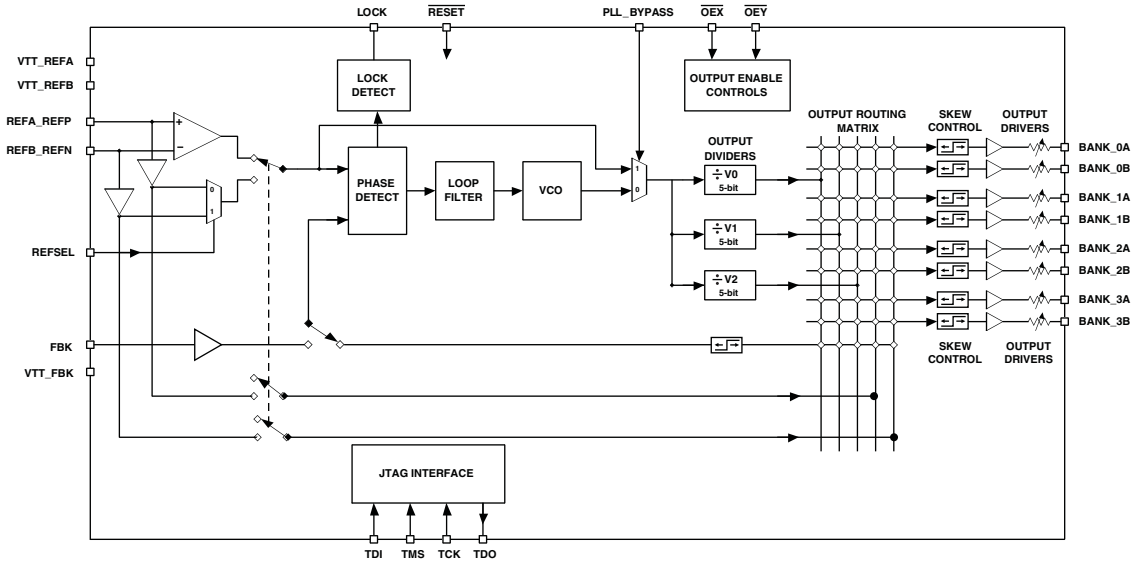


Figure 3. ispClock5312S Functional Block Diagram

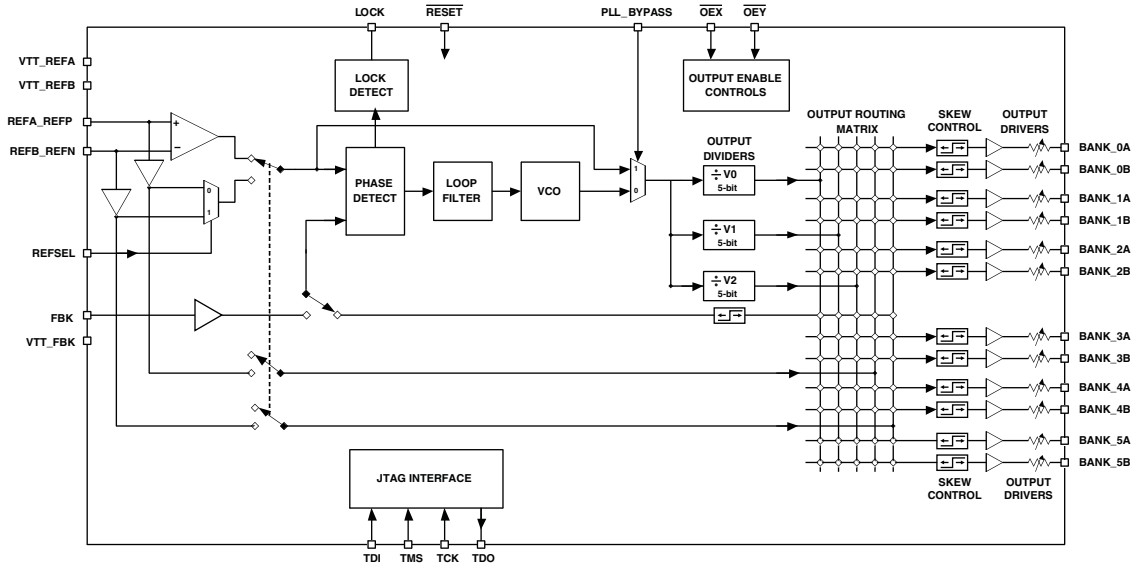


Figure 4. ispClock5316S Functional Block Diagram

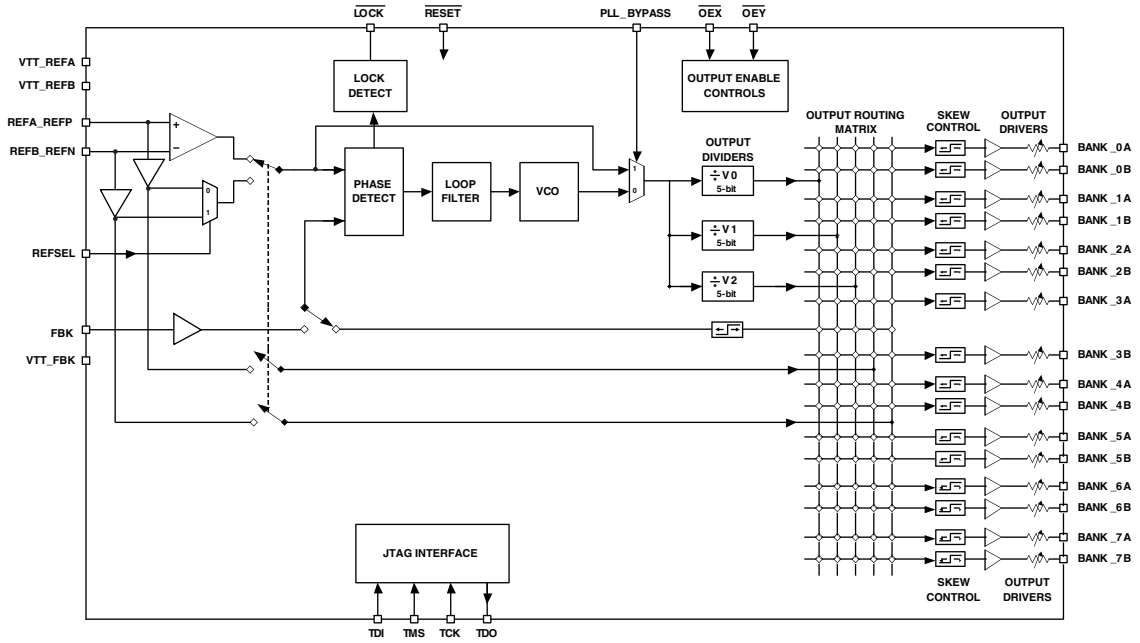
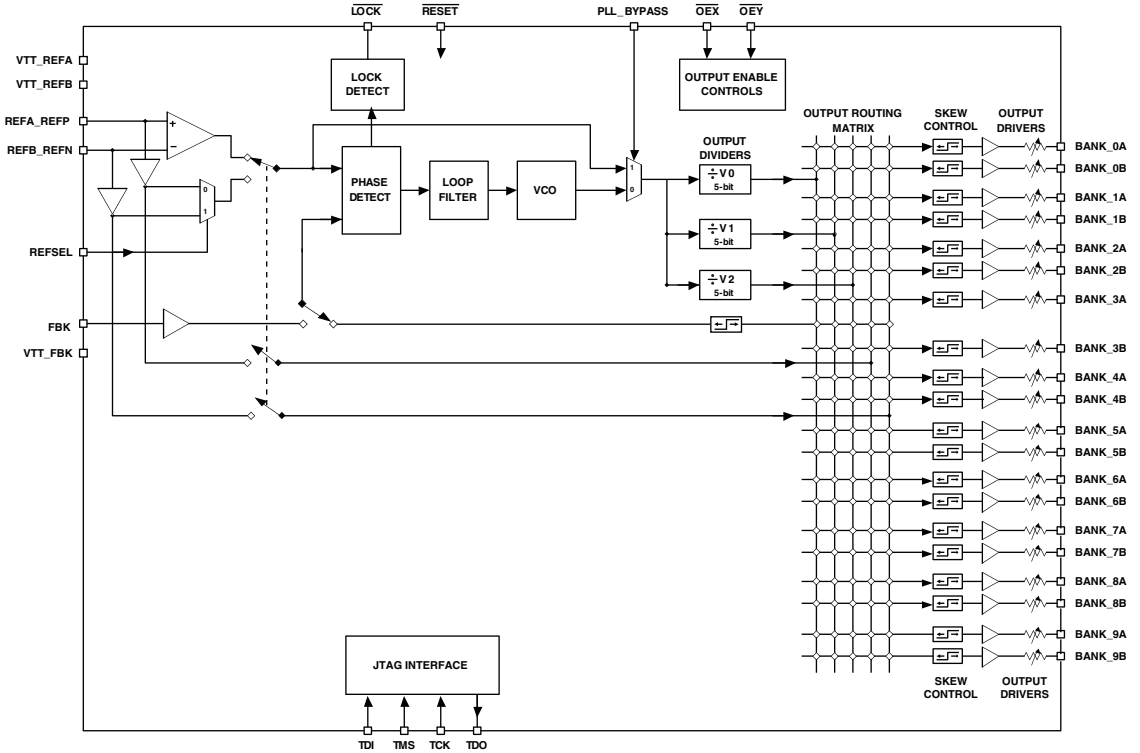


Figure 5. ispClock5320S Functional Block Diagram



Absolute Maximum Ratings

	ispClock5300S
Core Supply Voltage V_{CCD}	-0.5 to 5.5V
PLL Supply Voltage V_{CCA}	-0.5 to 5.5V
JTAG Supply Voltage V_{CCJ}	-0.5 to 5.5V
Output Driver Supply Voltage V_{CCO}	-0.5 to 4.5V
Input Voltage	-0.5 to 4.5V
Output Voltage[1]	-0.5 to 4.5V
Storage Temperature	-65 to 150°C
Junction Temperature with power supplied	-40 to 130°C

1. When applied to an output when in high-Z condition

Recommended Operating Conditions

Symbol	Parameter	Conditions	ispClock5300S		Units
			Min.	Max.	
V_{CCD}	Core Supply Voltage		3.0	3.6	V
V_{CCJ}	JTAG I/O Supply Voltage		1.62	3.6	V
V_{CCA}	Analog Supply Voltage		3.0	3.6	V
$V_{CCXSLEW}$	V_{CC} Turn-on Ramp Rate	All supply pins	—	0.33	V/µs
T_{JOP}	Operating Junction Temperature	Commercial	0	120	°C
		Industrial	-40	130	
T_A	Ambient Operating Temperature	Commercial	0	70[1]	°C
		Industrial	-40	85[1]	

1. Device power dissipation may also limit maximum ambient operating temperature.

Recommended Operating Conditions – V_{CCO} vs. Logic Standard

Logic Standard	V_{CCO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL	3.0	3.3	3.6	—	—	—	—	—	—
LVCMOS 1.8V	1.71	1.8	1.89	—	—	—	—	—	—
LVCMOS 2.5V	2.375	2.5	2.625	—	—	—	—	—	—
LVCMOS 3.3V	3.0	3.3	3.6	—	—	—	—	—	—
SSTL1.8	1.71	1.8	1.89	0.84	0.90	0.95	—	0.5 x V_{CCO}	—
SSTL2 Class 1	2.375	2.5	2.625	1.15	1.25	1.35	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL3 Class 1	3.0	3.3	3.6	1.30	1.50	1.70	V_{REF} - 0.05	V_{REF}	V_{REF} + 0.05
HSTL Class 1	1.425	1.5	1.575	0.68	0.75	0.90	—	0.5 x V_{CCO}	—
eHSTL Class 1	1.71	1.8	1.89	0.84	0.90	0.95	—	0.5 x V_{CCO}	—

Note: '—' denotes V_{REF} or V_{TT} not applicable to this logic standard

E²CMOS Memory Write/Erase Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Erase/Reprogram Cycles		1000	—	—	

Performance Characteristics – Power Supply

Symbol	Parameter	Conditions	Typ.	Max.	Units
I_{CCD}	Core Supply Current[2]	f_{VCO} = 400MHz Feedback Output Active	110	150	mA
$I_{CCDADDER}$	Incremental I_{CCD} per Active Output	f_{OUT} = 267MHz		1.5	mA
I_{CCA}	Analog Supply Current[2]	f_{VCO} = 400MHz	5.5	7	mA
I_{CCO}	Output Driver Supply Current (per Bank)	V_{CCO} = 1.8V[1], LVCMOS, f_{OUT} = 267MHz	16	20	mA
		V_{CCO} = 2.5V[1], LVCMOS, f_{OUT} = 267MHz	21	27	mA
		V_{CCO} = 3.3V[1], LVCMOS, f_{OUT} = 267MHz	27	35	mA
I_{CCJ}	JTAG I/O Supply Current (static)	V_{CCJ} = 1.8V		300	µA
		V_{CCJ} = 2.5V		400	µA
		V_{CCJ} = 3.3V		400	µA

1. Supply current consumed by each bank, both outputs active, 5pF load.
2.All unused REFCLK and feedbacks connected to ground.

DC Electrical Characteristics – Single-Ended Logic

Logic Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min.	Max.	Min.	Max.				
LVTTL/LVCMOS 3.3V	-0.3	0.8	2	3.6	0.4	V_{CCO} - 0.4	12[3]	-12[3]
LVCMOS 1.8V	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	12[3]	-12[3]
LVCMOS 2.5V	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	12[3]	-12[3]
SSTL2 Class 1	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54[1]	V_{CCO} - 0.81[1]	7.6	-7.6
SSTL3 Class 1	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.9[1]	V_{CCO} - 1.3[1]	8	-8
HSTL Class 1	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4[2]	V_{CCO} - 0.4[2]	8	-8
eHSTL Class 1	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4[2]	V_{CCO} - 0.4[2]	8	-8

1. Specified for 40Ω internal series output termination.
2. Specified for ≈20Ω internal series output termination, fast slew rate setting.
3. For slower slew rate setting, I_{OH}, I_{OL} should be limited to 8mA.

DC Electrical Characteristics – LVDS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ICM}	Common Mode Input Voltage		V_{THD}/2		2.325	V
V_{THD}	Differential Input Threshold	$V_{ICM} \leq$ 2V	±100	—	—	mV
		2V < V_{ICM} < 2.325V	±150	—	—	mV
V_{IN}	Input Voltage		0	—	2.4	V

DC Electrical Characteristics – Differential LVPECL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input Voltage High	V_{CCD} = 3.0 to 3.6V	V_{CCD} - 1.17	—	V_{CCD} - 0.88	V
		V_{CCD} = 3.3V	2.14	—	2.42	
V_{IL}	Input Voltage Low	V_{CCD} = 3.0 to 3.6V	V_{CCD} - 1.81	—	V_{CCD} - 1.48	V
		V_{CCD} = 3.3V	1.49	—	1.83	

Electrical Characteristics – Differential SSTL18

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IL}	Low-Logic Level Input Voltage				0.61	V
V_{IH}	Hi Logic Level Input Voltage		1.17			V
V_{IX}	Input Pair Differential Crosspoint Voltage		V_{REF} -175mV		V_{REF} +175mV	V

Electrical Characteristics – Differential SSTL2

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		3.225	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.62		3.225	V_{PP}
V_{IX}	Input Pair Differential Crosspoint Voltage		V_{REF} - 200 mV		V_{REF} + 200 mV	V

Electrical Characteristics – Differential HSTL

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		3.325	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.4		3.325	V_{PP}
V_{IX}	Input Pair Differential Crosspoint Voltage		0.68		0.9	V

Electrical Characteristics – Differential eHSTL

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{SWING(DC)}$	DC Differential Input Voltage Swing		-0.03		3.325	V
$V_{SWING(AC)}$	AC Input Differential Voltage		0.4		3.325	V_{PP}
V_{IX}	Input Pair Differential Crosspoint Voltage		0.68		0.9	V

DC Electrical Characteristics – Input/Output Loading

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{LK}	Input Leakage	Note 1	—	—	±10	µA
I_{PU}	Input Pull-up Current	Note 2	—	80	120	µA
I_{PD}	Input Pull-down Current	REFSEL, PLL_BYPASS	—	120	150	µA
		$\overline{OEX}$, $\overline{OEY}$, 2.5V CMOS Logic Standard	—	120	150	µA
		$\overline{OEX}$, $\overline{OEY}$, & 3.3V CMOS Logic Standard	—	200	400	µA
I_{OLK}	Tristate Leakage Output	Note 4	—	—	±10	µA
C_{IN}	Input Capacitance	Notes 2, 3, 5	—	8	10	pF
		Note 6	—	10	11	pF

1. Applies to clock reference inputs when termination 'open'.
2. Applies to TDI, TMS and $\overline{RESET}$ inputs.
3. Applies to REFSEL and PLL_BYPASS, $\overline{OEX}$, $\overline{OEY}$.
4. Applies to all logic types when in tristated mode.
5. Applies to $\overline{OEX}$, $\overline{OEY}$, TCK, $\overline{RESET}$ inputs.
6. Applies to REFA_REFP, REFB_REFN, FBK.

Switching Characteristics – Timing Adders for I/O Modes

Adder Type	Description	Min.	Typ.	Max.	Units
t_{IOI} Input Adders[2]					
LVTTL_in	Using LVTTL Standard		0.00		ns
LVCMOS18_in	Using LVCMOS 1.8V Standard		0.10		ns
LVCMOS25_in	Using LVCMOS 2.5V Standard		0.00		ns
LVCMOS33_in	Using LVCMOS 3.3V Standard		0.00		ns
SSTL2_in	Using SSTL2 Standard		0.00		ns
SSTL3_in	Using SSTL3 Standard		0.00		ns
HSTL_in	Using HSTL Standard		1.15		ns
eHSTL_in	Using eHSTL Standard		1.10		ns
LVDS_in	Using LVDS Standard		0.60		ns
LVPECL_in	Using LVPECL Standard		0.60		ns
t_{IOO} Output Adders[1, 3]					
LVTTL_out	Output Configured as LVTTL Buffer		0.25		ns
LVCMOS18_out	Output Configured as LVCMOS 1.8V Buffer		0.25		ns
LVCMOS25_out	Output Configured as LVCMOS 2.5V Buffer		0.25		ns
LVCMOS33_out	Output Configured as LVCMOS 3.3V Buffer		0.25		ns
SSTL18_out	Output Configured as SSTL18 Buffer		0.00		ns
SSTL2_out	Output Configured as SSTL2 Buffer		0.00		ns
SSTL3_out	Output Configured as SSTL3 Buffer		0.00		ns
HSTL_out	Output Configured as HSTL Buffer		0.00		ns
eHSTL_out	Output Configured as eHSTL Buffer		0.00		ns
t_{IOS} Output Slew Rate Adders[1]					
Slew_1	Output Slew_1 (Fastest)	—	0.00	—	ps
Slew_2	Output Slew_2	—	475	—	ps
Slew_3	Output Slew_3	—	950	—	ps
Slew_4	Output Slew_4 (Slowest)	—	1900	—	ps

1. Measured under standard output load conditions – see Figures 6 and 7.
2. All input adders referenced to LVTTL.
3. All output adders referenced to SSTL/HSTL/eHSTL.

Output Rise and Fall Times – Typical Values[1, 2]

Output Type	Slew 1 (Fastest)		Slew 2		Slew 3		Slew 4 (Slowest)		Units
	t_R	t_F	t_R	t_F	t_R	t_F	t_R	t_F	
LVTTL	0.54	0.76	0.60	0.87	0.78	1.26	1.05	1.88	ns
LVCMOS 1.8V	0.75	0.69	0.88	0.78	0.83	1.11	1.20	1.68	ns
LVCMOS 2.5V	0.57	0.69	0.65	0.78	0.99	0.98	1.65	1.51	ns
LVCMOS 3.3V	0.55	0.77	0.60	0.87	0.78	1.26	1.05	1.88	ns
SSTL18	0.55	0.40	—	—	—	—	—	—	ns
SSTL2	0.50	0.40	—	—	—	—	—	—	ns
SSTL3	0.50	0.45	—	—	—	—	—	—	ns
HSTL	0.60	0.45	—	—	—	—	—	—	ns
eHSTL	0.55	0.40	—	—	—	—	—	—	ns

1. See Figures 6 and 7 for test conditions.
2. Measured between 20% and 80% points.

Output Test Loads

Figures 6 and 7 show the equivalent termination loads used to measure rise/fall times, output timing adders and other selected parameters as noted in the various tables of this data sheet.

Figure 6. CMOS Termination Load

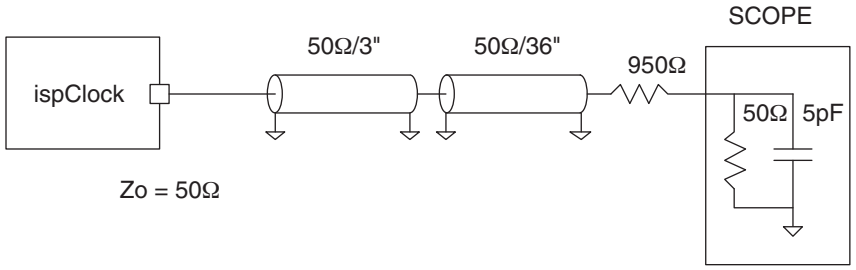
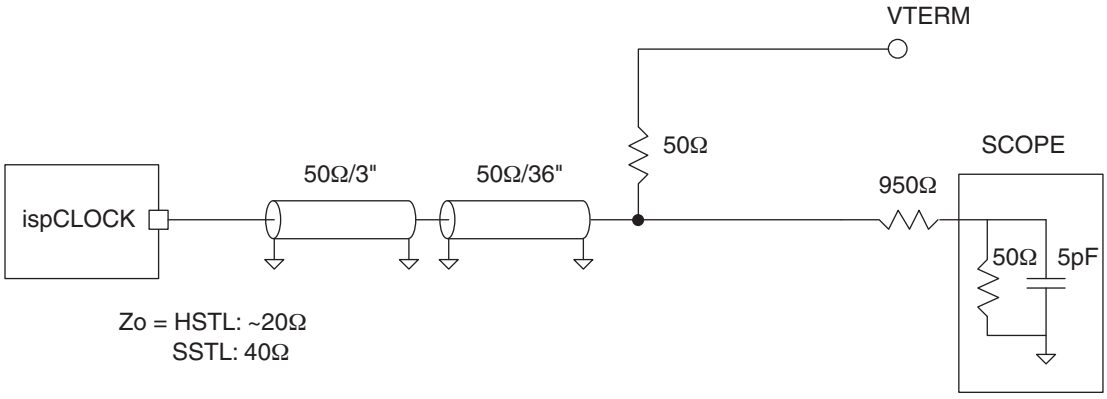


Figure 7. eHSTL/HSTL/SSTL Termination Load



Programmable Input and Output Termination Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{IN}	Input Resistance	Rin=40Ω setting	36	—	44	Ω
		Rin=45Ω setting	40.5	—	49.5	
		Rin=50Ω setting	45	—	55	
		Rin=55Ω setting	49.5	—	60.5	
		Rin=60Ω setting	54	—	66	
		Rin=65Ω setting	59	—	71.5	
		Rin=70Ω setting	61	—	77	
R_{OUT}	Output Resistance	Rout≈20Ω setting T_A = 25°C	—	14	—	Ω
		Rout≈40Ω setting T_A = 25°C	36	38	44	
		Rout≈45Ω setting T_A = 25°C	41	45	51	
		Rout≈50Ω setting T_A = 25°C	45	50	55	
		Rout≈55Ω setting T_A = 25°C	50	55	61	
		Rout≈60Ω setting T_A = 25°C	54	59	66	
		Rout≈65Ω setting T_A = 25°C	59	65	71	
		Rout≈70Ω setting T_A = 25°C	63	72	78	
R_{OUT_TEMPCO}	Output Resistor Temperature Coefficient		—	500	—	PPM/°C

Performance Characteristics – PLL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{REF}, f_{FBK}	Reference and feedback input frequency range		8		267	MHz
$t_{CLOCKHI}$, $t_{CLOCKLO}$	Reference and feedback input clock HIGH and LOW times		1.25			ns
t_{RINP}, t_{FINP}	Reference and feedback input rise and fall times	Measured between 20% and 80% levels			5	ns
f_{PFD}	Phase detector input frequency range		8		267	MHz
f_{VCO}	VCO operating frequency		160		400	MHz
V_{DIV}	Output divider range (Power of 2)		1		32	
f_{OUT}	Output frequency range[1]	Fine Skew Mode	5		267	MHz
		Coarse Skew Mode	2.5		200	MHz
t_{JIT} (cc)	Output adjacent-cycle jitter[5] (1000 cycle sample)	$f_{PFD} \geq$ 100MHz			70	ps (p-p)
t_{JIT} (per)	Output period jitter[5] (10000 cycle sample)	$f_{PFD} \geq$ 100MHz			9	ps (RMS)
$t_{JIT(\phi)}$	Reference clock to output jitter[5] (2000 cycle sample)	$f_{PFD} \geq$ 100MHz			50	ps (RMS)
$t\phi$	Static phase offset[4]	PFD input frequency ≥100MHz[3]	-40		100	ps
$t\phi_{DYN}$	Dynamic phase offset	100MHz, Spread Spectrum Modulation index = 0.5%		2	8	ps
DC_{ERR}	Output duty cycle error	Output type LVCMOS 3.3V[2] f_{OUT} >100 MHz	47		53	%
$t_{PDBYPASS}$	Reference clock to output propagation delay	V=1		6.5		ns
t_{PD_FOB}	Reference to output propagation delay in Non-Zero Delay Buffer Mode	V=1	2.5	3.5	5	ns
t_{DELAY}	Reference to output delay with internal feedback mode[3]	V=1		500		ps
t_{LOCK}	PLL lock time	From Power-up event		150		µs
		From $\overline{\text{RESET}}$ event		15		µs
t_{RELOCK}	PLL relock time	To same reference frequency		15		µs
		To different frequency		150		µs
PSR	Power supply rejection, period jitter vs. power supply noise	$f_{IN} = f_{OUT}$ = 100MHz $V_{CCA} = V_{CCD} = V_{CCO}$ modulated with 100kHz sinusoidal stimulus		0.05		$\frac{\text{ps(RMS)}}{\text{mV(p-p)}}$

1. In PLL Bypass mode (PLL_BYPASS = HIGH), output will support frequencies down to 0Hz (divider chain is a fully static design).
2. See Figures 6 and 7 for output loads.
3. Input and outputs LVCMOS mode
4. Inserted feedback loop delay < 7ns
5. Measured with f_{OUT} = 100MHz, f_{VCO} = 400MHz, input and output interface set to LVCMOS.

Timing Specifications

Skew Matching

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{SKEW}	Output-output Skew	Between any two identically configured and loaded outputs regardless of bank.	—	—	100	ps

Programmable Skew Control

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{SKRANGE}$	Skew Control Range[1]	Fine Skew Mode, f_{VCO} = 160 MHz	—	2.73	—	ns
		Fine Skew Mode, f_{VCO} = 400 MHz	—	1.09	—	
		Coarse Skew Mode, f_{VCO} = 160 MHz	—	5.46	—	
		Coarse Skew Mode, f_{VCO} = 400 MHz	—	2.19	—	
SK_{STEPS}	Skew Steps per Range		—	8	—	
t_{SKSTEP}	Skew Step Size[2]	Fine Skew Mode, f_{VCO} = 160 MHz	—	390	—	ps
		Fine Skew Mode, f_{VCO} = 400 MHz	—	156	—	
		Coarse Skew Mode, f_{VCO} = 160 MHz	—	780	—	
		Coarse Skew Mode, f_{VCO} = 400 MHz	—	312	—	
t_{SKERR}	Skew Time Error[3]	Fine skew mode	—	30	—	ps
		Coarse skew mode	—	50	—	

1. Skew control range is a function of VCO frequency (f_{VCO}). In fine skew mode $T_{SKRANGE} = 7/(16 \times f_{VCO})$. In coarse skew mode $T_{SKRANGE} = 7/(8 \times f_{VCO})$.
2. Skew step size is a function of VCO frequency (f_{VCO}). In fine skew mode $T_{SKSTEP} = 1/(16 \times f_{VCO})$. In coarse skew mode $T_{SKSTEP} = 1/(8 \times f_{VCO})$.
3. Only applicable to outputs with non-zero skew settings.

Control Functions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{DIS/OE}$	Delay Time, $\overline{OEX}$ or $\overline{OEY}$ to Output Disabled/ Enabled		—	10	20	ns
t_{PLL_RSTW}	PLL $\overline{RESET}$ Pulse Width[1]		1	—	—	ms
t_{RSTW}	Logic $\overline{RESET}$ Pulse Width[2]		20	—	—	ns
RST_SLEW	Reset Signal Slew Rate		0.1			V/µs

1. Will completely reset PLL.
2. Will only reset digital logic.

Static Phase Offset vs. Reference Clock Logic Type

Symbol	Reference Clock Logic (REFA/REFB)	Feedback Input Logic (FBK)	Feedback Output Logic (BANK_xA/BANK_xB)	Min.	Max.	Units
$t_{(\phi)}$ – Static Phase Offset	LVCMOS 33	LVCMOS33	LVCMOS33	-40	100	ps
	LVCMOS 25	LVCMOS25	LVCMOS25	-70	80	ps
	LVCMOS 18	LVCMOS18	LVCMOS18	-80	80	ps
	SSTL3	SSTL3	SSTL3	-70	390	ps
	SSTL2	SSTL2	SSTL2	-70	340	ps
	HSTL(1.5V)	HSTL(1.5V)	HSTL(1.5V)	-100	360	ps
	eHSTL(1.8V)	eHSTL(1.8V)	eHSTL(1.8V)	-100	360	ps
	LVDS (2.5V)[1]	LVDS-Single Ended	LVCMOS25	140	530	ps
	LVPECL[1]	LVPECL-Single Ended	LVCMOS33	80	300	ps

1. The output clock to feedback can be skewed to center the static phase offset spread.

Boundary Scan Logic

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK (BSCAN Test) Clock Cycle	40	—	ns
t_{BTCH}	TCK (BSCAN Test) Pulse Width High	20	—	ns
t_{BTCL}	TCK (BSCAN Test) Pulse Width Low	20	—	ns
t_{BTSU}	TCK (BSCAN Test) Setup Time	8	—	ns
t_{BTH}	TCK (BSCAN Test) Hold Time	10	—	ns
t_{BRF}	TCK (BSCAN Test) Rise and Fall Rate	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
t_{BTOZ}	TAP Controller Falling Edge of Clock to Data Output Disable	—	10	ns
t_{BTVO}	TAP Controller Falling Edge of Clock to Data Output Enable	—	10	ns
$t_{BVTCPSU}$	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCPH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BTUCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
t_{BTUOZ}	BSCAN Test Update Register, Falling Edge of Clock to Output Disable	—	25	ns
t_{BTUOV}	BSCAN Test Update Register, Falling Edge of Clock to Output Enable	—	25	ns

JTAG Interface and Programming Mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum TCK Clock Frequency		—	—	25	MHz
t_{CKH}	TCK Clock Pulse Width, High		20	—	—	ns
t_{CKL}	TCK Clock Pulse Width, Low		20	—	—	ns
t_{ISPEN}	Program Enable Delay Time		15	—	—	µs
t_{ISPDIS}	Program Disable Delay Time		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Program		30	—	—	µs
t_{HVDIS}	High Voltage Discharge Time, Erase		200	—	—	µs
t_{CEN}	Falling Edge of TCK to TDO Active		—	—	15	ns
t_{CDIS}	Falling Edge of TCK to TDO Disable		—	—	15	ns
t_{SU1}	Setup Time		8	—	—	ns
t_{H}	Hold Time		10	—	—	ns
t_{CO}	Falling Edge of TCK to Valid Output		—	—	15	ns
t_{PWV}	Verify Pulse Width		30	—	—	µs
t_{PWP}	Programming Pulse Width		20	—	—	ms
t_{BEW}	Bulk Erase Pulse Width		200	—	—	ms

Timing Diagrams

Figure 8. Erase (User Erase or Erase All) Timing Diagram

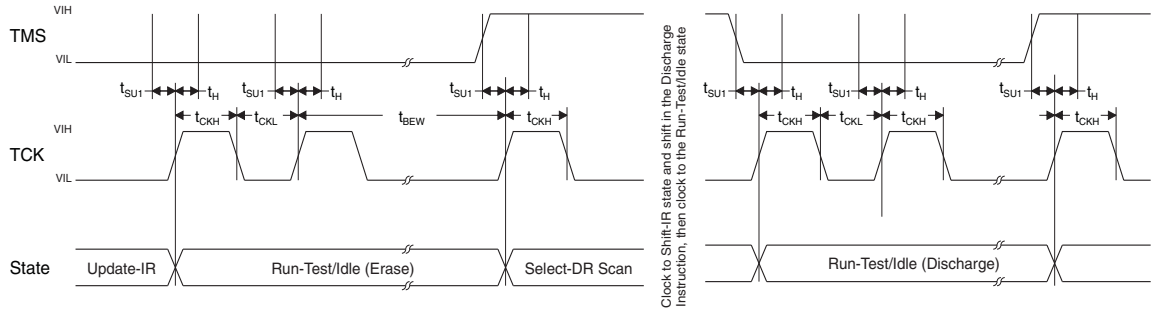


Figure 9. Programming Timing Diagram

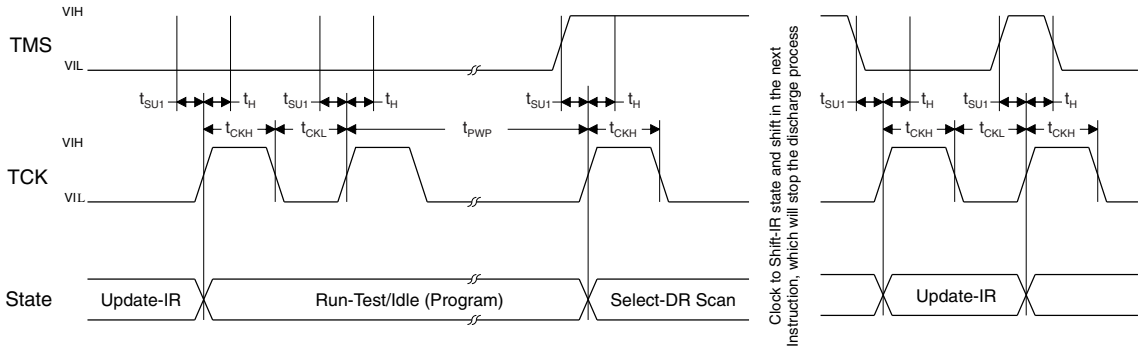


Figure 10. Verify Timing Diagram

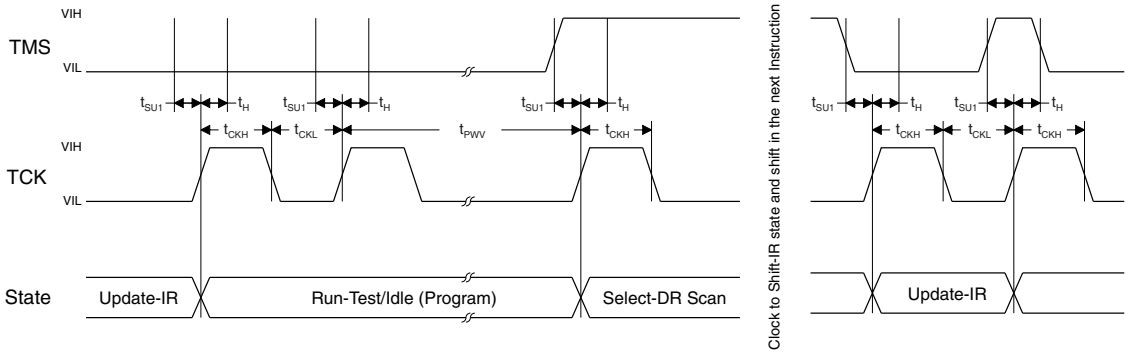
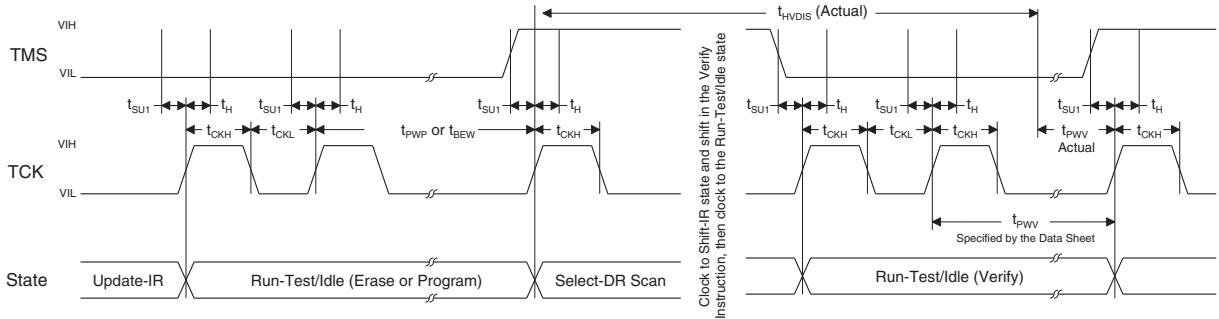
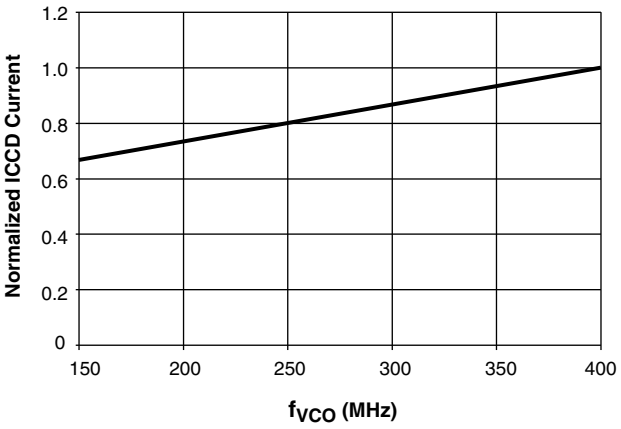


Figure 11. Discharge Timing Diagram

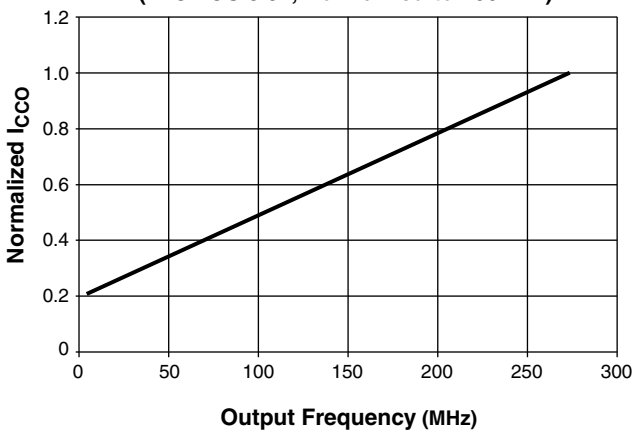


Typical Performance Characteristics

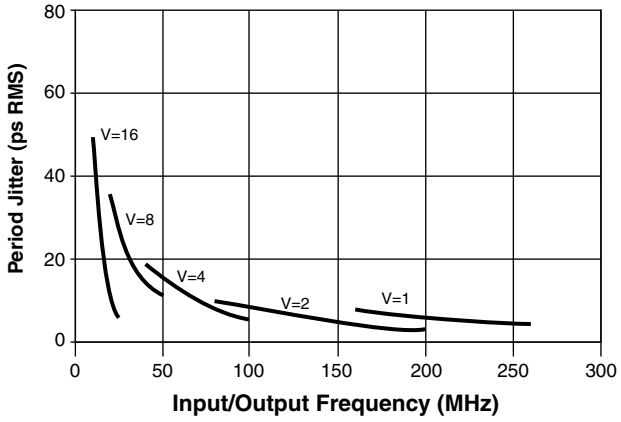
I_{CCD} vs. f_{VCO} (Normalized to 400MHz)



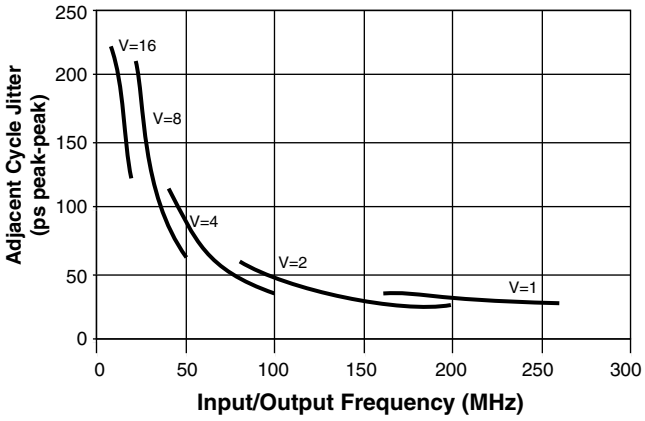
I_{CCO} vs. Output Frequency (LVCMOS 3.3V, Normalized to 266MHz)



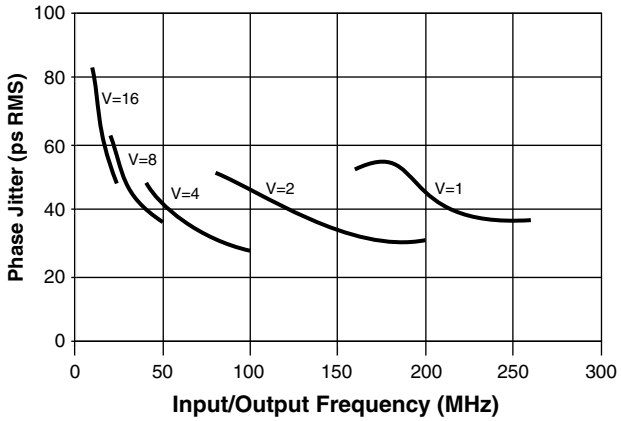
Period Jitter vs. Input/Output Frequency



Adjacent Cycle Jitter vs. Input/Output Frequency



Phase Jitter vs. Input/Output Frequency



Detailed Description

PLL Subsystem

The ispClock5300S provides an integral phase-locked-loop (PLL) which may be used to generate output clock signals at lower, higher, or the same frequency as a user-supplied input reference signal. The core functions of the PLL are an edge-sensitive phase detector, a programmable loop filter, and a high-speed voltage-controlled oscillator (VCO). Additionally, a set of programmable feedback dividers (V[0, 1, 2]) is provided to support the synthesis of different output frequencies.

Phase/Frequency Detector
The ispClock5300S provides an edge-sensitive phase/frequency detector (PFD), which means that the device will function properly over a wide range of input clock reference duty cycles. It is only necessary that the input reference clock meet specified minimum HIGH and LOW times ($t_{CLOCKHI,}$ $t_{CLOCKLO}$) for it to be properly recognized by the PFD. The PFD's output is of a classical charge-pump type, outputting charge packets which are then integrated by the PLL's loop filter.

A lock-detection feature is also associated with the PFD. When the ispClock5300S is in a LOCKED state, the LOCK output pin goes HIGH. The number of cycles required before asserting the LOCK signal in frequency-lock mode can be set from 16 through 256.

When the lock condition is lost the LOCK signal will be de-asserted (Logic '0') immediately.

Loop Filter: The loop filter parameters for each profile are automatically selected by the PAC-Designer software depending on the following:

- Maximum VCO operating frequency

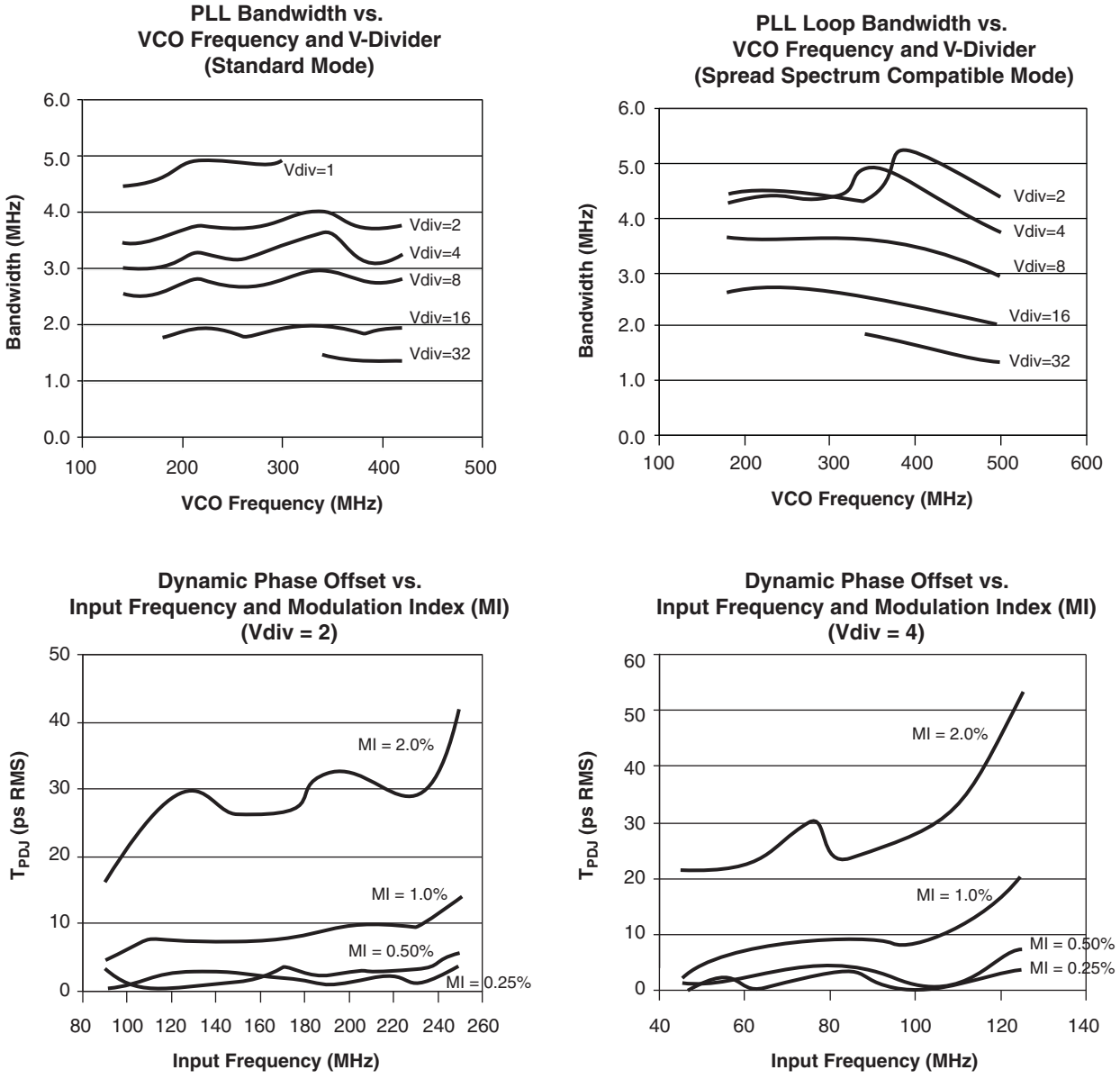
Spread Spectrum Support: The reference clock inputs of the ispClock5300S device are spread spectrum clock tolerant. The tolerance limits are:

- Center spread ±0.125% to ±2%
- Down spread -0.25% to 0.5%
- 30-33kHz modulation frequency

The ispClock5300S PLL has two modes of operation:

- Spread Spectrum setting turned on - Spread Spectrum modulation is transferred from input to output with minimal attenuation.
- Spread Spectrum setting turned off - Spread Spectrum modulation transfer from input to output is attenuated. The extent of attenuation depends on the VCO operating frequency and the feedback divider value.

Figure 12. PLL Loop Bandwidth vs. Feedback Divider Setting (Nominal)



VCO

The ispClock5300S provides an internal VCO which provides an output frequency ranging from 160MHz to 400MHz. The VCO is implemented using differential circuit design techniques which minimize the influence of power supply noise on measured output jitter. The VCO is also used to generate output clock skew as a function of the total VCO period. Using the VCO as the basis for controlling output skew allows for highly precise and consistent skew generation, both from device-to-device, as well as channel-to-channel within the same device.

Output V Dividers

The ispClock5300S incorporates a set of three 5-bit programmable Power of 2 dividers which provide the ability to synthesize output frequencies differing from that of the reference clock input.

Each one of the three V dividers can be independently programmed to provide division ratios ranging from 1 to 32 in Power of 2 steps (1, 2, 4, 8, 16, 32).

When the PLL is selected (PLL_BYPASS=LOW) and locked, the output frequency of each V divider (f_k) may be calculated as:

$$f_k = f_{ref} \frac{V_{fbk}}{V_k} \quad (1)$$

where

f_k is the frequency of V divider k
f_{ref} is the input reference frequency
V_{fbk} is the setting of the V divider used to close the PLL feedback path
V_k is the output divider K

Note that because the feedback may be taken from any V divider, V_k and V_{fbk} may refer to the same divider.

Because the VCO has an operating frequency range spanning 160 MHz to 400 MHz, and the V dividers provide division ratios from 1 to 32, the ispClock5300S can generate output signals ranging from 2.5 MHz to 267 MHz.

PLL_BYPASS Mode
The PLL_BYPASS mode is provided so that input reference signals can be coupled through to the outputs without using the PLL functions. When PLL_BYPASS mode is enabled (PLL_BYPASS=HIGH), the reference clock is routed directly to the inputs of the V dividers. The output frequency for a given V divider (f_K) will be determined by

$$f_k = \frac{f_{REF}}{V_K} \quad (2)$$

When PLL_BYPASS mode is enabled, features such as lock detect and skew generation are unavailable and the output clock is inverted when V_K=1.

Internal/External Feedback Support

The PLL feedback path can be sourced internally or externally through an output pin. When the internal feedback path is selected, one can use all output pins for clock distribution. The programmable skew feature for the feedback path is available in both feedback modes.

Reference and External Feedback Inputs

The ispClock5300S provides configurable, internally-terminated inputs for both clock reference and feedback signals.

The reference clock inputs pins can be interfaced with either one differential input (REFP, REFN) or two single-ended (REFA, REFB) inputs with the active clock selection control through REFSEL pin. The following diagram shows the possible reference clock configurations. Note: When the reference clock inputs are configured as differential input, the REFSEL pin should be grounded.

Table 2. REFSEL Operation for ispClock5300S Programmed as Single-Ended Clock Inputs

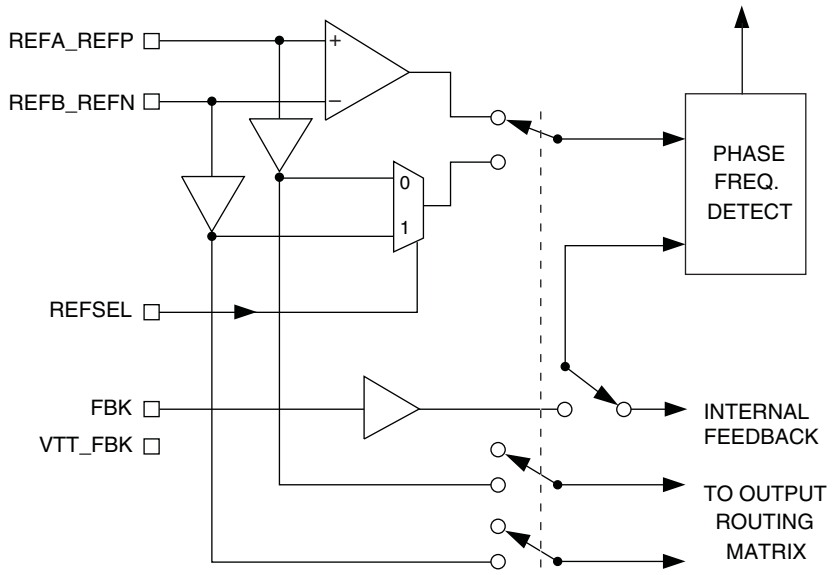
REFSEL	Selected Input
0	REFA
1	REFB

Supported input logic reference standards:

- LVTTL (3.3V)
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL

- eHSTL
- Differential SSTL1.8
- Differential SSTL2
- Differential SSTL3
- Differential HSTL
- LVDS
- LVPECL (differential, 3.3V)

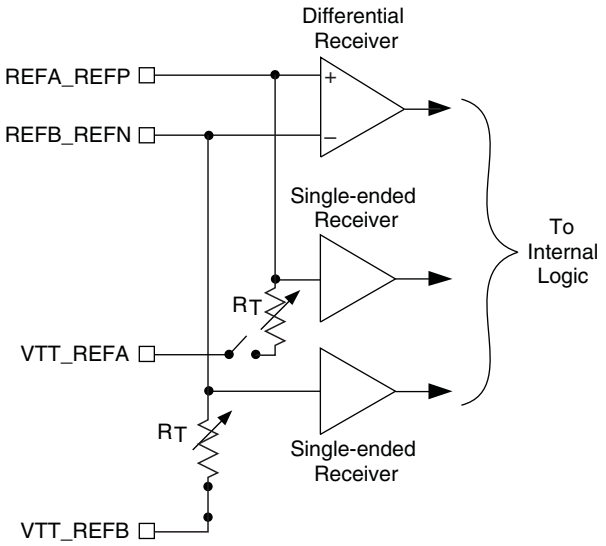
Figure 13. Reference and Feedback Input



Each input features internal programmable termination resistors as shown in Figure 14. The REFA and REFB inputs terminate to VTT_REFA and VTT_REFB respectively. In order to interface to differential clock input one should connect VTT_REFA and VTT_REFB pins together on circuit board and if necessary connect the common node to VTT supply.

The direct connection from REFA and REFB pins to the output routing matrix becomes unavailable when the REFA and REFB pins are configured as differential input pins.

Figure 14. Input Receiver Termination Configuration



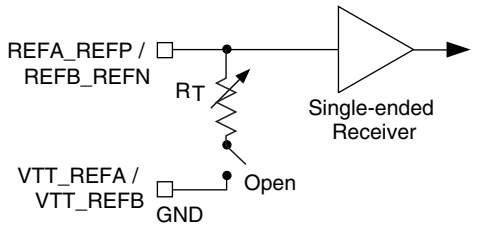
Feedback input is terminated to the VTT_FBK pin through a programmable resistor.

The following usage guidelines are suggested for interfacing to supported logic families.

LVTTL (3.3V), LVCMOS (1.8V, 2.5V, 3.3V)

The receiver should be set to LVCMOS or LVTTL mode, and the input signal can be connected to either the REFA or REFB pins. CMOS transmission lines are generally source terminated, so all termination resistors should be set to the OPEN state. Figure 15 shows the proper configuration. Please note that because switching thresholds are different for LVCMOS running at 1.8V, there is a separate configuration setting for this particular standard. Unused reference inputs and VTT pins should be grounded.

Figure 15. LVCMOS/LVTTL Input Receiver Configuration

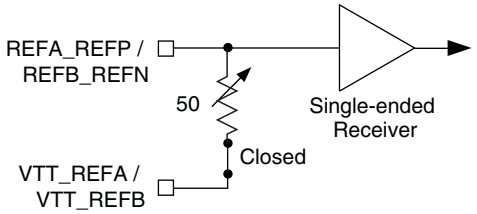


HSTL, eHSTL, SSTL2, SSTL3

The receiver should be set to HSTL/SSTL mode, and the input signal can be connected to the REFA or REFB terminal of the input pair and the associated VTT_REFA or VTT_REFB terminal should be tied to a VTT termination supply. The terminating resistor should be set to 50Ω and the engaging switch should be closed. Figure 16 shows an appropriate configuration. Refer to the "Recommended Operating Conditions - Supported Logic Standards" table in this data sheet for suitable values of V_{REF} and V_{TT}.

One important point to note is that the termination supplies must have low impedance and be able to both source and sink current without experiencing fluctuations. These requirements generally preclude the use of a resistive divider network, which has an impedance comparable to the resistors used, or of commodity-type linear voltage regulators, which can only source current. The best way to develop the necessary termination voltages is with a regulator specifically designed for this purpose. Because SSTL and HSTL logic is commonly used for high-performance memory busses, a suitable termination voltage supply is often already available in the system.

Figure 16. SSTL2, SSTL3, eHSTL, HSTL Receiver Configuration

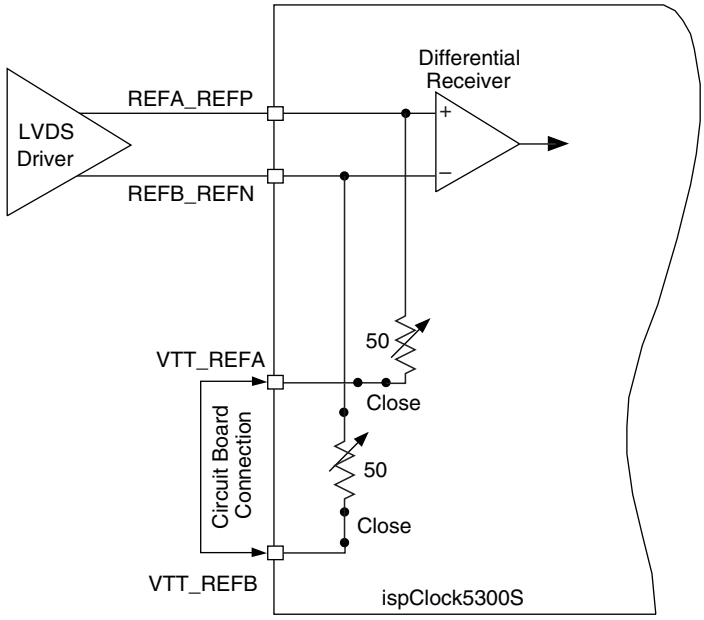


Differential LVPECL/LVDS

The receiver should be set to LVDS or LVPECL mode as required and both termination resistors should be engaged and set to 50Ω. The VTT_REFA and VTT_REFB pins, however, should be connected. This creates a floating 100Ω differential termination resistance across the input terminals. The LVDS termination configuration is shown in Figure 17.

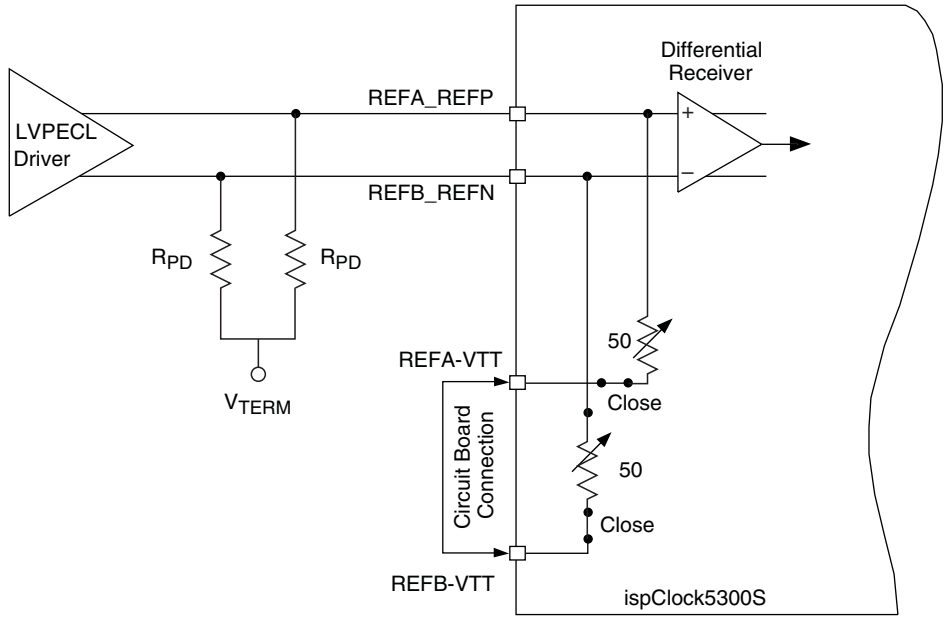
Note: the REFSEL pin should be grounded when the input receiver is configured as differential.

Figure 17. LVDS Input Receiver Configuration



Note that while a floating 100Ω resistor forms a complete termination for an LVDS signal line, additional circuitry may be required to satisfactorily terminate a differential LVPECL signal. This is because a true bipolar LVPECL output driver typically requires an external DC 'pull-down' path to a V_{TERM} termination voltage (typically VCC-2V) to properly bias its open emitter output stage. When interfacing to an LVPECL input signal, the ispClock5300S internal termination resistors should not be used for this pull-down function, as they may be damaged from excessive current. The pull-down should be implemented with external resistors placed close to the LVPECL driver (Figure 18)

Figure 18. LVPECL Input Receiver Configuration



Please note that while the above discussions specify using 50Ω termination impedances, the actual impedance required to properly terminate the transmission line and maintain good signal integrity may vary from this ideal. The

actual impedance required will be a function of the driver used to generate the signal and the transmission medium used (PCB traces, connectors and cabling). The ispClock5300S's ability to adjust input impedance over a range of 40Ω to 70Ω allows the user to adapt his circuit to non-ideal behaviors from the rest of the system without having to swap out components.

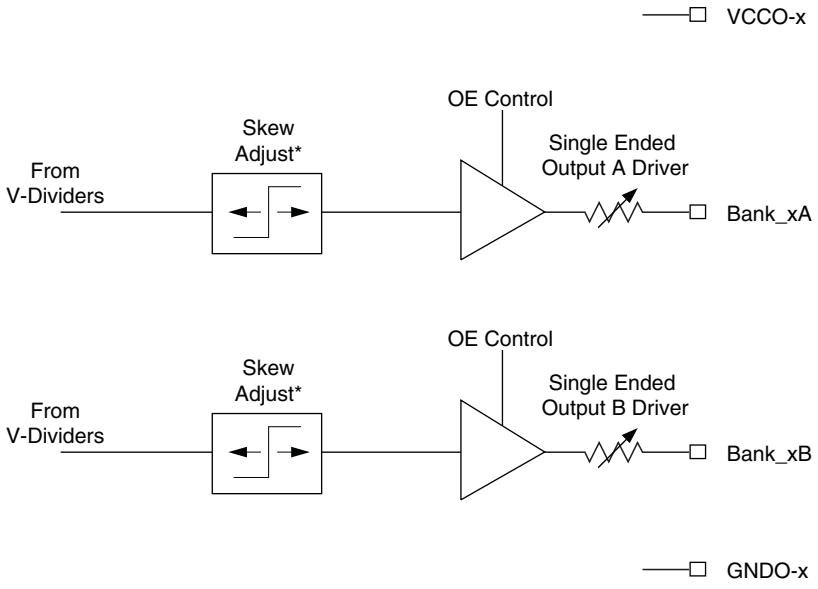
Output Drivers

The ispClock5300S provides multiple banks, with each bank supporting two high-speed clock outputs which are configurable and internally terminated. There are ten banks in the ispClock5320S, eight banks in the ispClock5316S, six banks in the ispClock5312S, four banks in the ispClock5308S and two banks in the ispClock5304S. Programmable internal source-series termination allows the ispClock5300S to be matched to transmission lines with impedances ranging from 40 to 70Ω. The outputs may be independently enabled or disabled, either from E^2CMOS configuration or by external control lines. Additionally, each can be independently programmed to provide a fixed amount of signal delay or skew, allowing the user to compensate for the effects of unequal PCB trace lengths or loading effects. Figure 19 shows a block diagram of a typical ispClock5300S output driver bank and associated skew control.

Because of the high edge rates which can be generated by the ispClock5300S clock output drivers, the VCCO power supply pin for each output bank should be individually bypassed. Low ESR capacitors with values ranging from 0.01 to 0.1 µF may be used for this purpose. Each bypass capacitor should be placed as close to its respective output bank power pins (VCCO and GNDO) pins as is possible to minimize interconnect length and associated parasitic inductances.

In the case where an output bank is unused, the associated VCCO pin may be either left floating or tied to ground to reduce quiescent power consumption. We recommend, however, that all unused VCCO pins be tied to ground where possible. All GNDO pins must be tied to ground, regardless of whether or not the associated bank is used.

Figure 19. ispClock5300S Output Driver and Skew Control



*Skew Adjust Mechanism is applicable only to outputs connected to one of the three V-Dividers and when PLL is active (PLL-Bypass pin = 0). For all other conditions, Skew Adjust Mechanism is bypassed.

Each of the ispClock5300S's output driver banks can be configured to support the following logic outputs:

- LVTTL
- LVCMOS (1.8V, 2.5V, 3.3V)
- SSTL2
- SSTL3
- HSTL
- eHSTL

To provide LVTTL, LVCMOS, SSTL2, SSTL3, HSTL and eHSTL outputs, the CMOS output drivers in each bank are enabled. These circuits provide logic outputs which swing from ground to the VCCO supply rail. The choice of VCCO to be supplied to a given bank is determined by the logic standard to which that bank is configured. Because each pair of outputs has its own VCCO supply pin, each bank can be independently configured to support a different logic standard. Note that the two outputs associated with a bank must necessarily be configured to the same logic standard. The source impedance of each of the two outputs in each bank may be independently set over a range of 40Ω to 70Ω in 5Ω steps. A low impedance option (≈20Ω) is also provided for cases where low source termination is desired on a given output.

Control of output slew rate is also provided in LVTTL, LVCMOS, SSTL2, SSTL3, HSTL and eHSTL output modes. Four output slew-rate settings are provided, as specified in the "Output Rise Times" and "Output Fall Times" tables in this data sheet.

Polarity control (true/inverted) is available for all output drivers. In the case of single-ended output standards, the polarity of each of the two output signals from each bank may be controlled independently.

Suggested Usage

Figure 20 shows a typical configuration for the ispClock5300S output driver when configured to drive an LVTTL or LVCMOS load. The ispClock5300S output impedance should be set to match the characteristic impedance of the transmission line being driven. The far end of the transmission line should be left open, with no termination resistors.

Figure 20. Configuration for LVTTL/LVCMOS Output Modes

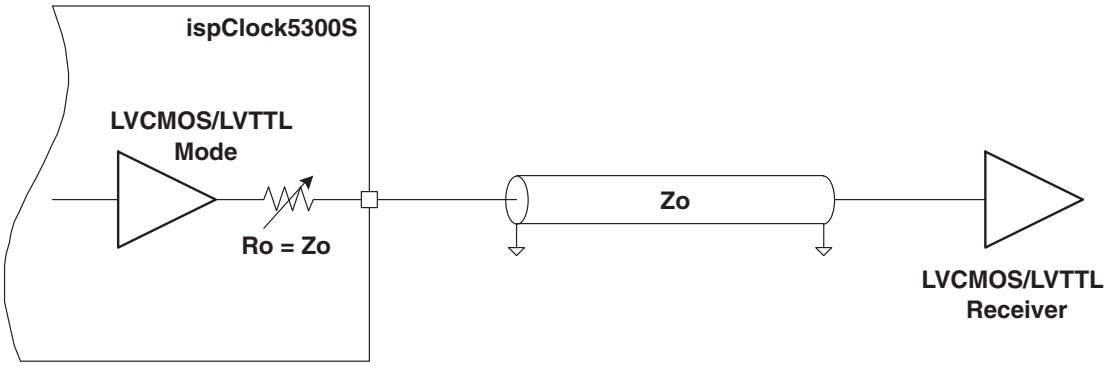
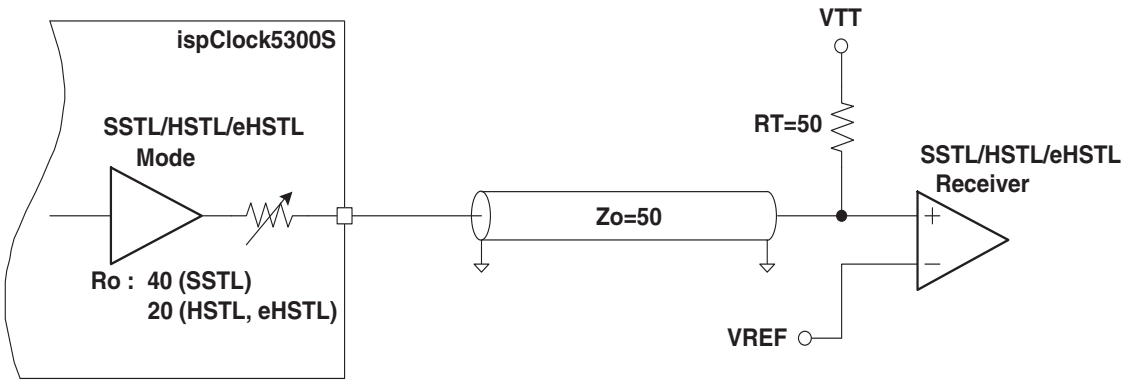


Figure 21 shows a typical configuration for the ispClock5300S output driver when configured to drive SSTL2, SSTL3, HSTL or eHSTL loads. The ispClock5300S output impedance should be set to 40Ω for driving SSTL2 or SSTL3 loads and to the ≈20Ω setting for driving HSTL and eHSTL. The far end of the transmission line must be terminated to an appropriate VTT voltage through a 50Ω resistor.

Figure 21. Configuration for SSTL2, SSTL3, and HSTL Output Modes



ispClock5300S Configurations

The ispClock5300S device can be configured to operate in four modes. They are:

- Zero Delay Buffer Mode
- Mixed Zero Delay and Non-Zero Delay Buffer Mode
- Non-Zero Delay Buffer mode 1
- Non-Zero Delay Buffer Mode 2

The output routing matrix of the ispClock5300S provides up to three independent any-to-any paths from inputs to outputs:

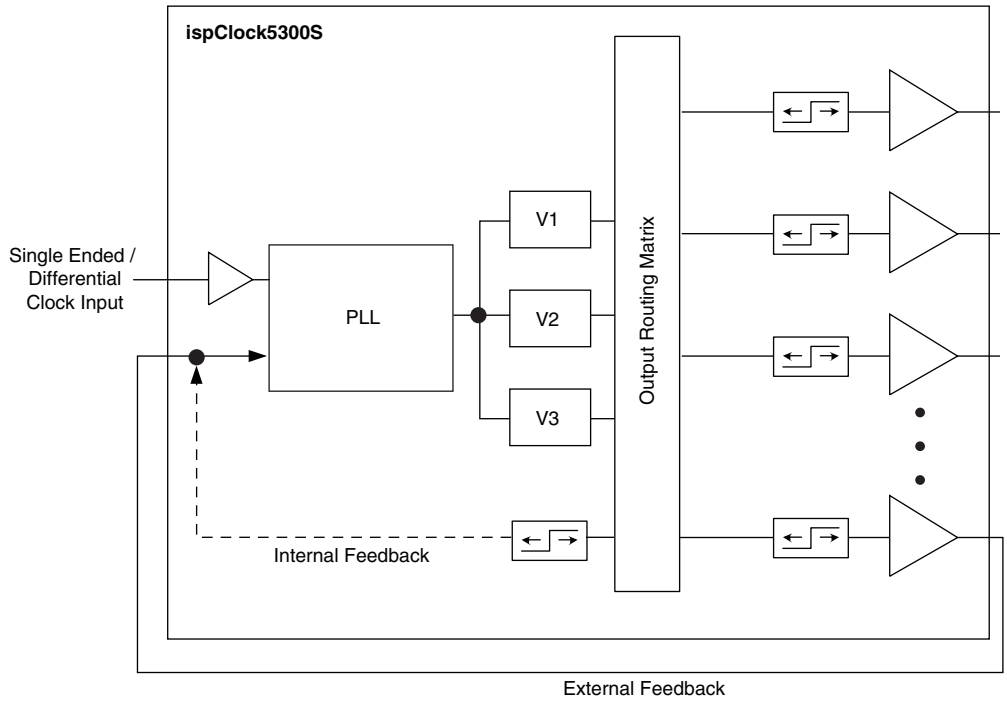
- From any V-Dividers to any output in ZDB mode or PLL Bypass modes
- From selected clock via REFSEL pin to any output (note single ended reference clock)
- From the other clock not selected by REFSEL pin to any output

Zero Delay Buffer Mode

Figure 22 shows the ispClock5300S device configured to operate in the Zero Delay Buffer mode. The Clock input can be single ended or differential. Two single ended clocks can be selected by the use of REFSEL pin and if the input is configured as a differential the REFSEL pin should be connected to GNDD. The input clock then drives the Phase frequency detector of the PLL. Up to 3 output clock frequencies can be generated from the input reference clock by the use of V-dividers at the output of PLL. Any V-divider output can be connected to any of the output pins. However, one of the V-dividers should be used in the feedback path to set the PLL operating frequency. The PLL can operate with internal or external feedback path.

In this mode, the skew control mechanism is active for all outputs.

Figure 22. ispClock5300S configured as Zero Delay Buffer Mode

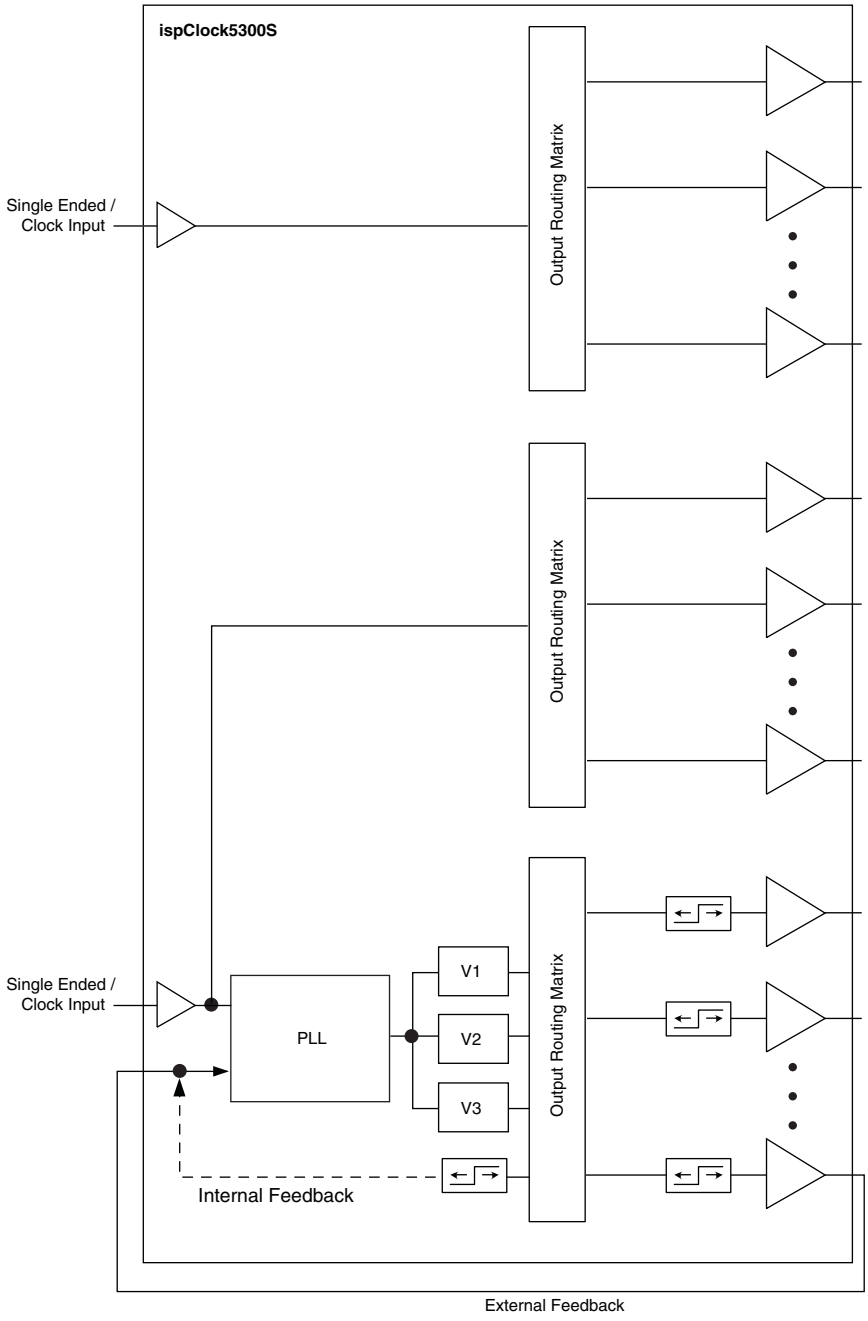


Mixed Zero Delay and Non-Zero Delay Buffer Mode

Figure 23 shows the operation of the ispClock5300S in Mixed Zero Delay and Non Zero Delay modes. In this mode the output switch matrix is configured to route non selected reference clock, selected reference clock, and the zero delay clock through the PLL.

The skew control mechanism is available only to clocks sourced from the PLL.

Figure 23. Mixed Zero Delay and Non Zero Delay Buffer Mode

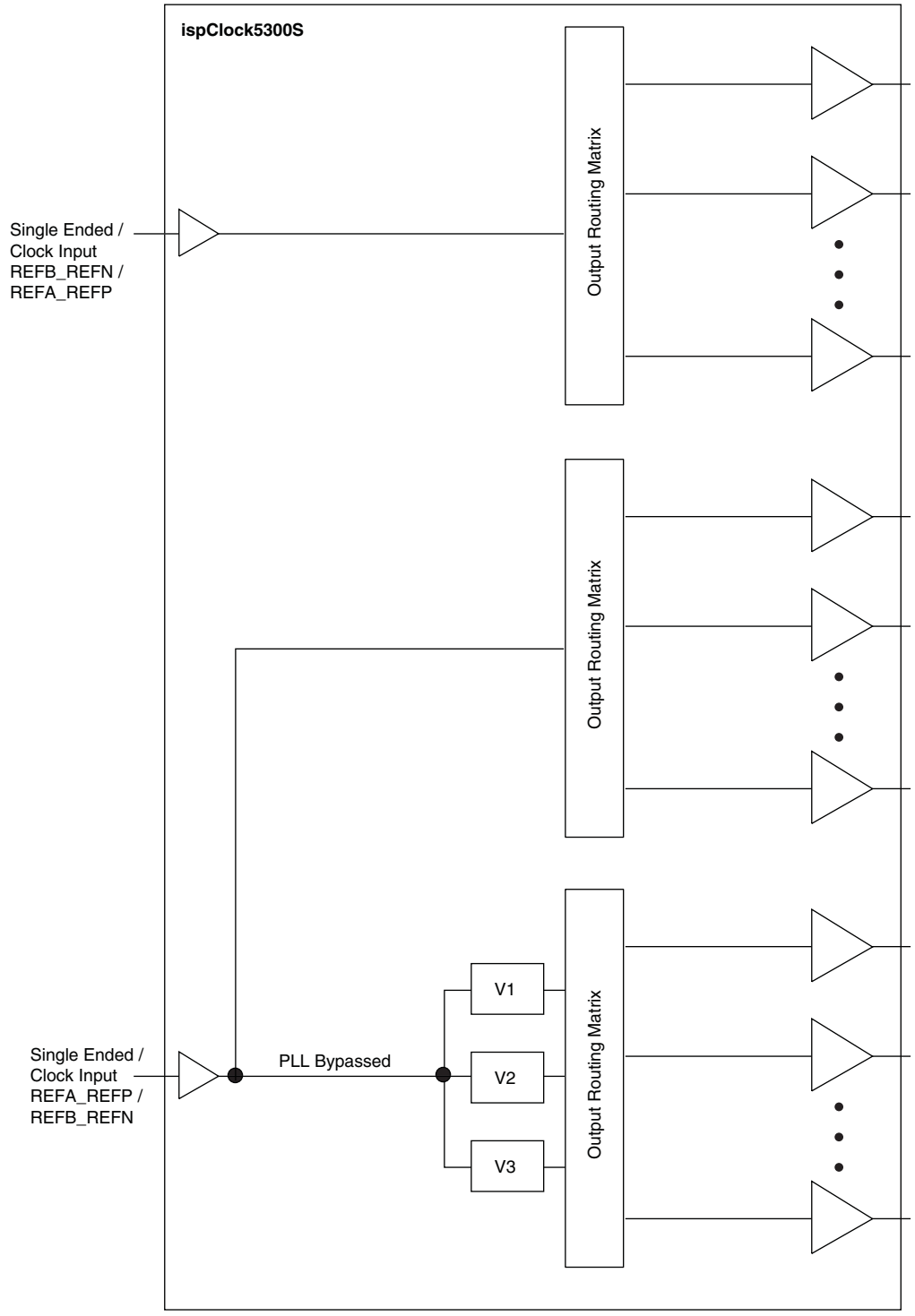


Non Zero Delay Buffer Mode 1

In the non zero delay buffer mode as shown in Figure 24 the output routing matrix completely bypasses the PLL. Each of the single ended input reference clocks can be routed to any number of available output clocks.

In this mode of operation there is no skew control.

Figure 24. Non Zero Delay Fan Out Buffer Mode 1



ispClock5300 Operating Configuration Summary

The following table summarizes the operating modes of the ispClock5300S.

Note:

- Whenever the input buffer is configured as differential input, the fan-out buffer paths become unavailable.
- Non-zero delay buffer for differential clock input is realized by using the PLL_BYPASS signal set to logical '1'.
- Output Skew control mechanism is available only to clock outputs sourced from PLL VCO.

Table 3. ispClock5300S Operating Modes

ispClock5300S Operating Mode	Reference Input Clocks	Skew Control	Output Clock Frequency Divider
Zero Delay Buffer Mode	Single Ended / Differential	Yes	Yes
Mixed Zero-Delay & Non-Zero Delay Buffer Mode	Single Ended Only	Only to Zero Delay Output Clocks	Only to Zero Delay Output Clocks
Non-Zero Delay Fan-out Buffer Mode 1	Single Ended Only	No	No
Non-Zero Delay Fan-out Buffer Mode 2	Single Ended / Differential	No	Only to Clocks Sourced From Bypassed PLL

Thermal Management

In applications where a majority of the ispClock5300S's outputs are active and operating at or near maximum output frequency, package thermal limitations may need to be considered to ensure a successful design. Thermal characteristics of the packages employed by Lattice Semiconductor may be found in the document *Thermal Management* which may be obtained at www.latticesemi.com.

The maximum current consumption of the digital and analog core circuitry for ispClock5312S is 150mA worst case (I_{CCD} + I_{CCA}), and each of the output banks may draw up to 16mA worst case (LVCMOS 3.60V, CL=5pF, f_{OUT}=100 MHz, both outputs in each bank enabled). This results in a total device dissipation:

$$P_{DMAX} = 3.60V \times (6 \times 16mA + 150mA) = 0.88W \quad (3)$$

With a maximum recommended operating junction temperature (T_{JOP}) of 130°C for an industrial grade device, the maximum allowable ambient temperature (T_{AMAX}) can be estimated as

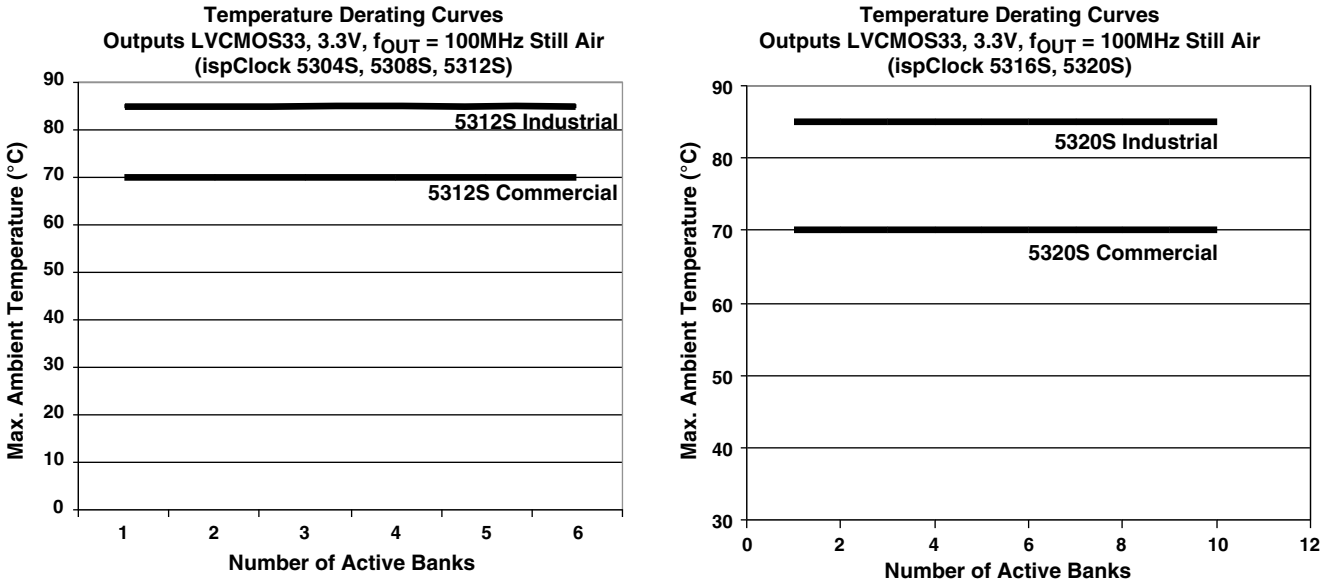
$$T_{AMAX} = T_{JOP} - PD_{MAX} \times \Theta_{JA} = 130°C - 0.88W \times 48°C/W = 85°C \quad (4)$$

where Θ_{JA} = 48°C/W for the 48 TQFP package in still air and Θ_{JA} = 42°C/W for the 64 TQFP package in still air.

The above analysis represents the worst-case scenario. Significant improvement in maximum ambient operating temperature can be realized with additional cooling. Providing a 200 LFM (Linear Feet per Minute) airflow reduces Θ_{JA} to 44°C/W for the 48 TQFP package.

While it is possible to perform detailed calculations to estimate the maximum ambient operating temperature from operating conditions, some simpler rule-of-thumb guidance can also be obtained through the derating curves shown in Figure 25 which shows the maximum ambient operating temperature permitted when operating a given number of output banks at the maximum output frequency.

Figure 25. Maximum Ambient Temperature vs. Number of Active Output Banks



Note that because of variations in circuit board mounting, construction, and layout, as well as convective and forced airflow present in a given design, actual die operating temperature is subject to considerable variation from that which may be theoretically predicted from package characteristics and device power dissipation.

Output Enable Controls ($\overline{OEX}$, $\overline{OEY}$)

The ispClock5300S family provides two output control pins for enabling and disabling clock outputs. In addition, the outputs can also be configured to be permanently enabled or permanently disabled.

Skew Control Units

Each of the ispClock5300S's clock outputs is supported by a skew control unit which allows the user to insert an individually programmable delay into each output signal. This feature is useful when it is necessary to de-skew clock signals to compensate for physical length variations among different PCB clock paths.

The ispClock5300S's skew adjustment feature provides exact and repeatable delays which exhibit extremely low channel-to-channel and device-to-device variation. This is achieved by deriving all skew timing from the VCO, which results in the skew increment being a linear function of the VCO period. For this reason, skews are defined in terms of 'unit delays', which may be programmed by the user over a range of 0 to 7. The ispClock5300S family also supports both 'fine' and 'coarse' skew modes. In fine skew mode, the unit skew ranges from 156ps to 390 ps, while in the coarse skew mode unit skew varies from 312ps to 780ps. The exact unit skew (TU) may be calculated from the VCO frequency (f_{vco}) by using the following expressions:

For fine skew mode, For coarse skew mode,

$$TU = \frac{1}{16f_{vco}} \qquad TU = \frac{1}{8f_{vco}} \tag{5}$$

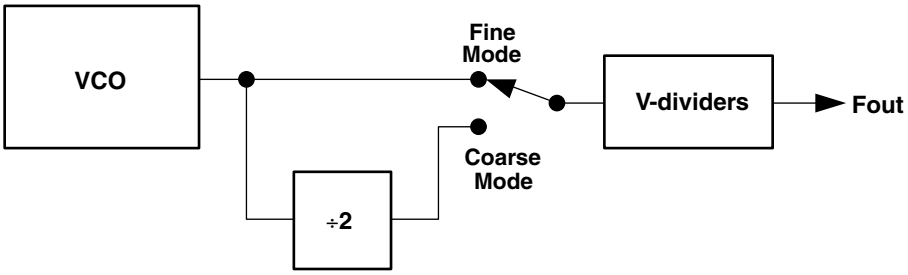
Please note that the skew control units are only usable when the PLL is selected. In PLL bypass mode (PLL_BYPASS=1), output skew settings will be ineffective and all outputs will exhibit skew consistent with the device's propagation delay and the individual delays inherent in the output drivers consistent with the logic standard selected.

Coarse Skew Mode

The ispClock5300S family provides the user with the option of obtaining longer skew delays at the cost of reduced time resolution through the use of coarse skew mode. Coarse skew mode provides unit delays ranging from 312ps

(f_{VCO} = 400MHz) to 780ps (f_{VCO} = 160MHz), which is twice as long as those provided in fine skew mode. When coarse skew mode is selected, an additional divide-by-2 stage is effectively inserted between the VCO and the V-divider bank, as shown in Figure 26. When assigning divider settings in coarse skew mode, one must account for this additional divide-by-two so that the VCO still operates within its specified range (160-400MHz).

Figure 26. Additional Factor-of-2 Division in Coarse Mode



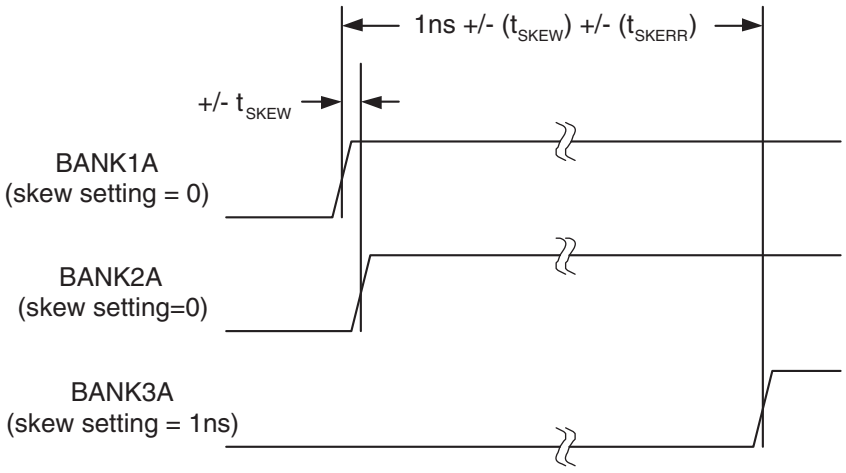
When one moves from fine skew mode to coarse skew mode with a given divider configuration, the VCO frequency will attempt to double to compensate for the additional divide-by-2 stage. Because the f_{VCO} range is not increased, however, one must modify the feedback path V-divider settings to bring f_{VCO} back into its specified operating range (160MHz to 400MHz). This can be accomplished by dividing all V-divider settings by two. All output frequencies will remain unchanged from what they were in fine mode.

Output Skew Matching and Accuracy

Understanding the various factors which relate to output skew is essential for realizing optimal skew performance in the ispClock5300S family of devices.

In the case where two outputs are identically configured, and driving identical loads, the maximum skew is defined by $t_{SKEW,}$ which is specified as a maximum of 100ps. In Figure 27 the Bank1A and BANK2A outputs show the skew error between two matched outputs.

Figure 27. Skew Matching Error Sources

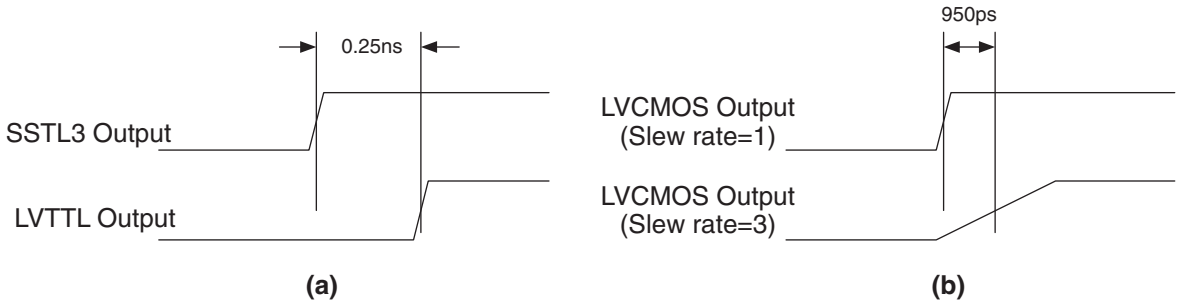


One can also program a user-defined skew between two outputs using the skew control units. Because the programmable skew is derived from the VCO frequency, as described in the previous section, the absolute skew is very accurate. The typical error for any non-zero skew setting is given by the t_{SKERR} specification. For example, if one is in fine skew mode with a VCO frequency of 250MHz, and selects a skew of 4TU, the realized skew will be 1ns, which will typically be accurate to within +/-30 ps. An example of error vs. skew setting can be found in the chart 'Typical Skew Error vs. Setting' in the typical performance characteristics section. Note that this parameter adds to output-to-output skew error only if the two outputs have *different* skew settings. The Bank1A and Bank3A

outputs in Figure 27 show how the various sources of skew error stack up in this case. Note that if two or more outputs are programmed to the same skew setting, then the contribution of the t_{SKERR} skew error term does not apply.

When outputs are configured or loaded differently, this also has an effect on skew matching. If an output is set to support a different logic type, this can be accounted for by using the t(ioo) output adders specified in the table 'Switching Characteristics'. That table specifies the additional skew added to an output using SSTL, HSTL, EHSTL as a base-line. For instance, if one output is specified as LVTTL, it has a delay adder relative to SSTL of 0.25ns. If another output is specified as SSTL3, then one would expect 0.25ns of additional skew between the two outputs due to this adder. This timing relationship is shown in Figure 28a.

Figure 28. Output Timing Adders for Logic Type (a) and Output Slew Rate (b)



By selecting the same feedback logic type and clock output, the output delay adders for the clock output are automatically compensated for. Similarly, a reference clock delay adder can be compensated for by selecting the same feedback input logic type and reference clock.

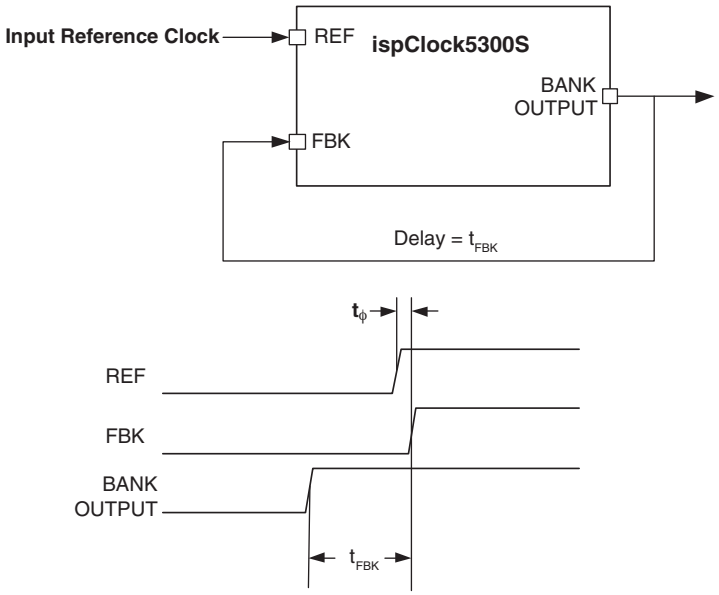
When the internal feedback mode is selected, however, one should add both input and output delay adders to t_{DELAY} specified in the Performance Characteristics PLL table to calculate the input-to-output delay.

Similarly, when one changes the slew rate of an output, the output slew rate adders (t_{IOS}) can be used to predict the resulting skew. In this case, the fastest slew setting (1) is used as the baseline against which other slews are measured. For example, in the case of outputs configured to the same logic type (e.g. LVCMOS 1.8V), if one output is set to the fastest slew rate (1, t_{IOS} = 0ps), and another set to slew rate 3 (t_{IOS} = 950ps), then one could expect 950ps of skew between the two outputs, as shown in Figure 28b.

Static Phase Offset and Input-Output Skew

The ispClock5300S's external feedback inputs can be used to obtain near-zero effective delays from the clock reference input pins to a designated output pin. Using external feedback (Figure 29), the PLL will attempt to force the output phase so that the rising edge phase ($t\phi$) at the feedback input matches the rising edge phase at the reference input. The residual error between the two is specified as the static phase error. Note that any propagation delay (t_{FBK}) in the external feedback path drives the phase of the output signal *backwards* in time as measured at the output. For this reason, if zero input-to-output delays are required, the length of the signal path between the output pin and the feedback pin should be minimized.

Figure 29. External Feedback Mode and Timing Relationships



Other Features

$\overline{\text{RESET}}$ and Power-up Functions

To ensure proper PLL startup and synchronization of outputs, the ispClock5300S provides both internally generated and user-controllable external reset signals. An internal reset is generated whenever the device is powered up. An external reset may be applied by asserting a logic LOW at the $\overline{\text{RESET}}$ pin. Asserting $\overline{\text{RESET}}$ resets all internal dividers, and will cause the PLL to lose lock. On losing lock, the VCO frequency will begin dropping. The length of time required to regain lock is related to the length of time for which $\overline{\text{RESET}}$ was asserted.

When the ispClock5300S begins operating from initial power-on, the VCO starts running at a very low frequency (<100 MHz) which gradually increases as it approaches a locked condition. To prevent invalid outputs from being applied to the rest of the system, assert $\overline{\text{OEX}}$ or $\overline{\text{OEY}}$ high. This will result in the BANK outputs being held in a high-impedance state until the $\overline{\text{OEX}}$ or $\overline{\text{OEY}}$ pin is pulled LOW.

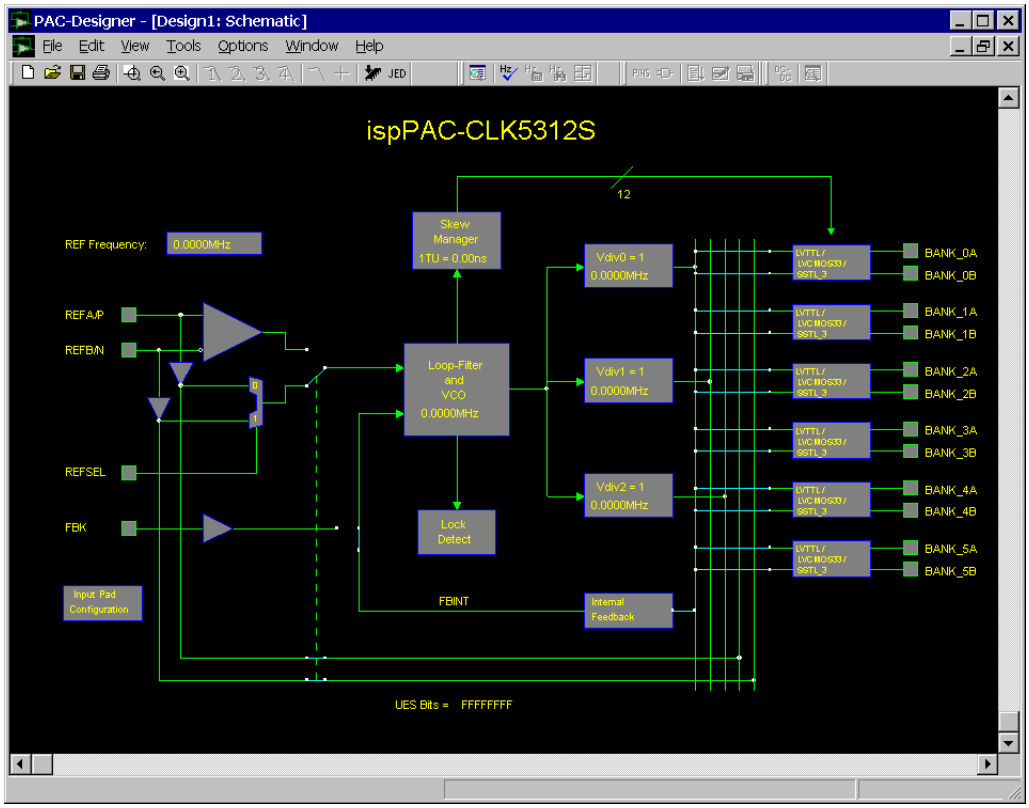
After in-system programming the device through the JTAG interface, the reset pin must be activated at least for a period of t_{PLL_RSTW} to reset the device.

If the $\overline{\text{RESET}}$ pin is not driven by an external logic it should be pulled up to V_{CCD} through a 10kΩ resistor.

Software-Based Design Environment

Designers can configure the ispClock5300S using Lattice's PAC-Designer software, an easy to use, Microsoft Windows compatible program. Circuit designs are entered graphically and then verified, all within the PAC-Designer environment. Full device programming is supported using PC parallel port I/O operations and a download cable connected to the serial programming interface pins of the ispClock5300S. A library of configurations is included with basic solutions and examples of advanced circuit techniques are available. In addition, comprehensive on-line and printed documentation is provided that covers all aspects of PAC-Designer operation. PAC-Designer is available for download from the Lattice web site at www.latticesemi.com. The PAC-Designer schematic window, shown in Figure 30 provides access to all configurable ispClock5300S elements via its graphical user interface. All analog input and output pins are represented. Static or non-configurable pins such as power, ground and the serial digital interface are omitted for clarity. Any element in the schematic window can be accessed via mouse operations as well as menu commands. When completed, configurations can be saved and downloaded to devices.

Figure 30. PAC-Designer Design Entry Screen



In-System Programming

The ispClock5300S is an In-System Programmable (ISP™) device. This is accomplished by integrating all E^{2}CMOS configuration control logic on-chip. Programming is performed through a 4-wire, IEEE 1149.1 compliant serial JTAG interface at normal logic levels. Once a device is programmed, all configuration information is stored on-chip, in non-volatile E^{2}CMOS memory cells. The specifics of the IEEE 1149.1 serial interface and all ispClock5300S instructions are described in the JTAG interface section of this data sheet.

User Electronic Signature

A user electronic signature (UES) feature is included in the E^{2}CMOS memory of the ispClock5300S. This consists of 32 bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control data. The specifics this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

Electronic Security

An electronic security “fuse” (ESF) bit is provided in every ispClock5300S device to prevent unauthorized readout of the E^{2}CMOS configuration bit patterns. Once programmed, this cell prevents further access to the functional user bits in the device. This cell can only be erased by reprogramming the device, so the original configuration can not be examined once programmed. Usage of this feature is optional. The specifics of this feature are discussed in the IEEE 1149.1 serial interface section of this data sheet.

Production Programming Support

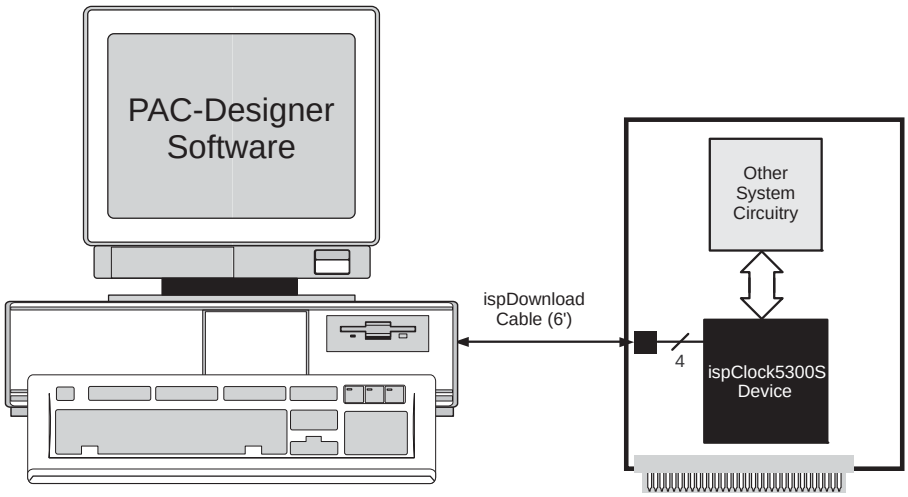
Once a final configuration is determined, an ASCII format JEDEC file can be created using the PAC-Designer software. Devices can then be ordered through the usual supply channels with the user’s specific configuration already preloaded into the devices. By virtue of its standard interface, compatibility is maintained with existing production programming equipment, giving customers a wide degree of freedom and flexibility in production planning.

Evaluation Fixture

Included in the basic ispClock5300S Design Kit is an engineering prototype board that can be connected to the parallel port of a PC using a Lattice ispDOWNLOAD® cable. It demonstrates proper layout techniques for the ispClock5300S and can be used in real time to check circuit operation as part of the design process. Input and output connections (SMA connectors for all RF signals) are provided to aid in the evaluation of the ispClock5300S for a given application. (Figure 31).

Part Number	Description
PAC-SYSTEMCLK5312S	Complete system kit, evaluation board, ispDOWNLOAD cable and software.

Figure 31. Download from a PC



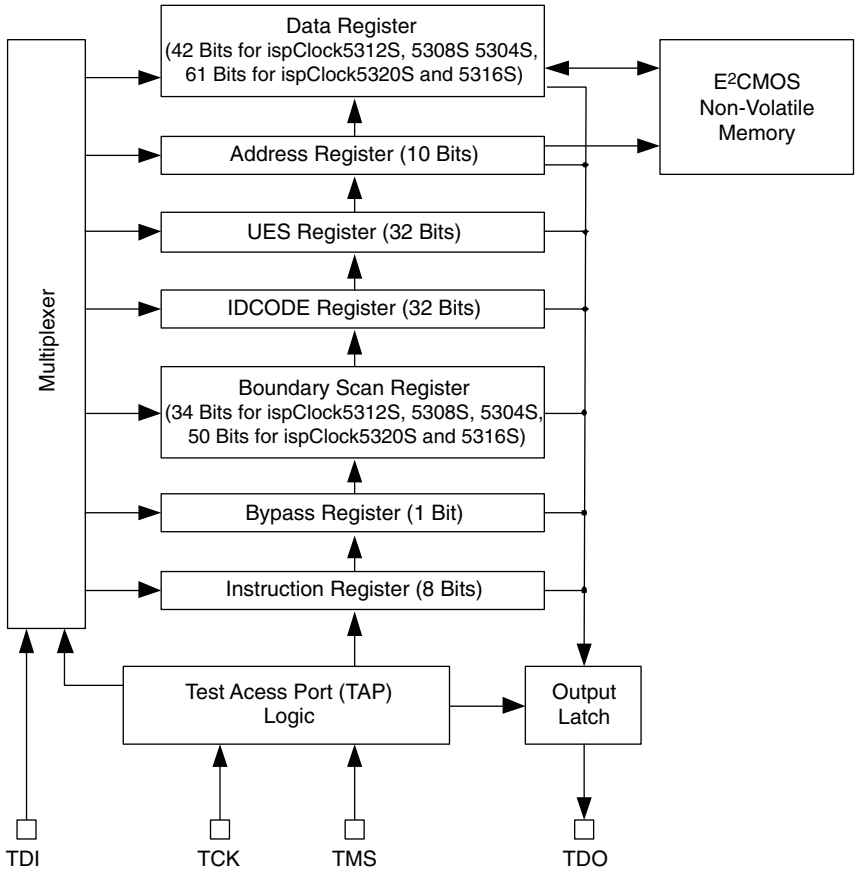
IEEE Standard 1149.1 Interface (JTAG)

Serial Port Programming Interface Communication with the ispClock5300S is facilitated via an IEEE 1149.1 test access port (TAP). It is used by the ispClock5300S both as a serial programming interface, and for boundary scan test purposes. A brief description of the ispClock5300S JTAG interface follows. For complete details of the reference specification, refer to the publication, Standard Test Access Port and Boundary-Scan Architecture, IEEE Std. 1149.1-1990 (which now includes IEEE Std. 1149.1a-1993).

Overview

An IEEE 1149.1 test access port (TAP) provides the control interface for serially accessing the digital I/O of the ispClock5300S. The TAP controller is a state machine driven with mode and clock inputs. Given in the correct sequence, instructions are shifted into an instruction register which then determines subsequent data input, data output, and related operations. Device programming is performed by addressing the configuration register, shifting data in, and then executing a program configuration instruction, after which the data is transferred to internal E^2CMOS cells. It is these non-volatile cells that store the configuration of the ispClock5300S. A set of instructions are defined that access all data registers and perform other internal control operations. For compatibility between compliant devices, two data registers are mandated by the IEEE 1149.1 specification. Others are functionally specified, but inclusion is strictly optional. Finally, there are provisions for optional data registers defined by the manufacturer. The two required registers are the bypass and boundary-scan registers. Figure 32 shows how the instruction and various data registers are organized in an ispClock5300S.

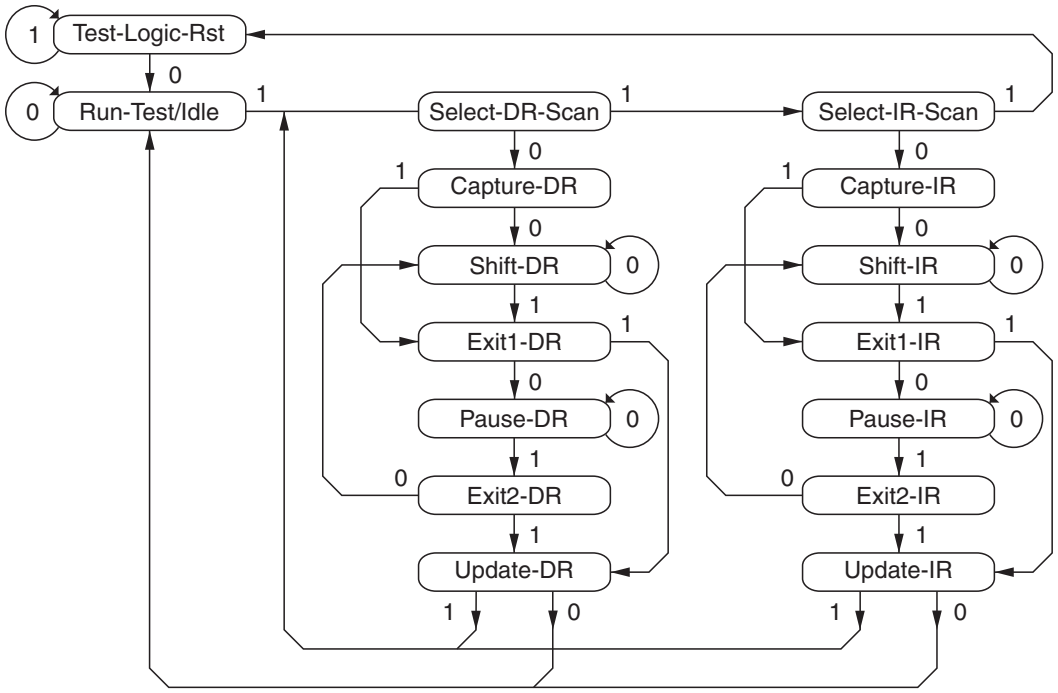
Figure 32. ispClock5300S TAP Registers



TAP Controller Specifics

The TAP is controlled by the Test Clock (TCK) and Test Mode Select (TMS) inputs. These inputs determine whether an Instruction Register or Data Register operation is performed. Driven by the TCK input, the TAP consists of a small 16-state controller design. In a given state, the controller responds according to the level on the TMS input as shown in Figure 33. Test Data In (TDI) and TMS are latched on the rising edge of TCK, with Test Data Out (TDO) becoming valid on the falling edge of TCK. There are six steady states within the controller: Test-Logic-Reset, Run-Test/Idle, Shift-Data-Register, Pause-Data-Register, Shift-Instruction-Register and Pause-Instruction-Register. But there is only one steady state for the condition when TMS is set high: the Test-Logic-Reset state. This allows a reset of the test logic within five TCKs or less by keeping the TMS input high. Test-Logic-Reset is the power-on default state.

Figure 33. TAP States



Note: The value shown adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

When the correct logic sequence is applied to the TMS and TCK inputs, the TAP will exit the Test-Logic-Reset state and move to the desired state. The next state after Test-Logic-Reset is Run-Test/Idle. Until a data or instruction shift is performed, no action will occur in Run-Test/Idle (steady state = idle). After Run-Test/Idle, either a data or instruction shift is performed. The states of the Data and Instruction Register blocks are identical to each other differing only in their entry points. When either block is entered, the first action is a capture operation. For the Data Registers, the Capture-DR state is very simple: it captures (parallel loads) data onto the selected serial data path (previously chosen with the appropriate instruction). For the Instruction Register, the Capture-IR state will always load the IDCODE instruction. It will always enable the ID Register for readout if no other instruction is loaded prior to a Shift-DR operation. This, in conjunction with mandated bit codes, allows a “blind” interrogation of any device in a compliant IEEE 1149.1 serial chain. From the Capture state, the TAP transitions to either the Shift or Exit1 state. Normally the Shift state follows the Capture state so that test data or status information can be shifted out or new data shifted in. Following the Shift state, the TAP either returns to the Run-Test/Idle state via the Exit1 and Update states or enters the Pause state via Exit1. The Pause state is used to temporarily suspend the shifting of data through either the Data or Instruction Register while an external operation is performed. From the Pause state, shifting can resume by reentering the Shift state via the Exit2 state or be terminated by entering the Run-Test/Idle state via the Exit2 and Update states. If the proper instruction is shifted in during a Shift-IR operation, the next entry into Run-Test/Idle initiates the test mode (steady state = test). This is when the device is actually programmed, erased or verified. All other instructions are executed in the Update state.

Test Instructions

Like data registers, the IEEE 1149.1 standard also mandates the inclusion of certain instructions. It outlines the function of three required and six optional instructions. Any additional instructions are left exclusively for the manufacturer to determine. The instruction word length is not mandated other than to be a minimum of two bits, with only the BYPASS and EXTEST instruction code patterns being specifically called out (all ones and all zeroes respectively). The ispClock5300S contains the required minimum instruction set as well as one from the optional instruction set. In addition, there are several proprietary instructions that allow the device to be configured and verified.

For ispClock5300S, the instruction word length is eight bits. All ispClock5300S instructions available to users are shown in Table 4.

The following table lists the instructions supported by the ispClock5300S JTAG Test Access Port (TAP) controller:

Table 4. ispClock5300S TAP Instruction Table

Instruction	Code	Description
EXTEST	0000 0000	External Test.
ADDRESS_SHIFT	0000 0001	Address register (10 bits)
DATA_SHIFT	0000 0010	Address column data register (42 bits for ispClock5312S, 5308S and 5304S; 61 bits for ispClock5320S and 5316S)
BULK_ERASE	0000 0011	Bulk Erase
PROGRAM	0000 0111	Program column data register to E^2
PROGRAM_SECURITY	0000 1001	Program Electronic Security Fuse
VERIFY	0000 1010	Verify column
DISCHARGE	0001 0100	Fast VPP Discharge
PROGRAM_ENABLE	0001 0101	Enable Program Mode
IDCODE	0001 0110	Address Manufacturer ID code register (32 bits)
USERCODE	0001 0111	Read UES data from E^2 and addresses UES register (32 bits)
PROGRAM_USERCODE	0001 1010	Program UES register into E^2
PROGRAM_DISABLE	0001 1110	Disable Program Mode
HIGHZ	0001 1000	Force all outputs to High-Z state
SAMPLE/PRELOAD	0001 1100	Capture current state of pins to boundary scan register
CLAMP	0010 0000	Drive I/Os with boundary scan register
INTEST	0010 1100	Performs in-circuit functional testing of device.
ERASE DONE	0010 0100	Erases the ‘Done’ bit only
PROG_INCR	0010 0111	Program column data register to E^2 and auto-increment address register
VERIFY_INCR	0010 1010	Load column data register from E^2 and auto-increment address register
PROGRAM_DONE	0010 1111	Programs the ‘Done’ Bit
NOOP	0011 0000	Functions Similarly to CLAMP instruction
BYPASS	1xxx xxxx	Bypass - Connect TDO to TDI

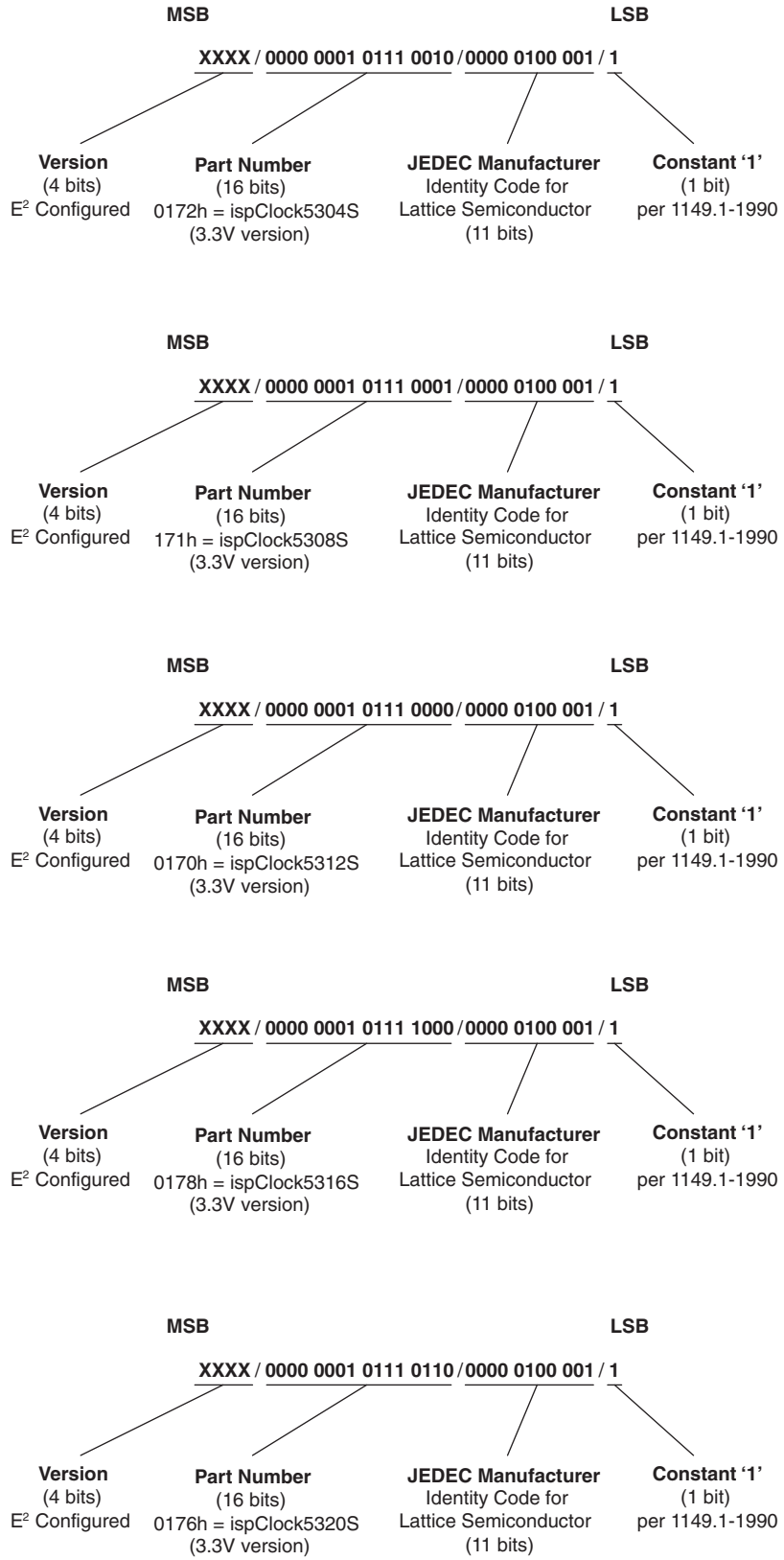
BYPASS is one of the three required instructions. It selects the Bypass Register to be connected between TDI and TDO and allows serial data to be transferred through the device without affecting the operation of the ispClock5300S. The IEEE 1149.1 standard defines the bit code of this instruction to be all ones (111111).

The required **SAMPLE/PRELOAD** instruction dictates the Boundary-Scan Register be connected between TDI and TDO. The bit code for this instruction is defined by Lattice as shown in Table 4.

The **EXTEST** (external test) instruction is required and will place the device into an external boundary test mode while also enabling the boundary scan register to be connected between TDI and TDO. The bit code of this instruction is defined by the 1149.1 standard to be all zeros (000000).

The optional **IDCODE** (identification code) instruction is incorporated in the ispClock5300S and leaves it in its functional mode when executed. It selects the Device Identification Register to be connected between TDI and TDO. The Identification Register is a 32-bit shift register containing information regarding the IC manufacturer, device type and version code (Figure 34). Access to the Identification Register is immediately available, via a TAP data scan operation, after power-up of the device, or by issuing a Test-Logic-Reset instruction. The bit code for this instruction is defined by Lattice as shown in Table 4.

Figure 34. ispClock5300S Family ID Codes



In addition to the four instructions described above, there are 20 unique instructions specified by Lattice for the ispClock5300S. These instructions are primarily used to interface to the various user registers and the E^2CMOS non-volatile memory. Additional instructions are used to control or monitor other features of the device, including boundary scan operations. A brief description of each unique instruction is provided in detail below, and the bit codes are found in Table 4.

PROGRAM_ENABLE – This instruction enables the ispClock5300S programming mode.

PROGRAM_DISABLE – This instruction disables the ispClock5300S programming mode.

BULK_ERASE – This instruction will erase all E^2CMOS bits in the device, including the UES data and electronic security fuse (ESF). A bulk erase instruction must be issued before reprogramming a device. The device must already be in programming mode for this instruction to execute.

ADDRESS_SHIFT – This instruction shifts address data into the address register (10 bits) in preparation for either a PROGRAM or VERIFY instruction.

DATA_SHIFT – This instruction shifts data into or out of the data register (43 bits for ispClock5312, 5308 and 5304; 61 bits for ispClock5320 and 5316), and is used with both the PROGRAM and VERIFY instructions.

PROGRAM – This instruction programs the contents of the data register to the E^2CMOS memory column pointed to by the address register. The device must already be in programming mode for this instruction to execute.

PROG_INCR – This instruction first programs the contents of the data register into E^2CMOS memory column pointed to by the address register and then auto-increments the value of the address register. The device must already be in programming mode for this instruction to execute.

PROGRAM_SECURITY – This instruction programs the electronic security fuse (ESF). This prevents data other than the ID code and UES strings from being read from the device. The electronic security fuse may only be reset by issuing a BULK_ERASE command. The device must already be in programming mode for this instruction to execute.

VERIFY – This instruction loads data from the E^2CMOS array into the column register. The data may then be shifted out. The device must already be in programming mode for this instruction to execute.

VERIFY_INCR – This instruction copies the E^2CMOS column pointed to by the address register into the data column register and then auto-increments the value of the address register. The device must already be in programming mode for this instruction to execute.

DISCHARGE – This instruction is used to discharge the internal programming supply voltage after an erase or programming cycle and prepares ispClock5300S for a read cycle.

PROGRAM_USERCODE – This instruction writes the contents of the UES register (32 bits) into E^2CMOS memory. The device must already be in programming mode for this instruction to execute.

USERCODE – This instruction both reads the UES string (32 bits) from E^2CMOS memory into the UES register and addresses the UES register so that this data may be shifted in and out.

HIGHZ – This instruction forces all outputs into a High-Z state.

CLAMP – This instruction drives I/O pins with the contents of the boundary scan register.

INTEST – This instruction performs in-circuit functional testing of the device.

ERASE_DONE – This instruction erases the ‘DONE’ bit only. This instruction is used to disable normal operation of the device while in programming mode until a valid configuration pattern has been programmed.

PROGRAM_DONE – This instruction programs the ‘DONE’ bit only. This instruction is used to enable normal device operation after programming is complete.

NOOP – This instruction behaves similarly to the CLAMP instruction.

Pin Descriptions – ispClock5304S, 5308S, 5312S

Pin Name	Description	Pin Type	Pin Number		
			ispClock5304S 48 TQFP	ispClock5308S 48 TQFP	ispClock5312S 48 TQFP
VCCO_0	Output Driver '0' VCC	Power	5	5	1
VCCO_1	Output Driver '1' VCC	Power	32	9	5
VCCO_2	Output Driver '2' VCC	Power	—	28	9
VCCO_3	Output Driver '3' VCC	Power	—	32	28
VCCO_4	Output Driver '4' VCC	Power	—	—	32
VCCO_5	Output Driver '5' VCC	Power	—	—	36
GNDO_0	Output Driver '0' Ground	GND	7	7	3
GNDO_1	Output Driver '1' Ground	GND	30	11	7
GNDO_2	Output Driver '2' Ground	GND	—	26	11
GNDO_3	Output Driver '3' Ground	GND	—	30	26
GNDO_4	Output Driver '4' Ground	GND	—	—	30
GNDO_5	Output Driver '5' Ground	GND	—	—	34
BANK_0A	Clock Output driver 0, 'A' output	Output	6	6	2
BANK_0B	Clock Output driver 0, 'B' output	Output	8	8	4
BANK_1A	Clock Output driver 1, 'A' output	Output	31	10	6
BANK_1B	Clock Output driver 1, 'B' output	Output	29	12	8
BANK_2A	Clock Output driver 2, 'A' output	Output	—	27	10
BANK_2B	Clock Output driver 2, 'B' output	Output	—	25	12
BANK_3A	Clock Output driver 3, 'A' output	Output	—	31	27
BANK_3B	Clock Output driver 3, 'B' output	Output	—	29	25
BANK_4A	Clock Output driver 4, 'A' output	Output	—	—	31
BANK_4B	Clock Output driver 4, 'B' output	Output	—	—	29
BANK_5A	Clock Output driver 5, 'A' output	Output	—	—	35
BANK_5B	Clock Output driver 5, 'B' output	Output	—	—	33
VCCA	Analog VCC for PLL circuitry	Power	46	46	46
GNDA	Analog Ground for PLL circuitry	GND	47	47	47
VCCD	Digital Core VCC	Power	21, 22	21, 22	21, 22
GNDD	Digital GND	GND	23, 24, 48	23, 24, 48	23, 24, 48
REFA_REFP	Clock Reference A/Positive Differential input[3]	Input	14	14	14
REFB_REFN	Clock Reference B/Negative Differential input[3]	Input	15	15	15
REFSEL	Clock Reference Select input (LVCMOS)	Input[1]	19	19	19
VTT_REFA	Termination voltage for reference input A	Power	13	13	13
FBK	Feedback Input[3]	Input	17	17	17
VTT_FBK	Termination voltage for feedback input	Power	18	18	18
VTT_REFB	Termination input for reference input B	Power	16	16	16
VCCJ	JTAG interface VCC	Power	41	41	41
TDO	JTAG TDO Output line	Output	37	37	37
TDI	JTAG TDI Input line	Input[2]	40	40	40
TCK	JTAG Clock Input	Input	39	39	39
TMS	JTAG Mode Select	Input[2]	38	38	38

Pin Descriptions – ispClock5304S, 5308S, 5312S (Continued)

Pin Name	Description	Pin Type	Pin Number		
			ispClock5304S 48 TQFP	ispClock5308S 48 TQFP	ispClock5312S 48 TQFP
LOCK	PLL Lock indicator, HIGH indicates PLL lock	Output	45	45	45
$\overline{OEX}$	Output Enable X	Input[1]	43	43	43
$\overline{OEY}$	Output Enable Y	Input[1]	42	42	42
PLL_BYPASS	PLL Bypass	Input[1]	44	44	44
$\overline{RESET}$	Reset PLL	Input[2]	20	20	20
NC	No internal connection	n/a	1, 2, 3, 4, 9, 10, 11, 12, 25, 26, 27, 28, 33, 34, 35, 36	1, 2, 3, 4, 33, 34, 35, 36	n/a

1. Internal pull-down resistor.
2. Internal pull-up resistor.
3. Must be connected to GNDD if this pin is not used.

Pin Descriptions – ispClock5316S, 5320S

Pin Name	Description	Pin Type	ispClock5316S 64 TQFP	ispClock5320S 64 TQFP
VCC_0	Output Driver '0' VCC	Power	63	63
VCC_1	Output Driver '1' VCC	Power	3	3
VCC_2	Output Driver '2' VCC	Power	7	7
VCC_3	Output Driver '3' VCC	Power	11	11
VCC_4	Output Driver '4' VCC	Power	38	17
VCC_5	Output Driver '5' VCC	Power	42	32
VCC_6	Output Driver '6' VCC	Power	46	38
VCC_7	Output Driver '7' VCC	Power	50	42
VCC_8	Output Driver '8' VCC	Power	—	46
VCC_9	Output Driver '9' VCC	Power	—	50
GND_0	Output Driver '0' GND	GND	64	64
GND_1	Output Driver '1' GND	GND	6	6
GND_2	Output Driver '2' GND	GND	10	10
GND_3	Output Driver '3' GND	GND	14	14
GND_4	Output Driver '4' GND	GND	35	18
GND_5	Output Driver '5' GND	GND	39	31
GND_6	Output Driver '6' GND	GND	43	35
GND_7	Output Driver '7' GND	GND	49	39
GND_8	Output Driver '8' GND	GND	—	43
GND_9	Output Driver '9' GND	GND	—	49
BANK_0A	Clock Output Driver 0, 'A' output	Output	1	1
BANK_0B	Clock Output Driver 0, 'B' output	Output	2	2
BANK_1A	Clock Output Driver 1, 'A' output	Output	4	4
BANK_1B	Clock Output Driver 1, 'B' output	Output	5	5
BANK_2A	Clock Output Driver 2, 'A' output	Output	8	8
BANK_2B	Clock Output Driver 2, 'B' output	Output	9	9
BANK_3A	Clock Output Driver 3, 'A' output	Output	12	12
BANK_3B	Clock Output Driver 3, 'B' output	Output	13	13
BANK_4A	Clock Output Driver 4, 'A' output	Output	37	15
BANK_4B	Clock Output Driver 4, 'B' output	Output	36	16
BANK_5A	Clock Output Driver 5, 'A' output	Output	41	34
BANK_5B	Clock Output Driver 5, 'B' output	Output	40	33
BANK_6A	Clock Output Driver 6, 'A' output	Output	45	37
BANK_6B	Clock Output Driver 6, 'B' output	Output	44	36
BANK_7A	Clock Output Driver 7, 'A' output	Output	48	41
BANK_7B	Clock Output Driver 7, 'B' output	Output	47	40
BANK_8A	Clock Output Driver 8, 'A' output	Output	—	45
BANK_8B	Clock Output Driver 8, 'B' output	Output	—	44
BANK_9A	Clock Output Driver 9, 'A' output	Output	—	48
BANK_9B	Clock Output Driver 9, 'B' output	Output	—	47
VCCA	Analog VCC for PLL Circuitry	Power	60	60
GNDA	Analog Ground for PLL circuitry	GND	61	61
VCCD	Digital Core VCC	Power	27, 28	27, 28

Pin Descriptions – ispClock5316S, 5320S (Continued)

Pin Name	Description	Pin Type	ispClock5316S 64 TQFP	ispClock5320S 64 TQFP
GNDD	Digital GND	GND	18, 29, 30, 31, 62	29, 30, 62
REFA_REFP	Clock Reference A/ Positive Differential Input[3]	Input	20	20
REFB_REFN	Clock Reference B/ Negative Differential Input[3]	Input	21	21
REFSEL	Clock Reference Select input (LVCMOS)	Input	25	25
VTT_REFA	Termination voltage for reference input A	Power	19	19
FBK	Feedback input[3]	Input	23	23
VTT_FBK	Termination voltage for feedback input	Power	24	24
VTT_REFB	Termination voltage for reference input B	Power	22	22
VCCJ	JTAG Interface VCC	Power	55	55
TDO	JTAG TDO output	Output	51	51
TDI	JTAG TDI input	Input[2]	54	54
TCK	JTAG Clock input	Input	53	53
TMS	JTAG Mode select	Input[2]	52	52
LOCK	PLL Lock indicator, HIGH indicates PLL Lock	Output	59	59
$\overline{OEX}$	Output enable X	Input[1]	57	57
$\overline{OEY}$	Output enable Y	Input[1]	56	56
PLL_BYPASS	PLL Bypass	Input[1]	58	58
$\overline{RESET}$	Reset PLL	Input[2]	26	26
NC	No internal connection	N/A	15, 16, 17, 32, 33, 34	—

1. Internal pull-down resistor.
2. Internal pull-up resistor.
3. Must be connected to GNDD if not used.

Detailed Pin Descriptions

VCCO_[0..9], GNDO_[0..9] – These pins provide power and ground for each of the output banks. In the case when an output bank is unused, its corresponding VCCO pin may be left unconnected or preferably should be tied to ground. ALL GNDO pins should be tied to ground regardless of whether the associated bank is used or not. When a bank is used, it should be individually bypassed with a capacitor in the range of 0.01 to 0.1µF as close to its VCCO and GNDO pins as is practical.

BANK_[0..9]A, BANK_[0..9]B – These pins provide clock output signals. The choice of output driver type (CMOS, SSTL, etc.) may be selected on a bank-by-bank basis. The output impedance and slew rate may be selected on an output-by-output basis.

VCCA, GNDA – These pins provide analog supply and ground for the ispClock5300S family's internal analog circuitry, and should be bypassed with a 0.1uF capacitor as close to the pins as is practical. To improve noise immunity, it is suggested that the supply to the VCCA pin be isolated from other circuitry with a ferrite bead.

VCCD, GNDD – These pins provide digital supply and ground for the ispClock5300S family's internal digital circuitry, and should be bypassed with a 0.1uF capacitor as close to the pins as is practical. To improve noise immunity it is suggested that the supply to the VCCD pins be isolated with ferrite beads.

VCCJ – This pin provides power and a reference voltage for use by the JTAG interface circuitry. It may be set to allow the ispClock5300S family devices to function in JTAG chains operating at voltages differing from VCCD.

REFA_REFP, REFB_REFN – These input pins provide the inputs for clock signals, and can accommodate either single ended or differential signal protocols.

REFSEL – This input pin is used to select which clock input pair (REFA or REB) is selected for use as the reference input. When REFSEL=0, REFA is used, and when REFSEL=1, REFB is used.

VTT_REFA, VTT_REFB – These pins are used to provide a termination voltage for the reference inputs when they are configured for SSTL or HSTL logic, and should be connected to a suitable voltage supply in those cases.

FBK – This input pin provides feedback sense of the output clock signal, and can accommodate any of the single-ended logic types.

VTT_FBK – This pin is used to provide a termination voltage for the feedback input when it is configured for SSTL or HSTL logic, and should be connected to a suitable voltage supply in those cases.

TDO, TDI, TCK, TMS – These pins comprise the ispClock5300S device's JTAG interface. The signal levels for these pins are determined by the selection of the VCCJ voltage.

LOCK – This output pin indicates that the device's PLL is in a locked condition when it goes HIGH.

$\overline{\text{OEX}}$, $\overline{\text{OEY}}$ – These pins are used to enable the outputs or put them into a high-impedance condition. Each output may be set so that it is always on, always off, enabled by $\overline{\text{OEX}}$ or enabled by $\overline{\text{OEY}}$.

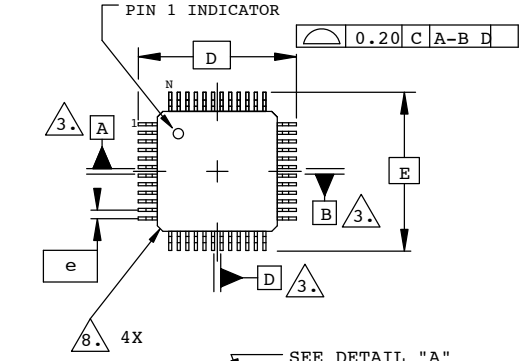
PLL_BYPASS – When this pin is pulled LOW, the V-dividers are driven from the output of the device's VCO, and the device behaves as a phase-locked loop. When this pin is pulled HIGH, the V-dividers are driven directly from a selected reference input, and the PLL functions are effectively bypassed.

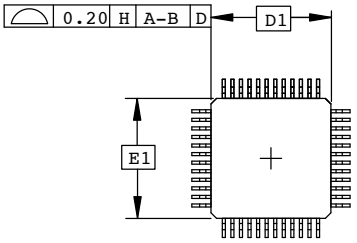
$\overline{\text{RESET}}$ – When this pin is pulled LOW, all on-board counters are reset, and lock is lost. If the $\overline{\text{RESET}}$ pin is not driven by an external logic it should be pulled up to V_{CCD} through a 10kΩ resistor.

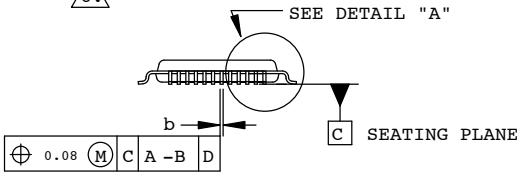
NC – These pins have no internal connection. It is recommended that they be left unconnected.

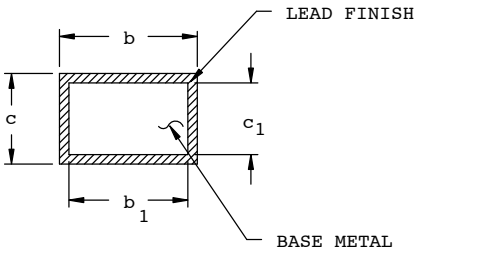
Package Diagrams

48-Pin TQFP (Dimensions in Millimeters)

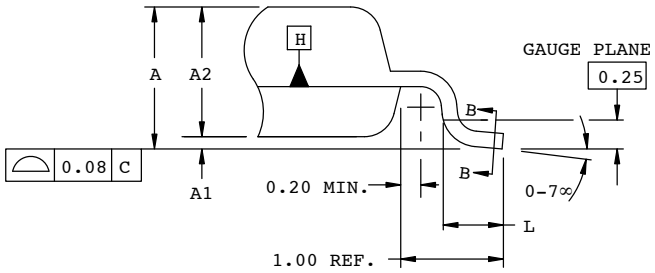








SECTION B - B



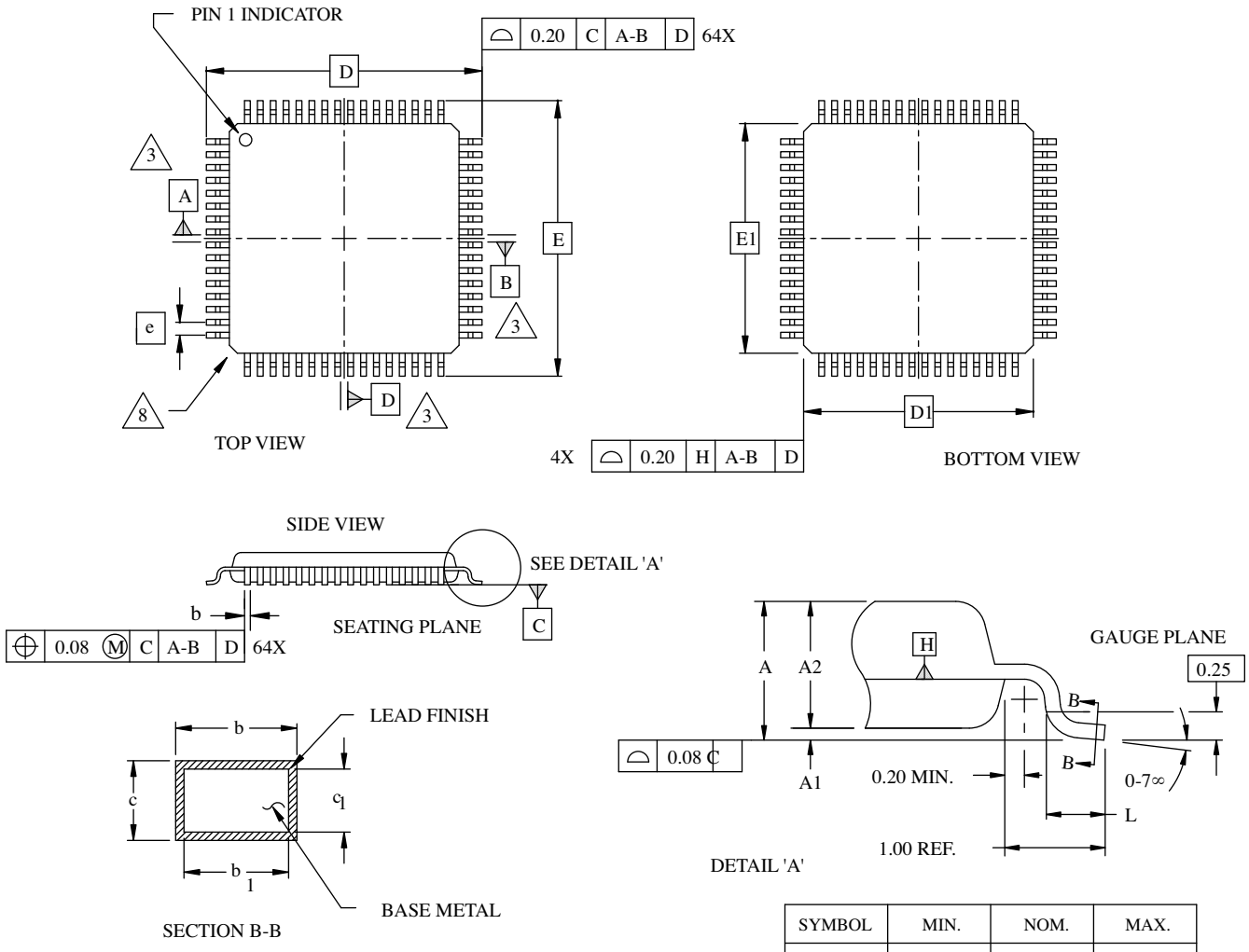
DETAIL "A"

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
5. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 MM.
6. SECTION B-B:
   THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 MM FROM THE LEAD TIP.
7. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D		9.00 BSC	
D1		7.00 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
N		48	
e		0.50 BSC	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	0.15	0.20
c1	0.09	0.13	0.16

64-Pin TQFP (Dimensions in Millimeters)

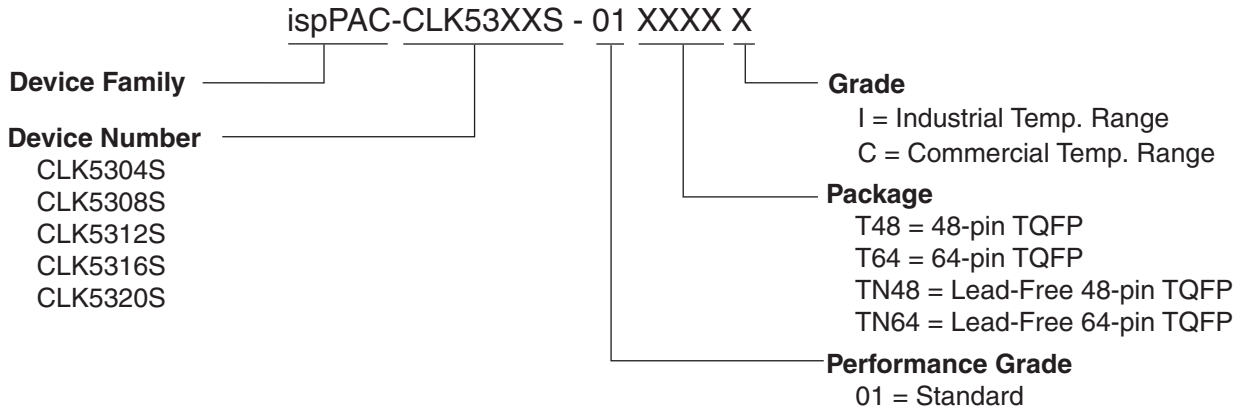


SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
L	0.45	0.60	0.75
N		64	
e		0.50 BSC	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	-	0.20
c1	0.09	-	0.16

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
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7. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

Part Number Description



Ordering Information

Conventional Packaging

Commercial

Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5320S-01T64C	20	3.3V	TQFP	64
ispPAC-CLK5316S-01T64C	16	3.3V	TQFP	64
ispPAC-CLK5312S-01T48C	12	3.3V	TQFP	48
ispPAC-CLK5308S-01T48C	8	3.3V	TQFP	48
ispPAC-CLK5304S-01T48C	4	3.3V	TQFP	48

Industrial

Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5320S-01T64I	20	3.3V	TQFP	64
ispPAC-CLK5316S-01T64I	16	3.3V	TQFP	64
ispPAC-CLK5312S-01T48I	12	3.3V	TQFP	48
ispPAC-CLK5308S-01T48I	8	3.3V	TQFP	48
ispPAC-CLK5304S-01T48I	4	3.3V	TQFP	48

Lead-Free Packaging

Commercial

Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5320S-01TN64C	20	3.3V	Lead-Free TQFP	64
ispPAC-CLK5316S-01TN64C	16	3.3V	Lead-Free TQFP	64
ispPAC-CLK5312S-01TN48C	12	3.3V	Lead-Free TQFP	48
ispPAC-CLK5308S-01TN48C	8	3.3V	Lead-Free TQFP	48
ispPAC-CLK5304S-01TN48C	4	3.3V	Lead-Free TQFP	48

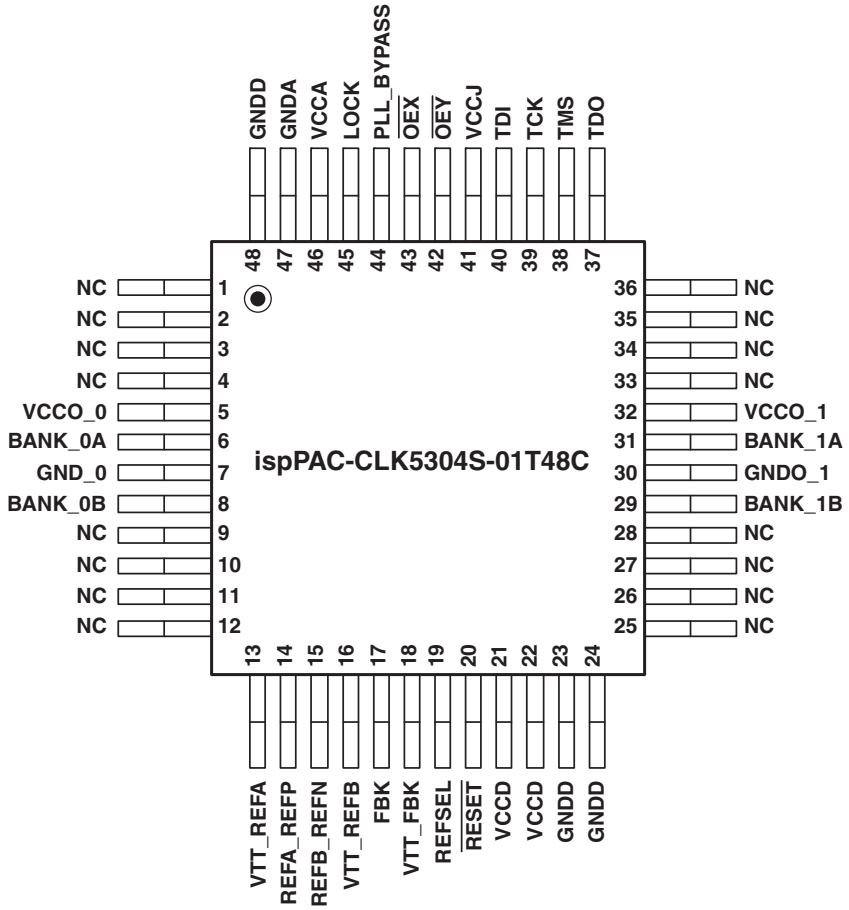
Lead-Free Packaging (Cont.)

Industrial

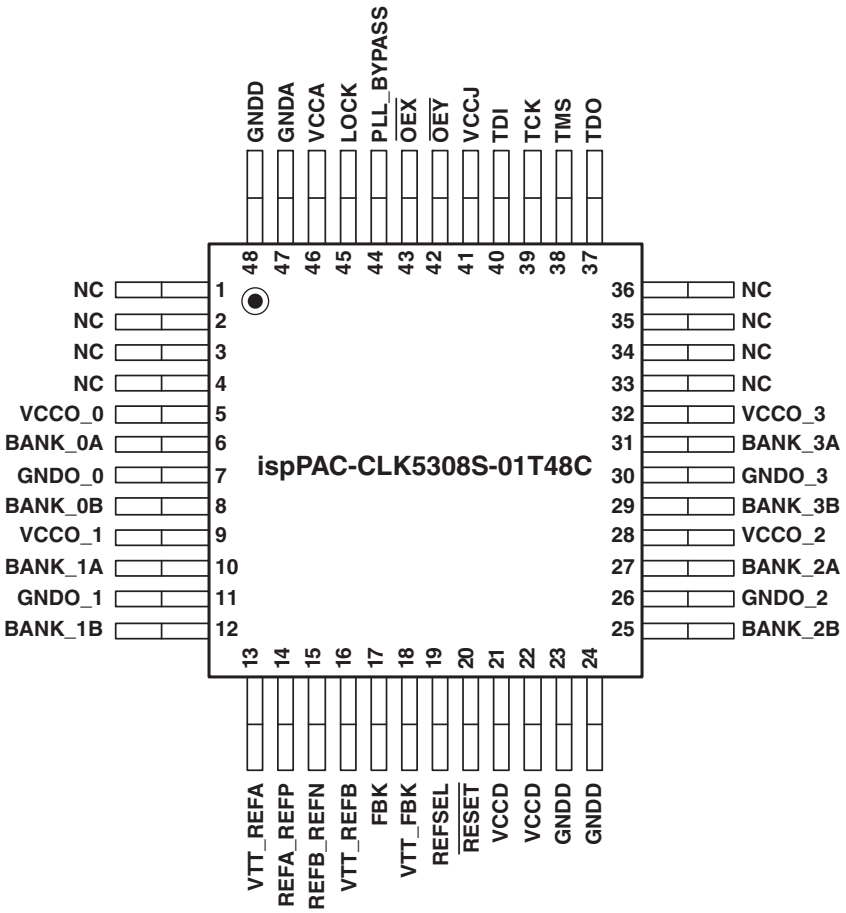
Part Number	Clock Outputs	Supply Voltage	Package	Pins
ispPAC-CLK5320S-01TN64I	20	3.3V	Lead-Free TQFP	64
ispPAC-CLK5316S-01TN64I	16	3.3V	Lead-Free TQFP	64
ispPAC-CLK5312S-01TN48I	12	3.3V	Lead-Free TQFP	48
ispPAC-CLK5308S-01TN48I	8	3.3V	Lead-Free TQFP	48
ispPAC-CLK5304S-01TN48I	4	3.3V	Lead-Free TQFP	48

Package Options

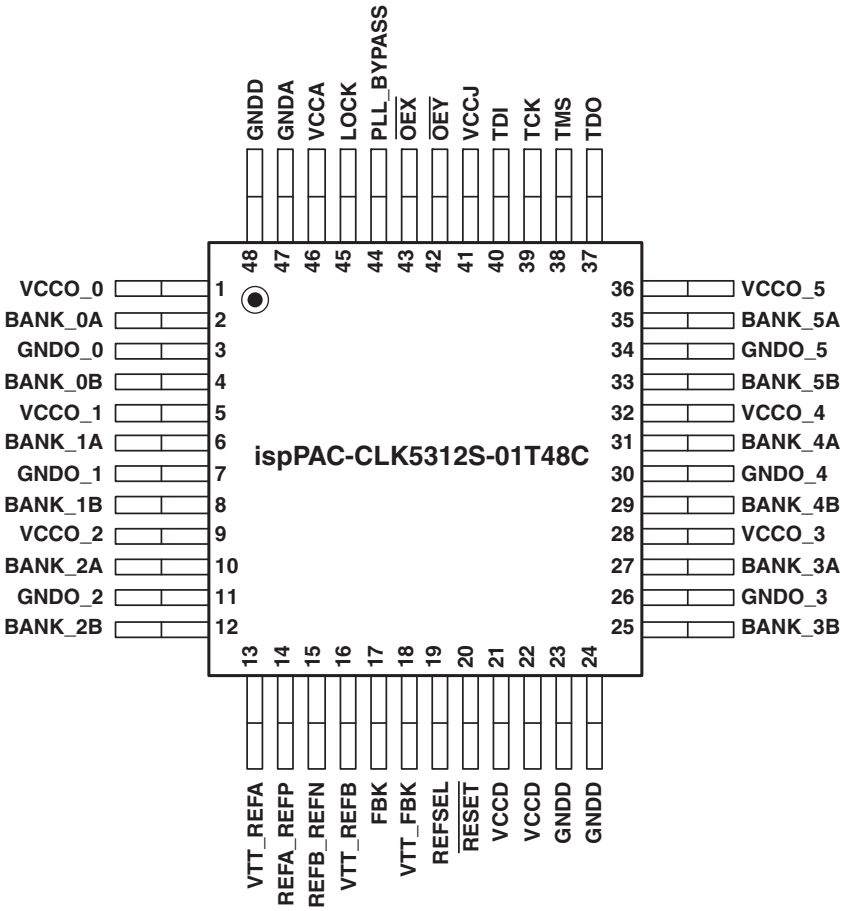
ispClock5304S: 48-pin TQFP



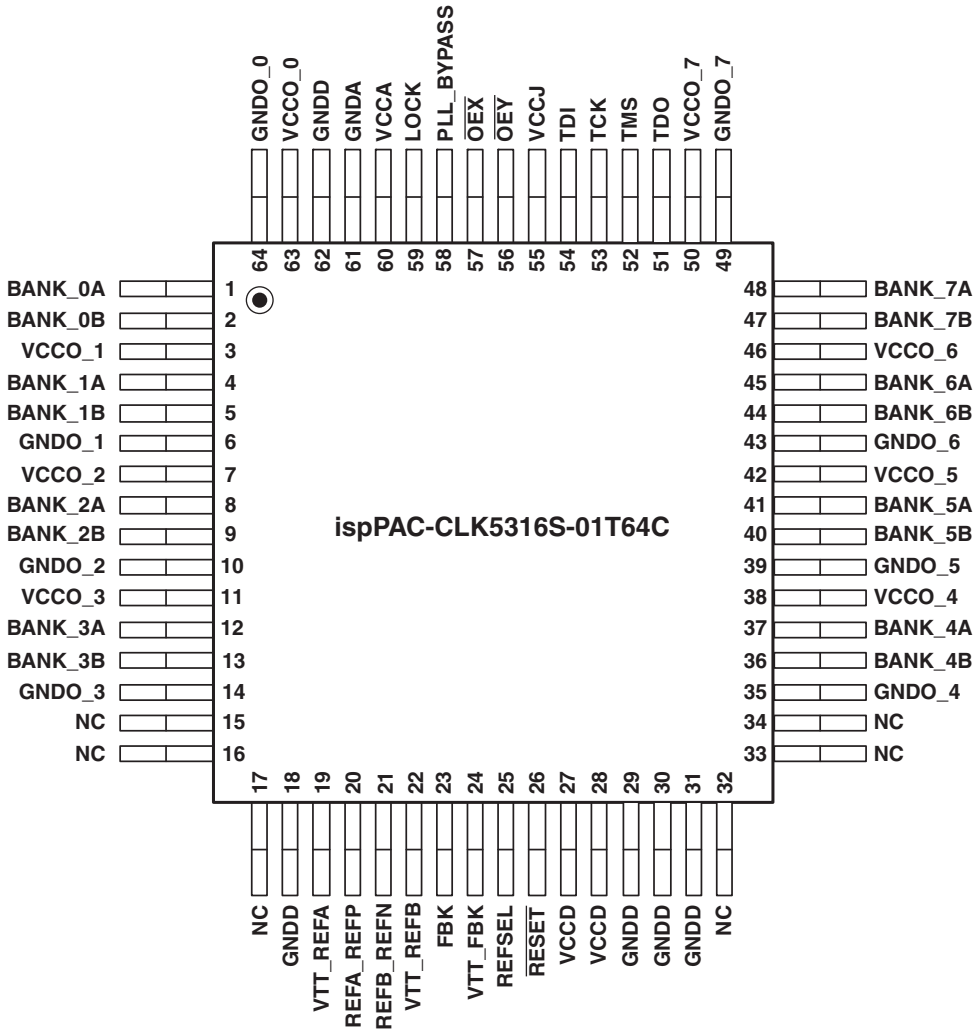
ispClock5308S: 48-pin TQFP



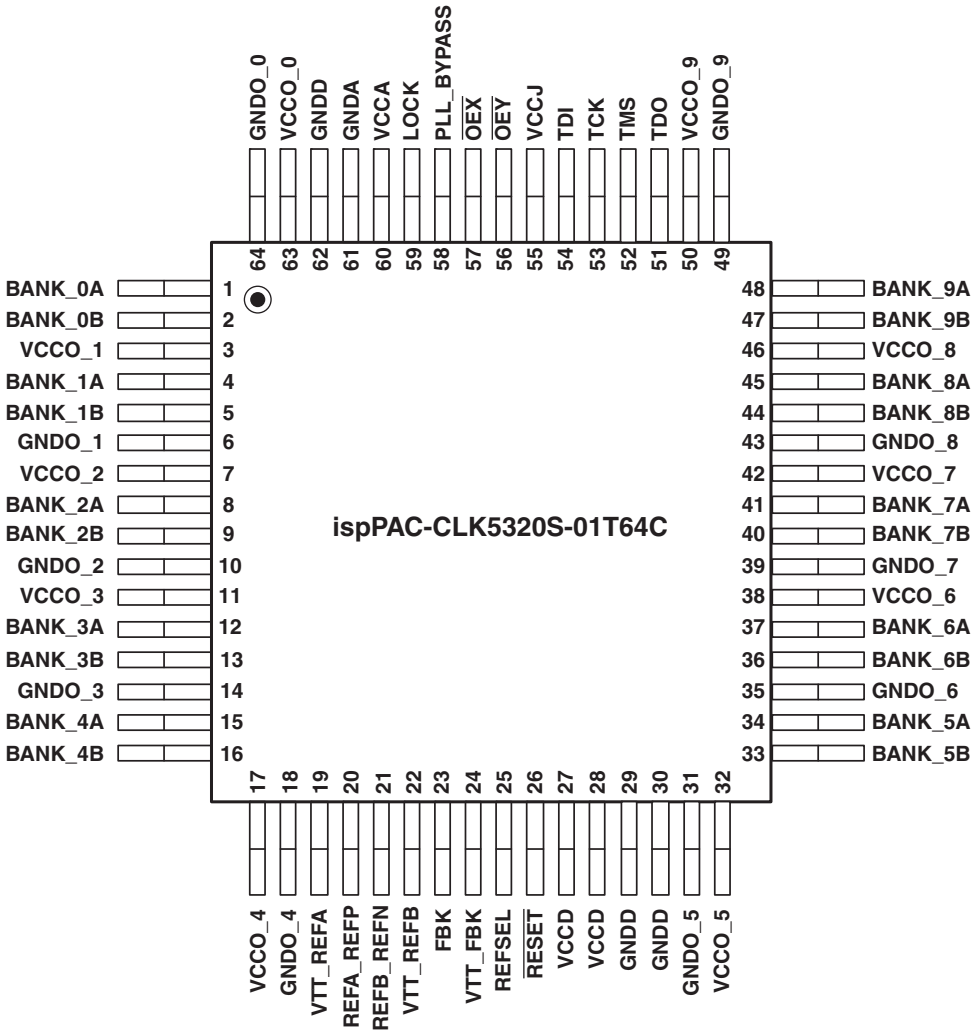
ispClock5312S: 48-pin TQFP



ispClock5316S: 64-pin TQFP



ispClock5320S: 64-pin TQFP



Technical Support Assistance

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Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
April 2006	01.0	Initial release.
May 2006	01.1	Performance Characteristics-PLL table - Correction to min. output frequency, f_{OUT} in Fine Skew Mode. Min frequency = 5MHz.
		Programmable Skew table - Correction to number of skew steps (from 16 to 8).
		Programmable Skew table - Correction to Skew control range.
		Output V Dividers section - Added explanation to V-divider settings as Power of 2 Settings (1, 2, 4, 8, 16, 32).
June 2006	01.2	Added Reset Signal Slew Rate specification to Control Functions table.
		Modified pin descriptions in Pin Descriptions table to reflect changes to pin 48 from NC to GNDD.
		Modified package diagrams to reflect the pin 48 changes from NC to GNDD.
		Modified RESET pin description to include pull-up resistor when not driven.
October 2006	01.3	Included references to ispClock5316S and ispClock5320S devices.
		Added typical performance graphs.
October 2007	01.4	Updated Boundary Scan Register information in ispClock5300S TAP Registers diagram.
		Added support for the Internal Feedback mode of operation.