



# AK09915D

## 3-axis Electronic Compass

### 1. General Description

AK09915D is 3-axis electronic compass IC with high sensitive Hall sensor technology.

Small package of AK09915D incorporates magnetic sensors for detecting terrestrial magnetism in the X-axis, Y-axis, and Z-axis, a sensor driving circuit, signal amplifier chain, and an arithmetic circuit for processing the signal from each sensor. Self-test function is also incorporated. From its compact foot print and thin package feature, it is suitable for map heading up purpose in GPS-equipped smart phone and tablet to realize pedestrian navigation function.

### 2. Features

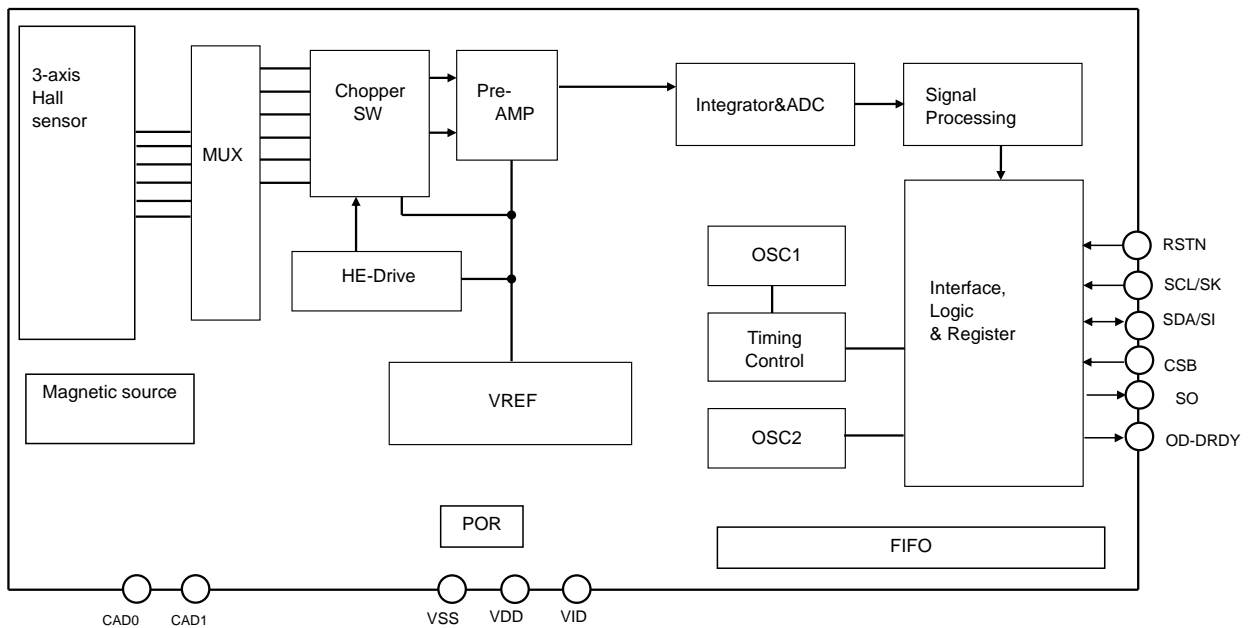
- Functions:
  - 3-axis magnetometer device suitable for compass application
  - Built-in A to D Converter for magnetometer data out
  - 16-bit data out for each 3-axis magnetic component
    - Sensitivity: 0.15  $\mu$ T/LSB (typ.)
  - Serial interface
    - I<sup>2</sup>C bus interface  
Standard, Fast and High-speed modes (up to 2.5 MHz) compliant with Philips I<sup>2</sup>C specification Ver.2.1
    - 4-wire SPI
  - Operation mode
    - Power-down, Single measurement, Continuous measurement and Self-test
  - Open Drain DRDY function for measurement data ready
  - Magnetic sensor overflow monitor function
  - Built-in oscillator for internal clock source
  - Power on Reset circuit
  - Self-test function with internal magnetic source
  - Built-in Noise Suppression Filter (NSF)
  - Selectable sensor drive
    - Low power drive / Low noise drive
  - Built-in magnetic sensitivity adjustment circuit
  - 32 FIFO data buffer
- Operating temperatures:
  - -30°C to +85°C
- Operating supply voltage:
  - Analog power supply +1.7V to +3.6V
  - Digital Interface supply +1.65V to analog power supply voltage
- Current consumption:
  - Power-down: 3  $\mu$ A (typ.)
  - Measurement:
    - Average current consumption at 100 Hz repetition rate
      - ✧ Low power drive: 0.9 mA (typ.)
      - ✧ Low noise drive: 1.8 mA (typ.)
- Package:
  - AK09915D 14-pin WL-CSP (BGA): 1.6 mm  $\times$  1.6 mm  $\times$  0.5 mm (typ.)

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**4. Block Diagram and Functions**



Block	Function
3-axis Hall sensor	Monolithic Hall elements.
MUX	Multiplexer for selecting Hall elements.
Chopper SW	Performs chopping.
HE-Drive	Magnetic sensor drive circuit for constant-current driving of sensor.
Pre-AMP	Fixed-gain differential amplifier used to amplify the magnetic sensor signal.
Integrator & ADC	Integrates and amplifies pre-AMP output or T-sensor output and performs analog-to-digital conversion.
OSC1	Generates an operating clock for sensor measurement.
OSC2	Generates an operating periodic clock for sequencer.
POR	Power on Reset circuit. Generates reset signal on rising edge of VDD.
VREF	Generates reference voltage and current.
FIFO	The buffer is capable up to 32sets of data.
Interface Logic & Register	Exchanges data with an external CPU. ODDRDY pin indicates sensor measurement has ended and data is ready to be read. I <sup>2</sup> C bus interface using two pins, namely, SCL and SDA. Standard, Fast and High-speed modes are supported. The low-voltage specification can be supported by applying 1.65V to the VID pin. 4-wire SPI is also supported by SK, SI, SO and CSB pins. 4-wire SPI works in VID pin voltage down to 1.65 V, too.
Signal Processing	Noise suppression function by the filtering process. Filtering process can be enabled or disabled.
Timing Control	Generates a timing signal required for internal operation from a clock generated by the OSC1.
Magnetic Source	Generates magnetic field for self-test of magnetic sensor.

### 5. Pin Configurations and Functions

Pin No.	Pin name	I/O	Power supply	Type	Function
A1	ODDRDY	O	VID	Open Drain	Open Drain Data Ready output pin. “L” active. Informs measurement ended and data is ready to be read. Connect to VID on contact with pull-up resistor. Do not apply more than VID voltage to ODDRDY pin.
A2	CSB	I	VID	CMOS	Chip select pin for 4-wire SPI. “L” active. Connect to VID when selecting I <sup>2</sup> C bus interface.
A3	SCL	I	VID	CMOS	When the I <sup>2</sup> C bus interface is selected (CSB pin is connected to VID). SCL: Control clock input pin Input: Schmitt trigger
	SK				When the 4-wire SPI is selected. SK: Serial clock input pin.
A4	SDA	I/O	VID	CMOS	When the I <sup>2</sup> C bus interface is selected (CSB pin is connected to VID). SDA: Control data input/output pin Input: Schmitt trigger, Output: Open-drain
	SI	I			When the 4-wire SPI is selected. SI: Serial data input pin
B1	VDD	-	-	Power	Positive power supply pin.
B3	N/C	-	-	-	Non-connect Connect to VSS or keep this pin non-connected.
B4	SO	O	VID	CMOS	When the I <sup>2</sup> C bus interface is selected (CSB pin is connected to VID) Hi-Z output. Keep this pin electrically non-connected.
					When the 4-wire SPI is selected. Serial data output pin
C1	VSS	-	-	Power	Ground pin
C2	N/C	-	-	-	Non-connect Connect to VSS or keep this pin non-connected.
C3	N/C	-	-	-	Non-connect Connect to VSS or keep this pin non-connected.
C4	VID	-	-	Power	Digital interface positive power supply pin.
D1	CAD0	I	VDD	CMOS	When the I <sup>2</sup> C bus interface is selected (CSB pin is connected to VID) CAD0:Slave address 0 input pin Connect to VSS or VDD.
					When the 4-wire serial interface is selected. Connect to VSS.
D2	CAD1	I	VDD	CMOS	When the I <sup>2</sup> C bus interface is selected (CSB pin is connected to VID). CAD1:Slave address 1 input pin Connect to VSS or VDD.
					When the 4-wire serial interface is selected. Connect to VSS.
D4	RSTN	I	VID	CMOS	Reset pin. Resets registers by setting to “L”. Connect to VID when not in use.

## 6. Absolute Maximum Ratings

V<sub>SS</sub> = 0V

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage (V <sub>DD</sub> , V <sub>ID</sub> )	V+	-0.3	+4.3	V
Input voltage (except for power supply pin)	V <sub>IN</sub>	-0.3	(V <sub>+</sub> )+0.3	V
Input current (except for power supply pin)	I <sub>IN</sub>	-	±10	mA
Storage temperature	T <sub>st</sub>	-40	+125	°C

If the device is used in conditions exceeding these values, the device may be destroyed. Normal operations are not guaranteed in such exceeding conditions.

## 7. Recommended Operating Conditions

V<sub>SS</sub> = 0V

Parameter	Remark	Symbol	Min.	Typ.	Max.	Unit
Operating temperature		T <sub>a</sub>	-30		+85	°C
Power supply voltage	V <sub>DD</sub> pin voltage	V <sub>DD</sub>	1.7	3.0	3.6	V
	V <sub>ID</sub> pin voltage	V <sub>ID</sub>	1.65		V <sub>DD</sub>	V

## 8. Electrical Characteristics

The following conditions apply unless otherwise noted:

V<sub>DD</sub> = 1.7V to 3.6V, V<sub>ID</sub> = 1.65V to V<sub>DD</sub>, Temperature range = -30 °C to +85 °C

### 8.1. DC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level input voltage 1	V <sub>IH1</sub>	CSB RSTN		70% V <sub>ID</sub>			V
Low level input voltage 1	V <sub>IL1</sub>					30% V <sub>ID</sub>	V
High level input voltage 2	V <sub>IH2</sub>	SK/SCL		70% V <sub>ID</sub>		V <sub>ID</sub> +0.3	V
Low level input voltage 2	V <sub>IL2</sub>	SI/SDA		-0.3V		30% V <sub>ID</sub>	V
High level input voltage 3	V <sub>IH3</sub>	CAD0 CAD1		70% V <sub>DD</sub>			V
Low level input voltage 3	V <sub>IL3</sub>					30% V <sub>DD</sub>	V
Input current 1	I <sub>IN1</sub>	SK/SCL SI/SDA CSB RSTN	V <sub>in</sub> = V <sub>SS</sub> or V <sub>ID</sub>	-10		+10	μA
		CAD0 CAD1	V <sub>in</sub> = V <sub>SS</sub> or V <sub>DD</sub>	-10		+10	
Hysteresis input voltage (Note 1)	V <sub>HS</sub>	SCL SDA	V <sub>ID</sub> ≥ 2V	5% V <sub>ID</sub>			V
			V <sub>ID</sub> < 2V	10% V <sub>ID</sub>			
High level output voltage 1 (Note 2)	V <sub>OH1</sub>	SO	I <sub>OH</sub> ≥ -100μA	80% V <sub>ID</sub>			V
Low level output voltage 1 (Note 2)	V <sub>OL1</sub>		I <sub>OL1</sub> ≤ +100μA			20% V <sub>ID</sub>	V
Low level output voltage 2 (Note 2) (Note 3)	V <sub>OL2</sub>	SDA	I <sub>OL2</sub> ≤ +3mA V <sub>ID</sub> ≥ 2V			0.4	V
			I <sub>OL2</sub> ≤ +3mA V <sub>ID</sub> < 2V			20% V <sub>ID</sub>	V
Low level output voltage 3 (Note 3)	V <sub>OL3</sub>	OD- DRDY	I <sub>OL3</sub> ≤ +300μA			0.1	V

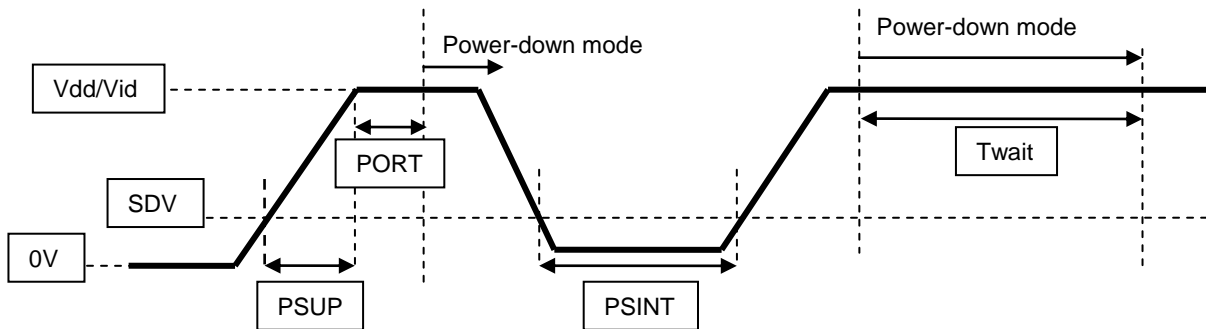
Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Current consumption (Note 4)	IDD1	VDD VID	Power-down mode Vdd = Vid = 3.0V		3	6	μA
	IDD2		When magnetic sensor is driven		2.1	3.5	mA
	IDD3		Self-test mode		3.2	4.7	mA
	IDD4		(Note 5)		0.1	5	μA

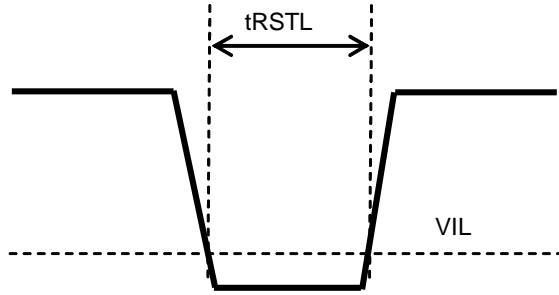
- (Note 1) Schmitt trigger input (reference value for design).
- (Note 2) IOH: High level output current. IOL1/IOL2: Low level output current.
- (Note 3) Output is open-drain. Connect to a pull-up resistor externally.
- (Note 4) Without any resistance load
- (Note 5) (case 1) Vdd = ON, Vid = ON, RSTN pin = “L”.  
 (case 2) Vdd = ON, Vid = OFF (0V), RSTN pin = “L”.  
 (case 3) Vdd = OFF (0V), Vid = ON.

**8.2. AC Characteristics**

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply rise time	PSUP	VDD VID	Period of time that VDD (VID) changes from 0.2V to Vdd (Vid).			50	ms
POR completion time (Note 6)	PORT		Period of time after PSUP to Power-down mode (Note 7)			100	μs
Power supply turn off voltage (Note 6)	SDV	VDD VID	Turn off voltage to enable POR to restart (Note 7)			0.2	V
Power supply turn on interval (Note 6)	PSINT	VDD VID	Period of time that voltage lower than SDV needed to be kept to enable POR to restart (Note 7)	100			μs
Wait time before mode setting	Twait			100			μs
Reset input effective pulse width (“L”)	tRSTL	RSTN		5			μs

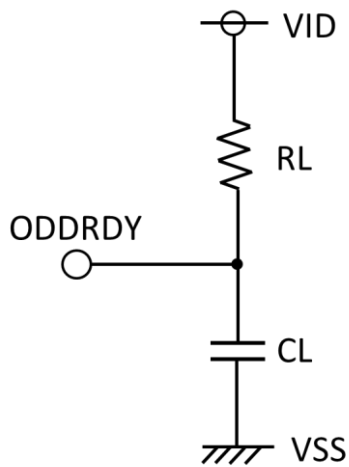
- (Note 6) Reference value for design.
- (Note 7) When POR circuit detects the rise of VDD/VID voltage, it resets internal circuits and initializes the registers. After reset, AK09915D transits to Power-down mode.



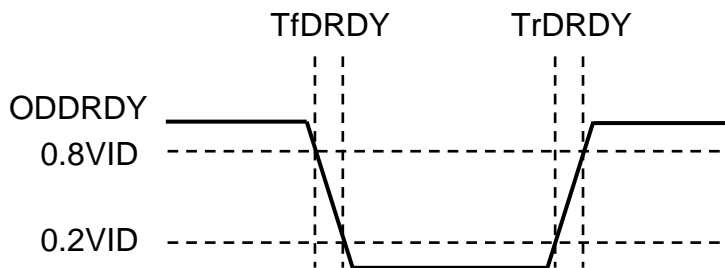


8.3. ODDRDY AC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
ODDRDY fall time	$T_{fDRDY}$	ODDRDY	$CL = 50 \text{ pF}, RL = 16 \text{ k}\Omega$			250	ns
ODDRDY rise time	$T_{rDRDY}$	ODDRDY	$CL = 50 \text{ pF}, RL = 24 \text{ k}\Omega$			2	$\mu\text{s}$



[Rise time and fall time]





**8.4. Analog Circuit Characteristics**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Measurement data output bit	DBIT		-	16	-	bit
Time for measurement	TSM	Single measurement mode SDR bit = "0" (refer to 9.6)		4.5		ms
		SDR bit = "1" (refer to 9.6)		8.5		
Magnetic sensor sensitivity	BSE	Ta = 25 °C	0.1425	0.15	0.1575	μT/LSB
Magnetic sensor measurement range (Note 8)	BRG	Ta = 25 °C	±4670	±4912	±5160	μT
Magnetic sensor initial offset (Note 9)		Ta = 25 °C	-2000		+2000	LSB

(Note 8) Reference value for design.

(Note 9) Value of measurement data register on shipment test without applying magnetic field on purpose.

**8.5. 4-wire SPI**

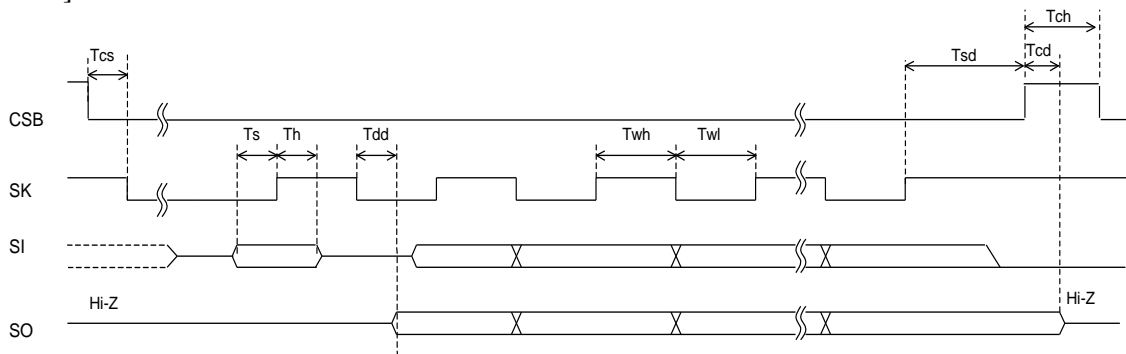
4-wire SPI is compliant with mode 3 (SPI-mode3).

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock Frequency	Fspi			4	MHz
CSB setup time	Tcs	50			ns
Data setup time	Ts	50			ns
Data hold time	Th	50			ns
SK high time	Twh	100			ns
SK low time	Twl	100			ns
SK setup time	Tsd	50			ns
SK to SO delay time (Note 10)	Tdd			50	ns
CSB to SO delay time (Note 10)	Tcd			50	ns
SK rise time (Note 11)	Tr			100	ns
SK fall time (Note 11)	Tf			100	ns
CSB high time	Tch	150			ns

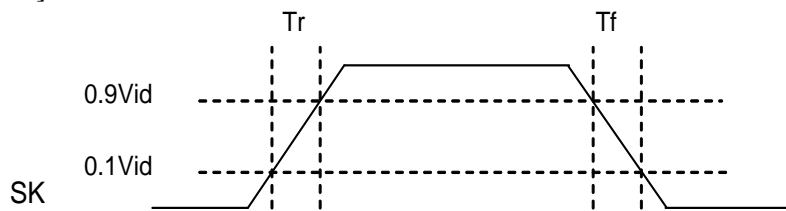
(Note 10) SO load capacitance: 20pF

(Note 11) Reference value for design.

[4-wire SPI]



[Rise time and fall time]



### 8.6. I<sup>2</sup>C Bus Interface

CSB pin = "H"

I<sup>2</sup>C bus interface is compliant with Standard mode, Fast mode and High-speed mode (Hs-mode).

Standard/Fast/Hs-mode is selected automatically by fSCL.

Standard mode

fSCL ≤ 100kHz

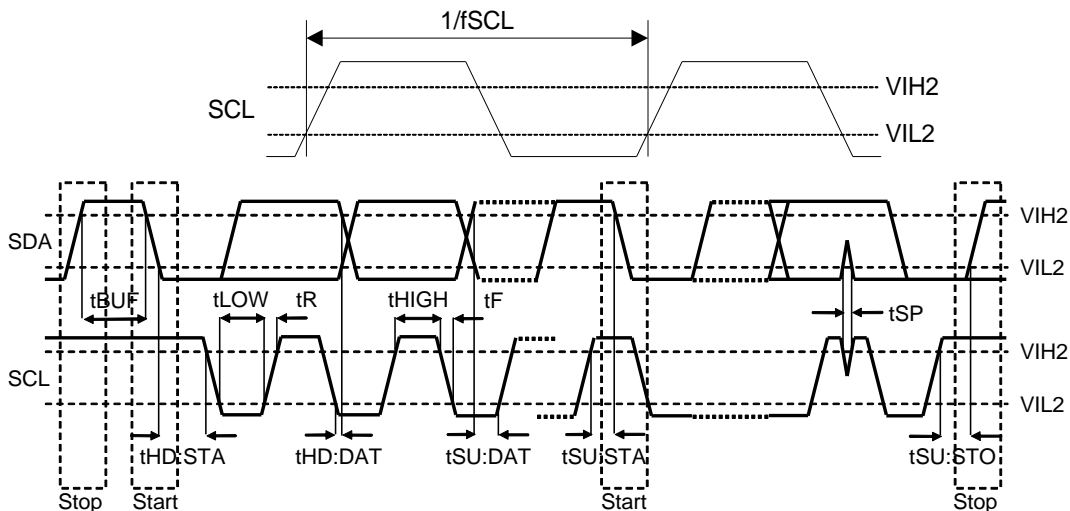
Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			100	kHz
tHIGH	SCL clock "High" time	4.0			μs
tLOW	SCL clock "Low" time	4.7			μs
tR	SDA and SCL rise time			1.0	μs
tF	SDA and SCL fall time			0.3	μs
tHD:STA	Start Condition hold time	4.0			μs
tSU:STA	Start Condition setup time	4.7			μs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0			μs
tSU:DAT	SDA setup time (vs. SCL rising edge)	250			ns
tSU:STO	Stop Condition setup time	4.0			μs
tBUF	Bus free time	4.7			μs

Fast mode

100kHz ≤ fSCL ≤ 400kHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			400	kHz
tHIGH	SCL clock "High" time	0.6			μs
tLOW	SCL clock "Low" time	1.3			μs
tR	SDA and SCL rise time			0.3	μs
tF	SDA and SCL fall time			0.3	μs
tHD:STA	Start Condition hold time	0.6			μs
tSU:STA	Start Condition setup time	0.6			μs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0			μs
tSU:DAT	SDA setup time (vs. SCL rising edge)	100			ns
tSU:STO	Stop Condition setup time	0.6			μs
tBUF	Bus free time	1.3			μs
tSP	Noise suppression pulse width			50	ns

[I<sup>2</sup>C bus interface timing]



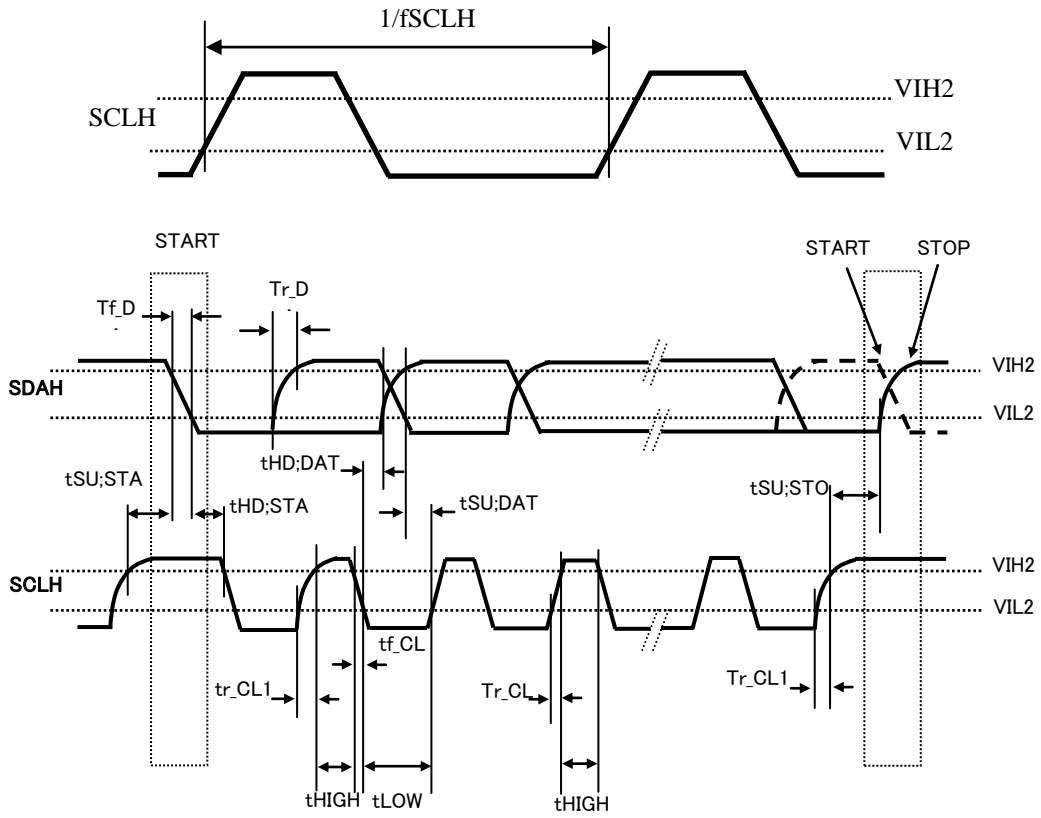
- High-speed mode (Hs-mode)
- $C_b \leq 100\text{pF}$  ( $C_b$ : load capacitance)
  - $f_{\text{SCLH}} \leq 2.5\text{MHz}$

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCLH	SCLH clock frequency			2.5	MHz
tHIGH	SCLH clock "High" time	110			ns
tLOW	SCLH clock "Low" time	220			ns
tR_CL	SCLH rise time	10		40	ns
tR_CL1	SCLH rise time after a repeated START condition and after an acknowledge bit	10		80	ns
tR_DA	SDAH rise time	10		80	ns
tF_CL	SCLH fall time	-		40	ns
tF_DA	SDAH fall time	-		80	ns
tHD:STA	Start Condition hold time	160			ns
tSU:STA	Start Condition setup time	160			ns
tHD:DAT	SDAH hold time (vs. SCLH falling edge)	0			ns
tSU:DAT	SDAH setup time (vs. SCLH rising edge)	10			ns
tSU:STO	Stop Condition setup time	160			ns
tSP	Noise suppression pulse width			10	ns

- $C_b \leq 400\text{pF}$
- $f_{\text{SCLH}} \leq 1.7\text{MHz}$

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCLH	SCLH clock frequency			1.7	MHz
tHIGH	SCLH clock "High" time	120			ns
tLOW	SCLH clock "Low" time	320			ns
tR_CL	SCLH rise time	20		80	ns
tR_CL1	SCLH rise time after a repeated START condition and after an acknowledge bit	20		160	ns
tR_DA	SDAH rise time	20		160	ns
tF_CL	SCLH fall time	-		80	ns
tF_DA	SDAH fall time	-		160	ns
tHD:STA	Start Condition hold time	160			ns
tSU:STA	Start Condition setup time	160			ns
tHD:DAT	SDAH hold time (vs. SCLH falling edge)	0			ns
tSU:DAT	SDAH setup time (vs. SCLH rising edge)	10			ns
tSU:STO	Stop Condition setup time	160			ns
tSP	Noise suppression pulse width			10	ns

[I<sup>2</sup>C bus interface timing of Hs-mode]



## 9. Functional Descriptions

### 9.1. Power States

When VDD and VID are turned on from Vdd = OFF (0V) and Vid = OFF (0V), all registers in AK09915D are initialized by POR circuit and AK09915D transits to Power-down mode.

All the states in the table below can be set, although the transition from state 2 to state 3 and the transition from state 3 to state 2 are prohibited.

Table 9.1 Power States

State	VDD	VID	Power state
1	OFF (0V)	OFF (0V)	OFF (0V).
2	OFF (0V)	1.65V to 3.6V	It doesn't affect external interface. Digital pins other than SCL pin and SDA pin should be fixed to Power supply or "L" (0V). Refer to 5.
3	1.7V to 3.6V	OFF (0V)	
4	1.7V to 3.6V	1.65V to Vdd	ON

### 9.2. Reset Functions

When the power state is ON, always keep  $Vid \leq Vdd$ .

Power on Reset (POR) works until Vdd reaches to the operation effective voltage (about 1.1V: reference value for design) on power-on sequence.

When Vdd = 1.7 to 3.6V, POR circuit and VID monitor circuit are active. When Vid = 0V, AK09915D is in reset status and it consumes the current of reset state (IDD4).

AK09915D has four types of reset;

- (1) Power on Reset (POR)  
When Vdd rise is detected, POR circuit operates, and AK09915D is reset.
- (2) VID monitor  
When Vid is turned OFF (0V), AK09915D is reset.
- (3) Reset pin (RSTN)  
AK09915D is reset by Reset pin. When Reset pin is not used, connect to VID.
- (4) Soft reset  
AK09915D is reset by setting SRST bit.

After reset is completed, all registers and FIFO buffer are initialized and AK09915D transits to Power-down mode automatically.

### 9.3. Operation Modes

AK09915D has following nine operation modes:

- (1) Power-down mode
- (2) Single measurement mode
- (3) Continuous measurement mode 1
- (4) Continuous measurement mode 2
- (5) Continuous measurement mode 3
- (6) Continuous measurement mode 4
- (7) Continuous measurement mode 5
- (8) Continuous measurement mode 6
- (9) Self-test mode

By setting CNTL2 registers MODE[4:0] bits, the operation set for each mode is started. A transition from one mode to another is shown below.

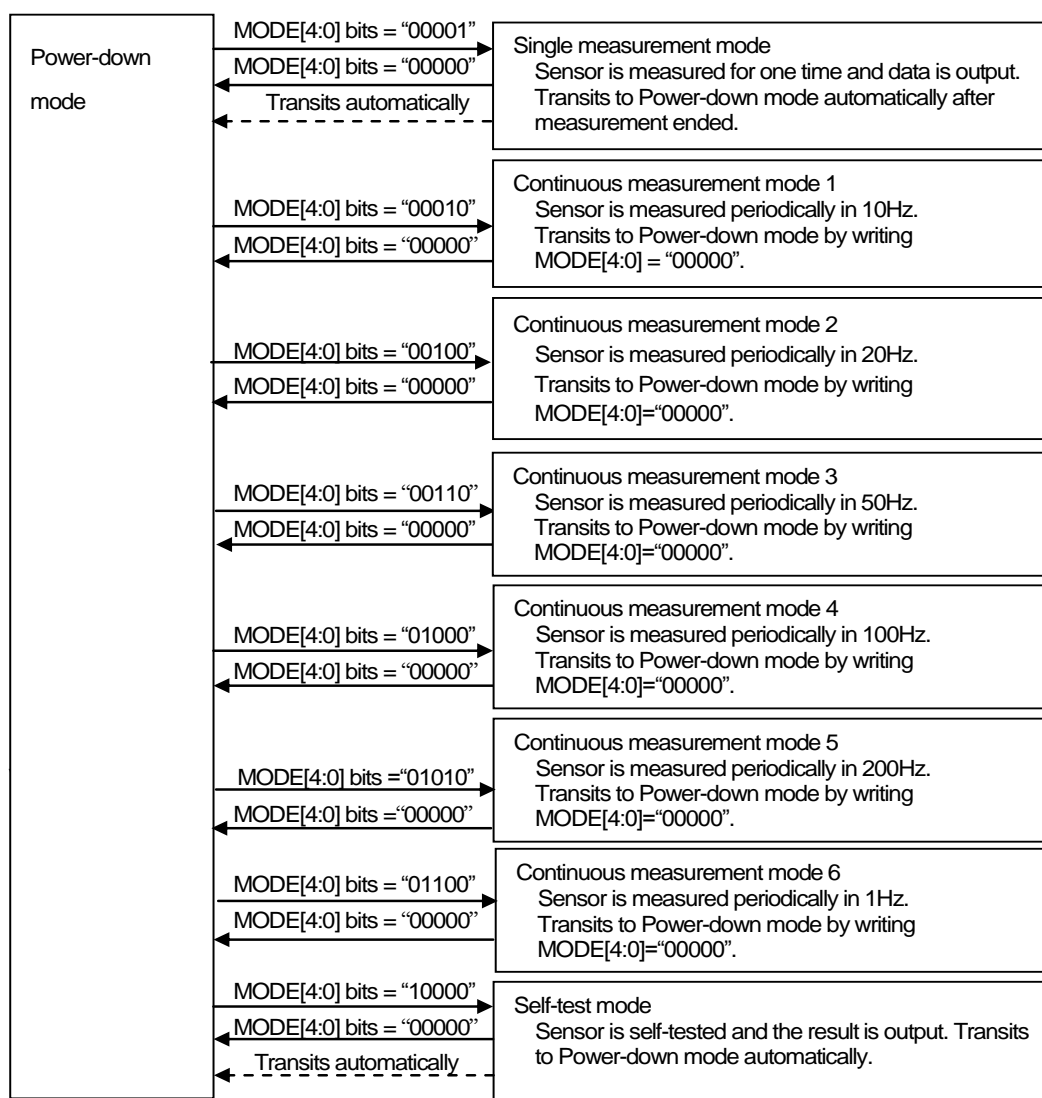


Figure 9.1 Operation mode

When power is turned ON, AK09915D is in Power-down mode. When a specified value is set to MODE[4:0] bits, AK09915D transits to the specified mode and starts operation. When user wants to change operation mode, transit to power-down mode first and then transit to other modes. After Power-down mode is set, at least 100  $\mu$ s ( $T_{wait}$ ) is needed before setting another mode.

**9.4. Description of Each Operation Mode**

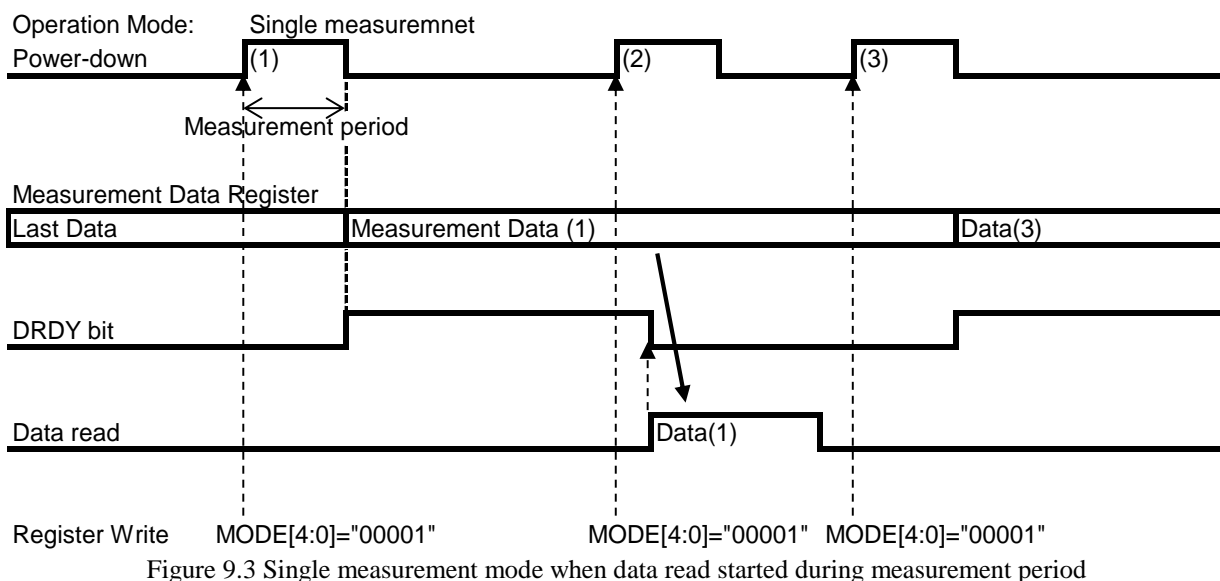
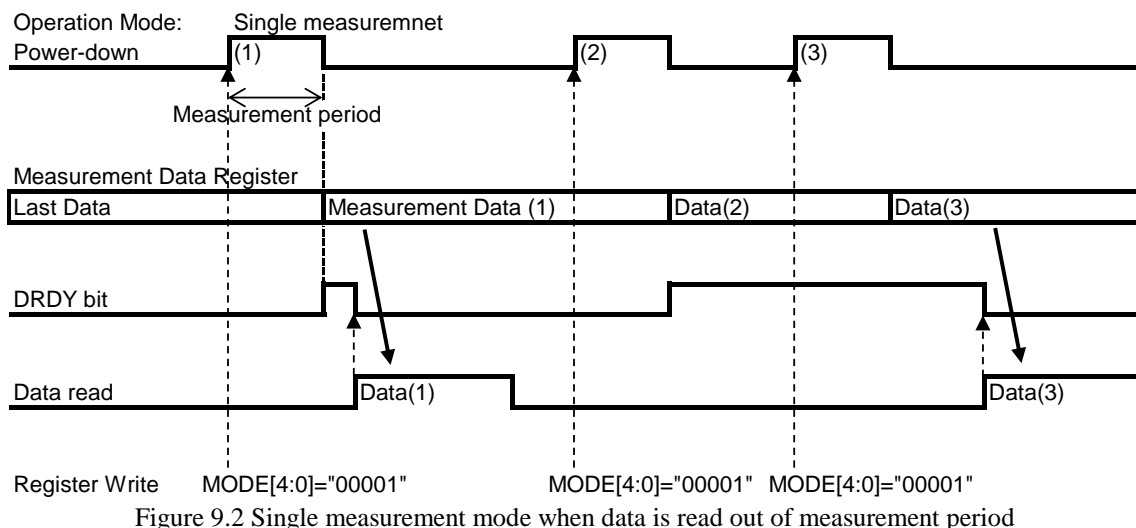
**9.4.1. Power-down Mode**

Power to almost all internal circuits is turned off. All registers are accessible in Power-down mode. Data stored in read/write registers are remained. They can be reset by soft reset.

**9.4.2. Single Measurement Mode**

When Single measurement mode (MODE[4:0] bits = “00001”) is set, magnetic sensor measurement is started. After magnetic sensor measurement and signal processing is finished, measurement magnetic data is stored to measurement data registers (HXL to HZH), then AK09915D transits to Power-down mode automatically. On transition to Power-down mode, MODE[4:0] bits turns to “00000”. At the same time, DRDY bit in ST1 register turns to “1”. This is called “Data Ready”. When any of measurement data registers (HXL to TMPS) or ST2 register is read, DRDY bit turns to “0”. It remains “1” on transition from Power-down mode to another mode. When DRDY bit turn to “1”, ODDRDY pin is “L”. When DRDY bit turn to “0”, ODDRDY pin is “H”. ODDRDY pin is low active.(Figure 9.2)

When sensor is measuring (Measurement period), measurement data registers (HXL to TMPS) keep the previous data. Therefore, it is possible to read out data even in measurement period. Data read out in measurement period are previous data. (Figure 9.3)





### 9.4.3. Continuous Measurement Mode 1, 2, 3, 4, 5 and 6

When Continuous measurement modes (1 to 6) are set, magnetic sensor measurement is started periodically at 10 Hz, 20 Hz, 50 Hz, 100 Hz, 200 Hz and 1Hz respectively. After magnetic sensor measurement and signal processing is finished, measurement magnetic data is stored to measurement data registers (HXL to HZH) and all circuits except for the minimum circuit required for counting cycle length are turned off (PD). When the next measurement timing comes, AK09915D wakes up automatically from PD and starts measurement again. Continuous measurement mode ends when Power-down mode (MODE[4:0] bits = “00000”) is set. It repeats measurement until Power-down mode is set.

When Continuous measurement modes (1 to 6) are set again while AK09915D is already in Continuous measurement mode, a new measurement starts. ST1, ST2 and measurement data registers (HXL to TMPS) will not be initialized by this.

Table 9.2 Continuous measurement modes

Operation mode	Register setting (MODE[4:0] bits)	Measurement frequency [Hz]
Continuous measurement mode 1	00010	10
Continuous measurement mode 2	00100	20
Continuous measurement mode 3	00110	50
Continuous measurement mode 4	01000	100
Continuous measurement mode 5	01010	200
Continuous measurement mode 6	01100	1

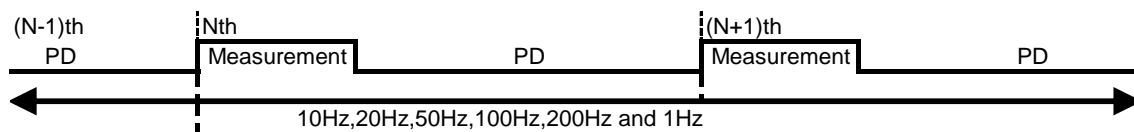


Figure 9.4 Continuous measurement mode

#### 9.4.3.1. Data Ready

When measurement data is stored and ready to be read, DRDY bit in ST1 register turns to “1”. This is called “Data Ready”. When DRDY bit turn to “1”, ODDRDY pin is “L”. When DRDY bit turn to “0”, ODDRDY pin is “H”. ODDRDY pin is low active. When measurement is performed correctly, AK09915D becomes Data Ready on transition to PD after measurement.

**9.4.3.2. Normal Read Sequence**

(1) Check Data Ready or not by any of the following method.

    Polling DRDY bit of ST1 register

    Monitor ODDRDY pin

    When Data Ready, proceed to the next step.

(2) Read ST1 register (not needed when polling ST1)

    DRDY bit: Shows Data Ready or not. Not when “0”, Data Ready when “1”.

    ODDRDY pin (connect to pull-up resistor): Shows Data Ready or not. Not when “H”, Data Ready when “L”.

    DOR: Shows if any data has been skipped before the current data or not. There are no skipped data when “0”, there are skipped data when “1”.

(3) Read measurement data

    When any of measurement data registers (HXL to TMPS) or ST2 register is read, AK09915D judges that data reading is started. When data reading is started, DRDY bit and DOR bit turns to “0”.

(4) Read ST2 register (required)

    HOFL: Shows if magnetic sensor is overflowed or not. “0” means not overflowed, “1” means overflowed.

    When ST2 register is read, AK09915D judges that data reading is finished. Stored measurement data is protected during data reading and data is not updated. By reading ST2 register, this protection is released. It is required to read ST2 register after data reading.

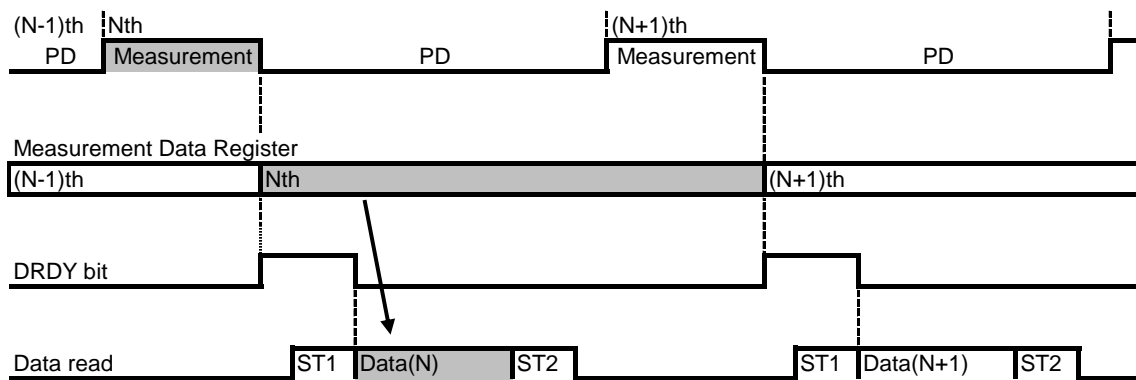


Figure 9.5 Normal read sequence

**9.4.3.3. Data Read Start during Measurement**

When sensor is measuring (Measurement period), measurement data registers (HXL to TMPS) keep the previous data. Therefore, it is possible to read out data even in measurement period. If data is started to be read during measurement period, previous data is read.

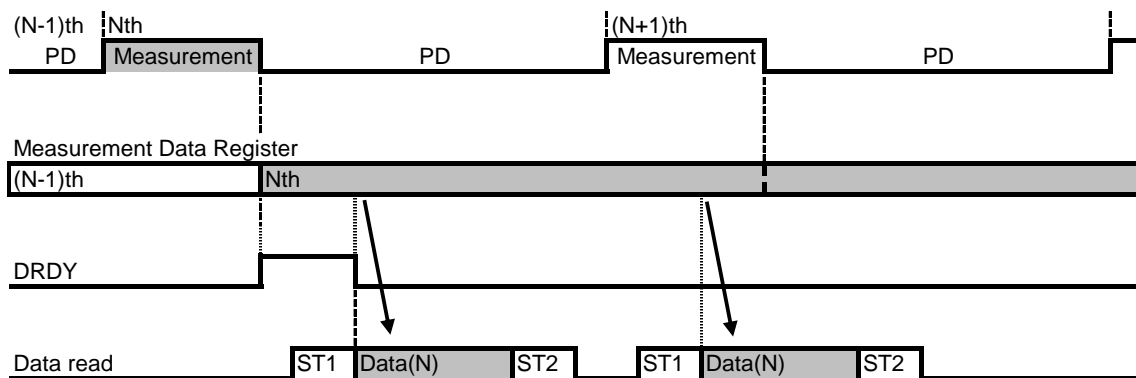


Figure 9.6 Data read start during measuring

**9.4.3.4. Data Skip**

When Nth data was not read before (N+1)th measurement ends, Data Ready remains until data is read. In this case, a set of measurement data is skipped so that DOR bit turns to “1”.

When data reading started after Nth measurement ended and did not finish reading before (N+1)th measurement ended, Nth measurement data is protected to keep correct data. In this case, a set of measurement data is skipped and not stored so that DOR bit turns to “1”.

In both case, DOR bit turns to “0” at the next start of data reading.

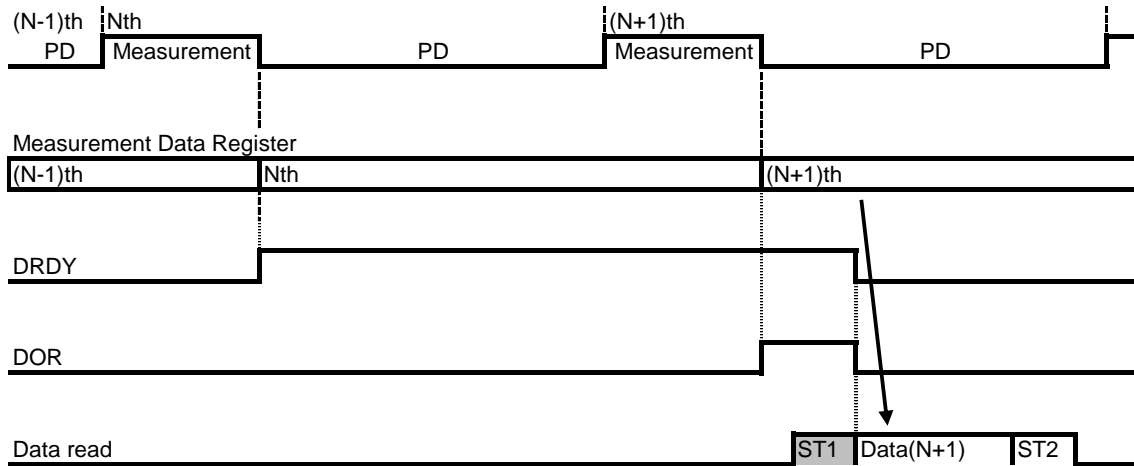


Figure 9.7 Data Skip: when data is not read

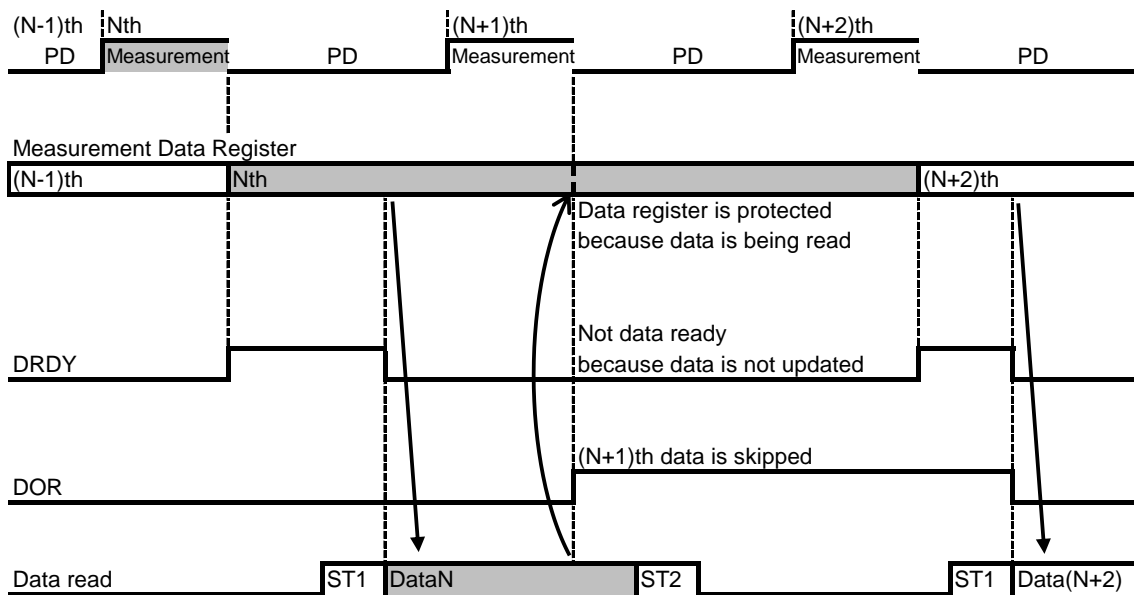


Figure 9.8 Data Skip: when data read has not been finished before the next measurement end

**9.4.3.5. End Operation**

Set Power-down mode (MODE[4:0] bits = “00000”) to end Continuous measurement mode.

### 9.4.3.6. Magnetic Sensor Overflow

AK09915D has the limitation for measurement range that the sum of absolute values of each axis should be smaller than 4912  $\mu\text{T}$ . (Note 12)

$$|X|+|Y|+|Z| < 4912 \mu\text{T}$$

When the magnetic field exceeded this limitation, data stored at measurement data are not correct. This is called Magnetic Sensor Overflow.

When magnetic sensor overflow occurs, HOFL bit turns to “1”. When measurement data register (HXL to HZH) is updated, HOFL bit is updated.

(Note 12) BSE: 0.15  $\mu\text{T}/\text{LSB}$

### 9.4.4. Self-test Mode

Self-test mode is used to check if the magnetic sensor is working normally.

When Self-test mode (MODE[4:0] bits = “10000”) is set, magnetic field is generated by the internal magnetic source and magnetic sensor is measured. Measurement data is stored to measurement data registers (HXL to HZH), then AK09915D transits to Power-down mode automatically.

Data read sequence and functions of read-only registers in Self-test mode is the same as Single measurement mode.

#### 9.4.4.1. Self-test Sequence

(1)Set Power-down mode. (MODE[4:0] bits = “00000”)

(2)Set Self-test mode. (MODE[4:0] bits = “10000”)

(3)Check Data Ready or not by any of the following method.

    Polling DRDY bit of ST1 register

    Monitor ODDRDY pin

    When Data Ready, proceed to the next step.

(4)Read measurement data (HXL to HZH)

#### 9.4.4.2. Self-test Judgment

When measurement data read by the above sequence is in the range of following table, AK09915D is working normally.

	HX[15:0] bits	HY[15:0] bits	HZ[15:0] bits
Criteria	$-200 \leq \text{HX} \leq +200$	$-200 \leq \text{HY} \leq +200$	$-800 \leq \text{HZ} \leq -200$

### 9.5. Noise Suppression Filter (NSF)

In Single measurement mode, Continuous measurement modes (1 to 6), output from the magnetic sensor can be filtered to suppress the noise. This filter name is Noise Suppression Filter (NSF). When NSF bit = “0”, NSF is “disable” and output magnetic data is not filtered. When NSF bit = “1”, output magnetic data is filtered.

NSF bit can be changed in Power-down mode only. Default NSF bit is “disable” (NSF bits = “0”).

### 9.6. Sensor Drive Select

AK09915D can choose “Low power” or “Low noise” drive.

“Low power” is used to save the current consumption and “Low noise” is used to reduce the noise of the AK09915D. When Low power (SDR bit = “0”) is set, average current consumption at 100 Hz repetition rate is reduced from 1.8 mA to 0.9 mA. When Low noise (SDR bit = “1”) is set, output magnetic data noise is less than Low power (about 70% of Low power).

SDR bit can be changed in Power-down mode only. Default SDR bit is Low power enable (SDR bit = “0”).

## 9.7. FIFO

FIFO function is available in Continuous measurement modes. FIFO function is enabled by setting FIFO bit = "1". It is prohibited to enable FIFO function in any modes other than Continuous measurement modes.

When FIFO function is enabled, Measurement Magnetic Data (HXL to HZH) and HOFL bit are stored to the buffer as a set of data. The buffer is capable up to 32 sets of data. If a new data is measured when 32 sets of data are already stored, the oldest data set is deleted and the new data set is stored. If measurement data registers are read when FIFO function is enabled, the oldest data set is read as first-in first-out method.

When reading out data from the buffer, always start with HXL register and finish with ST2 register. By accessing HXL register, the oldest data set is loaded to the measurement data registers from the buffer. Reading ST2 register is regarded as the finish of reading out one set of data. Then the read data set is deleted and the next oldest data set will be ready to be read. If ST2 register or HXL register is not read, the same set of data is kept in the measurement data registers.

When FIFO function is enabled, DRDY bit and DOR bit functions differently. DRDY bit informs that data set is stored up to Watermark. Refer to 9.7.1 for details. DOR bit informs that data set is overflowed from the buffer. If a set of new data is measured when the buffer is full, DOR bit turns to "1". If at least one data set is read from the buffer, DOR bit turns to "0".

If data is read out when the buffer is empty, INV bit is turned to "1" and measurement data registers (HXL to HZH) are forced to fixed value 7FFFh. If a set of new data is measured, INV bit turns to "0".

When AK09915D is reset (refer to 9.2), FIFO buffer are initialized.

### 9.7.1. Watermark

When FIFO function is enabled, Watermark function is available. By setting WM[4:0] bits, AK09915D informs that data set is stored up to or more than Watermark. If the number of stored data set is equal to or more than the number set to WM[4:0] bits, DRDY bit turns to "1". If the number of stored data set is less than the number set to WM[4:0] bits, DRDY bit turns to "0". When DRDY bit turn to "1", ODDRDY pin is "L". When DRDY bit turn to "0", ODDRDY pin is "H".

WM[4:0] bits should be changed in the Power-down mode only. It is prohibited to write WM[4:0] bits in other modes.

**10. Serial Interface**

AK09915D supports I<sup>2</sup>C bus interface and 4-wire SPI. A selection is made by CSB pin. When used as 3-wire SPI, set SI pin and SO pin wired-OR externally.

- CSB pin = "L": 4-wire SPI
- CSB pin = "H": I<sup>2</sup>C bus interface

**10.1. 4-wire SPI**

The 4-wire SPI consists of four digital signal lines: SK, SI, SO, and CSB, and is provided in 16bit protocol. Data consists of Read/Write control bit (R/W), register address (7-bit) and control data (8-bit). To read out all axes measurement data (X, Y, Z), an option to read out more than one byte data using automatic increment command is available. (Sequential read operation)

CSB pin is low active. Input data is taken in on the rising edge of SK pin, and output data is changed on the falling edge of SK pin. (SPI-mode3)

Communication starts when CSB pin transits to "L" and stops when CSB pin transits to "H". SK pin must be "H" during CSB pin is in transition. Also, it is prohibited to change SI pin during CSB pin is "H" and SK pin is "H".

**10.1.1. Writing Data**

Input 16 bits data on SI pin in synchronous with the 16-bit serial clock input on SK pin. Out of 16 bits input data, the first 8-bit specify the R/W control bit (R/W = "0" when writing) and register address (7-bit), and the latter 8-bit are control data (8-bit). When any of addresses listed on Table 11.1 is input, AK09915D recognizes that it is selected and takes in latter 8-bit as setting data.

If the number of clock pulses is less than 16, no data is written. If the number of clock pulses is more than 16, data after the 16th clock pulse on SI pin are ignored.

It is not compliant with serial write operation for multiple addresses.

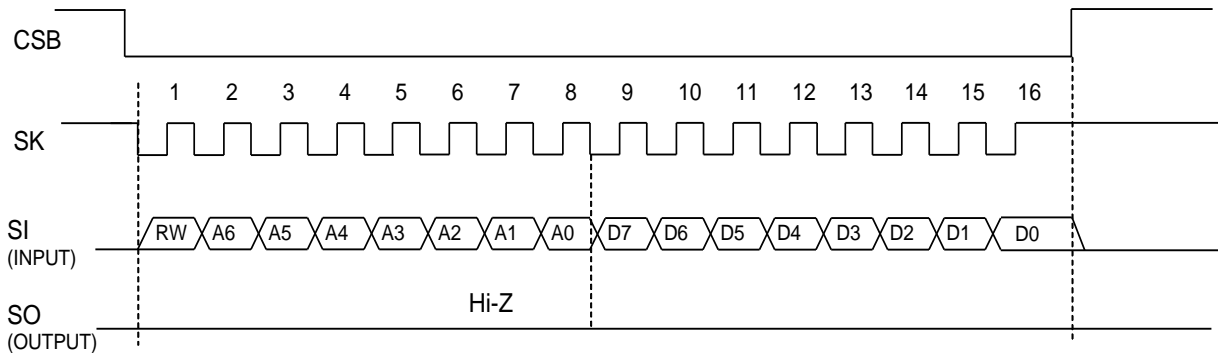


Figure 10.1 4-wire SPI Writing Data

### 10.1.2. Reading Data

Input the R/W control bit (R/W = “1”) and 7-bit register address on SI pin in synchronous with the first 8-bit of the 16 bits of a serial clock input on SK pin. Then AK09915D outputs the data held in the specified register with MSB first from SO pin.

When clocks are input continuously after one byte of data is read, the address is incremented and data in the next address is output. Accordingly, after the falling edge of the 15th clock and CSB pin is “L”, the data in the next address is output on SO pin. When CSB pin is driven “L” to “H”, SO pin is placed in the high-impedance state.

AK09915D has three incrementation lines; 00h to 18h, 30h to 32h and 60h to 62h. In line 00h to 18h, the incrementation depends on FIFO bit. When FIFO function is disabled, AK09915D increments as follows: 00h → 01h → 02h → 03h → 10h → 11h ... → 18h → 00h → 01h ... . When FIFO function is enabled: 00h → 01h → 02h → 03h → 10h → 11h ... → 18h → 11h → 12h ... . In line 30h to 32h and 60h to 62h, it increments as: 30h → 31h → 32h → 30h ..., and 60h → 61h → 62h → 60h ... .

33h to 35h and 37h are reserved addresses. Do not access to those addresses.

When specified address is other than 00h to 18h, 30h to 37h and 60h to 62h, AK09915D recognizes that it is not selected and keeps SO pin in high-impedance state. Therefore, user can use other addresses for other devices.

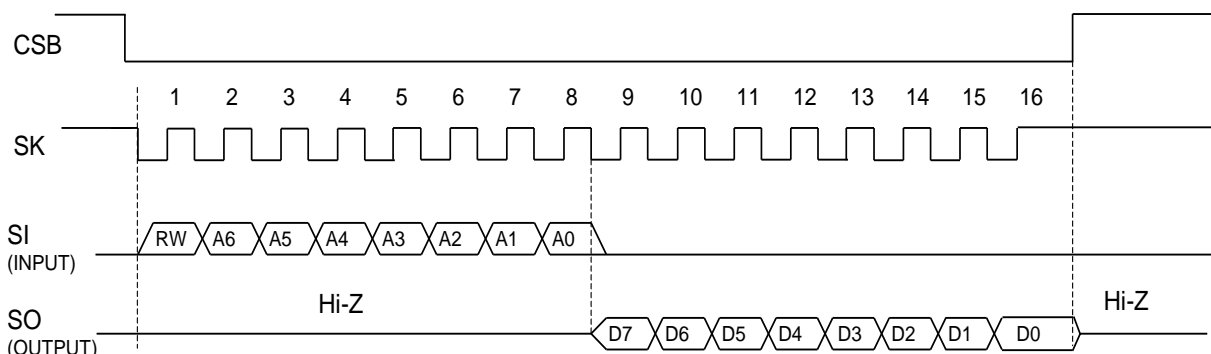


Figure 10.2 4-wire SPI Reading Data

## 10.2. I<sup>2</sup>C Bus Interface

The I<sup>2</sup>C bus interface of AK09915D supports the Standard mode (100 kHz max.), the Fast mode (400 kHz max.), and High-speed mode (Hs-mode, 2.5 MHz max.).

### 10.2.1. Data Transfer

To access AK09915D on the bus, generate a start condition first.

Next, transmit a one-byte slave address including a device address. At this time, AK09915D compares the slave address with its own address. If these addresses match, AK09915D generates an acknowledgement, and then executes READ or WRITE instruction. At the end of instruction execution, generate a stop condition.

**10.2.1.1. Change of Data**

A change of data on the SDA line must be made during “Low” period of the clock on the SCL line. When the clock signal on the SCL line is “High”, the state of the SDA line must be stable. (Data on the SDA line can be changed only when the clock signal on the SCL line is “Low”.)

During the SCL line is “High”, the state of data on the SDA line is changed only when a start condition or a stop condition is generated.

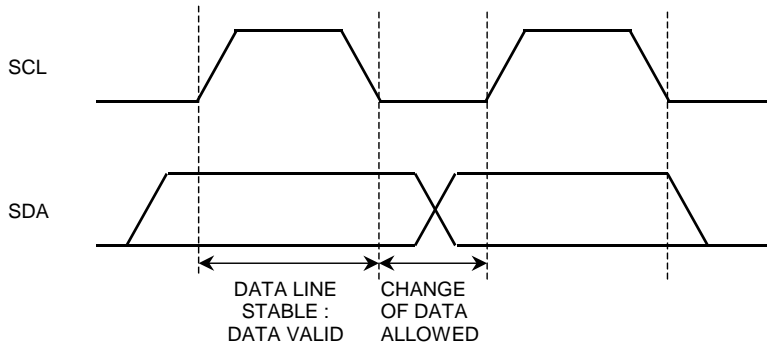


Figure 10.3 Data Change

**10.2.1.2. Start/Stop Condition**

If the SDA line is driven to “Low” from “High” when the SCL line is “High”, a start condition is generated. Every instruction starts with a start condition.

If the SDA line is driven to “High” from “Low” when the SCL line is “High”, a stop condition is generated. Every instruction stops with a stop condition.

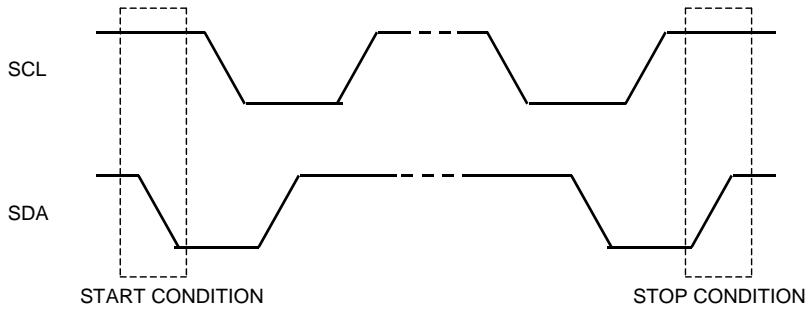


Figure 10.4 Start and Stop Condition



**10.2.1.3. Acknowledge**

The IC that is transmitting data releases the SDA line (in the “High” state) after sending 1-byte data. The IC that receives the data drives the SDA line to “Low” on the next clock pulse. This operation is referred as acknowledge. With this operation, whether data has been transferred successfully can be checked. AK09915D generates an acknowledge after reception of a start condition and slave address. When a WRITE instruction is executed, AK09915D generates an acknowledge after every byte is received. When a READ instruction is executed, AK09915D generates an acknowledge then transfers the data stored at the specified address. Next, AK09915D releases the SDA line then monitors the SDA line. If a master IC generates an acknowledge instead of a stop condition, AK09915D transmits the 8-bit data stored at the next address. If no acknowledge is generated, AK09915D stops data transmission.

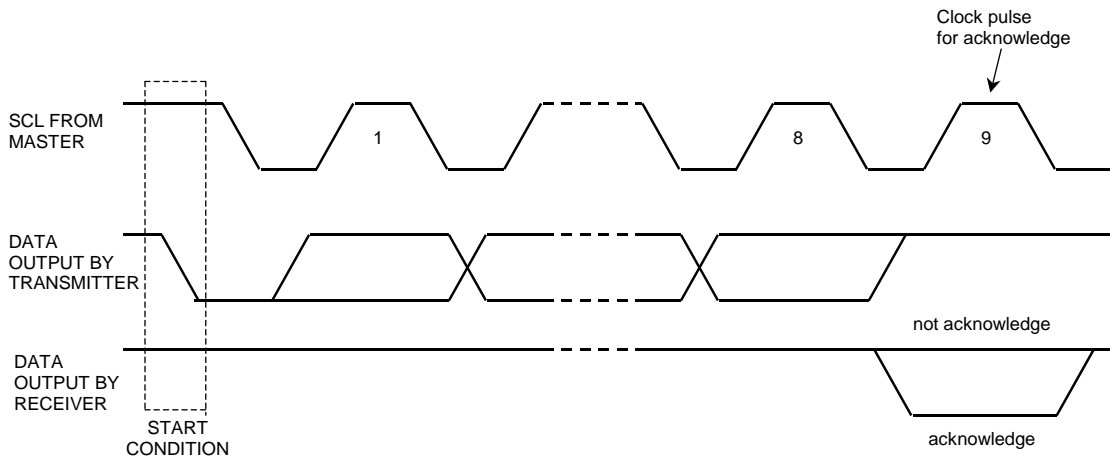


Figure 10.5 Generation of Acknowledge

**10.2.1.4. Slave Address**

The slave address of AK09915D can be selected from the following list by setting CAD0/1 pin. When CAD pin is fixed to VSS, the corresponding slave address bit is “0”. When CAD pin is fixed to VDD, the corresponding slave address bit is “1”.

Table 10.1 Slave Address and CAD0/1 pin

CAD1	CAD0	Slave Address
0	0	0Ch
0	1	0Dh
1	0	0Eh
1	1	0Fh

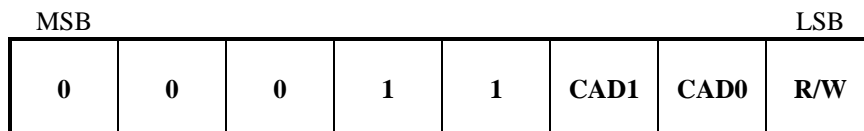


Figure 10.6 Slave Address

The first byte including a slave address is transmitted after a start condition, and an IC to be accessed is selected from the ICs on the bus according to the slave address. When a slave address is transferred, the IC whose device address matches the transferred slave address generates an acknowledge then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit. When the R/W bit is set to “1”, READ instruction is executed. When the R/W bit is set to “0”, WRITE instruction is executed.

**10.2.2.WRITE Instruction**

When the R/W bit is set to “0”, AK09915D performs write operation.

In write operation, AK09915D generates an acknowledge after receiving a start condition and the first byte (slave address) then receives the second byte. The second byte is used to specify the address of an internal control register and is based on the MSB-first configuration.

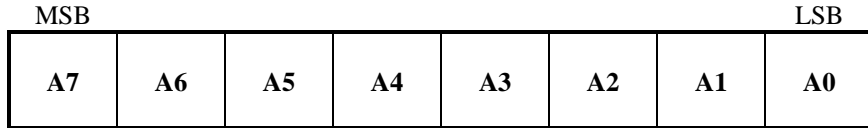


Figure 10.7 Register Address

After receiving the second byte (register address), AK09915D generates an acknowledge then receives the third byte.

The third and the following bytes represent control data. Control data consists of 8-bit and is based on the MSB-first configuration. AK09915D generates an acknowledge after every byte is received. Data transfer always stops with a stop condition generated by the master.

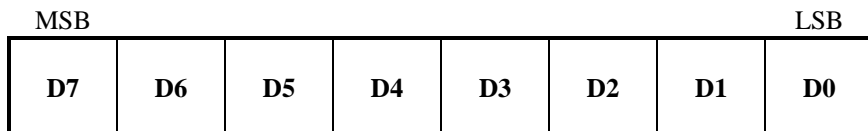


Figure 10.8 Control Data

AK09915D can write multiple bytes of data at a time.

After reception of the third byte (control data), AK09915D generates an acknowledge then receives the next data. If additional data is received instead of a stop condition after receiving one byte of data, the address counter inside the LSI chip is automatically incremented and the data is written at the next address.

The address is incremented from 00h to 18h from 30h to 32h, or from 60h to 62h. When the address is between 00h and 18h, in case that FIFO function is disabled, the address is incremented 00h → 01h → 02h → 03h → 10h → 11h ... → 18h, and the address goes back to 00h after 18h. In case that FIFO function is enabled, the address is incremented 00h → 01h → 02h → 03h → 10h → 11h ... → 18h, and the address goes back to 11h after 18h. When the address is between 30h and 32h, the address goes back to 30h after 32h. When the address is between 30h and 32h, the address goes back to 30h after 32h.

Actual data is written only to Read/Write registers (Table 11.2)

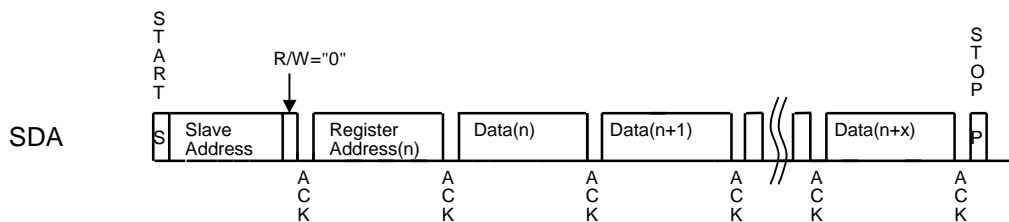


Figure 10.9 WRITE Instruction

**10.2.3.READ Instruction**

When the R/W bit is set to “1”, AK09915D performs read operation.

If a master IC generates an acknowledge instead of a stop condition after AK09915D transfers the data at a specified address, the data at the next address can be read.

Address can be 00h to 18h, 30h to 32h, or 60h to 62h. When the address is between 00h and 18h, in case that FIFO function is disabled, the address is incremented 00h → 01h → 02h → 03h → 10h → 11h ... → 18h, and the address goes back to 00h after 18h. In case that FIFO function is enabled, the address is incremented 00h → 01h → 02h → 03h → 10h → 11h ... → 18h, and the address goes back to 11h after 18h. When the address

is between 30h and 32h, the address goes back to 30h after 32h. When the address is between 60h and 62h, the address goes back to 60h after 62h.

AK09915D supports current address read and random address read..

### 10.2.3.1. Current Address Read

AK09915D has an address counter inside the LSI chip. In current address read operation, the data at an address specified by this counter is read.

The internal address counter holds the next address of the most recently accessed address.

For example, if the address most recently accessed (for READ instruction) is address “n”, and a current address read operation is attempted, the data at address “n+1” is read.

In current address read operation, AK09915D generates an acknowledge after receiving a slave address for the READ instruction (R/W bit = “1”). Next, AK09915D transfers the data specified by the internal address counter starting with the next clock pulse, then increments the internal counter by one. If the master IC generates a stop condition instead of an acknowledge after AK09915D transmits one byte of data, the read operation stops.

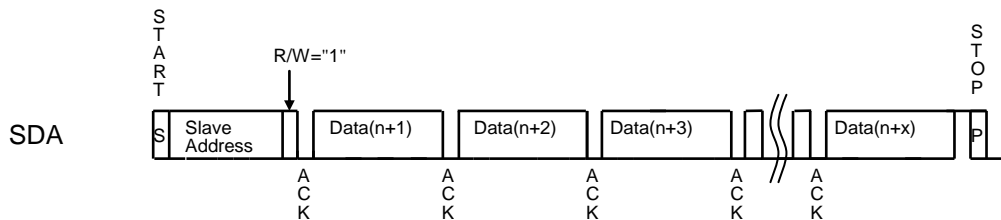


Figure 10.10 Current Address READ

### 10.2.3.2. Random Address Read

By random address read operation, data at an arbitrary address can be read.

The random address read operation requires to execute WRITE instruction as dummy before a slave address for the READ instruction (R/W bit = “1”) is transmitted. In random read operation, a start condition is first generated then a slave address for the WRITE instruction (R/W bit = “0”) and a read address are transmitted sequentially.

After AK09915D generates an acknowledge in response to this address transmission, a start condition and a slave address for the READ instruction (R/W bit = “1”) are generated again. AK09915D generates an acknowledge in response to this slave address transmission. Next, AK09915D transfers the data at the specified address then increments the internal address counter by one. If the master IC generates a stop condition instead of an acknowledge after data is transferred, the read operation stops.

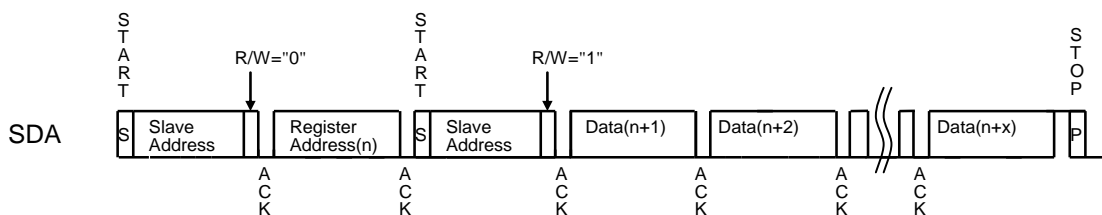


Figure 10.11 Random Address READ

**10.2.4.High-speed Mode (Hs-mode)**

AK09915D supports the Hs-mode.

Hs-mode can only commence after the following conditions (all of which are in Fast/Standard-mode):

- START condition (S)
- 8-bit master code (00001XXX)
- not-acknowledge bit ( $\bar{A}$ )

The diagram below shows data flow of the Hs-mode.

After start condition, feed master code 00001XXX for transfer to the Hs-mode. And then AK09915D feeds back not-acknowledge bit and switch over to circuit for the Hs-mode between times  $t_1$  and  $t_H$ . AK09915D can communicate at the Hs-mode from next START condition. At time  $t_{FS}$ , AK09915D switches its internal circuit from the Hs-mode to the First mode with the STOP condition (P). This transfer completes in the bus free time ( $t_{BUF}$ ).

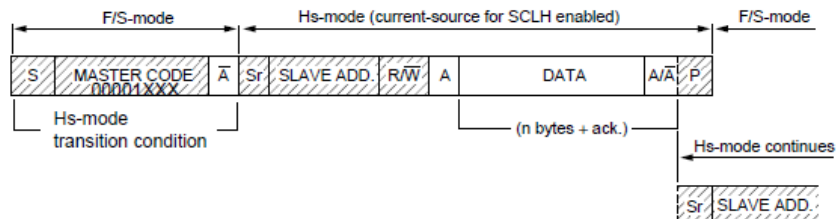


Figure 10.12 Data transfer format in Hs-mode

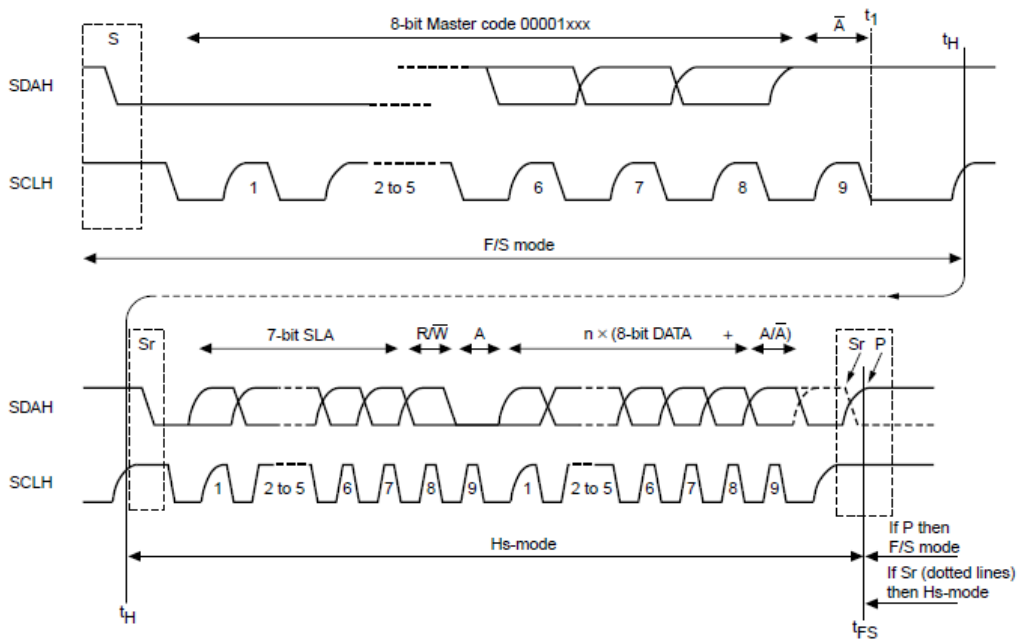


Figure 10.13 Hs-mode transfer

<b>11. Registers</b>
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**11.1. Description of Registers**

AK09915D has registers of 29 addresses as indicated in Table 11.1. Every address consists of 8-bit data. Data is transferred to or received from the external CPU via the serial interface described previously.

Table 11.1 Register Table

Name	Address	READ/ WRITE	Description	Bit width	Remarks
WIA1	00h	READ	Company ID	8	
WIA2	01h	READ	Device ID	8	
RSV	02h	READ	Reserved	8	
INFO	03h	READ	Information	8	
ST1	10h	READ	Status 1	8	Data status
HXL	11h	READ	Measurement Magnetic Data	8	X-axis data
HXH	12h	READ		8	
HYL	13h	READ		8	Y-axis data
HYH	14h	READ		8	
HZL	15h	READ		8	Z-axis data
HZH	16h	READ		8	
TMPS	17h	READ	Dummy	8	Dummy
ST2	18h	READ	Status 2	8	Data status
CNTL1	30h	READ/WRITE	Control 1	8	Control settings
CNTL2	31h	READ/WRITE	Control 2	8	Control settings
CNTL3	32h	READ/WRITE	Control 3	8	Control settings
TS1	33h	READ/WRITE	Test	8	DO NOT ACCESS
TS2	34h	READ/WRITE	Test	8	DO NOT ACCESS
TS3	35h	READ/WRITE	Test	8	DO NOT ACCESS
I2CDIS	36h	READ/WRITE	I <sup>2</sup> C disable	8	
TS4	37h	READ/WRITE	Test	8	DO NOT ACCESS
ASAX	60h	READ	Dummy	8	Dummy
ASAY	61h	READ	Dummy	8	Dummy
ASAZ	62h	READ	Dummy	8	Dummy
TPH1	C0h	READ/WRITE	Test	8	DO NOT ACCESS
TPH2	C1h	READ/WRITE	Test	8	DO NOT ACCESS
RR	C2h	READ/WRITE	Test	8	DO NOT ACCESS
SYT	C3h	READ/WRITE	Test	8	DO NOT ACCESS
DT	C4h	READ/WRITE	Test	8	DO NOT ACCESS

Addresses 00h to 18h, 30h to 32h and 60h to 62h are compliant with automatic increment function of serial interface respectively. When the address is in 00h to 18h, in case that FIFO function is disabled, the address is incremented 00h → 01h → 02h → 03h → 10h → 11h ... → 18h, and the address goes back to 00h after 18h. In case that FIFO function is enabled, the address is incremented 00h → 01h → 02h → 03h → 10h → 11h ... → 18h, and the address goes back to 11h after 18h. When the address is in 30h to 32h, the address goes back to 30h after 32h. When the address is in 60h to 62h, the address goes back to 60h after 62h.

## 11.2. Register Map

Table 11.2 Register Map

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
00h	WIA1	0	1	0	0	1	0	0	0
01h	WIA2	0	0	0	1	0	0	0	0
02h	RSV	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
03h	INFO	0	0	0	0	0	0	0	0
10h	ST1	HSM	0	0	0	0	0	DOR	DRDY
11h	HXL	HX7	HX6	HX5	HX4	HX3	HX2	HX1	HX0
12h	HXH	HX15	HX14	HX13	HX12	HX11	HX10	HX9	HX8
13h	HYL	HY7	HY6	HY5	HY4	HY3	HY2	HY1	HY0
14h	HYH	HY15	HY14	HY13	HY12	HY11	HY10	HY9	HY8
15h	HZL	HZ7	HZ6	HZ5	HZ4	HZ3	HZ2	HZ1	HZ0
16h	HZH	HZ15	HZ14	HZ13	HZ12	HZ11	HZ10	HZ9	HZ8
17h	TMPS	0	0	0	0	0	0	0	0
18h	ST2	0	0	0	0	HOFL	INV	0	0
Read/Write register									
30h	CNTL1	0	0	NSF	WM4	WM3	WM2	WM1	WM0
31h	CNTL2	FIFO	SDR	0	MODE4	MODE3	MODE2	MODE1	MODE0
32h	CNTL3	0	0	0	0	0	0	0	SRST
33h	TS1	-	-	-	-	-	-	-	-
34h	TS2	-	-	-	-	-	-	-	-
35h	TS3	-	-	-	-	-	-	-	-
36h	I2CDIS	I2CDIS7	I2CDIS6	I2CDIS5	I2CDIS4	I2CDIS3	I2CDIS2	I2CDIS1	I2CDIS0
37h	TS4	-	-	-	-	-	-	-	-
Read-only register									
60h	ASAX	1	0	0	0	0	0	0	0
61h	ASAY	1	0	0	0	0	0	0	0
62h	ASAZ	1	0	0	0	0	0	0	0
Read/Write register									
C0h	TPH1	-	-	-	-	-	-	-	-
C1h	TPH2	-	-	-	-	-	-	-	-
C2h	RR	-	-	-	-	-	-	-	-
C3h	SYT	-	-	-	-	-	-	-	-
C4h	DT	-	-	-	-	-	-	-	-

When VDD is turned ON, POR function works and all registers of AK09915D are initialized regardless of VID status. To write data to or to read data from register, VID must be ON.

TS1, TS2, TS3, TS4, TPH1, TPH2, RR, SYT and DT are test register for shipment test. Do not access these registers.

### 11.3. Detailed Description of Registers

#### 11.3.1.WIA: Who I Am

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
00h	WIA1	0	1	0	0	1	0	0	0
01h	WIA2	0	0	0	1	0	0	0	0

WIA1[7:0] bits: Company ID of AKM. It is described in one byte and fixed value.

48h: fixed

WIA2[7:0] bits: Device ID of AK09915D. It is described in one byte and fixed value.

10h: fixed

#### 11.3.2.RSV: Reserved

Addr.	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
02h	RSV	RSV17	RSV16	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10

RSV[7:0] bits: Reserved register for AKM.

#### 11.3.3.INFO: Information

Addr.	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
03h	INFO	0	0	0	0	0	0	1	0

INFO[7:0] bits: Administrative information of AKM. It is described in one byte and fixed value.

02h: fixed

#### 11.3.4.ST1: Status 1

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
10h	ST1	HSM	0	0	0	0	0	DOR	DRDY
Reset		0	0	0	0	0	0	0	0

DRDY bit: Data Ready

“0”: Normal

“1”: Data is ready

When FIFO is disabled (FIFO bit = “0”);

DRDY bit turns to “1” when data is ready in Single measurement mode, Continuous measurement mode 1, 2, 3, 4, 5, 6 or Self-test mode. It returns to “0” when any one of ST2 register or measurement data register (HXL to TMPS) is read. When DRDY bit turn to “1”, ODDRDY pin is “L”. When DRDY bit turn to “0”, ODDRDY pin is “H”

When FIFO is enabled (FIFO bit = “1”);

If the number of stored data set is equal to or more than the number set to WM[4:0] bits, DRDY bit turns to “1”. If the number of stored data set is less than the number set to WM[4:0] bits, DRDY bit turns to “0”. When DRDY bit turn to “1”, ODDRDY pin is “L”. When DRDY bit turn to “0”, ODDRDY pin is “H”

DOR bit: Data Overrun

“0”: Normal

“1”: Data overrun

When FIFO is disabled (FIFO bit = “0”);

DOR bit turns to “1” when data has been skipped in Continuous measurement mode 1, 2, 3, 4, 5 or 6. It returns to “0” when any one of ST2 register or measurement data register (HXL to TMPS) is read.

When FIFO is enabled (FIFO bit = “1”);

If a set of new data is measured when the buffer is full, DOR bit turns to “1”. If at least one data set is read from the buffer, DOR bit turns to “0”.

HSM bit: I<sup>2</sup>C Hs-mode

“0”: Standard/Fast mode

“1”: Hs-mode

HSM bit turns to “1” when I<sup>2</sup>C bus interface is changed from Standard or Fast mode to High-speed mode (Hs-mode).

### 11.3.5.HXL to HZH: Measurement magnetic data

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
11h	HXL	HX7	HX6	HX5	HX4	HX3	HX2	HX1	HX0
12h	HXH	HX15	HX14	HX13	HX12	HX11	HX10	HX9	HX8
13h	HYL	HY7	HY6	HY5	HY4	HY3	HY2	HY1	HY0
14h	HYH	HY15	HY14	HY13	HY12	HY11	HY10	HY9	HY8
15h	HZL	HZ7	HZ6	HZ5	HZ4	HZ3	HZ2	HZ1	HZ0
16h	HZH	HZ15	HZ14	HZ13	HZ12	HZ11	HZ10	HZ9	HZ8
Reset		0	0	0	0	0	0	0	0

Measurement data of magnetic sensor X-axis/Y-axis/Z-axis

HXL[7:0] bits: X-axis measurement data lower 8-bit

HXH[15:8] bits: X-axis measurement data higher 8-bit

HYL[7:0] bits: Y-axis measurement data lower 8-bit

HYH[15:8] bits: Y-axis measurement data higher 8-bit

HZL[7:0] bits: Z-axis measurement data lower 8-bit

HZH[15:8] bits: Z-axis measurement data higher 8-bit



Measurement data is stored in two's complement and Little Endian format. Measurement range of each axis is -32752 to 32752 in 16-bit output.

Table 11.3 Measurement magnetic data format

Measurement data (each axis) [15:0] bits			Magnetic flux density [ $\mu$ T]
Two's complement	Hex	Decimal	
0111 1111 1111 0000	7FF0	32752	4912(max.)
0000 0000 0000 0001	0001	1	0.15
0000 0000 0000 0000	0000	0	0
1111 1111 1111 1111	FFFF	-1	-0.15
1000 0000 0001 0000	8010	-32752	-4912(min.)

When FIFO is enabled (FIFO bit = "1");

By accessing HXL register, the oldest data set is passed to the read register from the buffer. Reading ST2 register is regarded as the finish of reading out one set of data. Then the read data set is deleted and the next oldest data set will be ready to be read. If ST2 register or HXL register is not read, the same set of data is kept in the read register. When reading out data, always start with HXL register and finish with ST2 register.

### 11.3.6. TMPS: Dummy

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
17h	TMPS	0	0	0	0	0	0	0	0
Reset		0	0	0	0	0	0	0	0

TMPS[7:0] bits: Dummy register

### 11.3.7. ST2: Status 2

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
18h	ST2	0	0	0	0	HOFL	INV	0	0
Reset		0	0	0	0	0	0	0	0

HOFL bit: Magnetic sensor overflow

"0": Normal

"1": Magnetic sensor overflow occurred

In Single measurement mode, Continuous measurement modes (1 to 6) and Self-test mode, magnetic sensor may overflow even though measurement data registers are not saturated. In this case, measurement data is not correct and HOFL bit turns to "1". When measurement data register (HXL to HZH) is updated, HOFL bit is updated. Refer to 9.4.3.6 for detailed information.

INV bit: Invalid data

“0”: Normal

“1”: Data is invalid

INV bit functions only when FIFO is enabled (FIFO bit = “1”). If data is read out when there is no data set in the buffer, INV bit is turned to “1” and measurement data registers (HXL to HZH) are forced to fixed value 7FFFh. If a set of new data is measured, INV bit turns to “0”.

When FIFO is disabled (FIFO bit = “0”);

ST2 register has a role as data reading end register, also. When any of measurement data register (HXL to TMPS) is read in Continuous measurement modes (1 to 6), it means data reading start and taken as data reading until ST2 register is read. Therefore, when any of measurement data is read, be sure to read ST2 register at the end.

When FIFO is enabled (FIFO bit = “1”);

ST2 register is a part of one set of data stored in the buffer. If any of data register (HXL to TMPS) is read, be sure to read ST2 register at the end. If read data set includes magnetic sensor over flow, HOFL bit is “1”. If there is no data set in the buffer, INV bit is “1”.

### 11.3.8.CNTL1: Control 1

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
30h	CNTL1	0	0	NSF	WM4	WM3	WM2	WM1	WM0
Reset		0	0	0	0	0	0	0	0

NSF bit : Noise suppression filter setting

“0”: disable

“1”: enable

Output data from magnetic sensor is filtered to suppress the noise according to the setting. Refer to 9.5 for detailed information.

Do not write “1” in D6 register.

WM[4:0] bits: Watermark level setting

“00000”: 1 step

“00001”: 2 steps

“00010”: 3 steps

|

“11111”: 32 steps (upper limit)

Watermark level can be set every 1 step. The upper limit of watermark level is 32 steps (WM[4:0] bits = “11111”).

It is prohibited to change WM[4:0] bits in any other modes than Power-down mode.

**11.3.9. CNTL2: Control 2**

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
31h	CNTL2	FIFO	SDR	0	MODE4	MODE3	MODE2	MODE1	MODE0
Reset		0	0	0	0	0	0	0	0

MODE[4:0] bits: Operation mode setting

“00000”: Power-down mode

“00001”: Single measurement mode

“00010”: Continuous measurement mode 1

“00100”: Continuous measurement mode 2

“00110”: Continuous measurement mode 3

“01000”: Continuous measurement mode 4

“01010”: Continuous measurement mode 5

“01100”: Continuous measurement mode 6

“10000”: Self-test mode

When each mode is set, AK09915D transits to the set mode. Refer to 9.3 for detailed information. If other value is set, AK09915D transits to power-down mode automatically.

SDR bit: Sensor drive setting

“0”: Low power drive

“1”: Low noise drive

Default SDR bit is Low power drive (SDR bit = “0”). By writing “1” to SDR bit, AK09915D is switched from Low power drive to Low noise drive.

FIFO bit: FIFO setting

“0”: disable

“1”: enable

By writing “1” to FIFO bit, FIFO function is enabled. By writing “0”, FIFO function is disabled and the buffer is cleared at the same time. FIFO function is available only in Continuous measurement mode. It is prohibited to enable it other than Continuous measurement mode

**11.3.10. CNTL3: Control 3**

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
32h	CNTL3	0	0	0	0	0	0	0	SRST
Reset		0	0	0	0	0	0	0	0

SRST bit: Soft reset

“0”: Normal

“1”: Reset

When “1” is set, all registers are initialized. After reset, SRST bit turns to “0” automatically.

**11.3.11. TS1, TS2, TS3: Test**

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
33h	TS1	-	-	-	-	-	-	-	-
34h	TS2	-	-	-	-	-	-	-	-
35h	TS3	-	-	-	-	-	-	-	-
Reset		0	0	0	0	0	0	0	0

TS1, TS2 and TS3 registers are AKM internal test registers. Do not access these registers.

**11.3.12. I2CDIS: I<sup>2</sup>C Disable**

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
36h	I2CDIS	I2CDIS7	I2CDIS6	I2CDIS5	I2CDIS4	I2CDIS3	I2CDIS2	I2CDIS1	I2CDIS0
Reset		0	0	0	0	0	0	0	0

This register disables I<sup>2</sup>C bus interface. I<sup>2</sup>C bus interface is enabled in default. To disable I<sup>2</sup>C bus interface, write “00011011” to I2CDIS[7:0] bits. Then I<sup>2</sup>C bus interface is disabled. Once I<sup>2</sup>C bus interface is disabled, it is impossible to write other value to I2CDIS register. To enable I<sup>2</sup>C bus interface, reset AK09915D or input start condition 8 times continuously.

**11.3.13. TS4: Test**

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
37h	TS4	-	-	-	-	-	-	-	-
Reset		0	0	0	0	0	0	0	0

TS4 register is test register for shipment test. Do not access this registers.

**11.3.14. ASAX,ASAY,ASAZ: Dummy**

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
60h	ASAX	1	0	0	0	0	0	0	0
61h	ASAY	1	0	0	0	0	0	0	0
62h	ASAZ	1	0	0	0	0	0	0	0
Reset		1	0	0	0	0	0	0	0

ASAX, ASAY and ASAZ registers are dummy registers for ensuring the compatibility with other AKM compass.

These registers are fixed value (80h).

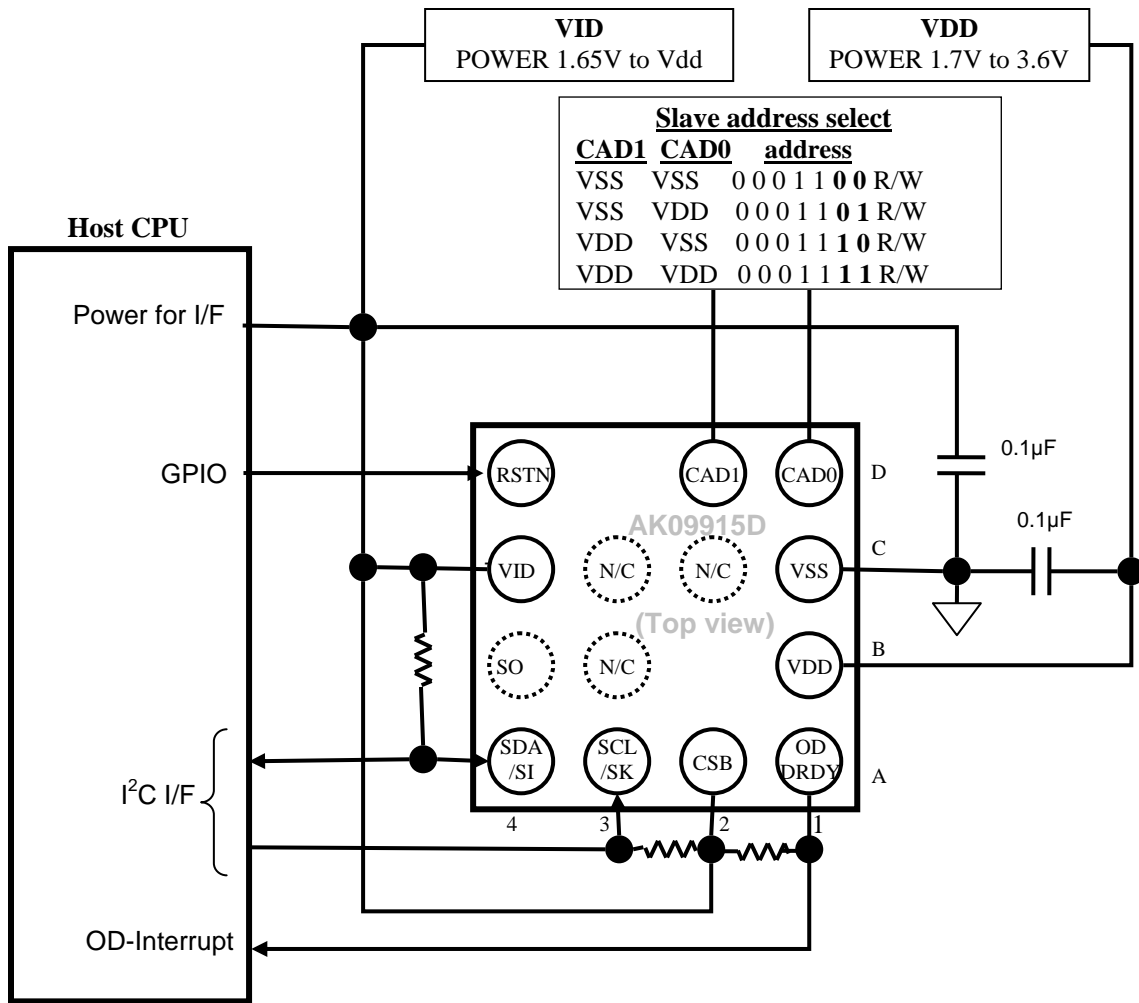
**11.3.15. TPH1,TPH2,RR,SYT,DT: Test**

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
C0h	TPH1	-	-	-	-	-	-	-	-
C1h	TPH2	-	-	-	-	-	-	-	-
C3h	SYT	-	-	-	-	-	-	-	-
C4h	DT	-	-	-	-	-	-	-	-
Reset		0	0	0	0	0	0	0	0
Ch2	RR	-	-	-	-	-	-	-	-
Reset		0	0	0	0	0	0	1	1

TPH1, TPH2, RR, SYT and DT registers are AKM internal test registers. Do not access these registers.

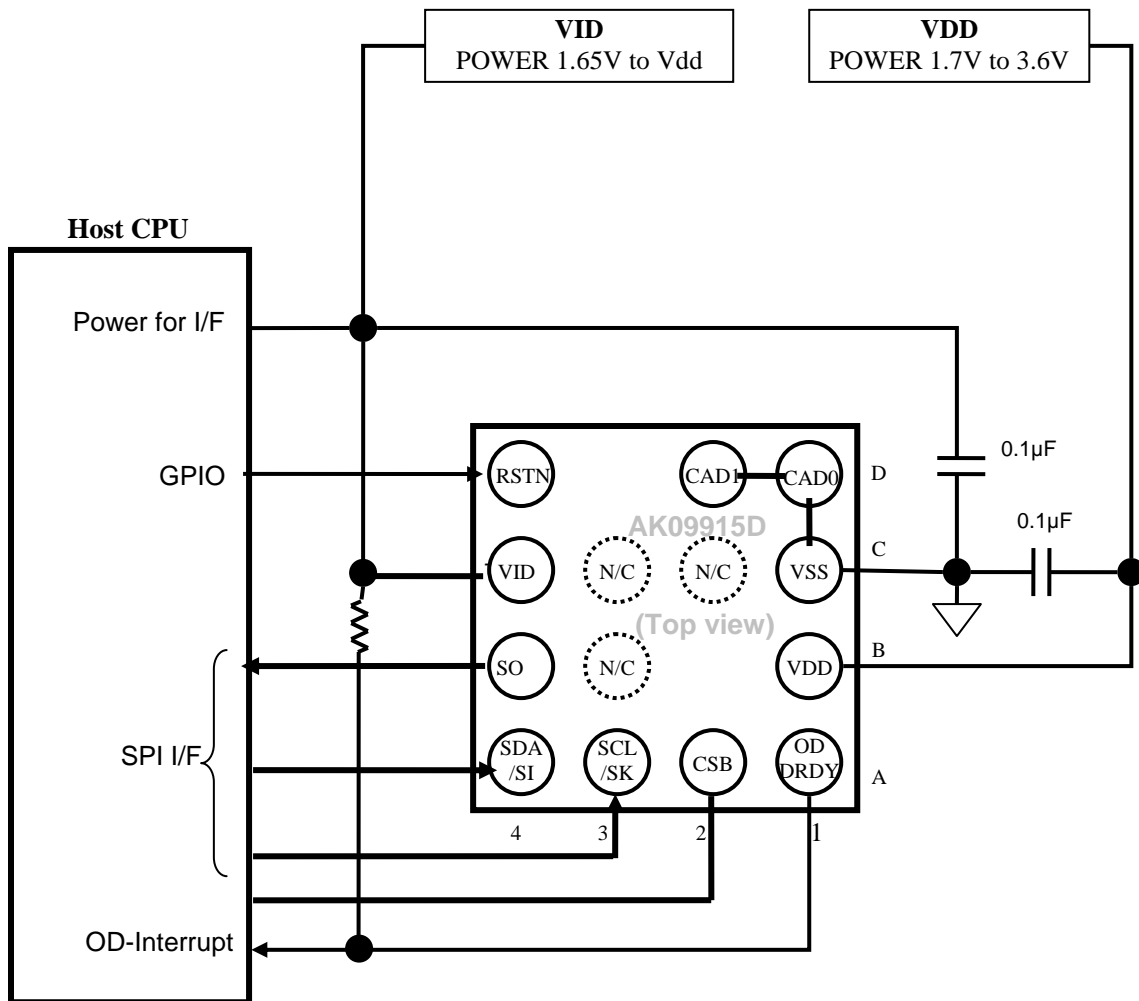
**12. Example of Recommended External Connection**

**12.1. I<sup>2</sup>C Bus Interface**



Pins of dot circle should be kept non-connected.

12.2. 4-wire SPI

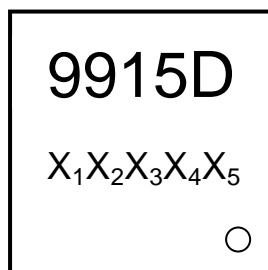


Pins of dot circle should be kept non-connected.

<b>13. Package</b>
--------------------

**13.1. Marking**

Product name: 9915D

Date code: X<sub>1</sub>X<sub>2</sub>X<sub>3</sub>X<sub>4</sub>X<sub>5</sub>X<sub>1</sub> = IDX<sub>2</sub> = Year codeX<sub>3</sub> = Month codeX<sub>4</sub>X<sub>5</sub> = Lot

&lt;Top view&gt;

**13.2. Pin Assignment**

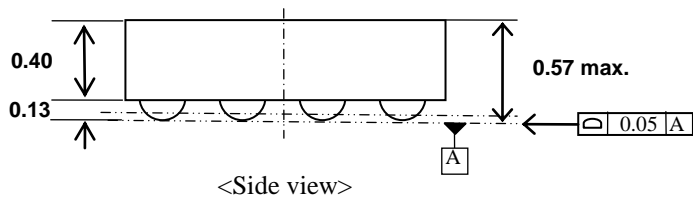
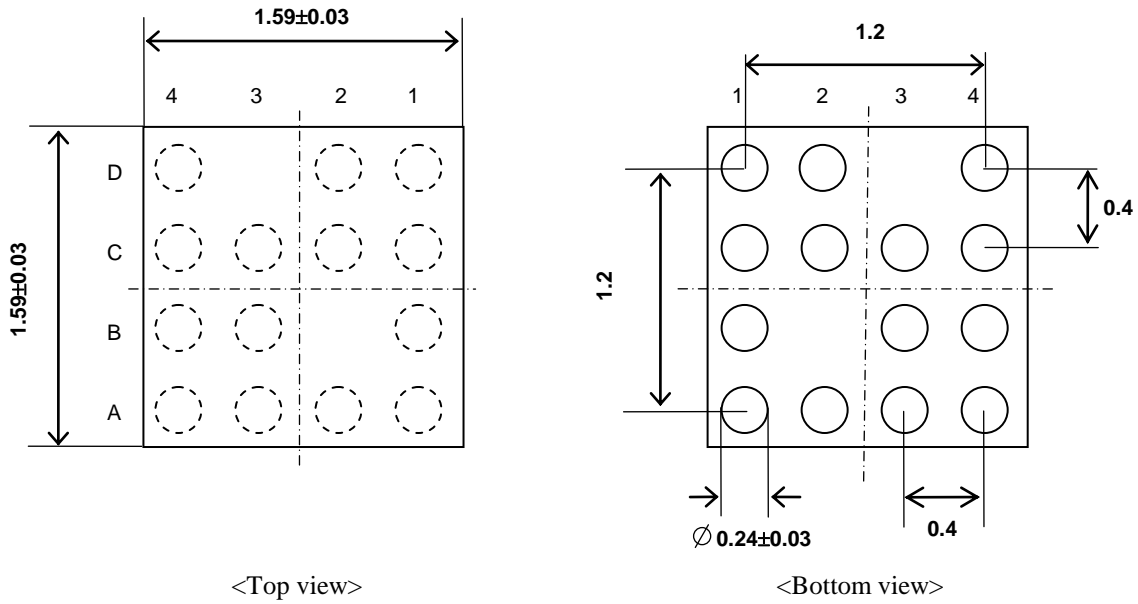
	4	3	2	1
D	RSTN	/	CAD1	CAD0
C	VID	N/C	N/C	VSS
B	SO	N/C	/	VDD
A	SDA/SI	SCL/SK	CSB	ODDRDY

&lt;Top view&gt;



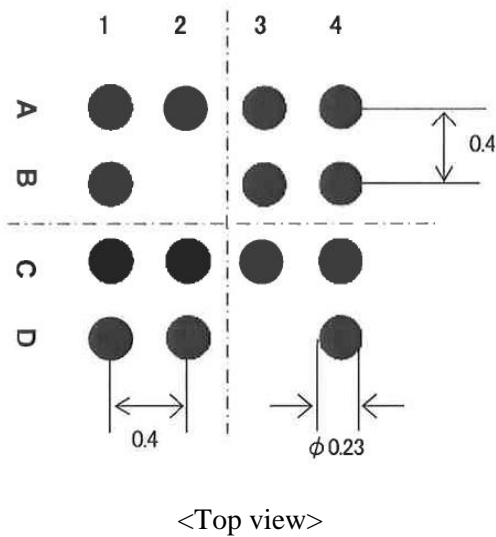
13.3. Outline Dimensions

[mm]



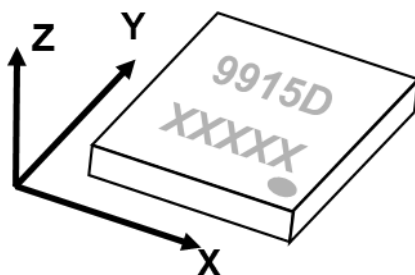
13.4. Recommended Foot Print Pattern

[mm]



**14. Relationship between the Magnetic Field and Output Code**

The measurement data increases as the magnetic flux density increases in the arrow directions.



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