MOSFETs Silicon N-channel MOS (U-MOSⅧ-H)

TK55S10N1

1. Applications

- Automotive
- Switching Voltage Regulators
- Motor Drivers

2. Features

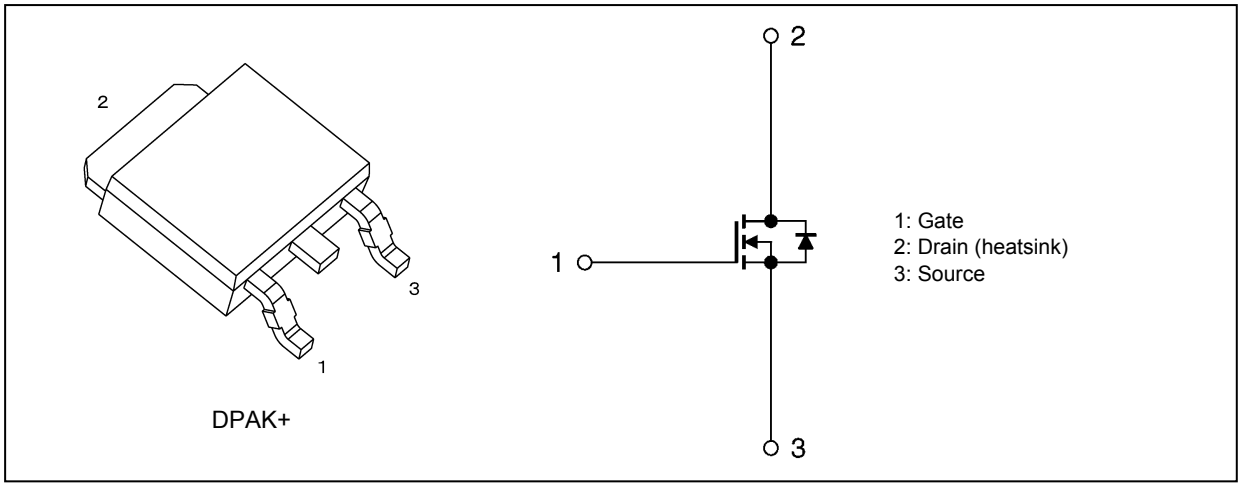
(1) AEC-Q101 qualified

(2) Low drain-source on-resistance: $R_{DS(ON)}$ = 5.5 mΩ (typ.) (V_{GS} = 10 V)

(3) Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 100 V)

(4) Enhancement mode: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_D = 0.5 mA)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) (T_a = 25°C unless otherwise specified)

Characteristics			Symbol	Rating	Unit
Drain-source voltage			V_{DSS}	100	V
Gate-source voltage			V_{GSS}	±20	
Drain current (DC)		(Note 1)	I_D	55	A
Drain current (pulsed)		(Note 1)	I_{DP}	165	
Power dissipation	(T_c = 25°C)	(Note 2)	P_D	157	W
Single-pulse avalanche energy		(Note 3)	E_{AS}	93	mJ
Single-pulse avalanche current			I_{AS}	55	A
Channel temperature		(Note 4)	T_{ch}	175	°C
Storage temperature		(Note 4)	T_{stg}	-55 to 175	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production
2013-02

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5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	0.95	°C/W

Note 1: Ensure that the channel temperature does not exceed 175°C.

Note 2: The power dissipation value is calculated based on the channel-to-case thermal resistance. However, the safe operating area is not only limited to thermal limits but also the current concentration phenomenon. This device should not be used under conditions outside its safe operating area shown herein.

Note 3: V_{DD} = 80 V, T_{ch} = 25°C (initial), L = 24 μH, R_G = 25 Ω, I_{AS} = 55 A

Note 4: The definitions of the absolute maximum channel and storage temperatures are qualified per AEC-Q101.

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

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6. Electrical Characteristics

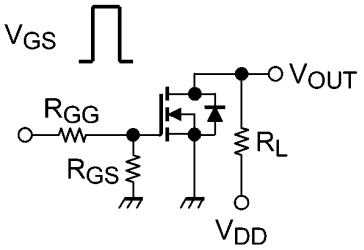
6.1. Static Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±1	μA
Drain cut-off current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	I_D = 10 mA, V_{GS} = 0 V	100	—	—	V
Drain-source breakdown voltage (Note 5)	$V_{(BR)DSX}$	I_D = 10 mA, V_{GS} = -20 V	65	—	—	
Gate threshold voltage	V_{th}	V_{DS} = 10 V, I_D = 0.5 mA	2.0	—	4.0	
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 27.5 A	—	5.5	6.5	mΩ

Note 5: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

6.2. Dynamic Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	3280	—	pF
Reverse transfer capacitance	C_{rss}		—	210	—	
Output capacitance	C_{oss}		—	1520	—	
Switching time (rise time)	t_r	See Figure 6.2.1.	—	11	—	ns
Switching time (turn-on time)	t_{on}		—	28	—	
Switching time (fall time)	t_f		—	19	—	
Switching time (turn-off time)	t_{off}		—	51	—	



V_{DD} ≈ 50 V
V_{GS} = 10 V/0 V
I_D = 16.5 A
R_L = 3 Ω
R_{GS} = 4.7 Ω
R_{GG} = 4.7 Ω
Duty ≤ 1 %, t_w = 10 μs

Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} ≈ 80 V, V_{GS} = 10 V, I_D = 55 A	—	49	—	nC
Gate-source charge 1	Q_{gs1}		—	15	—	
Gate-drain charge	Q_{gd}		—	14	—	

6.4. Source-Drain Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (DC) (Note 6)	I_{DR}	—	—	—	55	A
Reverse drain current (pulsed) (Note 6)	I_{DRP}		—	—	165	
Diode forward voltage	V_{DSF}	I_{DR} = 55 A, V_{GS} = 0 V	—	—	-1.2	V
Reverse recovery time (Note 7)	t_{rr}	I_{DR} = 55 A, V_{GS} = 0 V $-dI_{DR}/dt$ = 50 A/μs	—	75	—	ns
Reverse recovery charge (Note 7)	Q_{rr}		—	73	—	nC

Note 6: Ensure that the channel temperature does not exceed 175°C.
Note 7: Ensure that V_{DS} peak does not exceed V_{DSS}.

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7. Marking (Note)

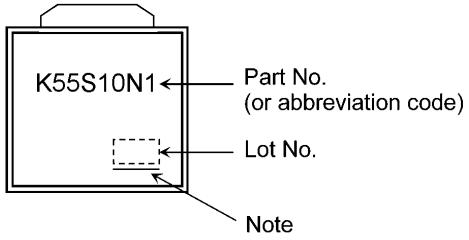


Fig. 7.1 Marking

Note: A line under a Lot No. identifies the indication of product Labels.
Not underlined: [[Pb]]/INCLUDES > MCV
Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]
Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.
The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

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8. Characteristics Curves (Note)

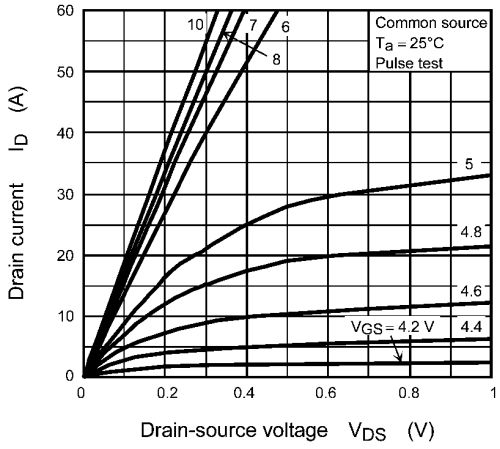


Fig. 8.1 I_D - V_{DS}

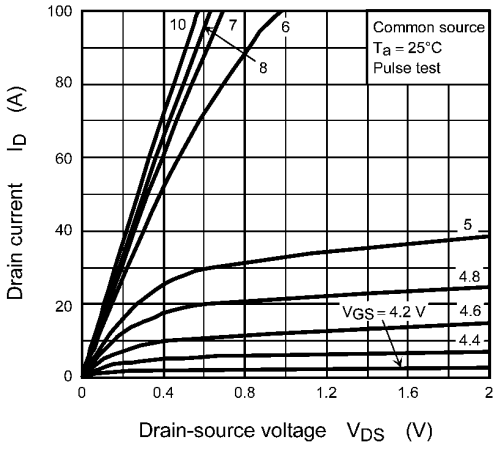


Fig. 8.2 I_D - V_{DS}

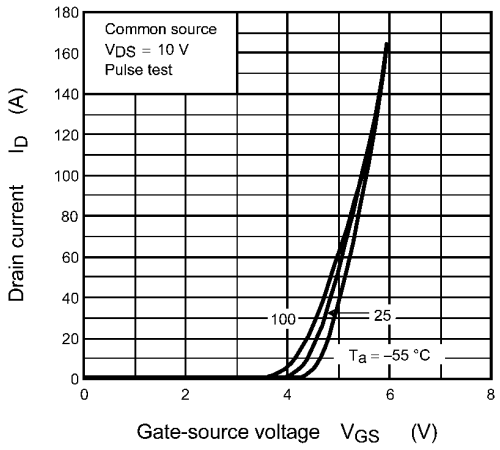


Fig. 8.3 I_D - V_{GS}

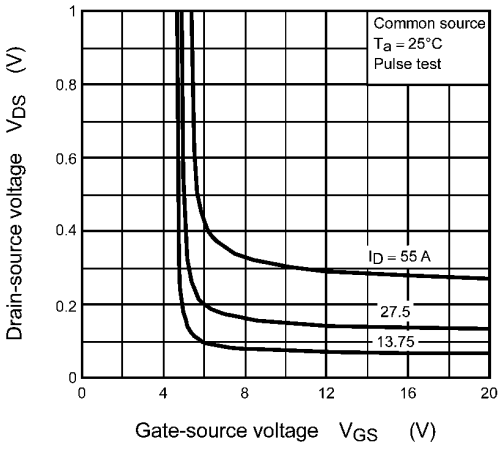


Fig. 8.4 V_{DS} - V_{GS}

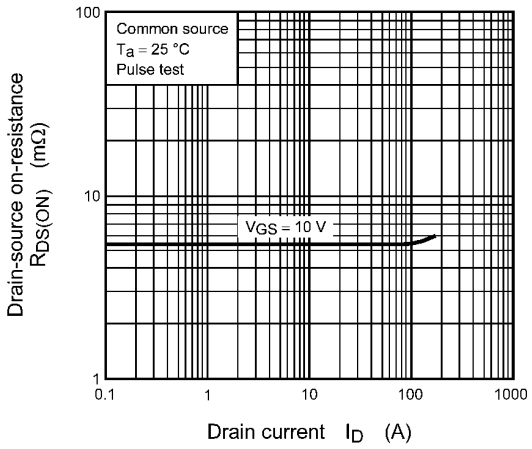


Fig. 8.5 $R_{DS(ON)}$ - I_D

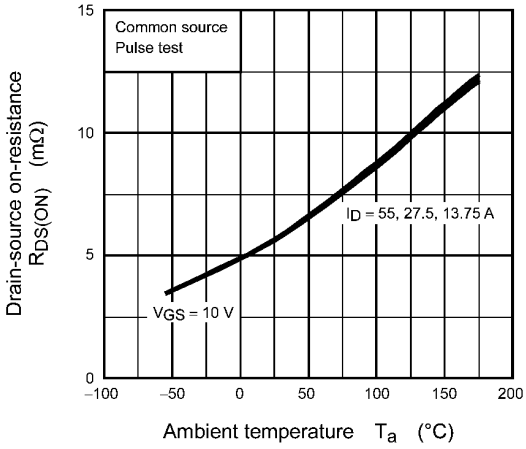


Fig. 8.6 $R_{DS(ON)}$ - T_a

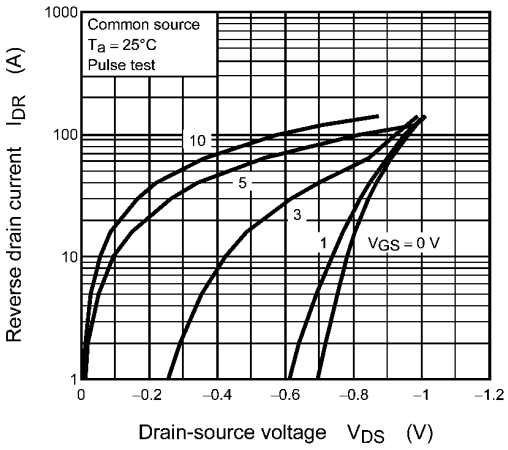


Fig. 8.7 I_{DR} - V_{DS}

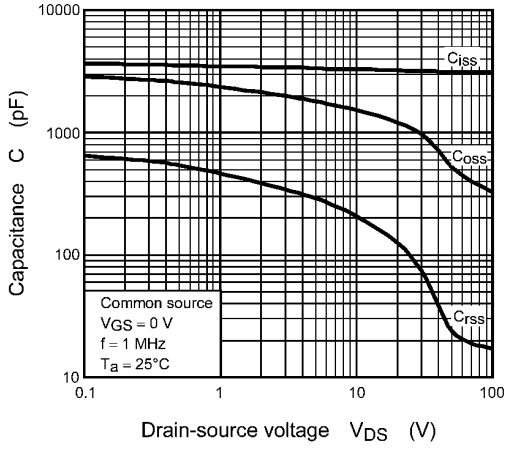


Fig. 8.8 Capacitance - V_{DS}

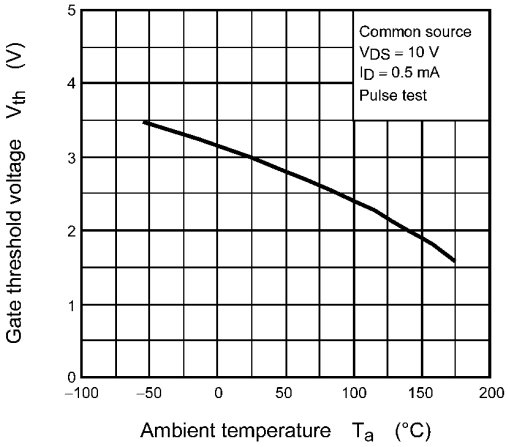


Fig. 8.9 V_{th} - T_a

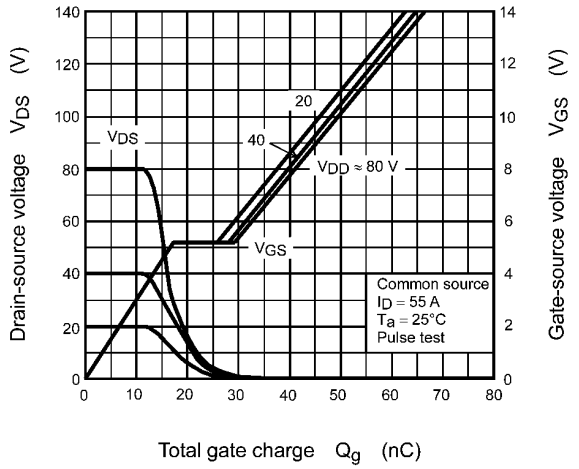


Fig. 8.10 Dynamic Input/Output Characteristics

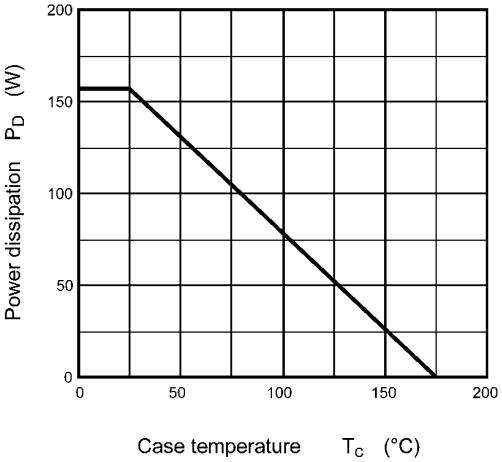


Fig. 8.11 P_D - T_c
(Guaranteed Maximum)

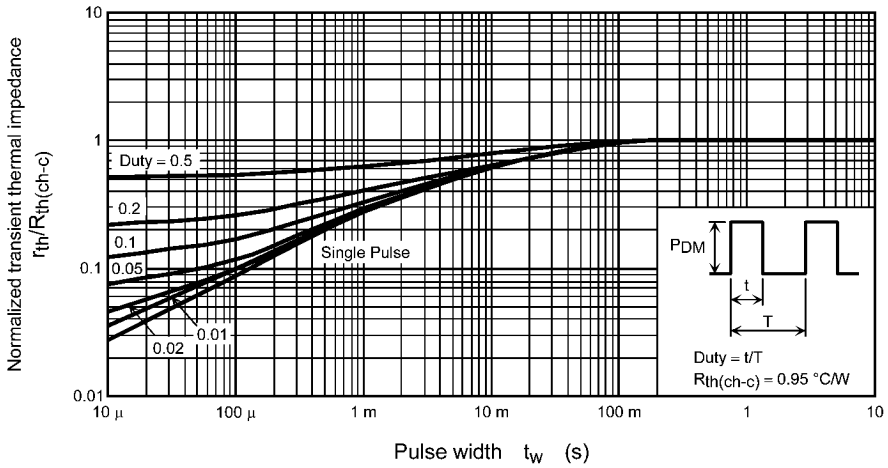


Fig. 8.12 $r_{th}/R_{th(ch-c)}$ - t_w (Guaranteed Maximum)

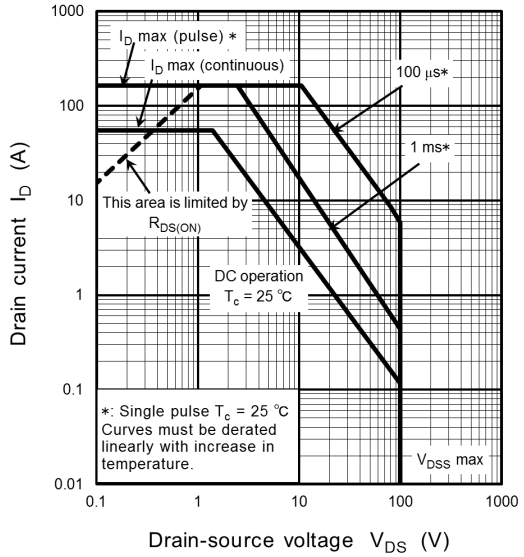


Fig. 8.13 Safe Operating Area (Guaranteed Maximum)

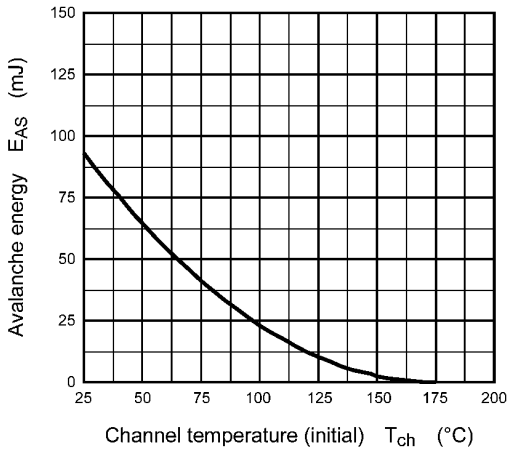
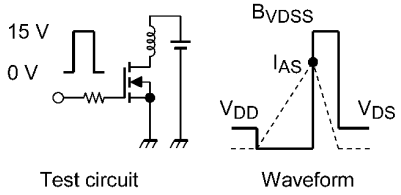


Fig. 8.14 E_{AS} - T_{ch} (Guaranteed Maximum)



$R_G = 25\ \Omega$
$V_{DD} = 80$ V, L = 24 μH

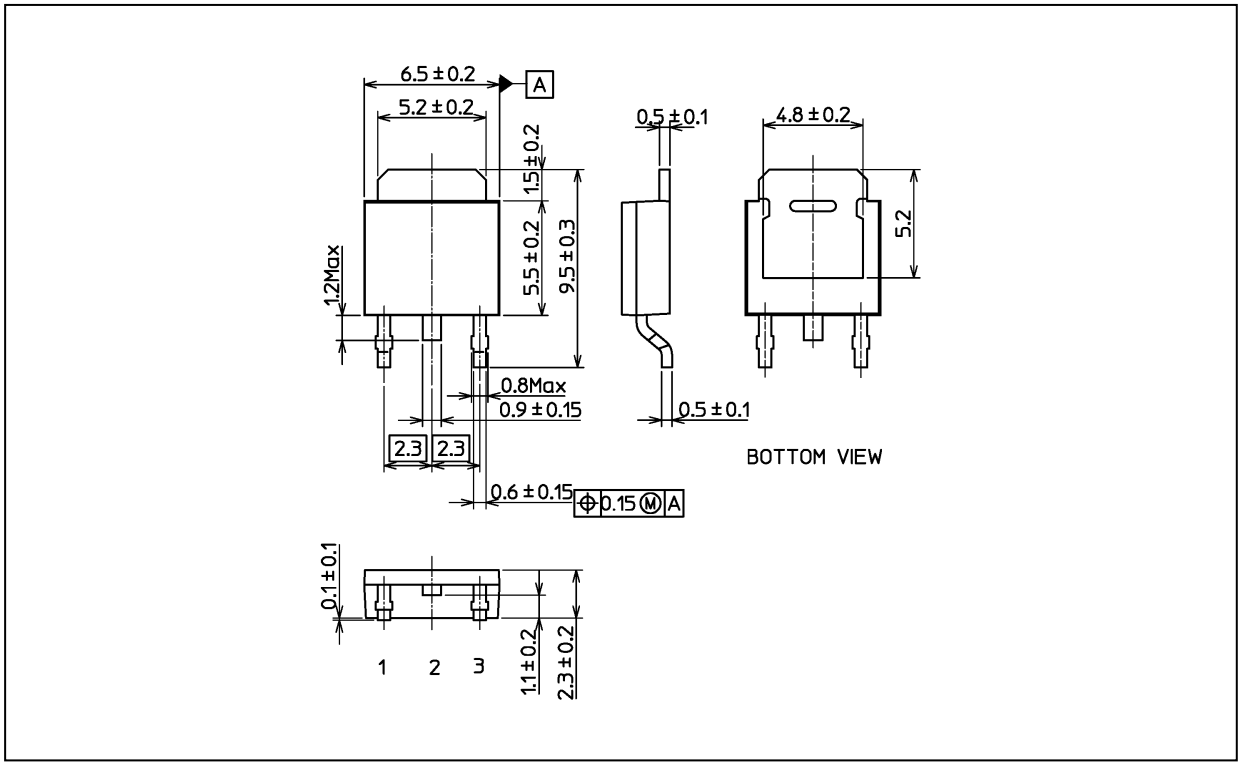
$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

Fig. 8.15 Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.36 g (typ.)

Package Name(s)
TOSHIBA: 2-7M1A
Nickname: DPAK+

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