TEXAS INSTRUMENTS

THS6182DWEVM

User's Guide

August 2003

High Performance Linear Products

SLOU152A

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Read This First

About This Manual

How to Use This Manual

This document contains the following chapters:

- ❑ Chapter 1 − Introduction and Description
- ❑ Chapter 2 − Using the THS6182DWEVM
- ❑ Chapter 3 − THS6182DWEVM Applications
- ❑ Chapter 4 − EVM Hardware Description

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

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Electrostatic Sensitive Components

This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, refer to SSYA008.

Related Documentation From Texas Instruments

The URL's below are correct as of the date of publication of this manual. Texas Instruments applications apologizes if they change over time.

- THS6182 data sheet (SLLLS544)
- Application report (SLMA002), *PowerPAD Thermally Enhanced Package*, http://www−s.ti.com/sc/psheets/slma004/slma002.pdf
- Application report (SLMA004), *PowerPAD Made Easy*, http://www−s.ti.com/sc/psheets/slma004/slma004.pdf
- Application report (SSYA008), *Electrostatic Discharge (ESD)*, http://www−s.ti.com/sc/psheets/ssya008/ssya008.pdf
- Application report (SLOA100), *Active Output Impedance for ADSL Line Drivers*, http://www−s.ti.com/sc/psheets/sloa100/sloa100.pdf

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Contents

1 Introduction and Description 1-1
1.1 Evaluation Modue Features 1-2
1.2 THS6182DWEVM Operating Conditions 1-2
1.3 EVM Default Configuration 1-2

2 Using the THS6182DWEVM 2-1

3 THS6182DWEVM Applications 3-1
3.1 Standard Gain Configuration 3-2
3.2 Active Termination 3-3
3.3 Receive Path Implementation 3-6
3.4 High-Pass Filter 3-7
3.5 Single-Ended Gain Stages 3-8

4 EVM Hardware Description 4-1

Figures

1−1 Full Schematic of the Populated Circuit on the THS6182DWEVM (Default Configuration) 1-3
2−1 Interconnection Diagram 2-1
3−1 Default Configuration Operation 3-2
3−2 Differential Positive Feedback 3-3
3−3 Implementation of the Receive Signal Path 3-6
3−4 ADSL Spectrum and High-Pass Filter Response 3-7
3−5 Single-Ended Amplifier Configuration 3-8
4−1 Top Layer 1 (Signals for THS6182DWEVM) 4-2
4−2 Internal Plane (Layer 2) (Ground 1 Plane) 4-3
4−3 Internal Plane (Layer 3) (Power Plane) 4-3
4−4 Bottom (Layer 4) (Ground and Signal) 4-4

Tables

4−1 THS6182DWEVM Bill of Materials 4-1

Chapter 1

Introduction and Description

The Texas Instruments THS6182DW evaluation module (EVM) helps designers evaluate the performance of the THS6182 operational amplifier. Also, this EVM is a good example of high-speed PCB design.

This document details the THS6182DWEVM. It includes a list of EVM features, a brief description of the module illustrated with a series of schematic diagrams, EVM specifications, details on connecting and using the EVM, and a discussion of high-speed amplifier design considerations.

This EVM enables the user to implement various circuits to clarify the available configurations presented by the schematic of the EVM. The user is not limited to the circuit configurations presented. The EVM provides enough hardware hooks that the only limitation should be the creativity of the user.

Topic **Page**

1.1 Evaluation Module Features 1-2

1.2 THS6182DWEVM Operating Conditions 1-2

1.3 EVM Default Configuration 1-2

1.1 Evaluation Modue Features

The THS6182EVM provides a platform for developing high-speed operational amplifier application circuits. It contains the THS6182 high-speed dual operational amplifier, a number of passive components, and various features and footprints that enable the user to experiment with, test, and verify various operational amplifier circuit implementations. The PC board measures 4.0 by 2.8 inches. THS6182 high-speed operational amplifier EVM features include:

- Active termination capability (R3 and R12)
- Snubber circuit (R1 and C1), for use with active termination
- Hooks for a recieve path signal (TP1 through TP4)
- Noninverting gain configuration for DSL
- High-pass filter (HPF) function for ADSL (C2 and R23)
- Short-loop length for the power supply differential high-frequency path (C9)

1.2 THS6182DWEVM Operating Conditions

Supply voltage range, $\pm V_{CC}$	±5 to ±15 Vdc (see the device data sheet)
Supply current, I_{CC}	(see the device data sheet)

For complete THS6182 amplifier IC specifications, parameter measurement information, and additional application information, see the THS6182 data sheet (SLLS544).

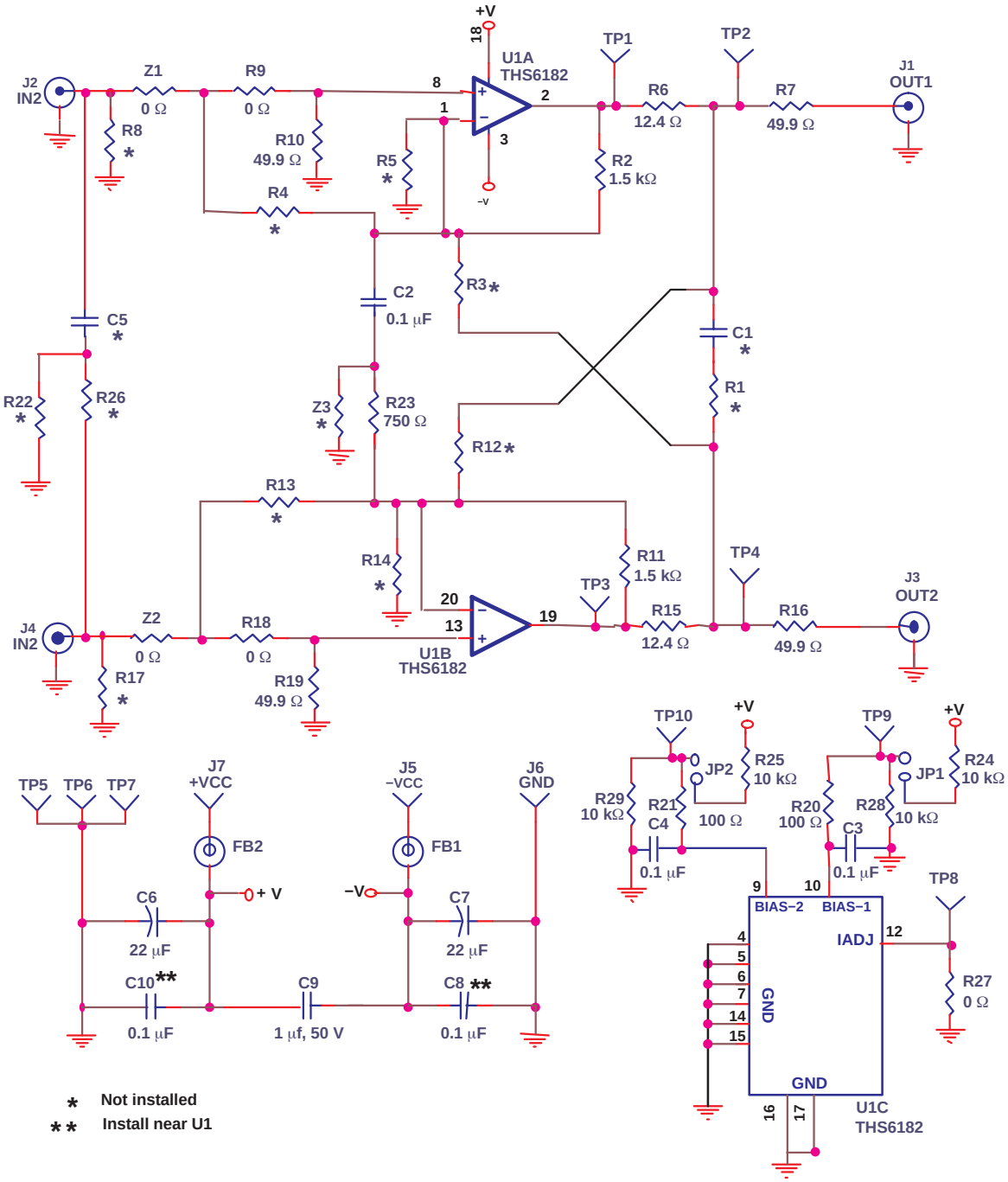
1.3 EVM Default Configuration

As delivered, the EVM has a fully functional example circuit, requiring added power supplies, a signal source, and monitoring instrument. See Figure 1−1 for the complete EVM schematic.

The default configuration has a differential gain of 2.22, as determined by R2, R23, and R11 in combination with series matching resistors R6, R7, R15, and R16, and a 50-Ω load on the outputs at J1 and J3.

Some components such as R20, R21, R24–R29, C3–C11, FB1, FB2, JP1, JP2, J5–J7, and TP8–TP10, etc., are omitted on the application schematics of Chapter 3 for clarity.

Figure 1−1. Full Schematic of the Populated Circuit on the THS6182DWEVM (Default Configuration)



Chapter 2

Using the THS6182DWEVM

This section describes how to connect the THS6182DWEVM to test equipment. It is recommended that the user connect the EVM as described in this section to avoid damage to the EVM or the THS6182 installed on the board.

Figure 2−1. Interconnection Diagram

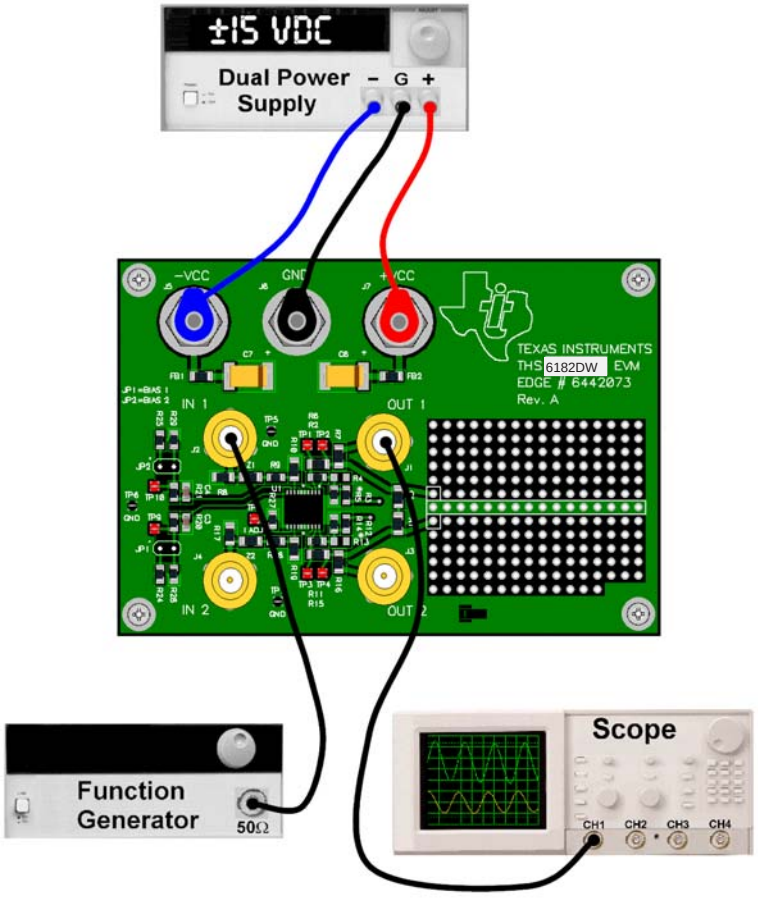


Figure 2−1 shows the connections to measure the output signal of output 1 while a single-ended signal is inserted into EVM channel 1's noninverting input. If the oscilloscope input is connected to J3 and the signal source is connected to J2, EVM channel 2 is also configured for a noninverting signal path. When the oscilloscope's input impedance is 50 Ω, the voltage gain from J2 to J3 is 1.33 V.

Once power is available at the power terminals of the EVM, removing either JP1 and/or JP2 causes bias current to flow at the desired amount. With both JP1 and JP2 installed, the circuit is disabled.

If a balanced (differential) signal is inserted into J2 and J4, a balanced signal is present at J1 and J3.

Chapter 3

THS6182DWEVM Applications

Example applications are presented in this chapter. These applications demonstrate the most popular circuits, but many other circuits can be constructed. The user is encouraged to experiment with different circuits, exploring new and creative design techniques.

Topic **Page**

3.1	Standard Gain Configuration	3-2
3.2	Active Termination	3-3
3.3	Receive Path Implementation	3-6
3.4	High-Pass Filter	3-7
3.5	Single-Ended Gain Stages	3-8

3.1 Standard Gain Configuration

The THS6182DWEVM default configuration is a fully differential input, fully differential output gain of about 2.2 (at the output connectors using an instrument with 50-Ω load on each input). A simplified schematic is shown in Figure 3−1. This gain is calculated according to an equation that is similar to the one that describes an instrumentation amplifier:

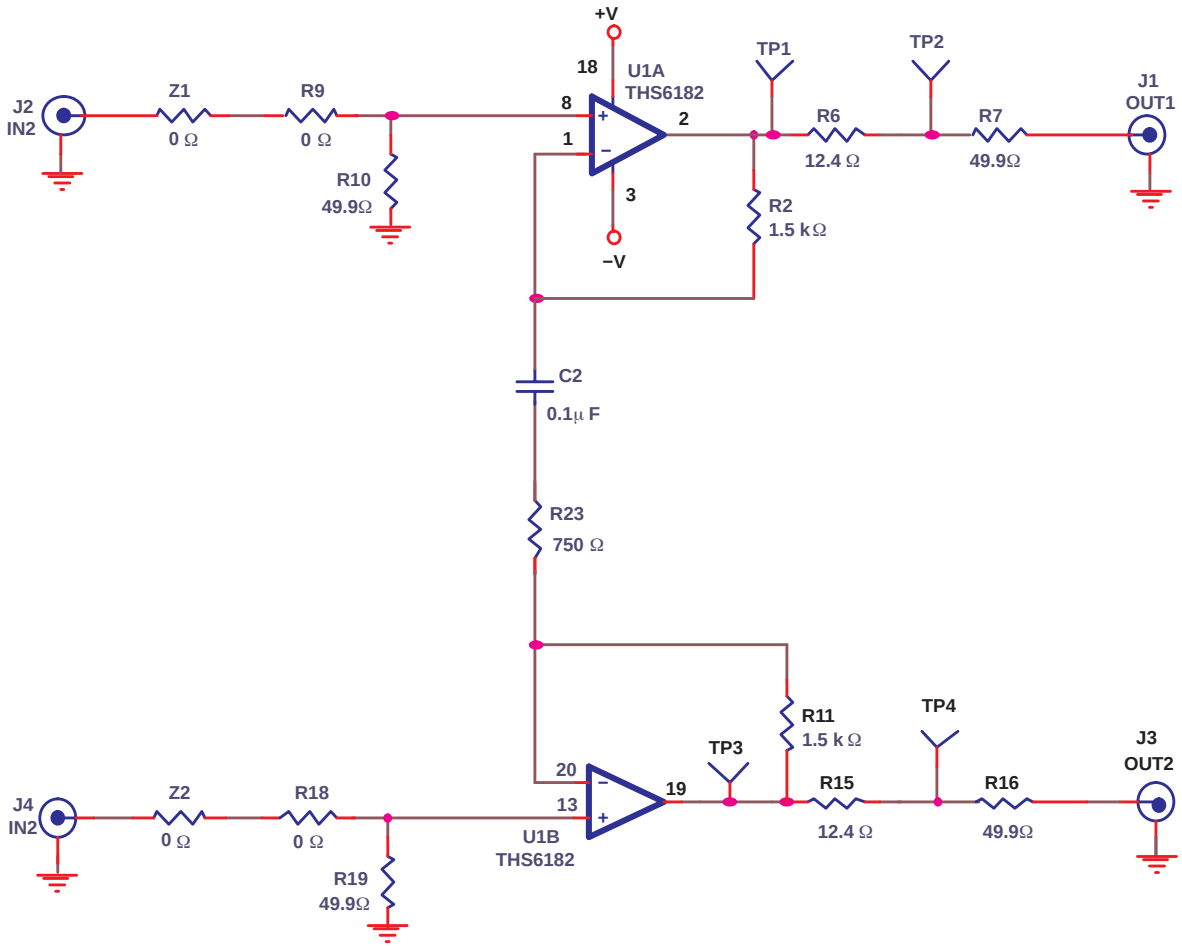
$$\text{Differential gain} = \frac{V_O(\text{diff})}{V_I(\text{diff})} = 1 + \frac{2 \times R2}{R23} \quad (1)$$

where

R2 = R11

Series resistors R6, R7, R15 and R16 affect output voltage at J1 and J3. The designer needs to take the voltage divider law into account for their load impedance and R6, R7, R15 and R16. When a designer monitors the output at TP1 and TP3 using a high-impedance differential probe, the default gain is 5 V.

Figure 3−1. Default Configuration Operation



3.2 Active Termination

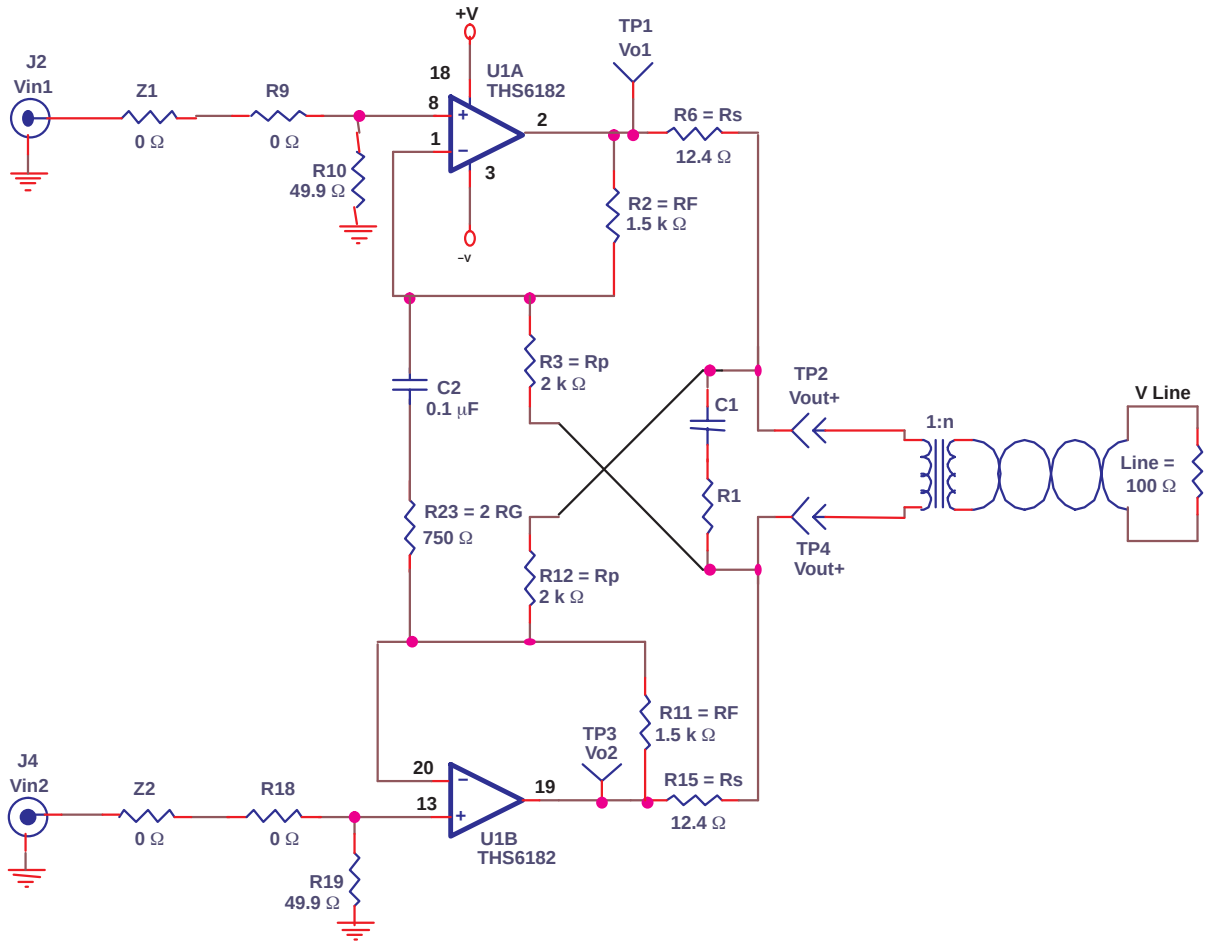
Although this application is specifically for use as an ADSL line driver, the principals shown can be applied to other applications.

Active termination is a technique that allows the designer to use a small value resistor for the series resistance (R6 and, or R15). The circuit then utilizes positive feedback to make the impedance of this resistor appear much larger, when looking from the line-side. This accomplishes two things:

- A very small resistance exists between the amplifier and the transformer. This lowers the output voltage swing range required from the driver stage.
- Proper matching impedance appears when looking from the line to the amplifier.

Figure 3−2 shows the basic circuit for differential positive feedback.

Figure 3−2. Differential Positive Feedback



Active feedback creates larger impedance (Z) than what is actually placed there by series resistors R_S:

$$Z(\Omega) = \frac{R_S}{1 - \frac{R_F}{R_P}} \tag{2}$$

The important thing to consider is that regardless of the forward gain from Vin to Vo, the active impedance (Z) value remains constant.

Solving equation 2 for Rp, the following equation is produced:

$$R_P = \frac{R_F}{1 - \frac{R_S}{P}} \tag{3}$$

Using Z = 50 Ω and values from Figure 3−2 in equation 3, yields 1995 Ω for R_P. The closest E96(1%) value to 1995 Ω is 2 kΩ, as shown in Figure 3−2.

Now that the return impedance is corrected, forward voltage gain from input to output is calculated. Equation 3 shows the simplified forward gain from Vin to Vo.

$$A_V = \frac{V_O \pm}{V_{in} \pm} = \frac{1 + \left(\frac{R_F}{R_G \| R_P}\right)}{1 - \left(\frac{R_F}{R_P}\right)\left(\frac{R_L}{R_L + R_S}\right)} \text{ if } R_L << R_P \tag{4}$$

where

$$R_L = \frac{R_{LINE}}{2\,n^2} \tag{5}$$

With a transformer ratio(n) of 1 and a R_{LINE} of 100 Ω, R_L is 50 Ω.

When the value R_L and the values in Figure 3−2 are used in equation 4, the resulting voltage gain is 14.5. Because R_G does not affect the value of the apparent output impedance of the circuit, voltage gain can be adjusted by changing R_G.

The reader is cautioned that active termination is a very complex topic, with many considerations. Please carefully read the Texas Instruments Application Report *Active Output Impedance for ADSL Line Drivers*, (SLOA100) to gain a more complete understanding of the topic and all the subtle implications of active termination.

R1 and C1 are located on the EVM so that a snubber circuit may be implemented. Some transformers have a high resonant frequency (as low as 25 MHz but as high as 150 MHz). When using traditional termination (just R6, and R15—no active termination), there is typically not a reason to use these components. But, when active termination is used, the effective impedance of these two resistor values drops substantially. Thus, there can be very small

resistor isolation between the amplifier and the transformer, causing a resonance problem. Couple this with the feedback path of R3 and R12, and this can cause the amplifier to oscillate. The snubber is utilized to eliminate this oscillation. As a rule of thumb, to select the proper snubber values, select:

$$R19 = 2 \times \frac{R_{LINE}}{n^2} \quad (6)$$

Then select C5:

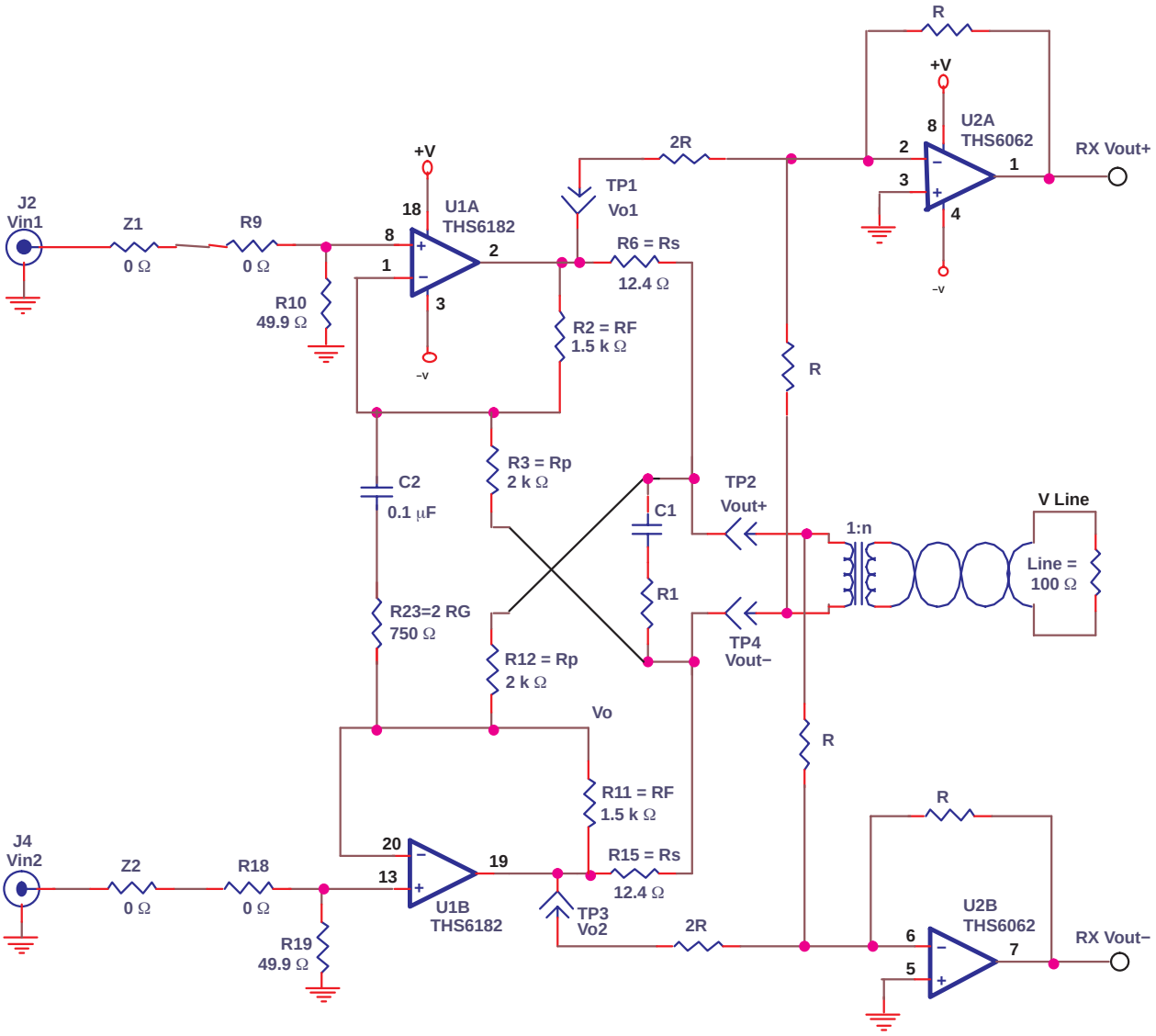
$$C5 = \frac{1}{2 \times \pi \times R19 \times F_C} \quad (7)$$

where F_C = at least 10X the highest operating frequency (1.104 MHz is the highest ADSL operating frequency). 20X or even larger may be preferable.

3.3 Receive Path Implementation

Test points TP1 through TP4 are located on the EVM to facilitate the addition of the receive signal path to the signal chain as shown in Figure 3−3. When implementing the receive path, a *hybrid* must be used as ADSL is full duplex. The hybrid cancels out the TX signal and allows the RX signal from the line to come through. The THS6182DWEVM does not have receive or *hybrid* circuitry included. Texas Instruments assumes that the customer has a proprietary hybrid design, and therefore they would prefer to implement it. The user should know their nominal line impedance characteristics and thus should be able to match them better. Texas Instruments does have an EVM that contains a THS6062 ADSL receiver, and this EVM can be purchased separately to facilitate construction of a complete ADSL transmit/receive interface.

Figure 3−3. Implementation of the Receive Signal Path

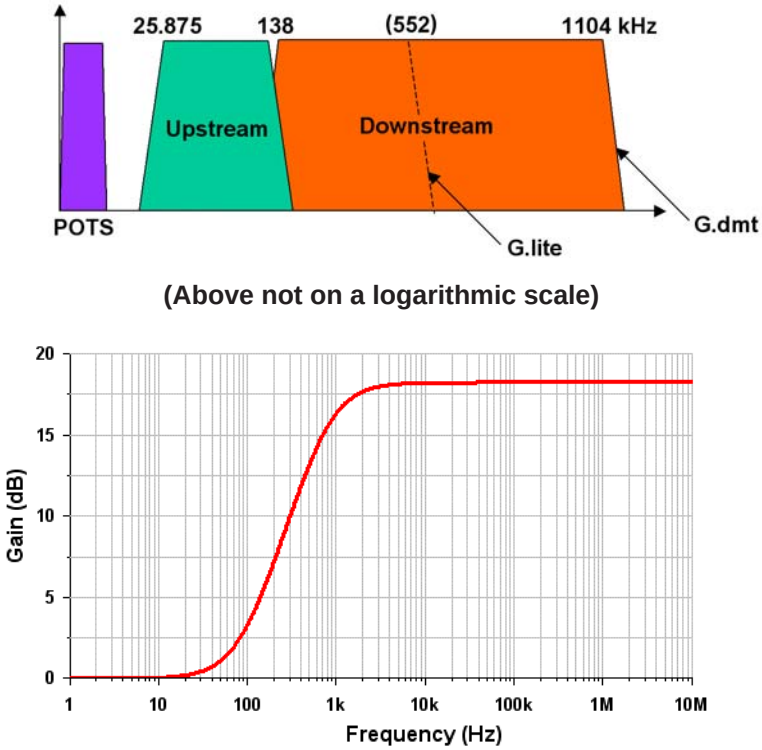


3.4 High-Pass Filter

Because ADSL CPE is designed to transmit from 25.875 kHz to 138 kHz, C2 and R23 can be used to implement an HPF function. These are selected to be 20X lower than 25 kHz (1.25 kHz). Some designs use a capacitor—some do not. This path allows for a common gain setting between the two channels. This helps (but does not assure) the signals are truly differential.

Figure 3−4 compares the frequency spectrum of ADSL to a simulation of the high-pass filter on the THS6182DWEVM.

Figure 3−4. ADSL Spectrum and High-Pass Filter Response



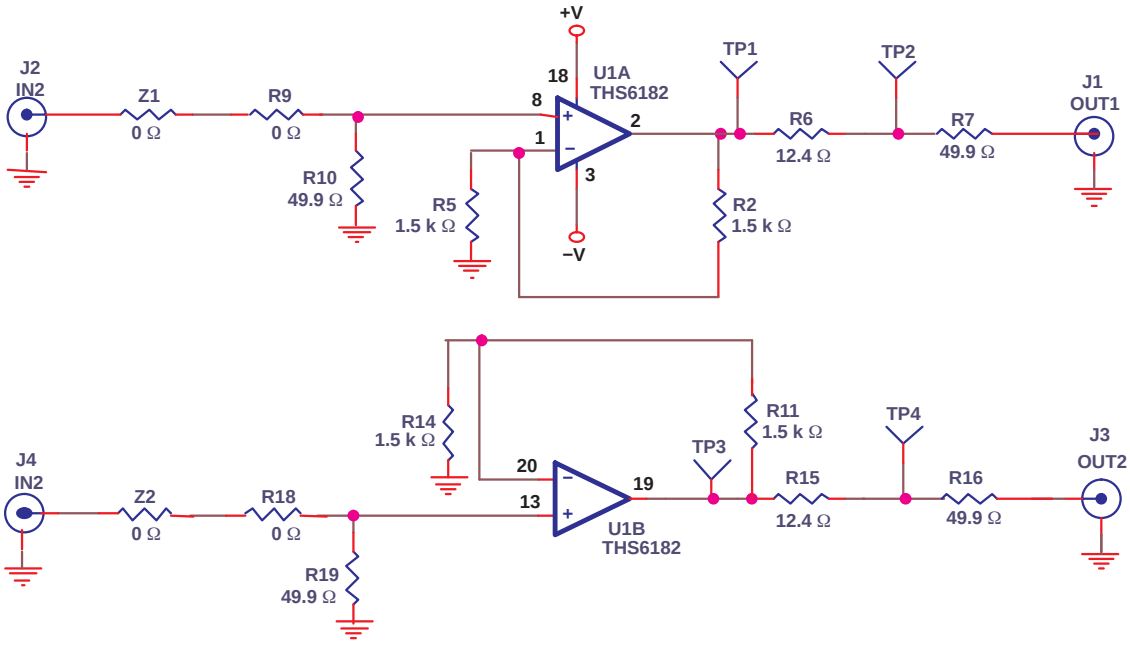
Note that the high-pass filter function is not a true high-pass filter. C2 in series with R23 creates a zero at about 10 Hz. As the frequency decreases from about 3 kHz to 10 Hz, the circuit changes from a gain stage into two unity gain buffers.

3.5 Single-Ended Gain Stages

Although ADSL is the obvious application for the THS6182DWEVM, it can also be configured for other applications. If the common gain resistor R8 is removed, there is an array of components that allow various dc and ac coupled gain stages to be constructed.

Referring to Figure 3−5, for example, two dc coupled gain stages are formed by removing R9 and adding R4 and R14. There are many other possibilities.

Figure 3−5. Single-Ended Amplifier Configuration



Chapter 4

EVM Hardware Description

This chapter describes the EVM hardware. It includes the EVM parts list, and printed circuit-board layout.

Table 4−1. THS6182DWEVM Bill of Materials

Item	Description	SMD Size	Reference Designator	PCB QTY	Manfacturer's Part #	Distributor's Part #
1	Bead, ferrite, 3A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R−00	(Digi−Key) 240−1010−1−ND
2	CAP, 22 µF, tantalum, 25 V, 10%	D	C6, C7	2	(AVX) TAJD226K025R	(Garrett) TAJD226K025R
3	CAP, 0.1 µF, ceramic, X7R, 50 V	0805	C3, C4, C8, C10	4	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
4	Open	1206	C1	1		
5	CAP, 0.1 µF, ceramic, X7R, 50 V	1206	C2	1	(AVX) 12065C104KAT2A	(Garrett) 12065C104KAT2A
6	CAP, 1.0 µF, ceramic, Y5V, 50 V	1206	C9	1	(AVX) 12065G105ZAT2A	(Garrett) 12065G105ZAT2A
7	Open	0805	R3, R4, R5, R12, R13, R14	6		
8	Resistor, 0 Ω, 1/8 W	0805	R9, R18, R27	3	(Phycomp) 9C08052A0R00JLHFT	(Garrett) 9C08052A0R00JLHFT
9	Resistor, 100 Ω, 1/8 W, 1%	0805	R20, R21	2	(Phycomp) 9C08052A1000FKHFT	(Garrett) 9C08052A1000FKHFT
10	Resistor, 750 Ω, 1/8 W, 1%	0805	R23	1	(Phycomp) 9C08052A7500FKHFT	(Garrett) 9C08052A7500FKHFT
11	Resistor, 1.5 kΩ, 1/8 W, 1%	0805	R2, R11	2	(Phycomp) 9C08052A1501FKHFT	(Garrett) 9C08052A1501FKHFT
12	Resistor, 10 kΩ, 1/8 W, 1%	0805	R24, R25, R28, R29	4	(Phycomp) 9C08052A1002FKHFT	(Garrett) 9C08052A1002FKHFT
13	Open	1206	R1, R8, R17, Z3	4		
14	Resistor, 0 Ω, 1/4 W	1206	Z1, Z2,	2	(Phycomp) 9C12063A0R00JLHFT	(Garrett) 9C12063A0R00JLHFT
15	Resistor, 12.4 Ω, 1/4 W, 1%	1206	R6, R15	2	(Phycomp) 9C12063A12R4FKRFT	(Garrett) 9C12063A12R4FKRFT
16	Resistor, 49.9 Ω, 1/4 W, 1%	1206	R7, R10, R16, R19	4	(Phycomp) 9C12063A49R9FKRFT	(Garrett) 9C12063A49R9FKRFT

Table 4−1. THS6182DWEVM Bill of Material (Continued)

Item	Description	SMD Size	Reference Designator	PCB QTY	Manfacturer's Part #	Distributor's Part #
17	Connector, BNC, vertical, PCB		J1, J2, J3, J4	4	(Amphenol) 31−5329	(Newark) 89F2885
18	Jack, banana, 0.25" diameter hole		J5, J6, J7	3	(HH Smith) 101	(Newark) 35F865
19	Header, 0.1" centers, 0.025" square pins	2 POS.	JP1, JP2	2	(Sullins) PZC36SAAN	(Digi−Key) S1011−36−ND
20	Shunts		JP1, JP2	2	(Sullins) SSC02SYAN	(Digi−Key) S9002−ND
21	Test point, black		TP5, TP6, TP7	3	(Keystone) 5001	(Digi−Key) 5001K−ND
22	Test points, red		TP1, TP2, TP3, TP4, TP8, TP9, TP10	7	(Keystone) 5000	(Digi−Key) 5000K−ND
23	Standoff, 4−40 hex, 0.625" length			4	(Keystone) 1804	(Allied) 839−2089
24	Screw, Phillips, 4−40, .250"			4	SHR−0440−016−SN	
25	IC, THS6182	U1		1	(TI) THS6182DW	
26	Printed-circuit board			1	(TI) EDGE #6442073	

Figure 4−1. Top Layer 1 (Signals for THS6182DWEVM)

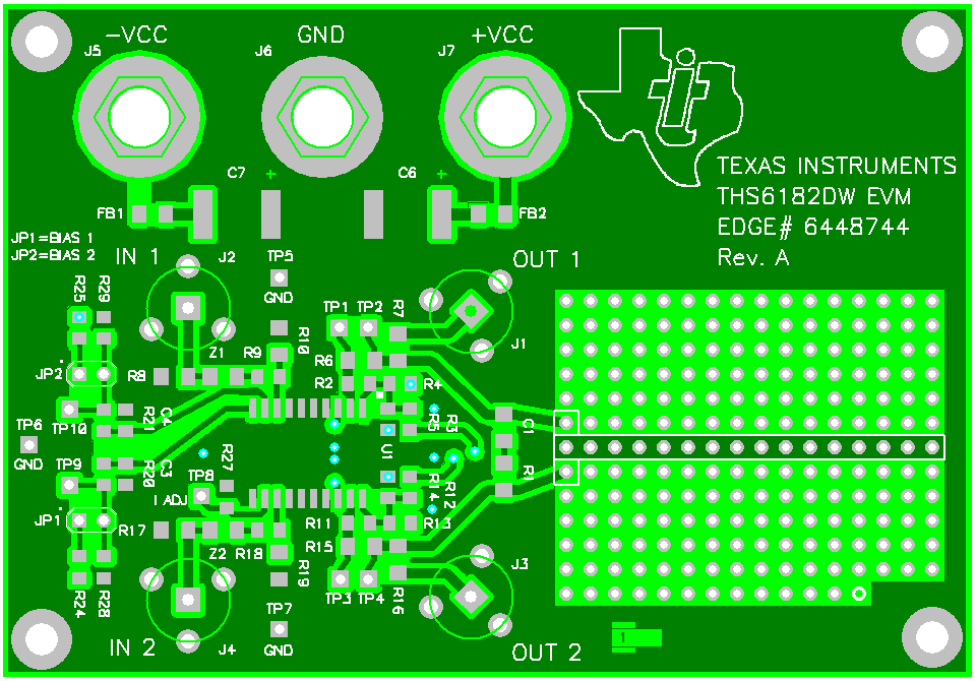


Figure 4−2. Internal Plane (Layer 2) (Ground 1 Plane)

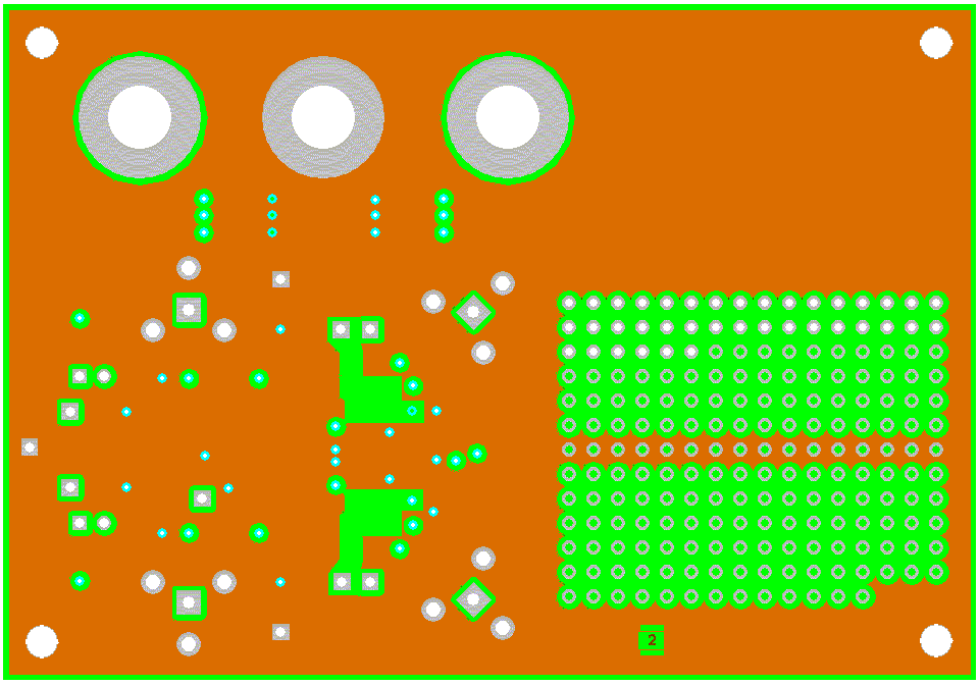


Figure 4−3. Internal Plane (Layer 3) (Power Plane)

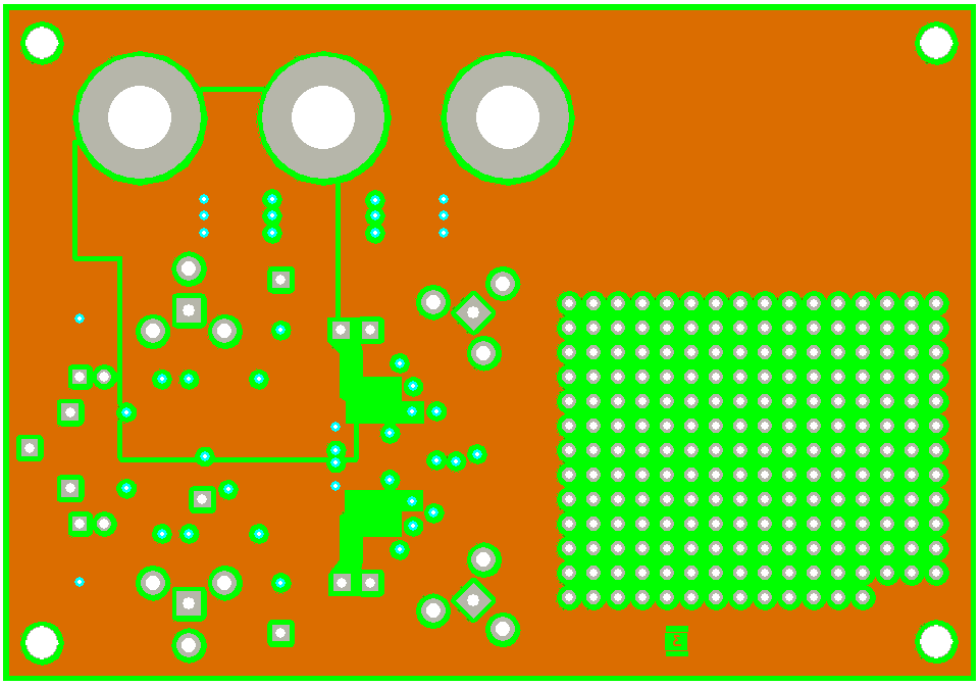


Figure 4−4. Bottom (Layer 4) (Ground and Signal)