Intel® Stratix® 10 GX FPGA Development Kit User Guide

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Contents

1. Overview

The Intel® Stratix® 10 GX FPGA development board provides a hardware platform for evaluating the performance and features of the Intel Stratix 10 GX device.

This development board comes in two different versions as shown in the table below.

Table 1. Intel Stratix 10 GX FPGA Development Kit Versions

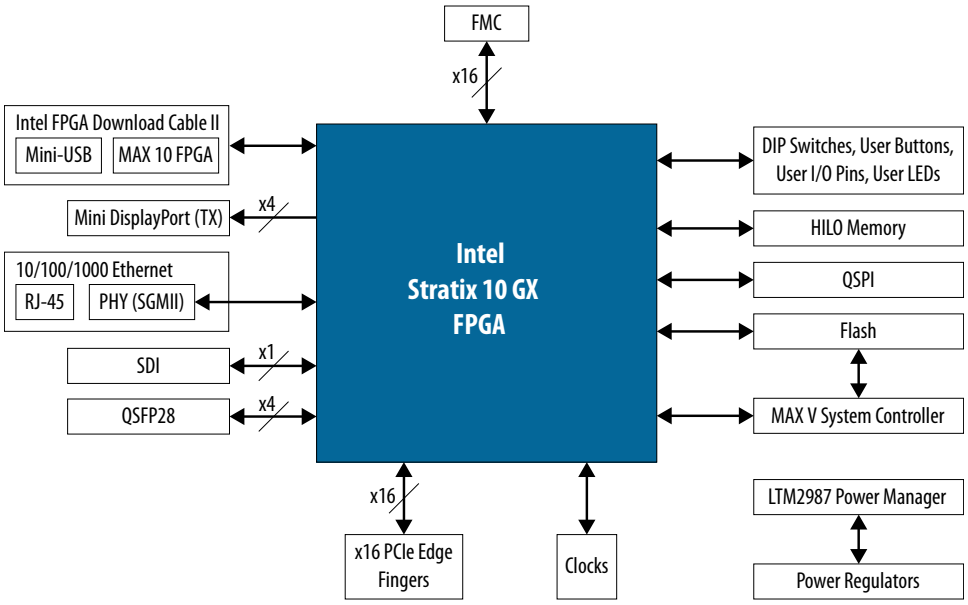
Version	Ordering Code	Device Part Number
Intel Stratix 10 GX FPGA L-Tile	DK-DEV-1SGX-L-A	1SG280LU2F50E2VG
Intel Stratix 10 GX FPGA H-Tile	DK-DEV-1SGX-H-A	1SG280HU2F50E2VG

Note: The development kits listed in the *Table 1* are production only. For more information about the Engineering Samples (ES) editions development kits, please contact your Intel sales representative.

The FPGA capabilities vary depending on the development kit version selected, but the board remains same between the two versions of the development kits. For more information on the Intel Stratix 10 L-tile and H-tile, refer to Intel Stratix 10 FPGA product page on Intel website.

1.1. General Development Board Description

Figure 1. Intel Stratix 10 GX Block Diagram



1.2. Recommended Operating Conditions

- Recommended ambient operating temperature range: 0C to 45C
- Maximum ICC load current: 100 A
- Maximum ICC load transient percentage: 30 %
- FPGA maximum power supported by the supplied heatsink/fan: 200 W

1.3. Handling the Board

When handling the board, it is important to observe static discharge precautions.

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Caution: This development kit should not be operated in a Vibration environment.

2. Getting Started

2.1. Installing Intel Quartus® Prime Software

The new Intel Quartus® Prime Design Suite design software includes everything needed to design for Intel FPGAs, SoCs and CPLDs from design entry and synthesis to optimization, verification and simulation.

The Intel Quartus Prime Design Suite software is available in three editions based on specific design requirements: Pro, Standard, and Lite Edition. The Intel Stratix 10 GX FPGA Development Kit is supported by the Intel Quartus Prime Pro Edition.

Intel Quartus Prime Pro Edition: The Intel Quartus Prime Pro Edition is optimized to support the advanced features in Intel's next generation FPGAs and SoCs, starting with the Intel Arria® 10 device family and requires a paid license.

Included in the Intel Quartus Prime Pro Edition are the Intel Quartus Prime software, Nios® II EDS and the Intel FPGA IP Library. To install Intel's development tools, download the Intel Quartus Prime Pro Edition software from the Intel Quartus Prime Pro Edition page in the Download Center of Intel's website.

2.1.1. Activating Your License

Before using the Intel Quartus Prime software, you must activate your license, identify specific users and computers and obtain and install license file. If you already have a licensed version of the Standard Edition or Pro Edition, you can use that license file with this kit. If not follow these steps:

1. Log on at the My Intel Account Sign In web page and click ***Sign In.***
2. On the My Intel Home web page, click the Self-Service Licensing Center link.
3. Locate the serial number printed on the side of the development kit box below the bottom bar code. The number consists of alphanumeric characters and does not contain hyphens.
4. On the Self-Service Licensing Center web page, click the Find it with your License Activation Code link.
5. In the ***Find/Activate Products*** dialog box, enter your development kit serial number and click ***Search*.**
6. When your product appears, turn on the check box next to the product name.
7. Click ***Activate Selected Products*** and click Close.
8. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the License Setup page of the ***Options*** dialog box in the Quartus Prime software to enable the software.

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Intel Quartus Prime Design Suite software. Your DKE license is valid only for one year and you cannot use this version of the Intel Quartus Prime after one year. To continue using the Intel Quartus Prime software, you should download the free Quartus Prime Lite Edition or purchase a paid license for the Intel Quartus Prime Pro Edition.

2.2. Development Board Package

Download the Intel Stratix 10 GX FPGA Development Kit package from the Intel Stratix 10 GX FPGA Development Kit page of the Intel website.

Unzip the Intel Stratix 10 GX FPGA Development Kit package.

Figure 2. Installed Development Kit Directory Structure

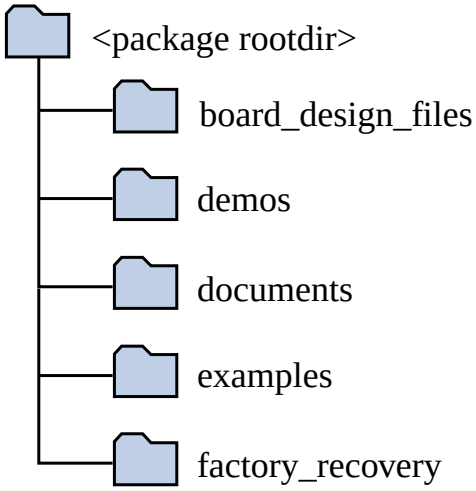


Table 2.

Directory Name	Description of Directory Contents
board_design_files	Contains schematic, layout, assembly and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications when available.
documents	Contains documentation.
examples	Contains sample design files for this board.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Note: To view the the layout `*.brd` files in the board package, you can download the Cadence® Allegro®/OrCAD® Free Viewer from Cadence's website.

Related Information

Cadence Allegro Downloads

2.3. Installing the Intel FPGA Download Cable II Driver

The development board includes integrated Intel FPGA Download Cable II circuits for FPGA programming. However, for the host computer and board to communicate, you must install the On-Board Intel FPGA Download Cable II driver on the host computer.

Installation instructions for the On-Board Intel FPGA Download Cable II driver for your operating system are available on the Intel website.

On the Cable and Adapter Drivers Information web page of the Intel website, locate the table entry for your configuration and click the link to access the instructions.

3. Development Board Setup

This chapter describes how to apply power to the development board and provides default switch and jumper settings.

3.1. Applying Power to the Development Board

This development kit is designed to operate in two modes:

1. **As a PCIe* add-in card**

   When operating the card as a PCIe system, insert the card into an available PCIe slot and connect a 2x4 and 2x3 pin PCIe power cable from the system to power connectors at J26 and J27 of the board respectively.

   Note: When operating as a PCIe add-in card, the board does not power on unless power is supplied to J26 and J27.

2. **In bench-top mode**

   In Bench-top mode, you must supply the board with provided power 240W power supply connected to the power connector J27. The following describes the operation in bench-top mode.

This development board ships with its switches preconfigured to support the design examples in the kit.

If you suspect that your board may not be correctly configured with the default settings, follow the instructions in the Default Switch and Jumper Settings section of this chapter.

1. The development board ships with design examples stored in the flash memory device. To load the design stored in the factory portion of the flash memory, verify SW3.3 is set to ON. This is the default setting.
2. Connect the supplied power supply to an outlet and the DC Power Jack (J27) on the FPGA board.

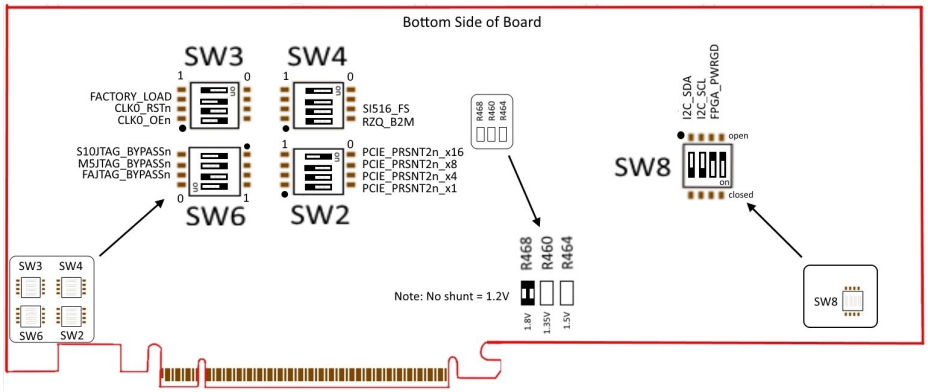
   Note: Use only the supplied power supply. Power regulation circuits on the board can be damaged by power supplies with greater voltage.
3. Set the power switch (SW7) to the ON position.

When the board powers up, the parallel flash loader (PFL) on the MAX® V reads a design from flash memory and configures the FPGA. When the configuration is complete, green LEDs illuminate signaling the device configured successfully. If the configuration fails, the red LED illuminates.

3.2. Default Switch and Jumper Settings

This topic shows you how to restore the default factory settings and explains their functions.

Figure 3. Default Switch Settings



1. Set DIP switch bank (SW2) to match the following table

Table 3. SW2 DIP PCIe Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	x1	ON for PCIe x1	OFF
2	x4	ON for PCIe x4	OFF
3	x8	ON for PCIe x8	OFF
4	x16	ON for PCIe x16	ON

2. If all of the resistors are open, the FMC VCCIO value is 1.2 V. To change that value, add resistors as shown in the following table.

Table 4. Default Resistor Settings for the FPGA Mezzanine (FMC) Ports (Board Bottom)

Board Reference	Board Label	Description
R460	1.35V	1.35V FMC VCCIO select
R464	1.5V	1.5V FMC VCCIO select
R468	1.8V	1.8V FMC VCCIO select *Note:* A 0 Ohm resistor is installed by default

3. Set DIP switch bank (SW6) to match the following table.

Table 5. SW6 JTAG Bypass DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	Intel Stratix 10	OFF to enable the Intel Stratix 10 in the JTAG chain. ON to bypass the Intel Stratix 10 in the JTAG chain.	OFF
2	MAX V	OFF to enable the MAX V in the JTAG chain. ON to bypass the MAX V in the JTAG chain.	OFF
3	FMC	OFF to enable the FMC Connector in the JTAG chain. ON to bypass the FMC connector in the JTAG chain.	ON

4. SW1 DIP Switch Default Settings (Board TOP)

Table 6. SW1 DIP Switch Default Settings (Board TOP)

Switch	Board Label	Function
1	MSEL2	MSEL [2], MSEL [1] = [0,0] QSPI AS Fast Mode MSEL [2], MSEL [1] = [0,1] QSPI AS Normal Mode MSEL [2], MSEL [1] = [1,0] AVST x16 Mode (Default) MSEL [2], MSEL [1] = [1,1] JTAG Only Mode MSEL [0] is tied to Vcc
2	MSEL1	

5. Set DIP switch bank (SW6) to match the following table.

Table 7. SW3 DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	CLK0_OEn	ON to enable the Si5341A clock device OFF to disable the Si5341A clock device	ON
2	CLK0_RSTn	ON to hold the Si5341A clock device in reset OFF to allow the Si5341A clock device to function normally	OFF
3	FACTORY_LOAD	ON to load factory image from flash OFF to load user hardware1 from flash	ON

Table 8. SW4 DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	RZQ_B2M	ON for setting RZQ resistor of Bank 2M to 99.17 Ohm OFF for setting RZQ resistor of Bank 2M to 240 Ohm	OFF
2	SI516_FS	ON for setting the SDI REFCLK frequency to 148.35 MHz OFF for setting the SDI REFCLK frequency to 148.5 MHz	OFF

Table 9. SW8 DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	I2C_SDA	Connects VRM I2C to MAX V I2C chain	ON
2	I2C_SCL	Connects VRM I2C to MAX V I2C chain	ON
3	FPGA_PWRGD	Connects LT2987 Power Good to MAX V	OFF

4. Board Components

This chapter introduces all the important components on the development board. A complete set of schematics, a physical layout database and GERBER files for the development board reside in the development kit documents directory.

4.1. Board Overview

An image of the Intel Stratix 10 GX FPGA development board is shown below.

Figure 4. Intel Stratix 10 GX FPGA Development Board Image - Front

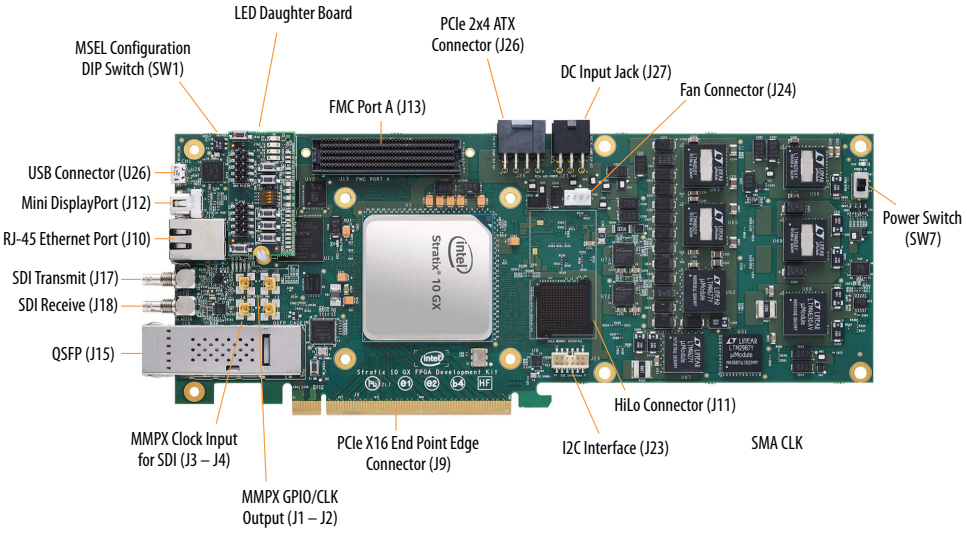


Figure 5. Intel Stratix 10 GX FPGA Development Board Image - LED Daughter Board Close Up

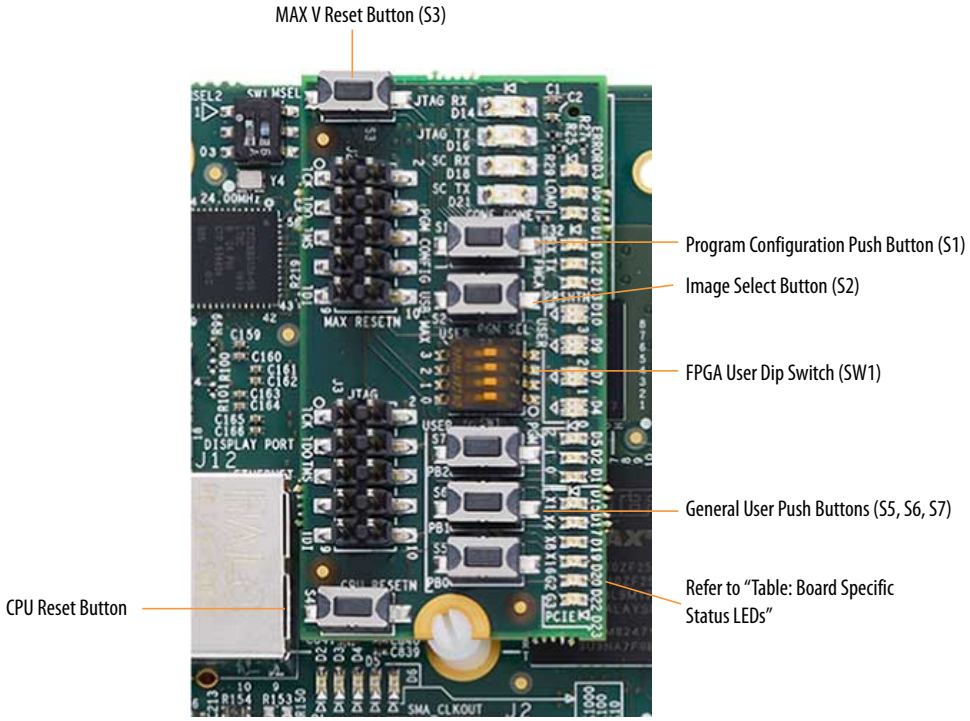


Figure 6. Intel Stratix 10 GX FPGA Development Board Image - Rear

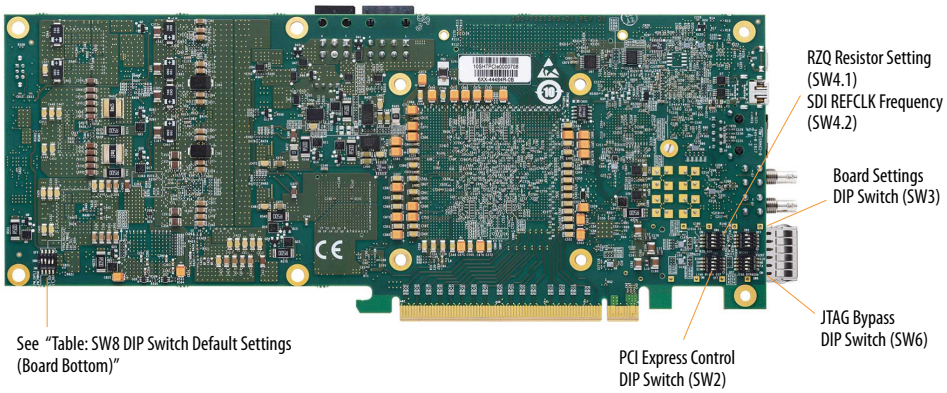


Table 10. Intel Stratix 10 GX FPGA Development Board Components

Board Reference	Type	Description
Featured Devices		
U1	FPGA	Intel Stratix 10 GX FPGA, 1SG280LU3F50E3VGS1. • Adaptive logic modules (ALMs): 933,120 • LEs (K): 2,753 • Registers: 3,732,480

continued...

Board Reference	Type	Description
		• M20K memory blocks: 11,721 • Transceiver Count: 96 • Package Type: 2397 BGA
U11	CPLD	MAX V CPLD, 2210 LEs, 256 FBGA, 1.8V VCCINT.
Configuration and Setup Elements		
CN1	On-board Intel FPGA Download Cable II	Micro-USB 2.0 connector for programming and debugging the FPGA.
SW2	PCI Express* Control DIP Switch	Enables PCI Express link widths x1, x4, x8 and x16.
SW6	JTAG Bypass DIP Switch	Enables and disables devices in the JTAG chain. This switch is located on the back of the board.
SW1	MSEL Configuration DIP Switch	Sets the Intel Stratix 10 MSEL pins.
SW3	Board settings DIP Switch	Controls the MAX V CPLD System Controller functions such as clock reset, clock enable, factory or user design load from flash and FACTORY signal command sent at power up. This switch is located at the bottom of the board.
S4	CPU reset push button	The default reset for the FPGA logic. This button resides on the LED daughter board.
S2	Image select push button	Toggles the configuration LEDs which selects the program image that loads from flash memory to the FPGA. This button resides on the LED daughter board.
S1	Program configuration push button	Configures the FPGA from flash memory image based on the program LEDs. This button resides on the LED daughter board.
S3	MAX V reset push button	The default reset for the MAX V CPLD System Controller. This button resides on the LED daughter board.
Status Elements		
D14, D16	JTAG LEDs	Indicates the transmit or receive activity of the System Console USB interface. The TX and RX LEDs would flicker if the link is in use and active. The LEDs are either off when not in use or on when in use but idle. These LEDs reside on the LED daughter board.
D18, D21	System Console LEDs	Indicates the transmit or receive activity of the System Console USB interface. The TX and RX LEDs would flicker if the link is in use and active. The LEDs are either off when not in use or on when in use but idle.
D1, D2, D5	Program LEDs	Illuminates to show the LED sequence that determines which flash memory image loads to the FPGA when you press the program load push button. The LEDs reside on the LED daughter card.
D8	Configuration Done LED	Illuminates when the FPGA is configured. This LED resides on the LED daughter board.
D6	Load LED	Illuminates during FPGA configuration. This LED resides on the LED daughter board.
D3	Error LED	Illuminates when the FPGA configuration fails. This LED resides on the LED daughter board.
D45	Power LED	Illuminates when the board is powered on.
D40	Temperature LED	Illuminates when an over temperature condition occurs for the FPGA device. Ensure that an adequate heatsink/fan is properly installed.

continued...

Board Reference	Type	Description
D2, D3, D4, D5, D6	Ethernet LEDs	Shows the connection speed as well as transmit or receive activity.
D9	SDI Cable LED	Illuminates to show the transmit or receive activity for the SDI interface.
D15, D17, D19, D20, D22, D23	PCI Express link LEDs	You can configure these LEDs to display the PCI Express link width (x1, x4, x8 and x16) and data rate (Gen2, Gen3). These LEDs reside on the LED daughter board.
D4, D7, D9, D10	User defined LEDs	Four bi-color LEDs (green and red) for 8 user LEDs. Illuminates when driven low. These LEDs reside on the LED daughter board.
D11, D12, D13	FMC LEDs	Illuminates for RX, TX, PRNSTn activity of the FMC daughter card (when present). These LEDs reside on the LED daughter board.
Clock Circuits		
X1	SDI Reference Clock	SW4.2 DIP switch controlled: FS=0: 148.35 MHz FS=1: 148.5 MHz
U7	Programmable Clock Generator	Si 5341A Programmable Clock Generator by the clock control GUI Default Frequencies are • Out0=155.25 MHz • Out1=644.53125 MHz • Out2= 135 MHz • Out3= Not Used • Out4=156.25 MHz • Out5= 625 MHz • Out6=Not used • Out7=125 MHz • Out8= 125 MHz • Out9=125 MHz
U9	Programmable Clock Generator	Si5338A Programmable Clock Generator by the clock control GUI. Default frequencies are: • CLK0= 100 MHz • CLK1= 100 MHz • CLK2= 133 MHz • CLK3= 50 MHz
J3, J4	Clock input MMPX connector	MMPX clock input for the SDI interface.
J1, J2	MMPX GPIO/CLK output from FPGA Bank 3I	MMPX GPIO/CLK output from FPGA Bank 3I.
J17, J18	Serial Digital Interface (SDI) transceiver connectors	Two HDBNC connectors. Drives serial data input/output to or from SDI video port.
Transceiver Interfaces		
J9	PCIe x16 gold fingers	PCIe TX/RX x16 interface from FPGA bank 1C, 1D and 1E.
J12	Mini Display Port Video Connector	Four TX channels of Display Port Video interface from FPGA Bank 1F.
J15	QSFP connector	Four TX/RX channels from FPGA Bank 1K
J17, J18	SDI HDBNC Video Connector	Single TX/RX channel from FPGA bank 1N.

continued...

Board Reference	Type	Description
J13	Intel FMC Interface	Sixteen TX/RX channels from FPGA banks 4C, 4D and 4E.
General User Input/Output		
SW1	FPGA User DIP Switch	Four user DIP switches. When switch is ON, a logic 0 is selected. This switch resides on the LED daughter board.
S5, S6, S7	General user push buttons	Three user push buttons. Driven low when pressed. These buttons reside on the LED daughter board.
D4, D7, D9, D10	User defined LEDs	Four bi-color user LEDs. Illuminates when driven low. These LEDs reside on the LED daughter board.
Memory Devices		
J11	HiLo Connector	One x72 memory interface supporting DDR3 (x72), DDR4 (x72), QDR4 (x36) and RLDRAM3 (x36). This development kit includes three plugin modules (daughtercards) that use the HiLo connector: • DDR4 memory (x72) 1333 MHz • DDR3 memory (x72) 1066 MHz • RLDRAM3 memory (x36) 1200 MHz
U12, U83	Flash Memory	ICS-1GBIT STRATA FLASH, 16-BIT DATA.
Communication Ports		
J9	PCI Express x16 edge connector	Gold-plated edge fingers for up to x16 signaling in either Gen1, Gen2 or Gen3 mode.
J13	FMC Port	FPGA mezzanine card ports
J10	Gbps Ethernet RJ-45 connector	RJ-45 connector which provides a 10/100/1000 Ethernet connection via a Marvell 88E1111 PHY and the FPGA-based Intel Triple Speed Ethernet MAC Intel FPGA IP core function in SGMII mode.
J15	QSFP Interface	Provides four transceiver channels for a 40G/100G QSFP module.
CN1	Micro-USB connector	Embedded Intel Intel FPGA Download Cable II JTAG for programming the FPGA via a USB cable.
Display Ports		
J12	Mini DisplayPort Connector	Mini DisplayPort male receptacle.
J17, J18	SDI video port	Two HDBNC connectors that provide a full-duplex SDI interface.
Power Supply		
J9	PCI Express edge connector	Interfaces to a PCI Express root port such as an appropriate PC motherboard.
J27	DC input jack	Accepts a 12 V DC power supply when powering the board from the provided power brick for lab bench operation. When operating from the PCIe slot, this input must also be connected to the 6-pin Aux PCIe power connector provided by the PC system along with J27, or else the board does not power on.
SW7	Power switch	Switch to power ON or OFF the board when supplied from the DC input jack.
J26	PCIe 2x4 ATX power connector	12 V ATX input. This input must be connected to the 8-pin Aux PCIe power connector provided by the PC system when the board is plugged into a PCIe slot, or else the board does not power on.

4.2. MAX V CPLD System Controller

The development board utilizes the EPM2210 System Controller, an Intel MAX V CPLD for the following purposes:

- FPGA configuration from flash memory
- Power consumption monitoring
- Temperature monitoring
- Fan control
- Control registers for clocks
- Control registers for remote update system

Table 11. MAX V CPLD System Controller Device Pin-Out

Schematic Signal Name	Pin Number	I/O Standard	Description
FMCA_PRSTn	G1	1.8V	FMC present
FPGA_AVST_CLK	J2	1.8V	Avalon stream clock
USB_MAX5_CLK	H5	1.8V	48 MHz USB clock
CLK_CONFIG	J5	1.8V	125 MHz configuration clock
FPGA_nSTATUS	J4	1.8V	Configuration nSTATUS signal
FPGA_CONF_DONE	K1	1.8V	Configuration DONE signal
USB_CFG2	K2	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG3	K5	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG4	L1	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG5	L2	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG6	K3	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG12	M1	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG7	M2	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG8	L4	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG9	L3	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG10	N1	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG0	M4	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG11	N2	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus

continued...

Schematic Signal Name	Pin Number	I/O Standard	Description
USB_CFG1	M3	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG13	N3	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG14	P2	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
FPGA_INIT_DONE	G4	1.8V	Initialization done signal
FPGA_AVST_VALID	F5	1.8V	Avalon stream valid signal
FPGA_AVST_READY	H1	1.8V	Avalon stream ready signal
FMCA_C2M_PWRGD	R16	1.8V	FMC card to mezzanine power good signal
M5_JTAG_TCK	P3	1.8V	Dedicated MAX V JTAG clock
M5_JTAG_TDI	L6	1.8V	Dedicated MAX V JTAG data in
M5_JTAG_TDO	M5	1.8V	Dedicated MAX V JTAG data out
M5_JTAG_TMS	N4	1.8V	Dedicated MAX V JTAG mode select
MAX_RESETn	C5	2.5V	MAX V reset signal
Si516_FS	A4	2.5V	Si516 device frequency select signal
OVERTEMP	E1	2.5V	FAN PWM control signal
CLK0_FINC	E9	2.5V	Si5341A device frequency increment signal
CLK0_FDEC	A10	2.5V	Si5341A device frequency decrement signal
MAX_CONF_DONE	D7	2.5V	Configuration done LED signal
CLK0_OEn	B12	2.5V	Si5341A device enable signal
CLK1_RSTn	C11	2.5V	Si5341A device reset signal
PGM_SEL	A7	2.5V	Program Select push button signal
PGM_CONFIG	A6	2.5V	Program Configuration push button signal
PGM_LED0	D6	2.5V	Program LED0 signal
PGM_LED1	C6	2.5V	Program LED1 signal
PGM_LED2	B7	2.5V	Program LED2 signal
FACTORY_LOAD	B5	2.5V	Load factory image DIP switch signal
MAX_ERROR	C7	2.5V	Configuration error LED
MAX_LOAD	B6	2.5V	Configuration loading LED

continued...

Schematic Signal Name	Pin Number	I/O Standard	Description
FPGA_PR_REQUEST	T4	1.8V	Partial reconfiguration request signal
FLASH_ADDR1	F15	1.8V	Flash address bus
FLASH_ADDR2	G16	1.8V	Flash address bus
FLASH_ADDR3	G15	1.8V	Flash address bus
FLASH_ADDR4	H16	1.8V	Flash address bus
FLASH_ADDR5	H15	1.8V	Flash address bus
FLASH_ADDR6	F16	1.8V	Flash address bus
FLASH_ADDR7	G14	1.8V	Flash address bus
FLASH_ADDR8	D16	1.8V	Flash address bus
FLASH_ADDR9	E15	1.8V	Flash address bus
FLASH_ADDR10	E16	1.8V	Flash address bus
FLASH_ADDR11	H14	1.8V	Flash address bus
FLASH_ADDR12	D15	1.8V	Flash address bus
FLASH_ADDR13	F14	1.8V	Flash address bus
FLASH_ADDR14	C14	1.8V	Flash address bus
FLASH_ADDR15	C15	1.8V	Flash address bus
FLASH_ADDR16	H3	1.8V	Flash address bus
FLASH_ADDR17	H2	1.8V	Flash address bus
FLASH_ADDR18	E13	1.8V	Flash address bus
FLASH_ADDR19	F13	1.8V	Flash address bus
FLASH_ADDR20	G13	1.8V	Flash address bus
FLASH_ADDR21	G12	1.8V	Flash address bus
FLASH_ADDR22	E12	1.8V	Flash address bus
FLASH_ADDR23	H13	1.8V	Flash address bus
FLASH_ADDR24	G5	1.8V	Flash address bus
FLASH_ADDR25	J13	1.8V	Flash address bus
FPGA_PR_DONE	J16	1.8V	Partial reconfiguration done signal
CLK_MAXV_50M	J12	1.8V	50 MHz MAX V clock
MAXV_OSC_CLK1	H12	1.8V	125 MHz MAX V clock
FLASH_DATA0	J15	1.8V	Flash data bus
FLASH_DATA1	L16	1.8V	Flash data bus
FLASH_DATA2	L14	1.8V	Flash data bus
FLASH_DATA3	K14	1.8V	Flash data bus

continued...

Schematic Signal Name	Pin Number	I/O Standard	Description
FLASH_DATA4	L13	1.8V	Flash data bus
FLASH_DATA5	L15	1.8V	Flash data bus
FLASH_DATA6	M15	1.8V	Flash data bus
FLASH_DATA7	M16	1.8V	Flash data bus
FLASH_DATA8	K16	1.8V	Flash data bus
FLASH_DATA9	K15	1.8V	Flash data bus
FLASH_DATA10	J14	1.8V	Flash data bus
FLASH_DATA11	K13	1.8V	Flash data bus
FLASH_DATA12	L12	1.8V	Flash data bus
FLASH_DATA13	N16	1.8V	Flash data bus
FLASH_DATA14	M13	1.8V	Flash data bus
FLASH_DATA15	L11	1.8V	Flash data bus
FLASH_CEn0	D14	1.8V	Flash chip enable 0
FLASH_OEn	P14	1.8V	Flash output enable
FLASH_RDYBSYn0	F12	1.8V	Flash ready/busy 0
FLASH_RESETn	D13	1.8V	Flash reset
FLASH_CLK	N15	1.8V	Flash clock
FLASH_ADVn	N14	1.8V	Flash address valid
FLASH_CEn1	F11	1.8V	Flash chip enable 1
FPGA_PR_ERROR	K12	1.8V	Partial reconfiguration error signal
FPGA_CvP_CONFDONE	M14	1.8V	CvP configuration done signal
FLASH_RDYBSYn1	P12	1.8V	Flash ready/busy 1
FPGA_CONFIG_D0	R1	1.8V	FPGA configuration data bus
FPGA_CONFIG_D1	T2	1.8V	FPGA configuration data bus
FPGA_CONFIG_D2	N6	1.8V	FPGA configuration data bus
FPGA_CONFIG_D3	N5	1.8V	FPGA configuration data bus
FPGA_CONFIG_D4	N7	1.8V	FPGA configuration data bus
FPGA_CONFIG_D5	N8	1.8V	FPGA configuration data bus
FPGA_CONFIG_D6	M12	1.8V	FPGA configuration data bus
FPGA_CONFIG_D7	T13	1.8V	FPGA configuration data bus
FPGA_CONFIG_D8	T15	1.8V	FPGA configuration data bus
FPGA_CONFIG_D9	R13	1.8V	FPGA configuration data bus
FPGA_CONFIG_D10	P4	1.8V	FPGA configuration data bus

continued...

Schematic Signal Name	Pin Number	I/O Standard	Description
FPGA_CONFIG_D11	R3	1.8V	FPGA configuration data bus
FPGA_CONFIG_D12	T10	1.8V	FPGA configuration data bus
FPGA_CONFIG_D13	P5	1.8V	FPGA configuration data bus
FPGA_CONFIG_D14	R4	1.8V	FPGA configuration data bus
FPGA_CONFIG_D15	R5	1.8V	FPGA configuration data bus
MAX5_OEn	N10	1.8V	MAX V output enable
MAX5_CSn	T11	1.8V	MAX V chip select
MAX5_WEn	R11	1.8V	MAX V write enable
MAX5_CLK	N11	1.8V	MAX V clock
MAX5_BEn0	R10	1.8V	MAX V byte enable
MAX5_BEn1	M10	1.8V	MAX V byte enable
MAX5_BEn2	T12	1.8V	MAX V byte enable
MAX5_BEn3	P10	1.8V	MAX V byte enable
CPU_RESETn	K4	1.8V	CPU reset button
I2C_1.8V_SCL	P13	1.8V	1.8V I^2C bus
I2C_1.8V_SDA	R14	1.8V	1.8V I^2C bus
OVERTEMPn_1.8V	N13	1.8V	Over temperature signal
TSENSE_ALERTn_1.8V	T7	1.8V	Temperature sense alert signal
QSPI_SS0_MSEL0	R12	1.8V	QSPI slave select 0/ MSEL [0] configuration select
MSEL1	P11	1.8V	MSEL [1] configuration select
MSEL2	M11	1.8V	MSEL [2] configuration select
SDI_MF2_MUTE	R7	1.8V	SDI device MF2
SDI_MF0_BYPASS	P8	1.8V	SDI device MF0
SDI_MF1_AUTO_SLEEP	R6	1.8V	SDI device MF1
SDI_TX_SD_HDn	P6	1.8V	SDI device SD/HD
FPGA_nCONFIG	E14	1.8V	nCONFIG configuration signal

4.3. FPGA Configuration

You can use the Quartus Programmer to configure the FPGA with your SRAM Object File (**.sof**).

Ensure the following:

- The Quartus Programmer and the Intel FPGA Download Cable II driver are installed on the host computer.
- The micro-USB cable is connected to the FPGA development board.
- Power to the board is ON, and no other applications that use the JTAG chain are running.

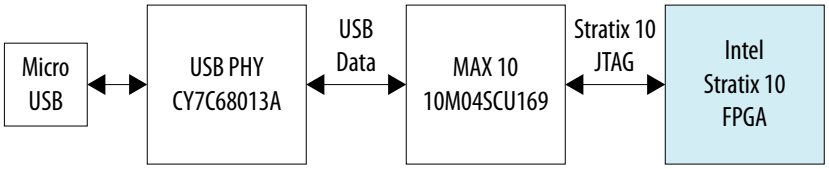
1. Start the Quartus Programmer.
2. Click **Auto Detect** to display the devices in the JTAG chain.
3. Click **Change File** and select the path to the desired **.sof**.
4. Turn on the **Program/Configure** option for the added file.
5. Click Start to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

Using the Quartus Programmer to configure a device on the board causes other JTAG-based applications such as the Board Test System and the Power Monitor to lose their connection to the board. Restart those applications after configuration is complete.

Programming the FPGA over Embedded Intel FPGA Download Cable II

The figure below shows the high-level conceptual block diagram for programming the Intel Stratix 10 FPGA over the Intel FPGA Download Cable II.

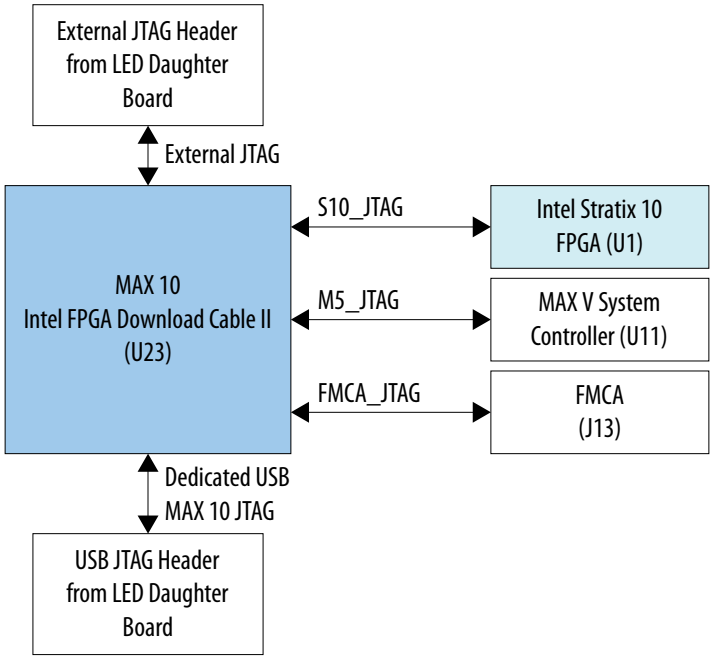
Figure 7. Intel FPGA Download Cable II Conceptual Block Diagram



Programming the FPGA over External Intel FPGA Download Cable II

The figure below shows the high-level conceptual block diagram for programming the Intel Stratix 10 FPGA over an external Intel FPGA Download Cable II.

Figure 8. JTAG Chain Conceptual Block Diagram



4.4. Status Elements

The Intel Stratix 10 GX FPGA development board includes status LEDs as listed below.

Table 12. Board-Specific Status LEDs

Board Reference	Schematic Signal Name	I/O Standard
D3 on the LED board	MAX_ERROR	2.5V
D6 on the LED board	MAX_LOAD	2.5V
D8 on the LED board	MAX_CONF_DONE	2.5V
D12 on the LED board	FMCA_TX_LED	1.8V
D11 on the LED board	FMCA_RX_LED	1.8V
D1 on the LED board	PGM_LED0	2.5V
D2 on the LED board	PGM_LED1	2.5V
D5 on the LED board	PGM_LED2	2.5V
D13 on the LED board	FMCA_PRSTn	1.8V
D15 on the LED board	PCIE_LED_X1	1.8V
D17 on the LED board	PCIE_LED_X4	1.8V
D19 on the LED board	PCIE_LED_X8	1.8V
D20 on the LED board	PCIE_LED_X16	1.8V
D22 on the LED board	PCIE_LED_G2	1.8V
D23 on the LED board	PCIE_LED_G3	1.8V
D14 on the LED board	JTAG_RX	1.8V
D16 on the LED board	JTAG_TX	1.8V
D18 on the LED board	SC_RX	1.8V
D21 on the LED board	SC_TX	1.8V
D4 on the LED board	USER_LED_G0, USER_LED_R0	1.8V
D7 on the LED board	USER_LED_G1, USER_LED_R1	1.8V
D9 on the LED board	USER_LED_G2, USER_LED_R2	1.8V

4.5. User Input-Output Components

4.5.1. User-Defined Push Buttons

The Intel Stratix 10 GX FPGA development board includes user-defined push buttons. When you press and hold down the button, the device pin is set to logic 0. When you release the button, the device pin is set to logic 1. There are no board-specific functions for these general user push buttons.

Table 13. User-defined Push Buttons

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard
S7 on LED board	USER_PB2	B17	1.8V
S6 on LED board	USER_PB1	A19	1.8V
S5 on LED board	USER_PB0	B20	1.8V
S4 on LED board	CPU_RESETn	A20	1.8V
S2 on LED board	PGM_SEL	–	2.5V
S1 on LED board	PGM_CONFIG	–	2.5V
S3 on LED board	MAX_RESETn	–	2.5V

4.5.2. User-Defined DIP Switches

The Intel Stratix 10 GX FPGA development board includes a set of four pin DIP switch. There are no board-specific functions for these switches. When the switch is in the OFF position, logic 1 is selected. When the switch is in the ON position, logic 0 is selected.

Table 14. User-defined DIP Switches

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard
SW1.1 on LED board	USER_DIPSW0	H18	1.8V
SW1.2 on LED board	USER_DIPSW1	G18	1.8V
SW1.3 on LED board	USER_DIPSW2	H20	1.8V
SW1.4 on LED board	USER_DIPSW3	G20	1.8V

4.5.3. User-Defined LEDs

The Intel Stratix 10 GX FPGA development board includes a set of four pairs of user-defined LEDs. The LEDs illuminate when a logic 0 is driven, and turn OFF when a logic 1 is driven. There are no board-specific functions for these LEDs.

Table 15. User-defined LEDs

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard
D4 on LED board	USER_LED_G0	B19	1.8V
D7 on LED board	USER_LED_G1	E17	1.8V
D9 on LED board	USER_LED_G2	D18	1.8V

continued...

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard
D10 on LED board	USER_LED_G3	D19	1.8V
D4 on LED board	USER_LED_R0	B18	1.8V
D7 on LED board	USER_LED_R1	F17	1.8V
D9 on LED board	USER_LED_R2	E18	1.8V
D10 on LED board	USER_LED_R3	E19	1.8V

4.6. Components and Interfaces

This section describes the development board's communication ports and interface cards relative to the Intel Stratix 10 GX FPGA device.

4.6.1. PCI Express

The Intel Stratix 10 GX FPGA development board is designed to fit entirely into a PC motherboard with a x16 PCI Express slot that can accommodate a full height, 3-slot long form factor add-in card. This interface uses the Intel Stratix 10 GX FPGA's PCI Express hard IP block, saving logic resources for the user logic application. The PCI Express edge connector has a presence detect feature to allow the motherboard to determine if a card is installed.

The PCI Express interface supports auto-negotiating channel width from x1 to x4 to x8 to x16 by using Intel's PCIe Intel FPGA IP. You can also configure this board to a x1, x4, x8 or x16 interface through a DIP switch that connects the PRSTn pins for each bus width.

The PCI Express edge connector has a connection speed of 2.5 Gbps/lane for a maximum of 40 Gbps full-duplex (Gen1), 5.0 Gbps/lane for maximum of 80 Gbps full-duplex (Gen 2), or 8.0 Gbps/lane for a maximum of 128 Gbps full-duplex (Gen3).

The power for the board can be sourced entirely from the PC host when installed into a PC motherboard with the PC's 2x3 and 2x4 ATX auxiliary power connected to the 12V ATX inputs (J26 and J27) of the Intel Stratix 10 development board. Although the board can also be powered by a laptop power supply for use on a lab bench, Intel recommends that you do not power up from both supplies at the same time. Ideal diode power sharing devices have been designed into this board to prevent damages or back-current from one supply to the other.

The PCIE_EDGE_REFCLK_P/N signal is a 100 MHz differential input that is driven from the PC motherboard onto this board through the edge connector. This signal connects directly to a Intel Stratix 10 GX FPGA REFCLK input pin pair using DC coupling. This clock is terminated on the motherboard and therefore, no on-board termination is required. This clock can have spread-spectrum properties that change its period between 9.847 ps to 10.203 ps. The I/O standard is High-Speed Current Steering Logic (HCSL). The JTAG and SMB are optional signals in the PCI Express TDI to PCI Express TDO and are not used on this board. The SMB signals are wired to the Intel Stratix 10 GX FPGA but are not required for normal operation.

Table 16. PCI Express Pin Assignments, Schematic Signal Names and Functions

Receive bus	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
A11	PCIE_EDGE_PERSTn	-	3V LVCMOS	Reset
A14	PCIE_EDGE_REFCLK_N	AK40	LVDS	Motherboard reference clock
A13	PCIE_EDGE_REFCLK_P	AK41	LVDS	Motherboard reference clock
B5	PCIE_EDGE_SMBCLK	-	1.8V	SMB clock
B6	PCIE_EDGE_SMBDAT	-	1.8V	SMB data

continued...

Receive bus	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
A1	PCIE_PRSNT1n	–	–	Link with DIP switch (SW2)
B17	PCIE_PRSNT2n_X1	–	–	Link with DIP switch (SW2)
B31	PCIE_PRSNT2n_X4	–	–	Link with DIP switch (SW2)
B48	PCIE_PRSNT2n_X8	–	–	Link with DIP switch (SW2)
B81	PCIE_PRSNT2n_X16	–	–	Link with DIP switch (SW2)
B15	PCIE_RX_N0	BH40	1.4 V PCML	Receive bus
B20	PCIE_RX_N1	BJ42	1.4 V PCML	Receive bus
B24	PCIE_RX_N2	BG42	1.4 V PCML	Receive bus
B28	PCIE_RX_N3	BE42	1.4 V PCML	Receive bus
B34	PCIE_RX_N4	BC42	1.4 V PCML	Receive bus
B38	PCIE_RX_N5	BD44	1.4 V PCML	Receive bus
B42	PCIE_RX_N6	BA42	1.4 V PCML	Receive bus
B46	PCIE_RX_N7	BB44	1.4 V PCML	Receive bus
B51	PCIE_RX_N8	AW42	1.4 V PCML	Receive bus
B55	PCIE_RX_N9	AY44	1.4 V PCML	Receive bus
B59	PCIE_RX_N10	AU42	1.4 V PCML	Receive bus
B63	PCIE_RX_N11	AV44	1.4 V PCML	Receive bus
B67	PCIE_RX_N12	AR42	1.4 V PCML	Receive bus
B71	PCIE_RX_N13	AT44	1.4 V PCML	Receive bus
B75	PCIE_RX_N14	AP44	1.4 V PCML	Receive bus
B79	PCIE_RX_N15	AN42	1.4 V PCML	Receive bus
B14	PCIE_RX_P0	BH41	1.4 V PCML	Receive bus
B19	PCIE_RX_P1	BJ43	1.4 V PCML	Receive bus
B23	PCIE_RX_P2	BG43	1.4 V PCML	Receive bus
B27	PCIE_RX_P3	BE43	1.4 V PCML	Receive bus
B33	PCIE_RX_P4	BC43	1.4 V PCML	Receive bus
B37	PCIE_RX_P5	BD45	1.4 V PCML	Receive bus
B41	PCIE_RX_P6	BA43	1.4 V PCML	Receive bus
B45	PCIE_RX_P7	BB45	1.4 V PCML	Receive bus
B50	PCIE_RX_P8	AW43	1.4 V PCML	Receive bus
B54	PCIE_RX_P9	AY45	1.4 V PCML	Receive bus

continued...

Receive bus	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
B58	PCIE_RX_P10	AU43	1.4 V PCML	Receive bus
B62	PCIE_RX_P11	AV45	1.4 V PCML	Receive bus
B66	PCIE_RX_P12	AR43	1.4 V PCML	Receive bus
B70	PCIE_RX_P13	AT45	1.4 V PCML	Receive bus
B74	PCIE_RX_P14	AP45	1.4 V PCML	Receive bus
B78	PCIE_RX_P15	AN43	1.4 V PCML	Receive bus
B11	PCIE_WAKEn_R	AU34	1.8V	Wake Signal

4.6.2. 10/100/1000 Ethernet PHY

The Intel Stratix 10 GX FPGA development board supports 10/100/1000 base-T Ethernet using an external Marvell 88E1111 PHY and Intel Triple-Speed Ethernet Intel FPGA IP core MAC function. The PHY-to-MAC interface employs SGMII using the Intel Stratix 10 GX FPGA LVDS pins in Soft-CDR mode at 1.25 Gbps transmit and receive. In 10 Mb or 100 Mb mode, the SGMII interface still runs at 1.25 GHz but the packet data is repeated 10 or 100 times. The MAC function must be provided in the FPGA for typical networking applications.

The Marvell 88E1111 PHY uses a 2.5V and 1.0V power rails and requires a 25 MHz reference clock driven from a dedicated oscillator. The PHY interfaces to a HALO HFJ11-1G02E model RJ45 with internal magnetics that can be used for driving copper lines with Ethernet traffic.

Figure 9. SGMII Interface between FPGA (MAC) and Marvell 88E1111 PHY

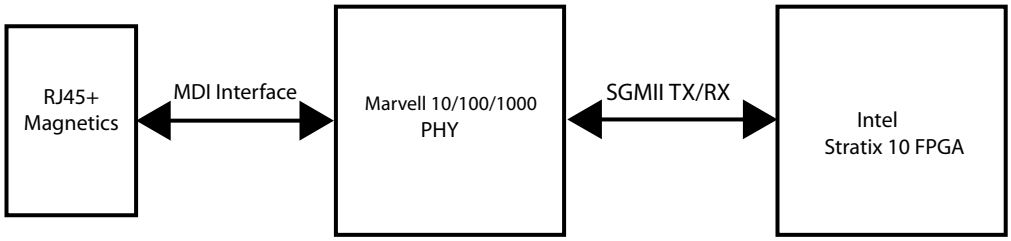


Table 17. Ethernet PHY Pin Assignments, Signal Names and Functions

Board Reference (U13)	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
23	ENET_INTn	AC35	3.0V	Management bus interrupt
25	ENET_MDC	AD35	3.0V	Management bus data clock
24	ENET_MDIO	AD34	3.0V	Management bus data
28	ENET_RESETn	AB34	3.0V	Device reset
76	ENET_LED_LINK10	–	2.5V	10 Mb link LED
74	ENET_LED_LINK100	–	2.5V	100 Mb LED

continued...

Board Reference (U13)	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
73	ENET_LED_LINK1000	–	2.5V	1000 Mb link LED
69	ENET_LED_RX	–	2.5V	RX data active LED
68	ENET_LED_TX	–	2.5V	TX data active LED
75	ENET_RX_N	AW25	LVDS	SGMII receive channel
77	ENET_RX_P	AV25	LVDS	SGMII receive channel
81	ENET_TX_N	AT25	LVDS	SGMII transmit channel
82	ENET_TX_P	AU25	LVDS	SGMII transmit channel
55	ENET_XTAL_25MHZ	–	2.5V	25 MHz RGMII transmit clock
31	MDI_N0	–	2.5V	Media dependent interface
34	MDI_N1	–	2.5V	Media dependent interface
41	MDI_N2	–	2.5V	Media dependent interface
43	MDI_N3	–	2.5V	Media dependent interface
29	MDI_P0	–	2.5V	Media dependent interface
33	MDI_P1	–	2.5V	Media dependent interface
39	MDI_P2	–	2.5V	Media dependent interface
42	MDI_P3	–	2.5V	Media dependent interface

4.6.3. HiLo External Memory Interface

This section describes the Intel Stratix 10 GX FPGA development board's external memory interface support and also their signal names, types and connectivity relative to the Intel Stratix 10 GX FPGA.

The HiLo connector supports plugins for the following memory interfaces:

- DDR3 x72 (included in the kit)
- DDR4 x72 (included in the kit)
- RLDRAM3 x36 (included in the kit)

Table 18. HiLo EMI Pin Assignments

Board Reference - HiLo Pin Number	HiLo Schematic Signal Name	FPGA Pin Number	I/O Standard
F1	MEM_ADDR_CMD0	K38	Adjustable
H1	MEM_ADDR_CMD1	L37	Adjustable

continued...

Board Reference - HiLo Pin Number	HiLo Schematic Signal Name	FPGA Pin Number	I/O Standard
F2	MEM_ADDR_CMD2	M37	Adjustable
G2	MEM_ADDR_CMD3	M38	Adjustable
H2	MEM_ADDR_CMD4	J39	Adjustable
J2	MEM_ADDR_CMD5	J38	Adjustable
K2	MEM_ADDR_CMD6	K39	Adjustable
G3	MEM_ADDR_CMD7	L39	Adjustable
J3	MEM_ADDR_CMD8	P37	Adjustable
L3	MEM_ADDR_CMD9	R37	Adjustable
E4	MEM_ADDR_CMD10	N37	Adjustable
F4	MEM_ADDR_CMD11	P38	Adjustable
G4	MEM_ADDR_CMD12	P35	Adjustable
H4	MEM_ADDR_CMD13	K36	Adjustable
J4	MEM_ADDR_CMD14	K37	Adjustable
K4	MEM_ADDR_CMD15	N36	Adjustable
M1	MEM_ADDR_CMD16	L36	Adjustable
M2	MEM_ADDR_CMD17	T35	Adjustable
N2	MEM_ADDR_CMD18	R36	Adjustable
L4	MEM_ADDR_CMD19	L35	Adjustable
P5	MEM_ADDR_CMD20	L40	Adjustable
M5	MEM_ADDR_CMD21	K40	Adjustable
P1	MEM_ADDR_CMD22	G38	Adjustable
R4	MEM_ADDR_CMD23	H38	Adjustable
M4	MEM_ADDR_CMD24	G40	Adjustable
R3	MEM_ADDR_CMD25	F40	Adjustable
L2	MEM_ADDR_CMD26	P36	Adjustable
K1	MEM_ADDR_CMD27	E40	Adjustable
P2	MEM_ADDR_CMD28	D40	Adjustable
N4	MEM_ADDR_CMD29	R33	Adjustable
P4	MEM_ADDR_CMD30	J40	Adjustable
N3	MEM_ADDR_CMD31	H40	Adjustable
V2	MEM_CLK_N	G39	Adjustable
V1	MEM_CLK_P	F39	Adjustable
B10	MEM_DMA0	E27	Adjustable
C4	MEM_DMA1	M27	Adjustable

continued...

Board Reference - HiLo Pin Number	HiLo Schematic Signal Name	FPGA Pin Number	I/O Standard
B17	MEM_DMA2	V30	Adjustable
F17	MEM_DMA3	P25	Adjustable
M16	MEM_DMB0	K32	Adjustable
U16	MEM_DMB1	J33	Adjustable
U11	MEM_DMB2	F37	Adjustable
U6	MEM_DMB3	C36	Adjustable
R6	MEM_DQ_ADDR_CMD0	T31	Adjustable
T1	MEM_DQ_ADDR_CMD1	R34	Adjustable
R2	MEM_DQ_ADDR_CMD2	R31	Adjustable
T2	MEM_DQ_ADDR_CMD3	U33	Adjustable
U2	MEM_DQ_ADDR_CMD4	U34	Adjustable
U3	MEM_DQ_ADDR_CMD5	T34	Adjustable
T4	MEM_DQ_ADDR_CMD6	U32	Adjustable
U4	MEM_DQ_ADDR_CMD7	V32	Adjustable
T5	MEM_DQ_ADDR_CMD8	P33	Adjustable
A4	MEM_DQA0	B27	Adjustable
B4	MEM_DQA1	F27	Adjustable
B5	MEM_DQA2	G27	Adjustable
B6	MEM_DQA3	C27	Adjustable
A8	MEM_DQA4	C26	Adjustable
B8	MEM_DQA5	B25	Adjustable
B9	MEM_DQA6	D26	Adjustable
A10	MEM_DQA7	D25	Adjustable
B1	MEM_DQA8	H27	Adjustable
B2	MEM_DQA9	H26	Adjustable
C2	MEM_DQA10	J25	Adjustable
C3	MEM_DQA11	H25	Adjustable
E3	MEM_DQA12	L27	Adjustable
D4	MEM_DQA13	L26	Adjustable
D1	MEM_DQA14	G25	Adjustable
D2	MEM_DQA15	K27	Adjustable
A12	MEM_DQA16	U29	Adjustable
B12	MEM_DQA17	T30	Adjustable
B13	MEM_DQA18	T29	Adjustable

continued...

Board Reference - HiLo Pin Number	HiLo Schematic Signal Name	FPGA Pin Number	I/O Standard
B14	MEM_DQA19	V26	Adjustable
C15	MEM_DQA20	U30	Adjustable
A16	MEM_DQA21	V25	Adjustable
B16	MEM_DQA22	U28	Adjustable
A18	MEM_DQA23	U27	Adjustable
C16	MEM_DQA24	T25	Adjustable
D16	MEM_DQA25	N27	Adjustable
E16	MEM_DQA26	L25	Adjustable
F16	MEM_DQA27	U25	Adjustable
D17	MEM_DQA28	N26	Adjustable
C18	MEM_DQA29	R26	Adjustable
D18	MEM_DQA30	P26	Adjustable
E18	MEM_DQA31	N25	Adjustable
E2	MEM_DQA32	F25	Adjustable
G16	MEM_DQA33	M25	Adjustable
H16	MEM_DQB0	K34	Adjustable
J16	MEM_DQB1	K33	Adjustable
K16	MEM_DQB2	N33	Adjustable
L16	MEM_DQB3	M33	Adjustable
H17	MEM_DQB4	J34	Adjustable
K17	MEM_DQB5	N32	Adjustable
K18	MEM_DQB6	N31	Adjustable
L18	MEM_DQB7	M34	Adjustable
M17	MEM_DQB8	E34	Adjustable
N18	MEM_DQB9	F34	Adjustable
P17	MEM_DQB10	H35	Adjustable
P18	MEM_DQB11	J35	Adjustable
R18	MEM_DQB12	G35	Adjustable
T16	MEM_DQB13	H36	Adjustable
T17	MEM_DQB14	F35	Adjustable
T18	MEM_DQB15	H33	Adjustable
U15	MEM_DQB16	D34	Adjustable
T14	MEM_DQB17	E38	Adjustable
U14	MEM_DQB18	D38	Adjustable

continued...

Board Reference - HiLo Pin Number	HiLo Schematic Signal Name	FPGA Pin Number	I/O Standard
V14	MEM_DQB19	E37	Adjustable
T13	MEM_DQB20	D35	Adjustable
T12	MEM_DQB21	D39	Adjustable
U12	MEM_DQB22	E39	Adjustable
V12	MEM_DQB23	H37	Adjustable
T10	MEM_DQB24	A37	Adjustable
U10	MEM_DQB25	B38	Adjustable
V10	MEM_DQB26	C38	Adjustable
T9	MEM_DQB27	A38	Adjustable
T8	MEM_DQB28	C37	Adjustable
U8	MEM_DQB29	B37	Adjustable
U7	MEM_DQB30	B35	Adjustable
V6	MEM_DQB31	C35	Adjustable
R16	MEM_DQB32	J36	Adjustable
T6	MEM_DQB33	D36	Adjustable
V5	MEM_DQS_ADDR_CMD_N	T32	Adjustable
V4	MEM_DQS_ADDR_CMD_P	R32	Adjustable
A7	MEM_DQSA_N0	F26	Adjustable
A3	MEM_DQSA_N1	K26	Adjustable
A15	MEM_DQSA_N2	V27	Adjustable
G18	MEM_DQSA_N3	R27	Adjustable
A6	MEM_DQSA_P0	E26	Adjustable
A2	MEM_DQSA_P1	J26	Adjustable
A14	MEM_DQSA_P2	V28	Adjustable
F18	MEM_DQSA_P3	T26	Adjustable
J18	MEM_DQSB_N0	L31	Adjustable
V18	MEM_DQSB_N1	G34	Adjustable
V17	MEM_DQSB_N2	F36	Adjustable
V9	MEM_DQSB_N3	A35	Adjustable
H18	MEM_DQSB_P0	L32	Adjustable
U18	MEM_DQSB_P1	G33	Adjustable
V16	MEM_DQSB_P2	E36	Adjustable
V8	MEM_DQSB_P3	A36	Adjustable
A11	MEM_QKA_P0	C25	Adjustable

continued...

Board Reference - HiLo Pin Number	HiLo Schematic Signal Name	FPGA Pin Number	I/O Standard
B18	MEM_QKA_P1	T27	Adjustable
M18	MEM_QKB_P0	L34	Adjustable
V13	MEM_QKB_P1	G37	Adjustable

4.6.4. FMC

The Intel Stratix 10 GX FPGA development board includes a high pin count (HPC) FPGA mezzanine card (FMC) connector that functions with a quadrature amplitude modulation (QAM) digital-to-analog converter (DAC) FMC module or daughtercard. This pin-out satisfies a QAM DAC that requires 58 low-voltage differential signaling (LVDS) data output pairs, one LVDS input clock pair and three low-voltage LVDS control pairs from the FPGA device. These pins also have the option to be used as single-ended I/O pins. The VCCIO supply for the FMC banks in the low pin count (LPC) and HPC provide a variable voltage of 1.2V, 1.35V, 1.5V and 1.8V (default).

Table 19. FMC Connector Pin Assignments

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard
D1	FMCA_C2M_PG	–	–
H5	FMCA_CLK_M2C_N0	AT17	Adjustable
G3	FMCA_CLK_M2C_N1	AR19	Adjustable
H4	FMCA_CLK_M2C_P0	AU17	Adjustable
G2	FMCA_CLK_M2C_P1	AT19	Adjustable
C3	FMCA_DP_C2M_N0	BJ5	1.4V PCML
A23	FMCA_DP_C2M_N1	BF6	1.4V PCML
A27	FMCA_DP_C2M_N2	BG4	1.4V PCML
A31	FMCA_DP_C2M_N3	BE4	1.4V PCML
A35	FMCA_DP_C2M_N4	BF2	1.4V PCML
A39	FMCA_DP_C2M_N5	BC4	1.4V PCML
B37	FMCA_DP_C2M_N6	BD2	1.4V PCML
B33	FMCA_DP_C2M_N7	BA4	1.4V PCML
B29	FMCA_DP_C2M_N8	BB2	1.4V PCML
B25	FMCA_DP_C2M_N9	AW4	1.4V PCML
K23	FMCA_DP_C2M_N10	AY2	1.4V PCML
K26	FMCA_DP_C2M_N11	AU4	1.4V PCML
K29	FMCA_DP_C2M_N12	AV2	1.4V PCML
K32	FMCA_DP_C2M_N13	AR4	1.4V PCML
K35	FMCA_DP_C2M_N14	AT2	1.4V PCML
K38	FMCA_DP_C2M_N15	AP2	1.4V PCML

continued...

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard
C2	FMCA_DP_C2M_P0	BJ4	1.4V PCML
A22	FMCA_DP_C2M_P1	BF5	1.4V PCML
A26	FMCA_DP_C2M_P2	BG3	1.4V PCML
A30	FMCA_DP_C2M_P3	BE3	1.4V PCML
A34	FMCA_DP_C2M_P4	BF1	1.4V PCML
A38	FMCA_DP_C2M_P5	BC3	1.4V PCML
B36	FMCA_DP_C2M_P6	BD1	1.4V PCML
B32	FMCA_DP_C2M_P7	BA3	1.4V PCML
B28	FMCA_DP_C2M_P8	BB1	1.4V PCML
B24	FMCA_DP_C2M_P9	AW3	1.4V PCML
K22	FMCA_DP_C2M_P10	AY1	1.4V PCML
K25	FMCA_DP_C2M_P11	AU3	1.4V PCML
K28	FMCA_DP_C2M_P12	AV1	1.4V PCML
K31	FMCA_DP_C2M_P13	AR3	1.4V PCML
K34	FMCA_DP_C2M_P14	AT1	1.4V PCML
K37	FMCA_DP_C2M_P15	AP1	1.4V PCML
C7	FMCA_DP_M2C_N0	BH10	1.4V PCML
A3	FMCA_DP_M2C_N1	BJ8	1.4V PCML
A7	FMCA_DP_M2C_N2	BG8	1.4V PCML
A11	FMCA_DP_M2C_N3	BE8	1.4V PCML
A15	FMCA_DP_M2C_N4	BC8	1.4V PCML
A19	FMCA_DP_M2C_N5	BD6	1.4V PCML
B17	FMCA_DP_M2C_N6	BA8	1.4V PCML
B13	FMCA_DP_M2C_N7	BB6	1.4V PCML
B9	FMCA_DP_M2C_N8	AW8	1.4V PCML
B5	FMCA_DP_M2C_N9	AY6	1.4V PCML
K5	FMCA_DP_M2C_N10	AU8	1.4V PCML
K8	FMCA_DP_M2C_N11	AV6	1.4V PCML
K11	FMCA_DP_M2C_N12	AR8	1.4V PCML
K14	FMCA_DP_M2C_N13	AT6	1.4V PCML
K17	FMCA_DP_M2C_N14	AP6	1.4V PCML
K20	FMCA_DP_M2C_N15	AN8	1.4V PCML
C6	FMCA_DP_M2C_P0	BH9	1.4V PCML
A2	FMCA_DP_M2C_P1	BJ7	1.4V PCML

continued...

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard
A6	FMCA_DP_M2C_P2	BG7	1.4V PCML
A10	FMCA_DP_M2C_P3	BE7	1.4V PCML
A14	FMCA_DP_M2C_P4	BC7	1.4V PCML
A18	FMCA_DP_M2C_P5	BD5	1.4V PCML
B16	FMCA_DP_M2C_P6	BA7	1.4V PCML
B12	FMCA_DP_M2C_P7	BB5	1.4V PCML
B8	FMCA_DP_M2C_P8	AW7	1.4V PCML
B4	FMCA_DP_M2C_P9	AY5	1.4V PCML
K4	FMCA_DP_M2C_P10	AU7	1.4V PCML
K7	FMCA_DP_M2C_P11	AV5	1.4V PCML
K10	FMCA_DP_M2C_P12	AR7	1.4V PCML
K13	FMCA_DP_M2C_P13	AT5	1.4V PCML
K16	FMCA_DP_M2C_P14	AP5	1.4V PCML
K19	FMCA_DP_M2C_P15	AN7	1.4V PCML
C34	FMCA_GA0	BJ20	Adjustable
D35	FMCA_GA1	BJ19	Adjustable
D5	FMCA_GBTCLK_M2C_N0	AP10	LVDS
B21	FMCA_GBTCLK_M2C_N1	AM10	LVDS
D4	FMCA_GBTCLK_M2C_P0	AP9	LVDS
B20	FMCA_GBTCLK_M2C_P1	AM9	LVDS
D34	FMCA_JTAG_RST	–	–
D29	FMCA_JTAG_TCK	–	–
D30	FMCA_JTAG_TDI	–	–
D31	FMCA_JTAG_TDO	–	–
D33	FMCA_JTAG_TMS	–	–
G7	FMCA_LA_RX_CLK_N0	AV10	LVDS
D9	FMCA_LA_RX_CLK_N1	BE21	LVDS
G6	FMCA_LA_RX_CLK_P0	AW10	LVDS
D8	FMCA_LA_RX_CLK_P1	BF21	LVDS
G10	FMCA_LA_RX_N0	AN18	LVDS
C11	FMCA_LA_RX_N1	AR21	LVDS
G13	FMCA_LA_RX_N2	AR18	LVDS
C15	FMCA_LA_RX_N3	AP20	LVDS
G16	FMCA_LA_RX_N4	AP16	LVDS

continued...

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard
C19	FMCA_LA_RX_N5	BA19	LVDS
G19	FMCA_LA_RX_N6	AR16	LVDS
C23	FMCA_LA_RX_N7	BF19	LVDS
G22	FMCA_LA_RX_N8	AT16	LVDS
G25	FMCA_LA_RX_N9	AT14	LVDS
G28	FMCA_LA_RX_N10	AU14	LVDS
C27	FMCA_LA_RX_N11	BJ18	LVDS
G31	FMCA_LA_RX_N12	AU13	LVDS
G34	FMCA_LA_RX_N13	AY13	LVDS
G37	FMCA_LA_RX_N14	BE11	LVDS
G9	FMCA_LA_RX_P0	AN17	LVDS
C10	FMCA_LA_RX_P1	AT21	LVDS
G12	FMCA_LA_RX_P2	AP18	LVDS
C14	FMCA_LA_RX_P3	AN20	LVDS
G15	FMCA_LA_RX_P4	AP15	LVDS
C18	FMCA_LA_RX_P5	BB19	LVDS
G18	FMCA_LA_RX_P6	AR17	LVDS
C22	FMCA_LA_RX_P7	BE19	LVDS
G21	FMCA_LA_RX_P8	AT15	LVDS
G24	FMCA_LA_RX_P9	AR14	LVDS
G27	FMCA_LA_RX_P10	AU15	LVDS
C26	FMCA_LA_RX_P11	BH18	LVDS
G30	FMCA_LA_RX_P12	AV13	LVDS
G33	FMCA_LA_RX_P13	AW13	LVDS
G36	FMCA_LA_RX_P14	BE12	LVDS
H8	FMCA_LA_TX_N0	AP14	LVDS
H11	FMCA_LA_TX_N1	AU12	LVDS
D12	FMCA_LA_TX_N2	AU20	LVDS
H14	FMCA_LA_TX_N3	AV12	LVDS
D15	FMCA_LA_TX_N4	AW20	LVDS
H17	FMCA_LA_TX_N5	AW11	LVDS
D18	FMCA_LA_TX_N6	BB18	LVDS
H20	FMCA_LA_TX_N7	AY12	LVDS
D21	FMCA_LA_TX_N8	BD18	LVDS

continued...

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard
H23	FMCA_LA_TX_N9	BA11	LVDS
H26	FMCA_LA_TX_N10	BB12	LVDS
D24	FMCA_LA_TX_N11	BF17	LVDS
H29	FMCA_LA_TX_N12	BB10	LVDS
D27	FMCA_LA_TX_N13	BH17	LVDS
H32	FMCA_LA_TX_N14	BC11	LVDS
H35	FMCA_LA_TX_N15	BD10	LVDS
H38	FMCA_LA_TX_N16	BF10	LVDS
H7	FMCA_LA_TX_P0	AP13	LVDS
H10	FMCA_LA_TX_P1	AT12	LVDS
D11	FMCA_LA_TX_P2	AT20	LVDS
H13	FMCA_LA_TX_P3	AV11	LVDS
D14	FMCA_LA_TX_P4	AW19	LVDS
H16	FMCA_LA_TX_P5	AY11	LVDS
D17	FMCA_LA_TX_P6	BC18	LVDS
H19	FMCA_LA_TX_P7	BA12	LVDS
D20	FMCA_LA_TX_P8	BE18	LVDS
H22	FMCA_LA_TX_P9	BA10	LVDS
H25	FMCA_LA_TX_P10	BC12	LVDS
D23	FMCA_LA_TX_P11	BE17	LVDS
H28	FMCA_LA_TX_P12	BC10	LVDS
D26	FMCA_LA_TX_P13	BG17	LVDS
H31	FMCA_LA_TX_P14	BD11	LVDS
H34	FMCA_LA_TX_P15	BE10	LVDS
H37	FMCA_LA_TX_P16	BF11	LVDS
F1	FMCA_M2C_PG	–	–
H2	FMCA_PRSNTN	B22	1.8V
C30	FMCA_SCL	BH21	3.3V
C31	FMCA_SDA	BH20	3.3V
J39	VIO_B_M2C	–	–
K40	VIO_B_M2C	–	–
K1	VREF_B_M2C	–	–
H1	VREF_FMC	–	–

4.6.5. QSFP

The Intel Stratix 10 GX FPGA development board includes a Quad Small Form-Factor Pluggable (QSFP) module.

Table 20. QSFP Pin Assignments

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
28	QSFP1_3p3V_INTERRUPTn	BE26	1.8V	QSFP interrupt
31	QSFP1_3p3V_LP_MODE	BD26	1.8V	QSFP low power mode
27	QSFP1_3p3V_MOD_PRSn	BF27	1.8V	Module present
8	QSFP1_3p3V_MOD_SELn	BF26	1.8V	Module select
9	QSFP1_3p3V_RSTn	BE27	1.8V	Module reset
11	QSFP1_3p3V_SCL	BJ26	1.8V	QSFP serial 2-wire clock
12	QSFP1_3p3V_SDA	BH27	1.8V	QSFP serial 2-wire data
18	QSFP1_RX_N0	AC42	1.4V PCML	QSFP receiver data
21	QSFP1_RX_N1	W42	1.4V PCML	QSFP receiver data
15	QSFP1_RX_N2	AB44	1.4V PCML	QSFP receiver data
24	QSFP1_RX_N3	AD44	1.4V PCML	QSFP receiver data
17	QSFP1_RX_P0	AC43	1.4V PCML	QSFP receiver data
22	QSFP1_RX_P1	W43	1.4V PCML	QSFP receiver data
14	QSFP1_RX_P2	AB45	1.4V PCML	QSFP receiver data
25	QSFP1_RX_P3	AD45	1.4V PCML	QSFP receiver data
37	QSFP1_TX_N0	AE46	1.4V PCML	QSFP transmitter data
2	QSFP1_TX_N1	AB48	1.4V PCML	QSFP transmitter data
34	QSFP1_TX_N2	AA46	1.4V PCML	QSFP transmitter data
5	QSFP1_TX_N3	AC46	1.4V PCML	QSFP transmitter data
36	QSFP1_TX_P0	AE47	1.4V PCML	QSFP transmitter data
3	QSFP1_TX_P1	AB49	1.4V PCML	QSFP transmitter data
33	QSFP1_TX_P2	AA47	1.4V PCML	QSFP transmitter data
6	QSFP1_TX_P3	AC47	1.4V PCML	QSFP transmitter data

4.6.6. I²C

I²C supports communication between integrated circuits on a board. It is a simple two-wire bus that consists of a serial data line (SDA) and a serial clock (SCL). The MAX V and the Intel Stratix 10 devices use the I²C for reading and writing to the various components on the board such as programmable clock generators, VID regulators, ADC and temperature sensors.

You can use the Intel Stratix 10 or MAX V as the I²C host to access these devices, change clock frequencies or get board status information such as voltage and temperature readings.

Figure 10. I²C Block Diagram

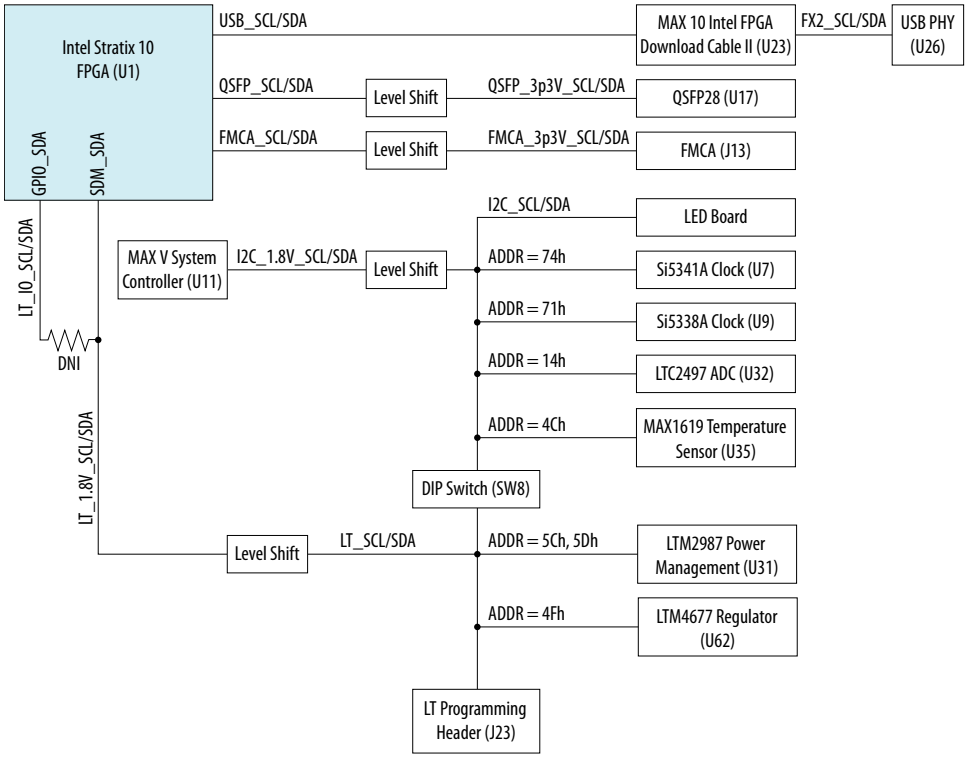


Table 21. MAX V I²C Signals

Schematic Signal Name	MAX V Pin Number	I/O Standard	Description
I2C_1.8V_SCL	P13	1.8V	I²C serial clock from MAX V
I2C_1.8V_SDA	R14	1.8V	I²C serial data from MAX V

Table 22. Intel Stratix 10 FPGA I²C Signals

Schematic Signal Name	Intel Stratix 10 FPGA Pin Number	I/O Standard	Description
LT_1.8V_SCL	BG22	1.8V	Intel Stratix 10 FPGA I²C from SDM IO pin (default)
LT_1.8V_SDA	BF22	1.8V	Intel Stratix 10 FPGA I²C from SDM IO pin (default)
LT_IO_SCL	V21	1.8V	Intel Stratix 10 FPGA I²C from GPIO pin
LT_IO_SDA	V22	1.8V	Intel Stratix 10 FPGA I²C from GPIO pin

Table 23. Intel Stratix 10 FPGA I²C Signals to Intel FPGA Download Cable II

Schematic Signal Name	Intel Stratix 10 FPGA Pin Number	I/O Standard	Description
USB_SCL	AB12	3.0V	Dedicated I²C to Intel FPGA Download Cable II
USB_SDA	AF17	3.0V	Dedicated I²C to Intel FPGA Download Cable II

Table 24. Intel Stratix 10 FPGA I²C Signals to QSFP module

Schematic Signal Name	Intel Stratix 10 FPGA Pin Number	I/O Standard	Description
QSFP_SCL	BJ26	1.8V	Dedicated I²C to QSFP module
QSFP_SDA	BH27	1.8V	Dedicated I²C to QSFP module

Table 25. Intel Stratix 10 FPGA I²C Signals to FMC Connector

Schematic Signal Name	Intel Stratix 10 FPGA Pin Number	FMC Connector Pin Number	I/O Standard	Description
FMCA_SCL	BH21	C30	1.8V	Dedicated I²C to FMC Connector
FMCA_SDA	BH20	C31	1.8V	Dedicated I²C to FMC Connector

4.6.7. DisplayPort

The Intel Stratix 10 GX FPGA development board includes a Mini-DisplayPort connector.

Table 26. Mini-DisplayPort Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
J12.4	DP_3p3V_CONFIG1	AN26	1.8V	–
J12.6	DP_3p3V_CONFIG2	AP26	1.8V	–
J12.2	DP_3p3V_HOT_PLUG	AU27	1.8V	Hot plug detect

continued...

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
J12.18	DP_AUX_CN	AN25	LVDS	Auxiliary channel (negative)
J12.16	DP_AUX_CP	AP25	LVDS	Auxiliary channel (positive)
J12.5	DP_ML_LANE_CN0	AK48	1.4V PCML	Lane 0 (negative)
J12.11	DP_ML_LANE_CN1	AL46	1.4V PCML	Lane 1 (negative)
J12.17	DP_ML_LANE_CN2	AH48	1.4V PCML	Lane 2 (negative)
J12.12	DP_ML_LANE_CN3	AJ46	1.4V PCML	Lane 3 (negative)
J12.3	DP_ML_LANE_CP0	AK49	1.4V PCML	Lane 0 (positive)
J12.9	DP_ML_LANE_CP1	AL47	1.4V PCML	Lane 1 (positive)
J12.15	DP_ML_LANE_CP2	AH49	1.4V PCML	Lane 2 (positive)
J12.10	DP_ML_LANE_CP3	AJ47	1.4V PCML	Lane 3 (positive)

4.6.8. SDI Video Input/Output Ports

The Intel Stratix 10 GX FPGA development board includes a SDI port, which consists of a M23428G-33 cable driver and a M23544G-14 cable equalizer. The PHY devices from Macom interface to single-ended HDBNC connectors.

The cable driver supports operation from 125 Mbps to 11.88 Gbps. Control signals are allowed for SD and HD modes selections, as well as device enable. The device can be clocked by the 148.5 MHz voltage-controlled crystal oscillator (VCXO) and matched to incoming signals within 50 ppm using the UP and DN voltage control lines to the VCXO.

Table 27. SDI Video Output Standards for the SD and HD Input

SD_HD Input	Supported Output Standards	Rise Time
0	SMPTE 424M, SMPTE 292M	Faster
1	SMPTE 259M	Slower

Table 28. SDI Video Output Interface Pin Assignments, Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard
U20.9	SDI_SD_HDn	AY40	1.8V
U20.5	SDI_TX_RESET	–	–
U20.1	SDI_TXCAP_N	G46	1.4V PCML
U20.16	SDI_TXCAP_P	G47	1.4V PCML
U20.10	SDI_TXDRV_N	–	–
U20.11	SDI_TXDRV_P	–	–

The cable equalizer supports operation at 270 Mbit SD, 1.5 Gbit HD and 3.0, 6.0, and 11.88 Gbit dual-link HD modes. Control signals are allowed for bypassing or disabling the device, as well as a carrier detect or auto-mute signal interface.

Table 29. SDI Cable Equalizer Lengths

Cable Type	Data Rate (Mbps)	Maximum Cable Length (m)
Belden 1694A	270	400
Belden 1694A	1485	140
Belden 1694A	2970	120

Table 30. SDI Video Input Interface Pin Assignments, Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard
U21.10	MF0_BYPASS	BA40	1.8V
U21.19	MF1_AUTO_SLEEP	BA39	1.8V
U21.21	MF2_MUTE	BB39	1.8V
U21.22	MF3_XSD	–	–
U21.6	MODE_SEL	–	–
U21.11	MUTEREF	–	–
U21.4	SDI_EQIN_N1	–	–
U21.3	SDI_EQIN_P1	–	–
U21.14	SDO_N/SDI_RX_N	G42	1.4V PCML
U21.15	SDO_P/SDI_RX_P	G43	1.4V PCML

4.7. Clock Circuits

4.7.1. On-Board Oscillators

Figure 11. Intel Stratix 10 GX FPGA Board - Clock Inputs and Default Frequencies

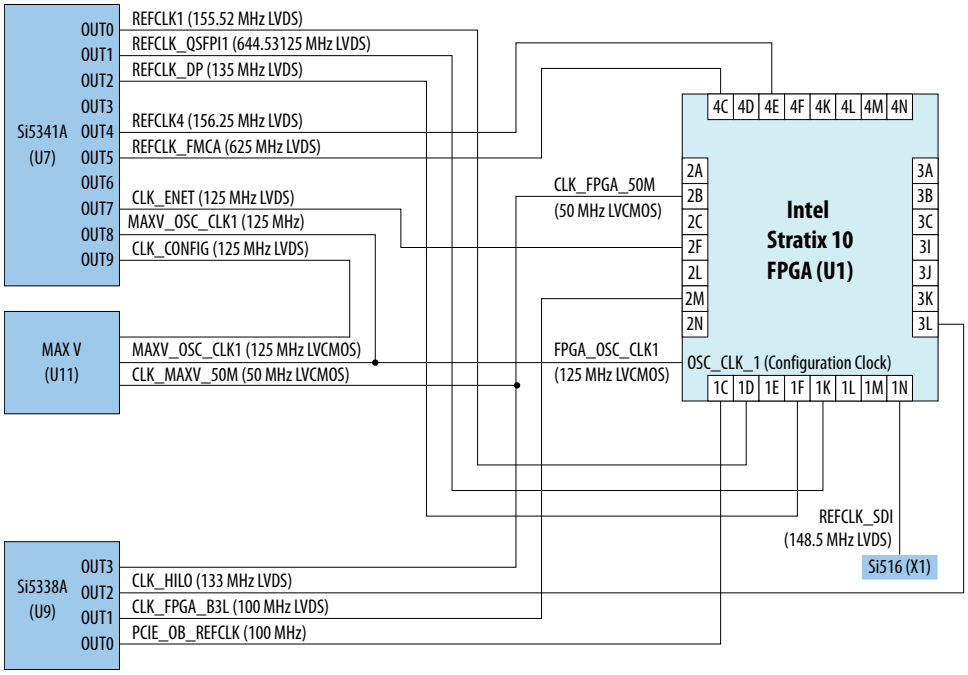


Table 31. On-Board Oscillators

Source	Schematic Signal Name	Frequency	I/O Standard	Intel Stratix 10 FPGA Pin Number	Application
U7	REFCLK1_P	155.52 MHz	LVDS	AM41	Transceiver reference clocks Bank 1D
	REFCLK1_N		LVDS	AM40	
	REFCLK_QSFP1_P	644.53125 MHz	LVDS	Y38	QSFP reference clocks
	REFCLK_QSFP1_N		LVDS	Y37	
	REFCLK_DP_P	135 MHz	LVDS	AK38	DisplayPort reference clocks
	REFCLK_DP_N		LVDS	AK37	
	REFCLK4_P	156.25 MHz	LVDS	AF9	Transceiver reference clocks Bank 4E
	REFCLK4_N		LVDS	AF10	
	REFCLK_FMCA_P	625 MHz	LVDS	AT9	FMC reference clocks
	REFCLK_FMCA_N		LVDS	AT10	
	CLK_ENET_P	125 MHz	LVDS	AN27	Ethernet clock
	CLK_ENET_N		LVDS	AN28	

continued...

Source	Schematic Signal Name	Frequency	I/O Standard	Intel Stratix 10 FPGA Pin Number	Application
	FPGA_OSC_CLK1	125 MHz	LVDS	BA22	FPGA configuration clock
	MAXV_OSC_CLK1	125 MHz	LVDS	–	MAX V clock
	CLK_CONFIG	125 MHz	LVDS	–	MAX V clock
U9	CLK_FPGA_50M	50 MHz	1.8V LVCMOS	BH33	FPGA clock
	CLK_MAXV_50M	50 MHz	1.8V LVCMOS	–	MAX V clock
	CLK_HILO_P	133 MHz	LVDS	M35	HiLo memory clock
	CLK_HILO_N		LVDS	N35	
	CLK_FOGA_B3L_P	100 MHz	LVDS	J20	FPGA clock for Bank 3L
	CLK_FPGA_B3L_N		LVDS	J19	
	PCIE_OB_REFCLK_P	100 MHz	LVDS	AP41	On board PCIe reference clock
	PCIE_ON_REFCLK_N		LVDS	AP40	
X1	REFCLK_SDI_P	148.5 MHz	LVDS	P41	SDI reference clocks
	REFCLK_SDI_N		LVDS	P40	

4.7.2. Off-Board Clock I/O

The development board has input and output clocks which can be driven onto the board. The output clocks can be programmed to different levels and I/O standards according to the FPGA device's specification.

Table 32. Off-Board Clock Inputs

Source	Schematic Signal Name	I/O Standard	Intel Stratix 10 FPGA Pin Number	Description
J3	SDI_REFCLK_SMA_P	LVDS	T41	SDI Refclk Input
J4	SDI_REFCLK_SMA_N	LVDS	T40	SDI Refclk Input

Table 33. Off-Board Clock Outputs

Source	Schematic Signal Names	I/O Standard	Intel Stratix 10 FPGA Pin Number	Description
J2	SMA_CLKOUT_P	1.8V	H23	SMA clock output
J1	SMA_CLKOUT_P	1.8V	G23	

4.8. Memory

This section describes the development board's memory interface support and also their signal names, types and connectivity relative to the FPGA.

4.8.1. Flash

The Intel Stratix 10 GX FPGA development board supports two 1 GB CFI-compatible synchronous flash devices for non-volatile storage of FPGA configuration data, board information, test application data and user code space. These devices are part of the shared bus that connects to the flash memory, FPGA and MAX V CPLD EPM2210 System Controller.

Table 34. Memory Map of the first 1G flash (x16)

Block Description	Size (KB)	Address Range
Board Test System scratch	512	0x0750.0000 - 0x0757.FFFF
User software	14336	0x0670.0000 - 0x074F.FFFF
Factory software	8192	0x05F0.0000 - 0x06FF.FFFF
Zips (html, web content)	8192	0x0570.0000 - 0x05EF.FFFF
User hardware1	44032	0x02C0.0000 - 0x056F.FFFF
Factory hardware	44032	0x0010.0000 - 0x02BF.FFFF
PFL option bits	256	0x000C.0000 - 0x000F.FFFF
Board information	256	0x0008.0000 - 0x000B.FFFF
Ethernet option bits	256	0x0004.0000 - 0x0007.FFFF
User design reset vector	256	0x0000.0000 - 0x0003.FFFF

Table 35. Memory Map of the second 1G flash (x16)

Block Description	Size (KB)	Address Range
User hardware2	44032	0x0010.0000 - 0x02BF.FFFF
PFL option bits	256	0x000C.0000 - 0x000F.FFFF
Reserved	256	0x0008.0000 - 0x000B.FFFF
Reserved	256	0x0004.0000 - 0x0007.FFFF
Reserved	256	0x0000.0000 - 0x0003.FFFF

Table 36. Flash Memory Pin Assignments

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
F6	FLASH_ADVN	BE28	1.8V	Address Valid
B4	FLASH_CEN1	BJ31	1.8V	Chip enable
E6	FLASH_CLK	BF31	1.8V	Clock
F8	FLASH_OEN	BJ30	1.8V	Output enable

continued...

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
F7	FLASH_RDYBSYN1	BJ28	1.8V	Ready
D4	FLASH_RESETN	BG30	1.8V	Reset
G8	FLASH_WEN	BH28	1.8V	Write Enable
C6	FLASH_WPN	–	1.8V	Write protect
A1	FLASH_ADDR1	AU28	1.8V	Address bus
B1	FLASH_ADDR2	AU29	1.8V	Address bus
C1	FLASH_ADDR3	AW29	1.8V	Address bus
D1	FLASH_ADDR4	AY29	1.8V	Address bus
D2	FLASH_ADDR5	BB28	1.8V	Address bus
A2	FLASH_ADDR6	BA29	1.8V	Address bus
C2	FLASH_ADDR7	AV28	1.8V	Address bus
A3	FLASH_ADDR8	AW28	1.8V	Address bus
B3	FLASH_ADDR9	AV30	1.8V	Address bus
C3	FLASH_ADDR10	AU30	1.8V	Address bus
D3	FLASH_ADDR11	AT30	1.8V	Address bus
C4	FLASH_ADDR12	AT29	1.8V	Address bus
A5	FLASH_ADDR13	BA30	1.8V	Address bus
B5	FLASH_ADDR14	BA31	1.8V	Address bus
C5	FLASH_ADDR15	BB29	1.8V	Address bus
D7	FLASH_ADDR16	BB30	1.8V	Address bus
D8	FLASH_ADDR17	BC32	1.8V	Address bus
A7	FLASH_ADDR18	BC31	1.8V	Address bus
B7	FLASH_ADDR19	BB32	1.8V	Address bus
C7	FLASH_ADDR20	BA32	1.8V	Address bus
C8	FLASH_ADDR21	AY32	1.8V	Address bus
A8	FLASH_ADDR22	BD30	1.8V	Address bus
G1	FLASH_ADDR23	BC30	1.8V	Address bus
H8	FLASH_ADDR24	BG28	1.8V	Address bus
B6	FLASH_ADDR25	BG29	1.8V	Address bus
B8	FLASH_ADDR26	BH30	1.8V	Address bus
F2	FLASH_DATA0	BD36	1.8V	Data bus
E2	FLASH_DATA1	BE36	1.8V	Data bus
G3	FLASH_DATA2	BC35	1.8V	Data bus
E4	FLASH_DATA3	BC36	1.8V	Data bus

continued...

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Description
E5	FLASH_DATA4	BB34	1.8V	Data bus
G5	FLASH_DATA5	BB33	1.8V	Data bus
G6	FLASH_DATA6	BD35	1.8V	Data bus
H7	FLASH_DATA7	BD34	1.8V	Data bus
E1	FLASH_DATA8	BC33	1.8V	Data bus
E3	FLASH_DATA9	BD33	1.8V	Data bus
F3	FLASH_DATA10	BF35	1.8V	Data bus
F4	FLASH_DATA11	BF36	1.8V	Data bus
F5	FLASH_DATA12	BF34	1.8V	Data bus
H5	FLASH_DATA13	BG34	1.8V	Data bus
G7	FLASH_DATA14	BJ34	1.8V	Data bus
E7	FLASH_DATA15	BJ33	1.8V	Data bus

4.8.2. Programming Flash using Quartus Programmer

You can use the Quartus Programmer to program the flash with your Programmer Object File (**.pof**).

Ensure the following conditions are met before you proceed:

- The Quartus Programmer and the Intel FPGA Download Cable II driver are installed on the host computer.
- The micro-USB cable is connected to the FPGA development board.
- Power to the board is on, and no other applications that use the JTAG chain are running.
- The design running in the FPGA does not drive the FM bus.

Execute the steps below to program the Flash

1. Start the Quartus Programmer.
2. Click **Auto Detect** to display the devices in the JTAG chain.
3. Select the flash attached to the MAX V and then click **Change File** and select the path to the desired **.pof**. If the flash is not detected, configure the FPGA with any configuration image which does not drive the flash signals and then go to step 2, refer to Configuring the FPGA using Quartus Programmer
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to program the selected file to flash. Programming is complete when the progress bar reaches 100%. If flash programming fails, change the TCK frequency to a lower frequency (16 MHz or 6 MHz). Run the command below in the Nios II command shell. `jtag --setparam <cable> JtagClock <frequency><Units>`. For example: `jtagconfig --setparam 1 JtagClock 16M` and then go to Step 4.

Attention: Using the Quartus Programmer to program a device on the board causes other JTAG-based applications such as the Board Test System and the Power Monitor to lose their connection to the board. Restart those applications after programming is complete.

4.9. Daughtercards

The Intel Stratix 10 GX FPGA development kit provides a full-featured hardware development platform for prototyping and testing high-speed interfaces to a Intel Stratix 10 GX FPGA.

Table 37. Intel Stratix 10 FPGA Development Kit Daughtercards

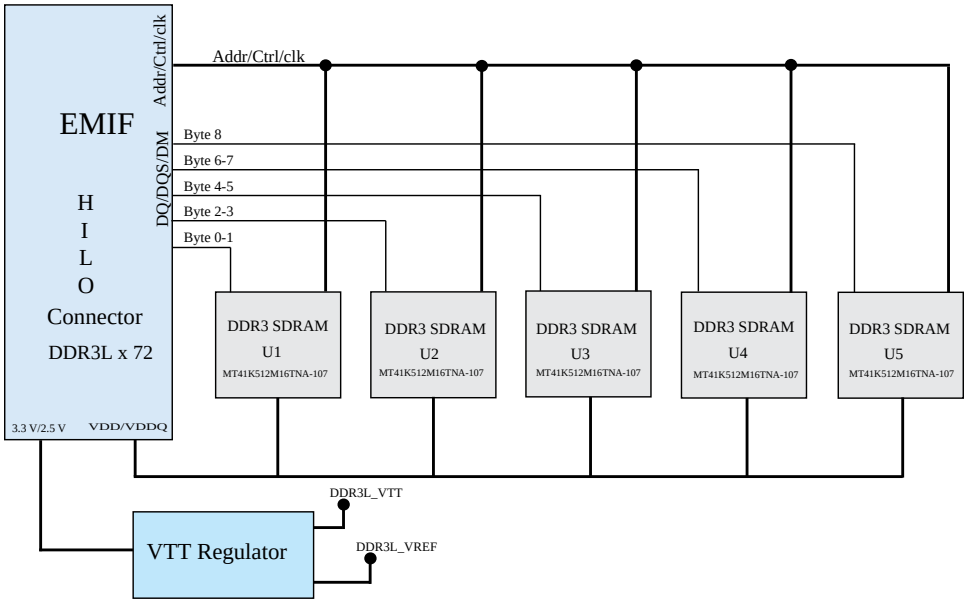
Memory Type	Transfer Rate (Mbps)	Maximum Frequency (MHz)
DDR3	2133	1066
DDR4	2666	1333
RLDRAM3	2400	1200
QDR-IV	2133	1066
FMC Loopback	10000	5000

4.9.1. External Memory Interface

4.9.1.1. DDR3L

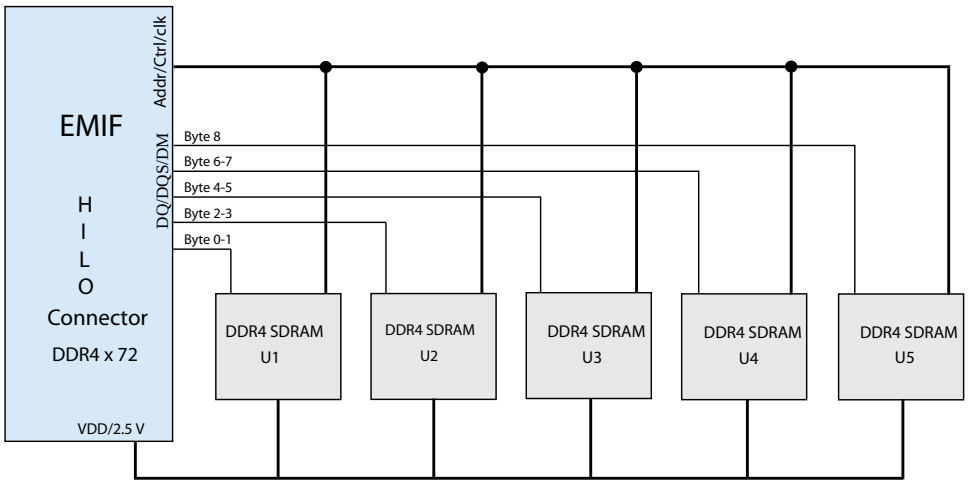
The DDR3Lx72 SDRAM (DDR3 Low voltage)

Figure 12. DDR3 Block Diagram



4.9.1.2. DDR4

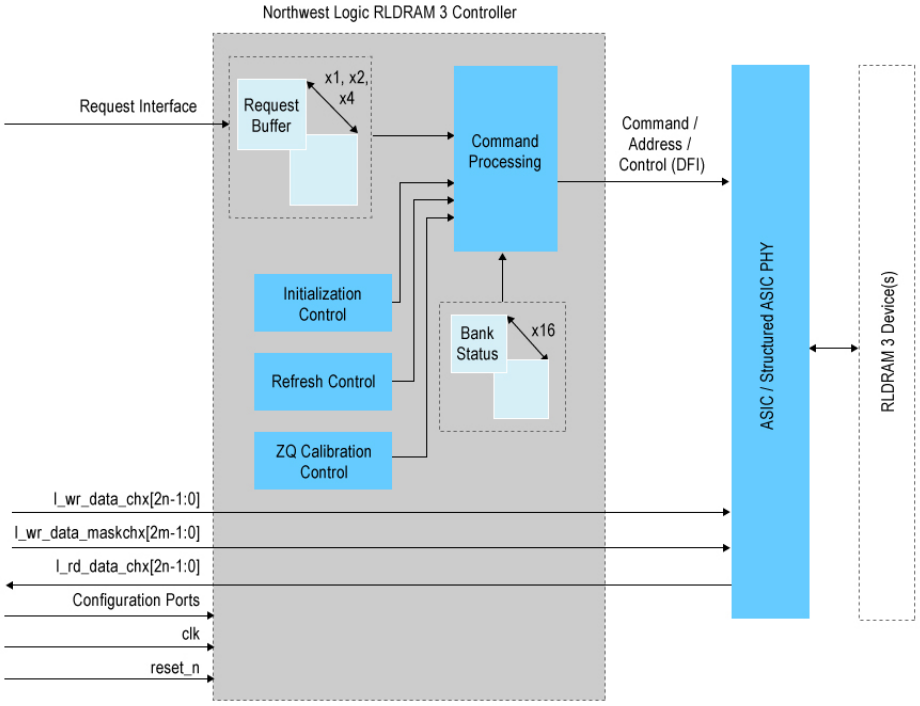
Figure 13. DDR4 Block Diagram



4.9.1.3. RLDRAM3

The RLDRAM3 x36 (reduced latency DRAM) controller is designed for use in applications requiring high memory throughput, high clock rates and full programmability.

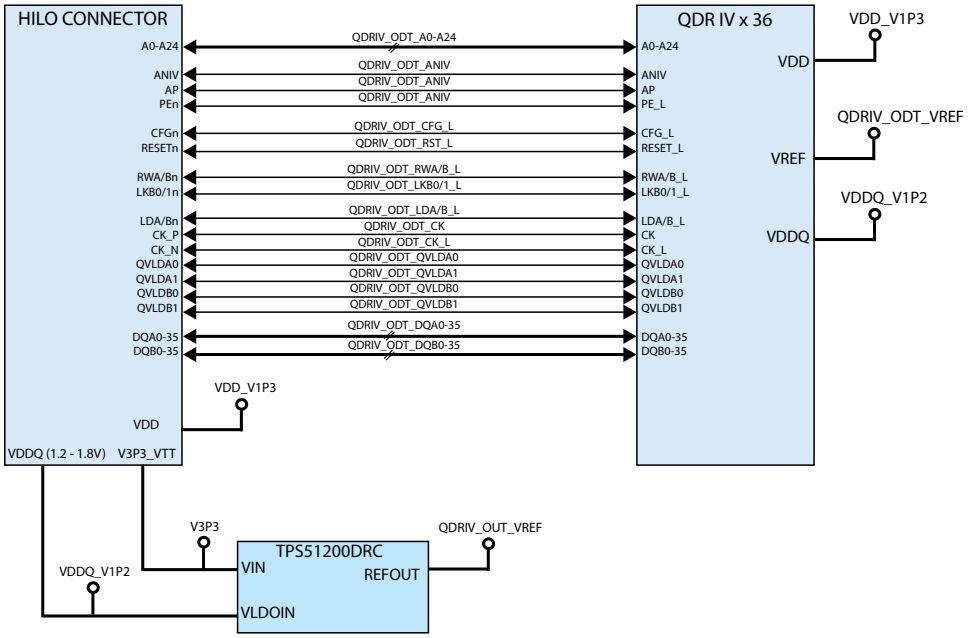
Figure 14. RLDRAM3 Block Diagram



4.9.1.4. QDR-IV

QDR-IV x 36 SRAM devices enable you to maximize bandwidth with separate read and write ports.

Figure 15. QDR-IV Block Diagram

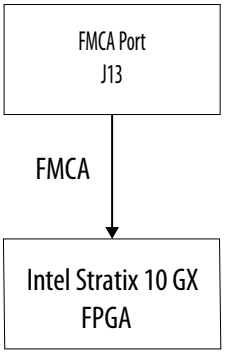


4.9.1.5. FMC Loopback Card

The Intel Stratix 10 GX FPGA development kit provides one FMC mezzanine interface port connected to the Intel Stratix 10 GX FPGA for interfacing to the Intel FMC add-in boards as shown in the figure below.

The FMC interface is mechanically compliant with the Vita57.1 specification for attaching a single width mezzanine module. However, in terms of signal connections, the Intel
FMC interface is not fully compliant with the Vita 57.1 specification. Instead, it contains a subset of the Vita57.1 interface signal to the connector as shown in the FMCA signal assignment tables.

Figure 16. Intel Stratix 10 GX FPGA Development Kit FMC Block Diagram



The following table shows the complete signal connections assigned for Intel FMC interface at the FMCA port.

Table 38. FMCA Connector (J13) Signal Assignments

Row Number	K	J	H	G	F	E	D	C	B	A
1	NC	GND	VREF_FMCA	GND	FMCA_M2C_PG	GND	FMCA_C2M_PG	GND	NC	GND
2	GND	NC	FMCA_PRSNTn	FMCA_CLK_M2C_P1	GND	NC	GND	FMCA_DP_C2M_P0	GND	FMCA_DP_M2C_P1
3	GND	NC	GND	FMCA_CLK_M2C_N1	GND	NC	GND	FMCA_DP_C2M_N0	GND	FMCA_DP_M2C_N1
4	FMCA_DP_M2C_P10	GND	FMCA_CLK_M2C_P0	GND	NC	GND	FMCA_GBTCLK_M2C_P0	GND	FMCA_DP_M2C_P9	GND
5	FMCA_DP_M2C_N10	GND	FMCA_CLK_M2C_N0	GND	NC	GND	FMCA_GBTCLK_M2C_N0	GND	FMCA_DP_M2C_N9	GND
6	GND	NC	GND	FMCA_LA_RX_CLK_P0	GND	NC	GND	FMCA_DP_M2C_P0	GND	FMCA_DP_M2C_P2
7	FMCA_DP_M2C_P11	GND	FMCA_LA_TX_P0	FMCA_LA_RX_CLK_N0	NC	NC	GND	FMCA_DP_M2C_N0	GND	FMCA_DP_M2C_N2
8	FMCA_DP_M2C_N11	GND	FMCA_LA_TX_N0	GND	NC	GND	FMCA_LA_RX_CLK_P1	GND	FMCA_DP_M2C_P8	GND
9	GND	NC	GND	FMCA_LA_RX_P0	GND	NC	FMCA_LA_RX_CLK_N1	GND	FMCA_DP_M2C_N8	GND
10	FMCA_DP_M2C_P12	GND	FMCA_LA_TX_P1	FMCA_LA_RX_N0	NC	NC	GND	FMCA_LA_RX_P1	GND	FMCA_DP_M2C_P3

continued...

Row Number	K	J	H	G	F	E	D	C	B	A
11	FMCA_DP_M2C_N12	GND	FMCA_LA_TX_N1	GND	NC	GND	FMCA_LA_TX_P2	FMCA_LA_RX_N1	GND	FMCA_DP_M2C_N3
12	GND	NC	GND	FMCA_LA_RX_P2	GND	NC	FMCA_LA_TX_N2	GND	FMCA_DP_M2C_P7	GND
13	FMCA_DP_M2C_P13	GND	FMCA_LA_TX_P3	FMCA_LA_RX_N2	NC	NC	GND	GND	FMCA_DP_M2C_N7	GND
14	FMCA_DP_M2C_N13	GND	FMCA_LA_TX_N3	GND	NC	GND	FMCA_LA_TX_P4	FMCA_LA_RX_P3	GND	FMCA_DP_M2C_P4
15	GND	NC	GND	FMCA_LA_RX_P4	GND	NC	FMCA_LA_TX_N4	FMCA_LA_RX_P3	GND	FMCA_DP_M2C_P4
16	FMCA_DP_M2C_P14	GND	FMCA_LA_TX_P5	FMCA_LA_RX_N4	NC	NC	GND	GND	FMCA_DP_M2C_P6	GND
17	FMCA_DP_M2C_N14	GND	FMCA_LA_TX_N5	GND	NC	GND	FMCA_LA_TX_P6	GND	FMCA_DP_M2C_N6	GND
18	GND	NC	GND	FMCA_LA_RX_P6	GND	NC	FMCA_LA_TX_N6	FMCA_LA_RX_P5	GND	FMCA_DP_M2C_P5
19	FMCA_DP_M2C_P15	GND	FMCA_LA_TX_P7	FMCA_LA_RX_N6	NC	NC	GND	FMCA_LA_RX_N5	GND	FMCA_DP_M2C_N5
20	FMCA_DP_M2C_N15	GND	FMCA_LA_TX_N7	GND	NC	GND	FMCA_LA_TX_P8	GND	FMCA_GBTCLK_M2C_N1	GND
21	GND	NC	GND	FMCA_LA_RX_P8	GND	NC	FMCA_LA_TX_N8	GND	FMCA_GBTCLK_M2C_N1	GND
22	FMCA_DP_C2M_P10	GND	FMCA_LA_TX_P9	FMCA_LA_RX_N8	NC	NC	GND	FMCA_LA_RX_P7	GND	FMCA_DP_C2M_P1
23	FMCA_DP_C2M_N10	GND	FMCA_LA_TX_N9	GND	NC	GND	FMCA_LA_TX_P11	FMCA_LA_RX_N7	GND	FMCA_DP_C2M_N1
24	GND	NC	GND	FMCA_LA_RX_P9	GND	NC	FMCA_LA_TX_N11	GND	FMCA_DP_C2M_P9	GND
25	FMCA_DP_C2M_P11	GND	FMCA_LA_TX_P10	FMCA_LA_RX_N9	NC	NC	GND	GND	FMCA_DP_C2M_N9	GND
26	FMCA_DP_C2M_N11	GND	FMCA_LA_TX_N10	GND	NC	GND	FMCA_LA_TX_P13	FMCA_LA_RX_P11	GND	FMCA_DP_C2M_P2

continued...

Row Number	K	J	H	G	F	E	D	C	B	A
27	GND	NC	GND	FMCA_LA_RX_P10	GND	NC	FMCA_LA_TX_N13	FMCA_LA_RX_N11	GND	FMCA_DP_C2M_N2
28	FMCA_DP_C2M_P12	GND	FMCA_LA_TX_P12	FMCA_LA_RX_N10	NC	NC	GND	GND	FMCA_DP_C2M_P8	GND
29	FMCA_DP_C2M_N12	GND	FMCA_LA_TX_N12	GND	NC	GND	FMCA_JTAG_TCK	GND	FMCA_DP_C2M_N8	GND
30	GND	NC	GND	FMCA_LA_RX_P12	GND	NC	FMCA_JTAG_TDI	FMCA_3P3V_SCL	GND	FMCA_DP_C2M_P3
31	FMCA_DP_C2M_P13	GND	FMCA_LA_TX_P14	FMCA_LA_RX_N12	NC	NC	FMCA_JTAG_TDO	FMCA_3P3V_SDA	GND	FMCA_DP_C2M_N3
32	FMCA_DP_C2M_N13	GND	FMCA_LA_RX_N14	GND	NC	GND	3.3V	GND	FMCA_DP_C2M_P7	GND
33	GND	NC	GND	FMCA_LA_RX_P13	GND	NC	FMCA_JTAG_TMS	GND	FMCA_DP_C2M_N7	GND
34	FMCA_DP_C2M_P14	GND	FMCA_LA_TX_P15	FMCA_LA_RX_N13	NC	NC	FMCA_JTAG_RST	FMCA_GA0	GND	FMCA_DP_C2M_P4
35	FMCA_DP_C2M_N14	GND	FMCA_LA_TX_N15	GND	NC	GND	FMCA_GA1	12V	GND	FMCA_DP_C2M_N4
36	GND	NC	GND	FMCA_LA_RX_P14	GND	NC	3.3V	GND	FMCA_DP_C2M_N6	GND
37	FMCA_DP_C2M_P15	GND	FMCA_LA_TX_P16	FMCA_LA_RX_N14	NC	NC	GND	12V	FMCA_DP_C2M_N6	GND
38	FMCA_DP_C2M_N15	GND	FMCA_LA_TX_N16	GND	NC	GND	3.3V	GND	GND	FMCA_DP_C2M_P5
39	GND	NC	GND	A10_VCCIO_FMCA	GND	A10_VCCIO_FMCA	GND	3.3V	GND	FMCA_DP_C2M_N5
40	NC	GND	A10_VCCIO_FMCA	GND	A10_VCCIO_FMCA	GND	3.3V	GND	NC	GND
41	NC	GND	A10_VCCIO_FMCA	GND	A10_VCCIO_FMCA	GND	3.3V	GND	NC	GND
			LPC Connector	LPC Connector			HPC Connector	HPC Connector		

High Pin Count (HPC)

The High Pin Count FMC connections are assigned to columns G and H in the FMCA connector as shown. The HPC signaling follows the Vita57.1 standard.

Low Pin Count (LPC)

The Low Pin Count FMC connections are assigned to columns C and D in the FMCA connector as shown. The LPC signaling follows the Vita57.1 standard.

5. System Power

This chapter describes the Intel Stratix 10 GX FPGA development board's power supply.

A laptop style DC power supply is provided with the development kit. Use only the supplied power supply. The power supply has an auto sensing input voltage of 100 ~ 240 V AC power and output of 12 V DC power at 20 A to the development board. The 12 V DC input power is then stepped down to various power rails used by the board components.

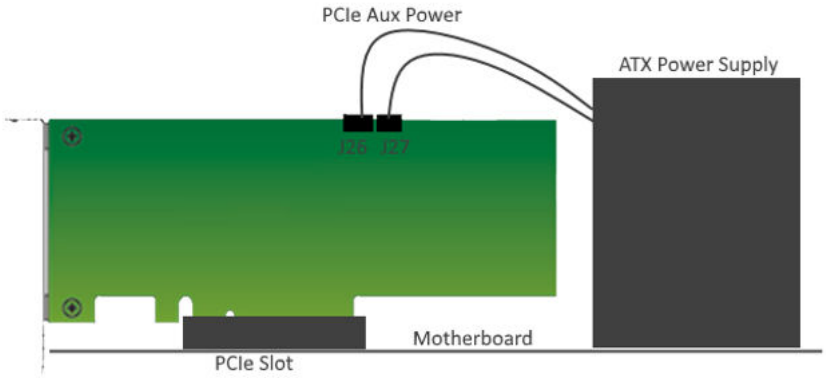
An on-board multi-channel analog-to-digital converter (ADC) measures both the voltage and current for several specific board rails. The power utilization is displayed on a graphical user interface (GUI) that can graph power consumption versus time.

5.1. Power Guidelines

The Intel Stratix 10 GX FPGA development kit has two modes of operation as described below.

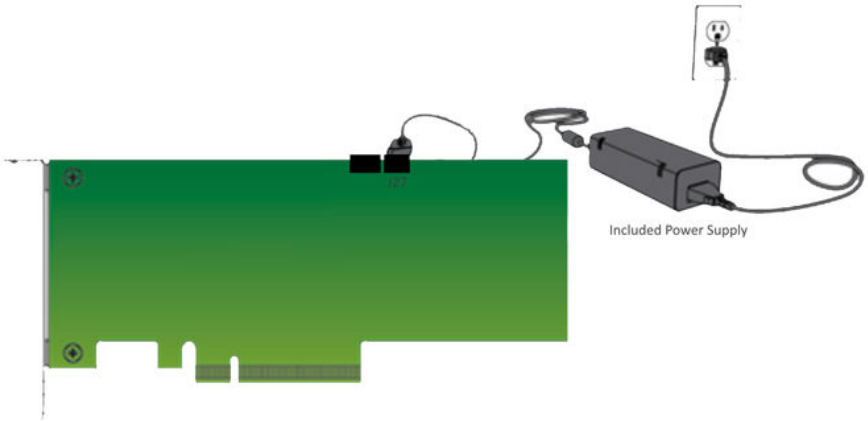
In a standard PCIe compliant system

In this mode, plug the board into an available PCI Express slot and connect the standard 2x4 and 2x3 auxiliary power cords available from the PC's ATX power supply to the respective mating connectors on the board (J26 and J27). The PCIe slot together with the two auxiliary PCIe power cords are required to power the entire board. If you do not connect the 2x4 or 2x3 auxiliary power connections, it prevent the board from powering on. The power switch SW7 is ignored when the board is used in the PCIe system.



As a stand-alone evaluation board powered by included power supply

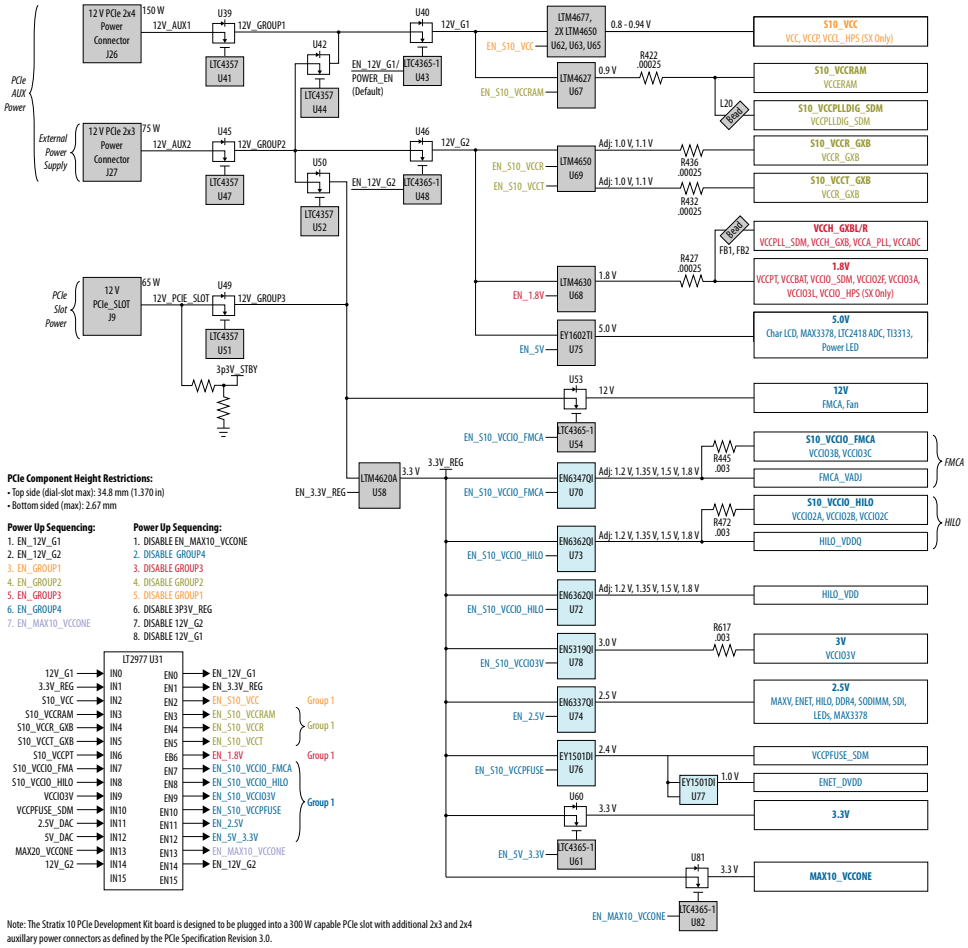
In this mode, plug the included power supply into the 2x3 pin connector (J27) and the AC power cord of the power supply into a power outlet. This power supply will provide the entire power to the board without the need to obtain power from the PCIe slot or the 2x4 power connector (J26). The power switch SW7 controls powering the board on/off.



5.2. Power Distribution System

The following figure below shows the power distribution system on the Intel Stratix 10 GX FPGA development board.

Figure 17. Power Distribution System Block Diagram



Note: The Stratix 10 PCIe Development Kit board is designed to be plugged into a 300 W capable PCIe slot with additional 2x3 and 2x4 auxillary power connectors as defined by the PCIe Specification Revision 3.0.

5.3. Power Measurement

There are eight power supply rails that have on-board voltage, current and wattage sense capabilities. Precision sense resistors split the ADC devices and rails from the primary supply plane for the ADC to measure voltage and current. An I^2C bus connects the ADC device to the MAX V CPLD EPM2210 System Controller as well as the Intel Stratix 10 GX FPGA.

The VCC rail for the FPGA core power is directly measured by the LTM4677 I^2C enabled voltage regulator module. Power measurements can be read from the LTM4677 device through its I^2C interface connected to the MAX V CPLD system controller.

5.4. Thermal Limitations and Protection

The Intel Stratix 10 GX FPGA development kit is designed to operate in a typical laboratory environment with an ambient temperature of approximately 25C. The cooling solution provided with the development kit allows sufficient cooling for the board to operate up to a maximum power consumption of 200 W under this environment.

A MAX1619 device is connected to the Intel Stratix 10 FPGA internal temperature diode to continuously monitor the FPGA internal temperature. In the meantime, a dedicated FPGA TSD real-time monitor solution under `~\ip\onchip_sensors\` is added to each transceiver or EMIF example design to monitor the temperatures of both FPGA core and each transceiver tile. Based on the data from both MAX1619, and the Intel Stratix 10 GX FPGA, MAX V runs at its maximum speed whenever any temperature is over 60C or immediately power off the board whenever the temperature crosses 100C.

Remember to unplug the power supply when the board is powered off when the temperature crosses 100C. Plug the power supply back again to ensure that the board can be normally turned on/off again.

6. Board Test System

The Intel Stratix 10 GX FPGA Development Kit includes a design example and an application called the Board Test System (BTS) to test the functionality of this board. The BTS provides an easy-to-use interface to alter functional settings and observe results. You can use the BTS to test board components, modify functional parameters, observe performance and measure power usage.

While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality that you are testing. The BTS is also useful as a reference for designing systems. The BTS communicates over the JTAG bus to a test design running in the Intel Stratix 10 GX FPGA device.

The figure below shows the Graphical User Interface (GUI) for a board that is in factory configuration.

Figure 18. BTS GUI

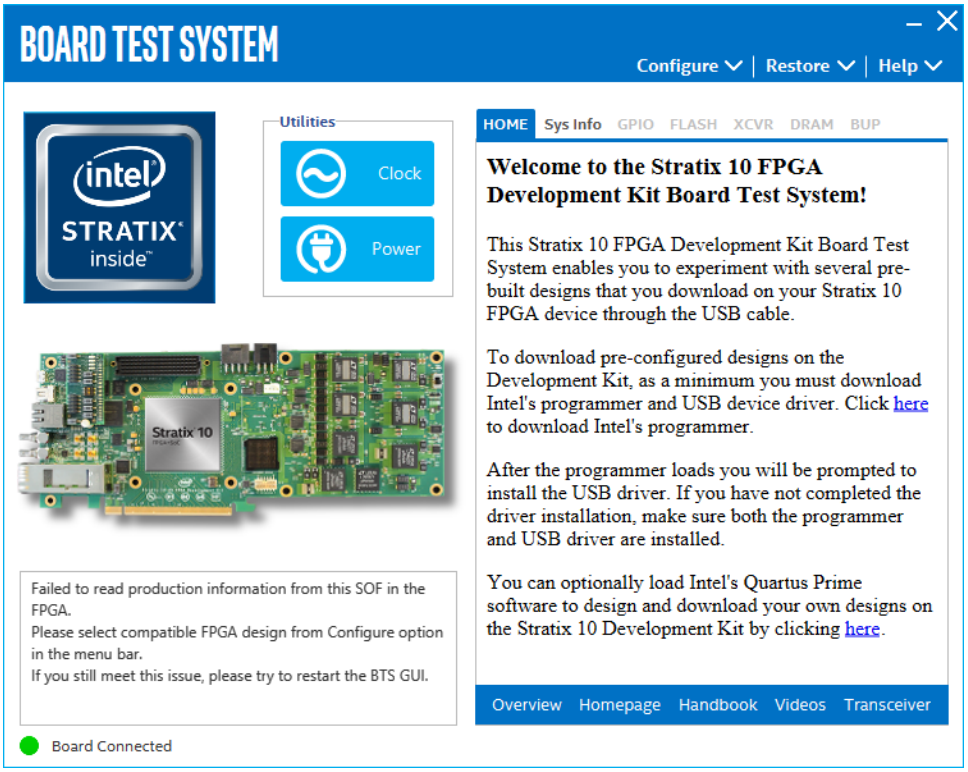
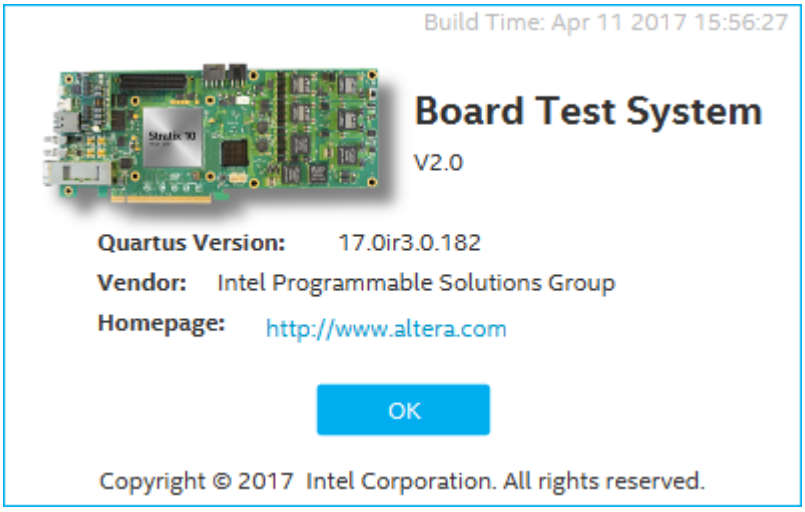


Figure 19. About BTS



6.1. Preparing the Board

Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure Menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears that allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The BTS communicates over the JTAG bus to a test design running in the FPGA. The BTS and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the Signal Tap II Embedded Logic Analyzer. Because the BTS is designed based on the Intel Quartus Prime software, be sure to close other applications before you use the BTS.

The BTS relies on the Intel Quartus Prime software's specific library. Before running the BTS, open the Intel Quartus Prime software to automatically set the environment variable `$QUARTUS_ROOTDIR`. The BTS uses this environment variable to locate the Intel Quartus Prime library. The version of Intel Quartus Prime software set in the `QUARTUS_ROOTDIR` environment variable should be newer than version 14.1. For example, the Development Kit Installer version 15.1 requires that the Intel Quartus Prime software 14.1 or later version to be installed.

Also, to ensure that the FPGA is configured successfully, you should install the latest Intel Quartus Prime software that can support the silicon on the development kit. For this board, we recommend you install Intel Quartus Prime version 17.0ir3.0.182.

Please refer to the `README.txt` file under `examples\board_test_system` directory.

6.2. Running the Board Test System

Before you begin

With the power to the board off, follow these steps:

1. Connect the USB cable to your PC and the board.
2. Ensure that the Ethernet patch cord is plugged into the RJ-45 connector.
3. Check whether the development board switches and jumpers are set according to your preferences.
4. Set the load selector switch (SW3.3) to OFF for user hardware1 (page#1). The development kit ships with the CFI Flash device preprogrammed with a default:
   - Factory FPGA configuration for running the Board Update Portal design example
   - User configuration for running the BTS demonstration
5. Turn on the power to the board. The board loads the design stored in the user hardware1 portion of flash memory into the FPGA. If your board is still in the factory configuration, or if you have downloaded a newer version of the BTS to the flash memory through the Board Update Portal, the design loads the GPIO, Ethernet and flash memory tests.

Note: To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The BTS cannot run correctly unless the USB cable is attached and the board is on.

To run the BTS

1. Navigate to the `<package dir>\examples\board_test_system` directory and run the `BoardTestSystem.exe` application.
2. A GUI appears, displaying the application tab corresponding to the design running in the FPGA. If the design loaded in the FPGA is not supported by the BTS GUI, you receive a message prompting you to configure your board with a valid BTS design. Refer to the Configure Menu on configuring your board.

Note: If some design is running in the FPGA, the BTS GUI loads the design file (`.sof`) in the image folder to check the current running design in the FPGA; therefore the design running in the FPGA must be the same as the design file in the image folder.

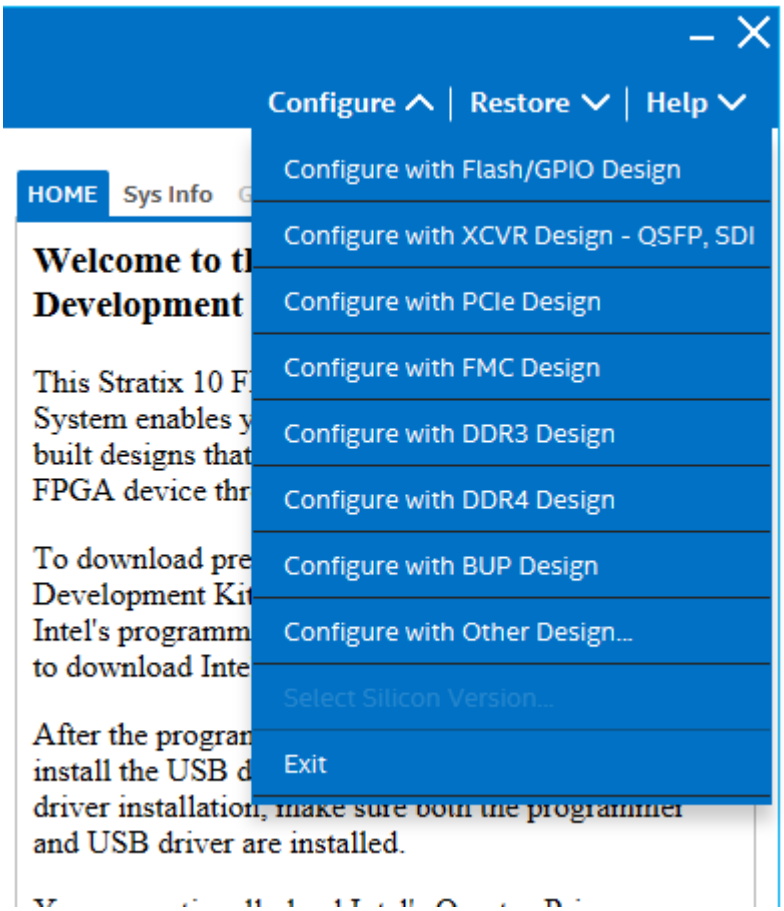
6.3. Using the Board Test System

This section describes each control in the BTS.

6.3.1. The Configure Menu

Use the Configure Menu to select the design you want to use. Each design example tests different board features. Select a design from this menu and the corresponding tabs become active for testing.

Figure 20. The Configure Menu



To configure the FPGA with a test system design, perform the following steps:

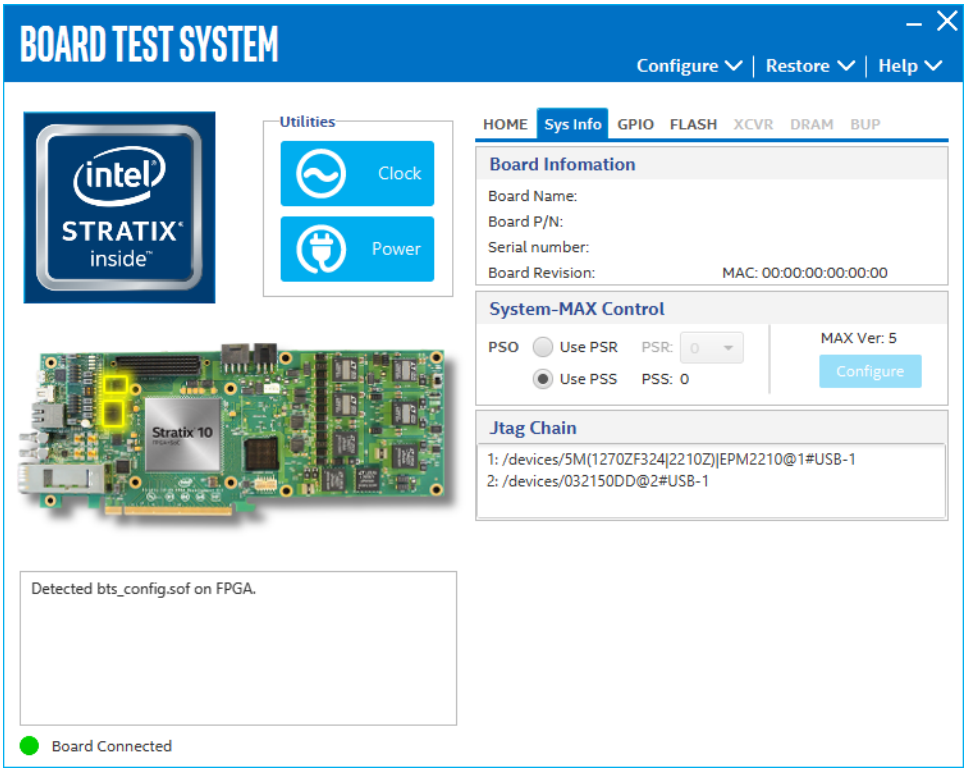
1. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click Configure to download the corresponding design to the FPGA.
3. When configuration finishes, close the Intel Quartus Prime if open. The design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled.

If you use the Intel Quartus Prime Programmer for configuration, rather than the BTS GUI, you may need to restart the GUI.

6.3.2. The System Info Tab

The System Info tab shows the board's current configuration. The tab displays the contents of the MAX V registers, the JTAG chain, the board's MAC address, and other details stored on the board.

Figure 21. The System Info tab



The following sections describe the controls of the System info tab

Board Information

The Board Information control displays static information about your board:

- Board Name: Indicates the official name of the board given by BTS
- Board P/N: Indicates the part number of the board
- Serial Number: Indicates the serial number of the board
- Board Revision: Indicates the revision of the board
- MAC: Indicates MAC Address of the board

System MAX Control

MAX Ver: Indicates the version of MAX V code currently running on the board.

The MAX V code resides in the `<package dir>\examples\max5` directory. Newer revisions of this code may be available on the Intel Stratix 10 GX FPGA Development kit link on the Intel website.

The MAX V register control allows you to view and change the current MAX V register values as described in the table below. Change to the register values with the GUI take effect immediately.

Table 39. MAX V Registers

MAX V Register Values	Description
Configure	Resets the system and reloads the FPGA with a design from the flash memory based on other MAX V register values.
PSO	Sets the MAX V PSO register.
PSR	Sets the MAX V PSR register. Allows PSR to determine the page of flash memory to use for FPGA reconfiguration. The numerical values in the list corresponds to the page of flash memory to load during the FPGA configuration.
PSS	Displays the MAX V PSS register value. Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.

JTAG Chain

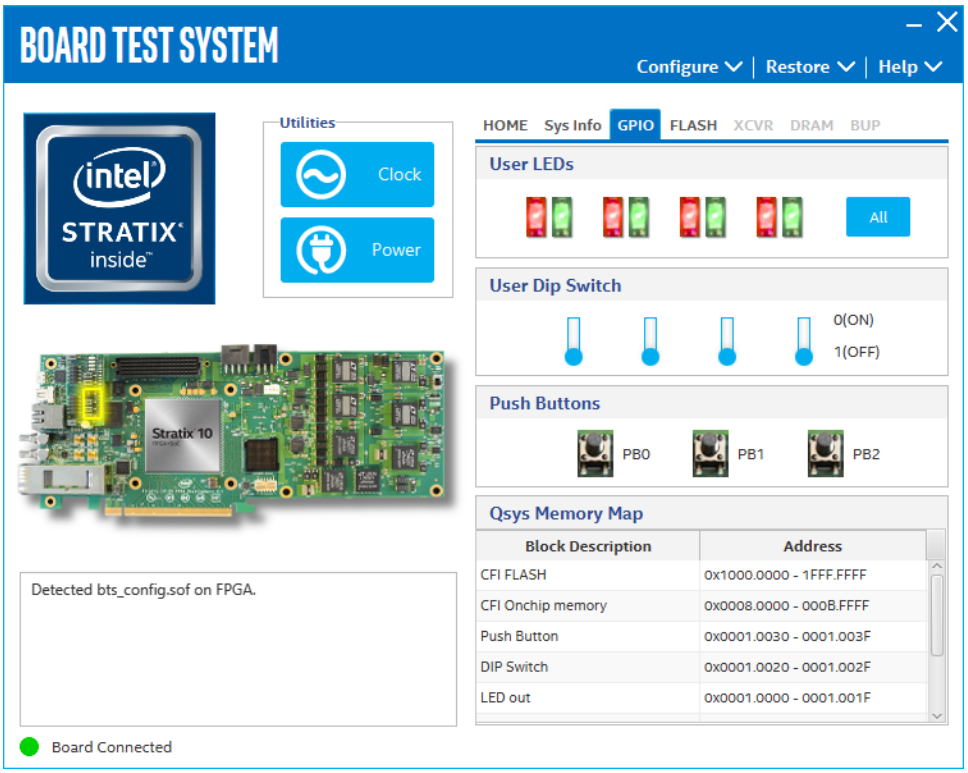
The JTAG chain shows all the devices currently in the JTAG chain.

Note: When set to 1, switch SW6.2 (MAX BYPASS) includes the MAX V DEVICE in the JTAG chain. When set to 0, the MAX V device is removed from the JTAG chain. System MAX and FPGA should all be present in the JTAG chain when running BTS GUI.

6.3.3. The GPIO Tab

The GPIO tab allows you to interact with all the general purpose user I/O components on your board. You can read DIP switch settings, turn LEDs on or off and detect push button presses.

Figure 22. The GPIO Tab



The following sections describe the controls on the GPIO tab.

User DIP Switches

The read-only User DIP Switches control displays the current positions of the switches in the user DIP switch bank (SW1). Change the switches on the board to see the graphical display change.

User LEDS

The User LEDs control displays the current state of the user LEDS. Toggle the LED buttons to turn the board LEDs on or off.

Push Buttons

Read only control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

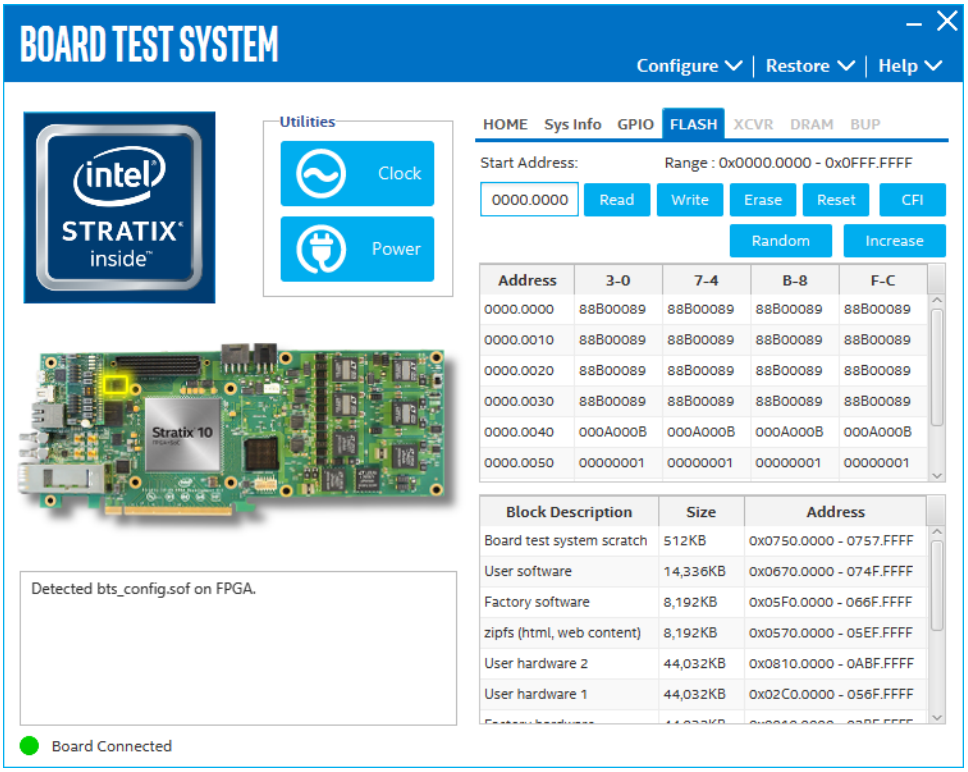
Platform Designer (Standard) Memory Map

The Platform Designer (Standard) memory map control shows the memory map of the `bts_config.sof` design running on your board. The memory map is visible only when `bts_config.sof` design is running on the board.

6.3.4. The Flash Tab

The Flash tab allows you to read and write flash memory on your board. The memory table displays the CFI ROM contents by default after you configure the FPGA.

Figure 23. The Flash Tab



The following sections describe the controls on the Flash tab

Read

Reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click Read. Values starting at the specified address in the table.

Write

Writes the flash memory on your board. To update the flash memory contents, change values in the table and click Write. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.

Random

Starts a random data pattern test to flash memory, limited to the 512K test system scratch page.

CFI

Updates the memory table, displaying the CFI ROM table contents from the flash device.

Increase

Starts an incrementing data pattern test to flash memory, limited to the 512K test system scratch page.

Reset

Executes the flash device's reset command and updates the memory table displayed on the Flash tab.

Erase

Erases flash memory.

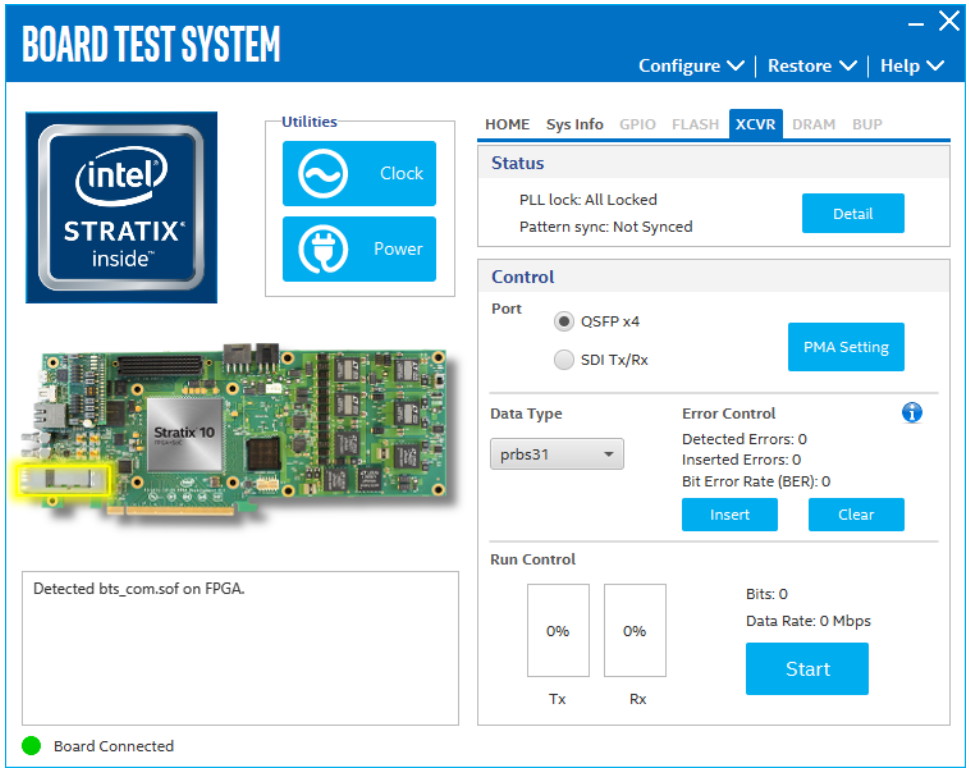
Flash Memory Map

Displays the flash memory map for the development board.

6.3.5. The XCVR Tab

This tab allows you to perform loopback tests on the QSFP and SDI ports.

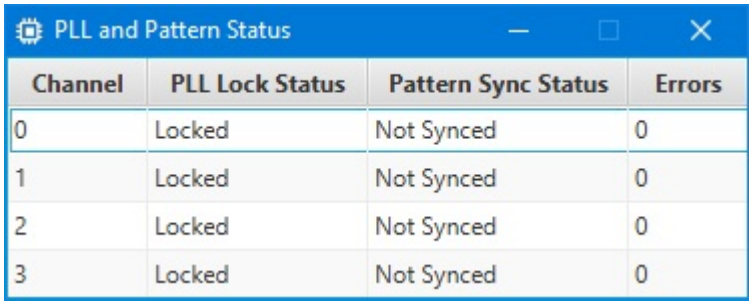
Figure 24. The XCVR Tab



Status

Displays the following status information during a loopback test:

- PLL lock: Shows the PLL locked or unlocked state.
- Pattern sync: Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern sync status:



Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Not Synced	0
1	Locked	Not Synced	0
2	Locked	Not Synced	0
3	Locked	Not Synced	0

Port

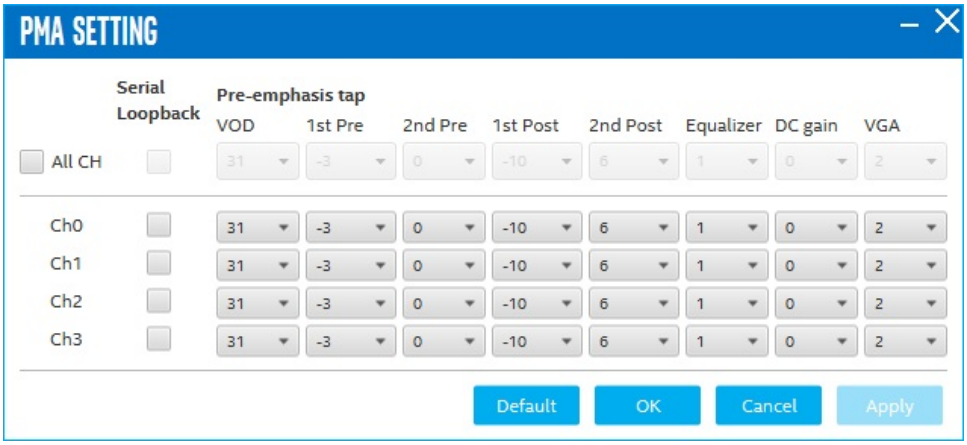
Allows you to specify which interface to test. The following port tests are available:

- QSFP
- SDI

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- Serial Loopback: Routes signals between the transmitter and the receiver.
- VOD: Specifies the voltage output differential of the transmitter buffer.
- Pre-emphasis tap:
  - 1st pre: Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - 2nd pre: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - 1st post: Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - 2nd post: Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- Equalizer: Specifies the AC gain setting for the receiver equalizer in four stage mode.
- DC gain: Specifies the DC gain setting for the receiver equalizer in four stage mode.
- VGA: Specifies the VGA gain value.



Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis:

- PRBS 7: Selects pseudo-random 7-bit sequences.
- PRBS 15: Selects pseudo-random 15-bit sequences.
- PRBS 23: Selects pseudo-random 23-bit sequences.
- PRBS 31: Selects pseudo-random 31-bit sequences.
- HF: Selects highest frequency divide-by-2 data pattern 10101010.
- LF: Selects lowest frequency divide-by-33 data pattern.

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- Detected errors: Displays the number of data errors detected in the hardware.
- Inserted errors: Displays the number of errors inserted into the transmit data stream.
- Insert: Inserts a one-word error into the transmit data stream each time you click the button. Insert is only enabled during transaction performance analysis.
- Clear: Resets the Detected errors and Inserted errors counters to zeroes.

Loopback

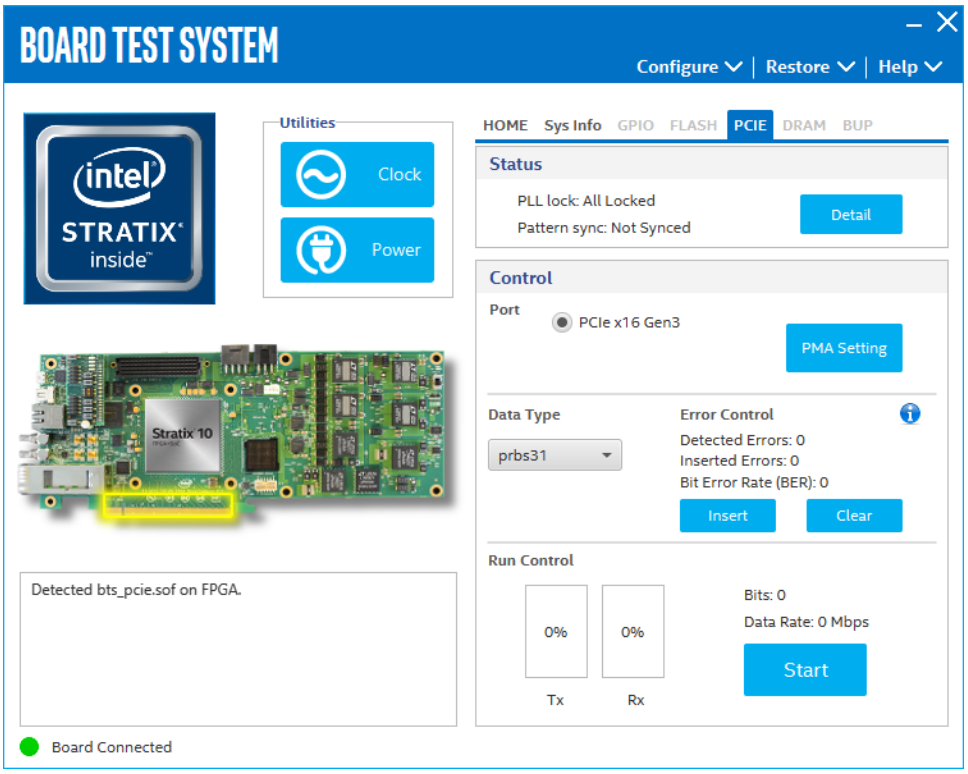
- Start: Initiates the selected ports transaction performance analysis.

  Note: Always click Clear before Start.
- Stop: Terminates transaction performance analysis.
- TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

6.3.6. The PCIe Tab

This tab allows you to run a PCIe loopback test on your board. You can also load the design and use an oscilloscope to measure an eye diagram of the PCIe transmit signals.

Figure 25. The PCIe Tab



The following sections describe the controls on the PCIe tab.

Status

Displays the following status information during a loopback test:

- PLL Lock: Shows the PLL locked or unlocked state.
- Pattern sync: Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern sync status:

PLL and Pattern Status

Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Not Synced	0
1	Locked	Not Synced	0
2	Locked	Not Synced	0
3	Locked	Not Synced	0
4	Locked	Not Synced	0
5	Locked	Not Synced	0
6	Locked	Not Synced	0
7	Locked	Not Synced	0
8	Locked	Not Synced	0
9	Locked	Not Synced	0
10	Locked	Not Synced	0
11	Locked	Not Synced	0
12	Locked	Not Synced	0
13	Locked	Not Synced	0
14	Locked	Not Synced	0
15	Locked	Not Synced	0

Port

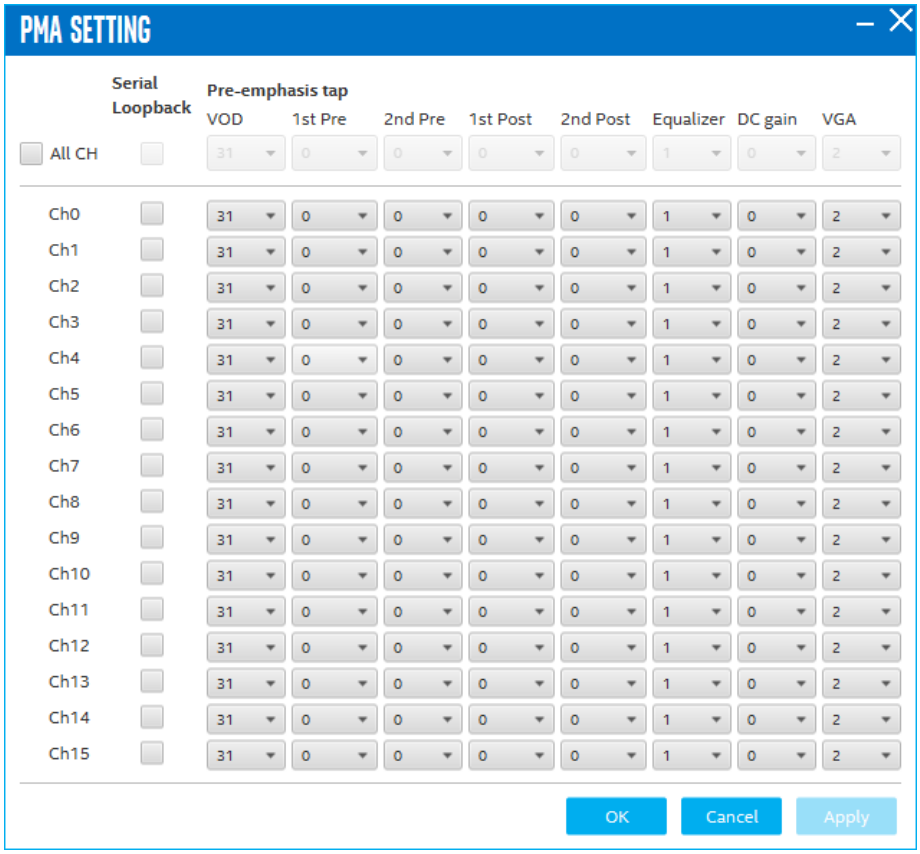
PCIe x16 Gen3

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- Serial Loopback: Routes signals between the transmitter and the receiver.
- VOD: Specifies the voltage output differential of the transmitter buffer.
- Pre-emphasis tap:
  - 1st pre: Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - 2nd pre: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - 1st post: Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - 2nd post: Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- Equalizer: Specifies the AC gain setting for the receiver equalizer in four stage mode.
- DC gain: Specifies the DC gain setting for the receiver equalizer in four stage mode.
- VGA: Specifies the VGA gain value.
- All PMA settings should be changed as given in the figure below:

Figure 26. PMA Settings



Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis:

- PRBS 7: Selects pseudo-random 7-bit sequences.
- PRBS 15: Selects pseudo-random 15-bit sequences.
- PRBS 23: Selects pseudo-random 23-bit sequences.
- PRBS 31: Selects pseudo-random 31-bit sequences.
- HF: Selects highest frequency divide-by-2 data pattern 10101010.
- LF: Selects lowest frequency divide-by-33 data pattern.

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- Detected errors: Displays the number of data errors detected in the hardware.
- Inserted errors: Displays the number of errors inserted into the transmit data stream.
- Insert error: Inserts a one-word error into the transmit data stream each time you click the button. Insert error is only enabled during transaction performance analysis.
- Clear: Resets the detected errors and inserted errors counters to zeroes.

Loopback

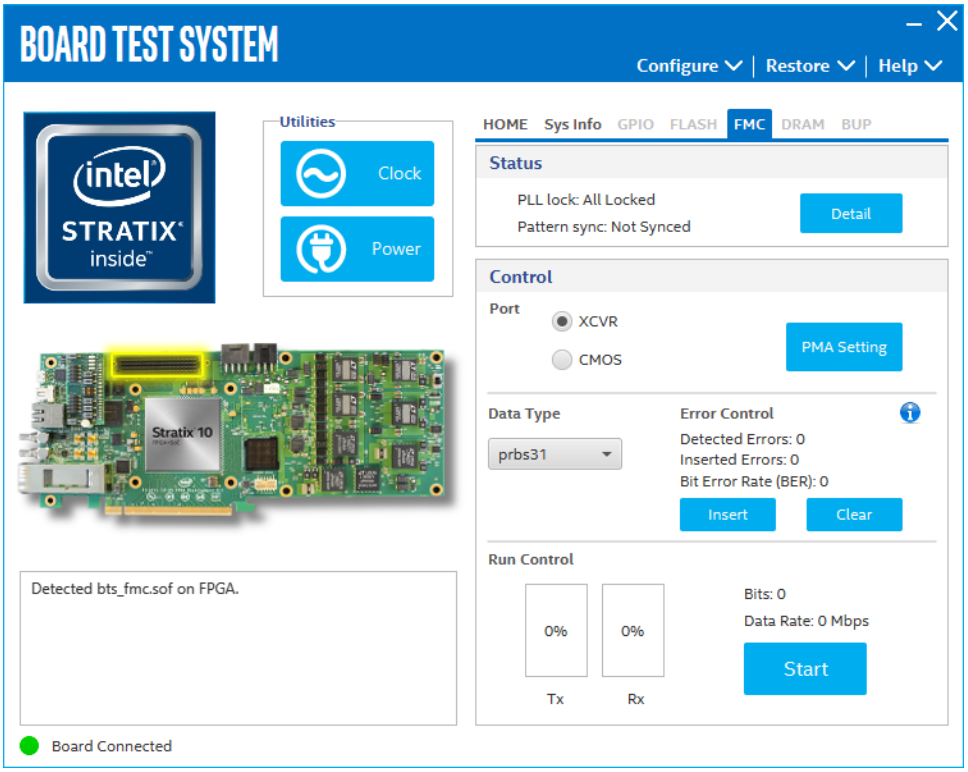
- Start: Initiates the selected ports transaction performance analysis.

  Note: Always click Clear before Start
- Stop: Terminates transaction performance analysis.
- TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

6.3.7. The FMC Tab

This tab allows you to perform loopback tests on the FMC port.

Figure 27. The FMC Tab



The following sections describe controls in the FMC tab.

Status

Displays the following status information during a loopback test:

- PLL Lock: Shows the PLL locked or unlocked state.
- Pattern Sync: Shows the pattern synced or not synced state. The pattern is considered synced when the start of he data data sequence is detected.
- Details: Shows the PLL lock and pattern sync detailed information per channel.

PLL and Pattern Status

Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Not Synced	0
1	Locked	Not Synced	0
2	Locked	Not Synced	0
3	Locked	Not Synced	0
4	Locked	Not Synced	0
5	Locked	Not Synced	0
6	Locked	Not Synced	0
7	Locked	Not Synced	0
8	Locked	Not Synced	0
9	Locked	Not Synced	0
10	Locked	Not Synced	0
11	Locked	Not Synced	0
12	Locked	Not Synced	0
13	Locked	Not Synced	0
14	Locked	Not Synced	0
15	Locked	Not Synced	0

Port

Allows you to specify the interface to test. The following port are available to test:

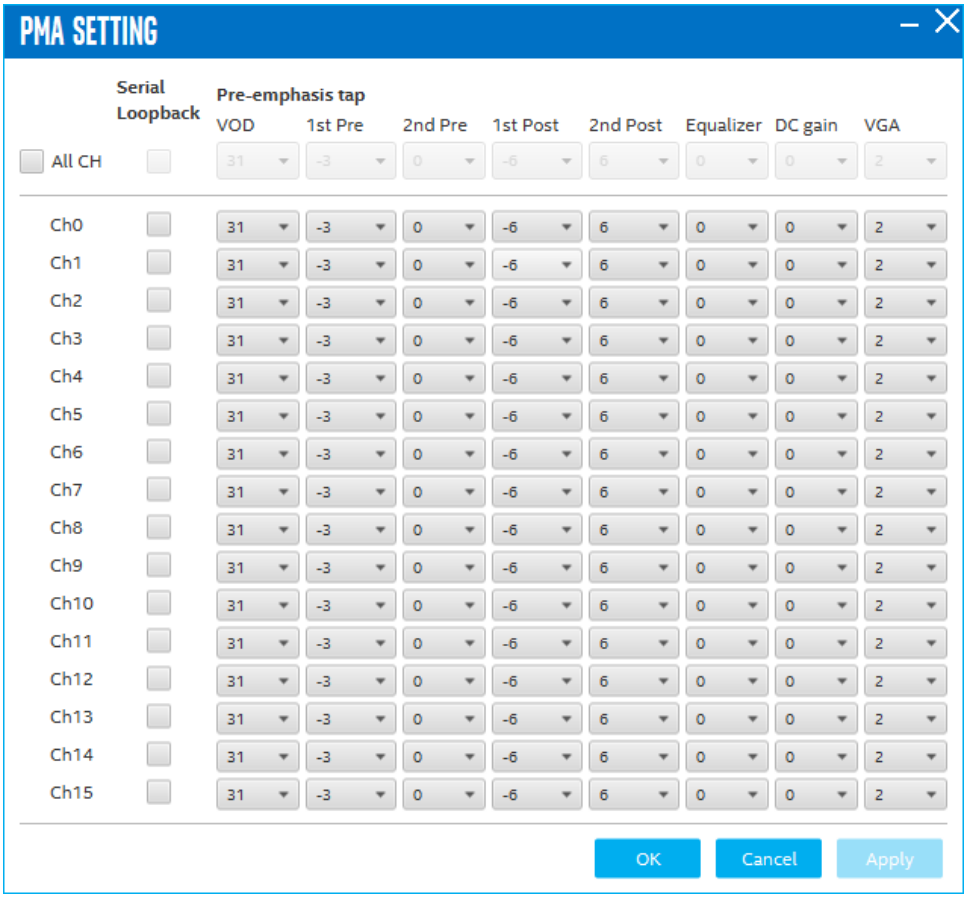
- XCVR
- CMOS

PMA Settings

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- Serial Loopback: Routes signals between the transmitter and receiver.
- VOD: Specifies the voltage output differential of the transmitter buffer.
- Pre-emphasis tap:
  - 1st pre - Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - 2nd pre - Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - 1st post - Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - 2nd post - Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- Equalizer: Specifies the AC gain setting for the receiver equalizer in four stage mode.
- DC gain: Specifies the DC gain setting for the receiver equalizer in four stage mode.
- VGA: Specifies the VGA gain value.

Figure 28. PMA Settings



Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- PRBS 7- Selects pseudo-random 7-bit sequences
- PRBS 15- Selects pseudo-random 15-bit sequences
- PRBS 23- Selects pseudo-random 23-bit sequences
- PRBS 31-Selects pseudo-random 31-bit sequences
- HF- Selects highest frequency divide-by-2 data pattern 10101010
- LF- Selects lowest frequency divide-by-33 data pattern

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- Detected errors - Displays the number of data errors detected in the hardware.
- Inserted errors - Displays the number of errors inserted into the transmit data stream.
- Insert Error - Inserts a one-word error into the transmit data stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- Clear - Resets the Detected error and Inserted error counters to zeroes.

Loopback

Start - Initiates the selected ports transaction performance analysis.

Note: Always click **Clear** before **Start**

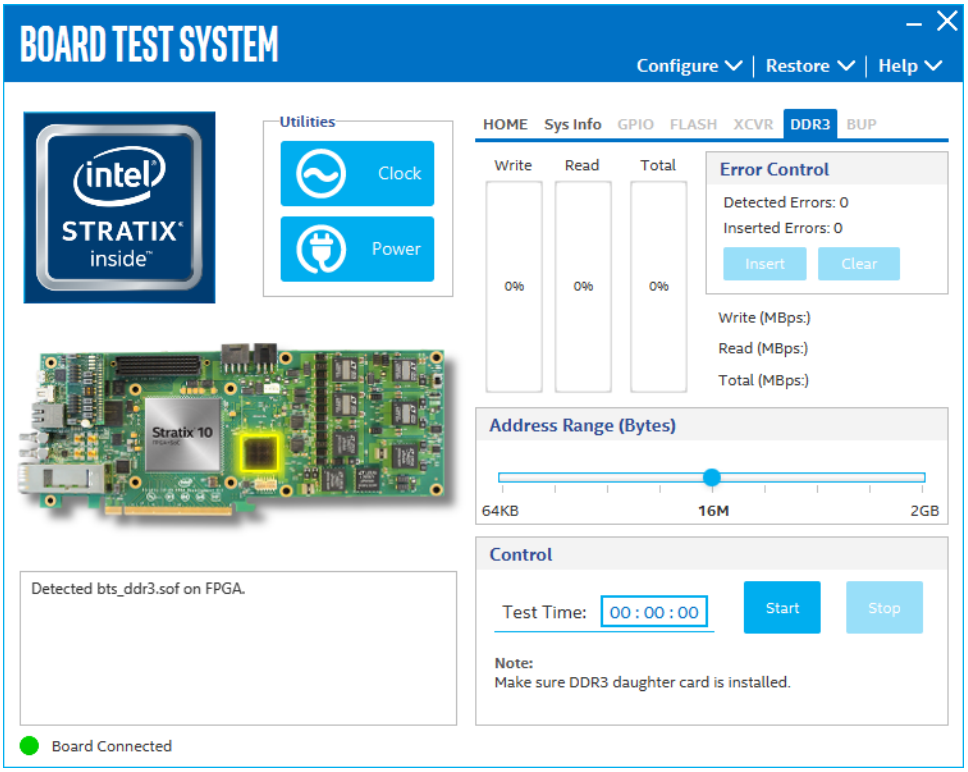
Stop - Terminates transaction performance analysis.

TX and RX performance bars - Shows the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

6.3.8. The DDR3 Tab

This tab allows you to read and write DDR3 memory on your board.

Figure 29. The DDR3 Tab



The following sections describe the controls on the DDR3 tab.

Start

Initiates DDR3 memory transaction performance analysis.

Stop

Terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked Start:

- **Write, Read and Total performance bars**: Shows the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps), Read(MBps) and Total(MBps)**: Show the number of bytes of data analyzed per second.
- **Data Bus**: 72 bits (8 bits ECC) wide and frequency is 1066 MHz double data rate. 2133 Mbps per pin. Equating to a theoretical maximum bandwidth of 136512 Mbps or 17064 MBps.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected errors**: Displays the number of data errors detected in the hardware.
- **Inserted errors**: Displays the number of errors inserted into the transaction stream.
- **Insert**: Inserts a one-word error into the transaction stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- **Clear**: Resets the Detected errors and Inserted errors counters to zeroes.

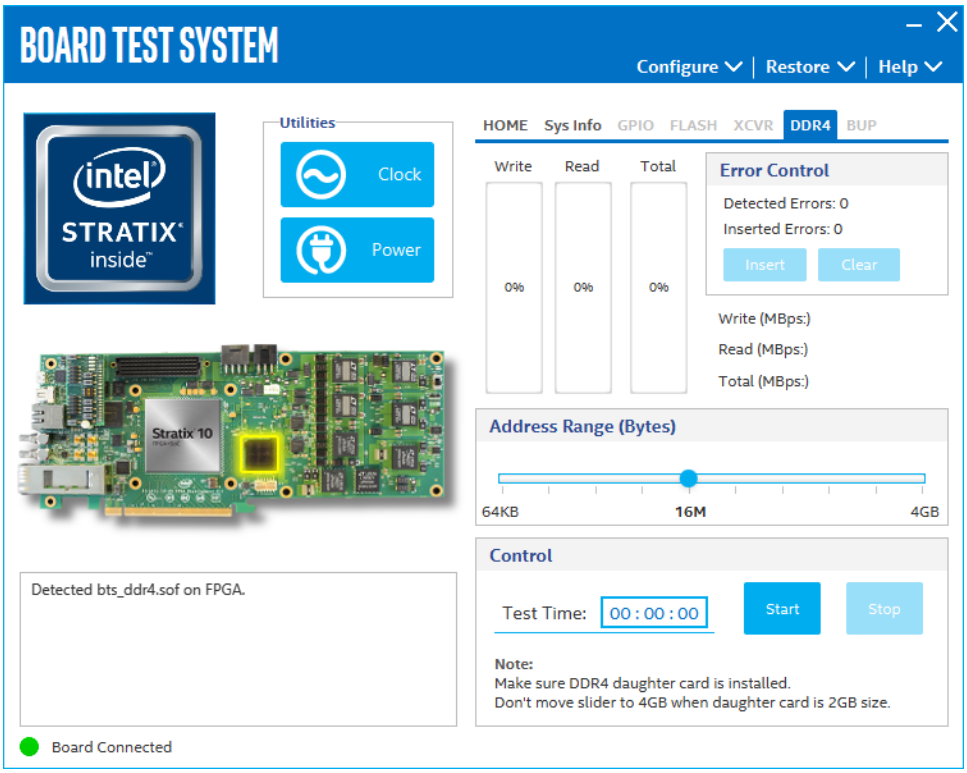
Number of Addresses to Write and Read

Determines the number of addresses to use in each iteration of reads and writes.

6.3.9. The DDR4 Tab

This tab allows you to read and write DDR4 memory on your board.

Figure 30. The DDR4 Tab



The following sections describe the controls on the DDR4 tab.

Start

Initiates DDR4 memory transaction performance analysis.

Stop

Terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked Start:

- Write, Read and Total performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- Write (MBps), Read (MBps) and Total (MBps): Show the number of bytes analyzed per second.
- Data Bus: 72 bits(8 bits ECC) wide and the frequency is 1066 MHz double data rate. 2133 Mbps per pin. Equating to a theoretical maximum bandwidth of 136,512 Mbps or 17,064 MBps.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- Detected errors: Displays the number of data errors detected in the hardware.
- Inserted errors: Displays the number of errors inserted into the transaction stream.
- Insert: Inserts a one-word error into the transaction stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- Clear: Resets the detected error and inserted error counters to zeroes.

Number of Addresses to Read and Write

Determines the number of addresses to use in each iteration of reads and writes.

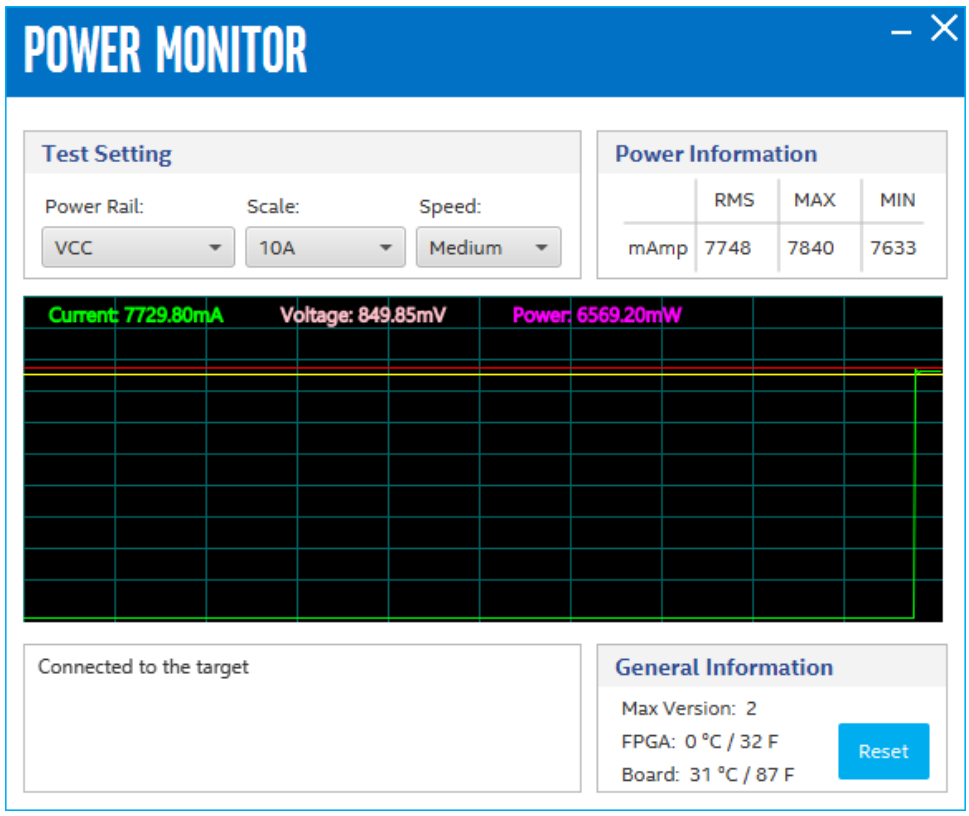
6.3.10. Power Monitor

The Power Monitor measures and reports current power information and communicates with the MAX V device on the board through the JTAG bus. A power monitor circuit attached to the MAX V device allows you to measure the power that the FPGA is consuming.

To start the application, click the Power Monitor icon in the BTS. You can also run the Power Monitor as a stand-alone application. The `PowerMonitor.exe` resides in the `<package dir>\examples\board_test_system` directory.

Note: You cannot run the stand-alone power application and the BTS simultaneously. Also, you cannot run power and clock interface at the same time.

Figure 31. Power Monitor Interface



The controls on the Power Monitor are described below.

Test Settings

Displays the following controls:

- Power Rails: Indicates the currently selected power rail. After selecting the desired rail, click Reset to refresh the screen with updated board readings.
- Scale: Specifies the amount to scale the power graph. Select a smaller number to zoom-in to see finer detail. Select a larger number to zoom-out to view the entire range of recorded values.
- Speed: Specifies how often to refresh the graph.

Power Information

Displays the root mean square (RMS) current, maximum and minimum numerical power readings in mA.

Graph

Displays the mA power consumption of your board over time. The green line indicates the current value. The red line indicates the maximum value read since the last reset. The yellow line indicates the minimum value read since the last reset.

General Information

Displays the MAX V version and current temperature of the FPGA and the board.

Reset

Clears the graph, resets the minimum and maximum values and restarts the Power Monitor.

6.3.11. Clock Controller

The Clock Controller application sets the Si5338 programmable oscillators to any frequency between 0.16 MHz and 710 MHz.

The Clock Controller application sets the Si5341 programmable oscillators to any frequency between 0.1 MHz and 712.5 MHz.

The Clock Control communicates with the MAX V on the board through the JTAG bus. The programmable oscillator are connected to the MAX V device through a 2-wire serial bus.

Figure 32. Clock Controller - Si5338

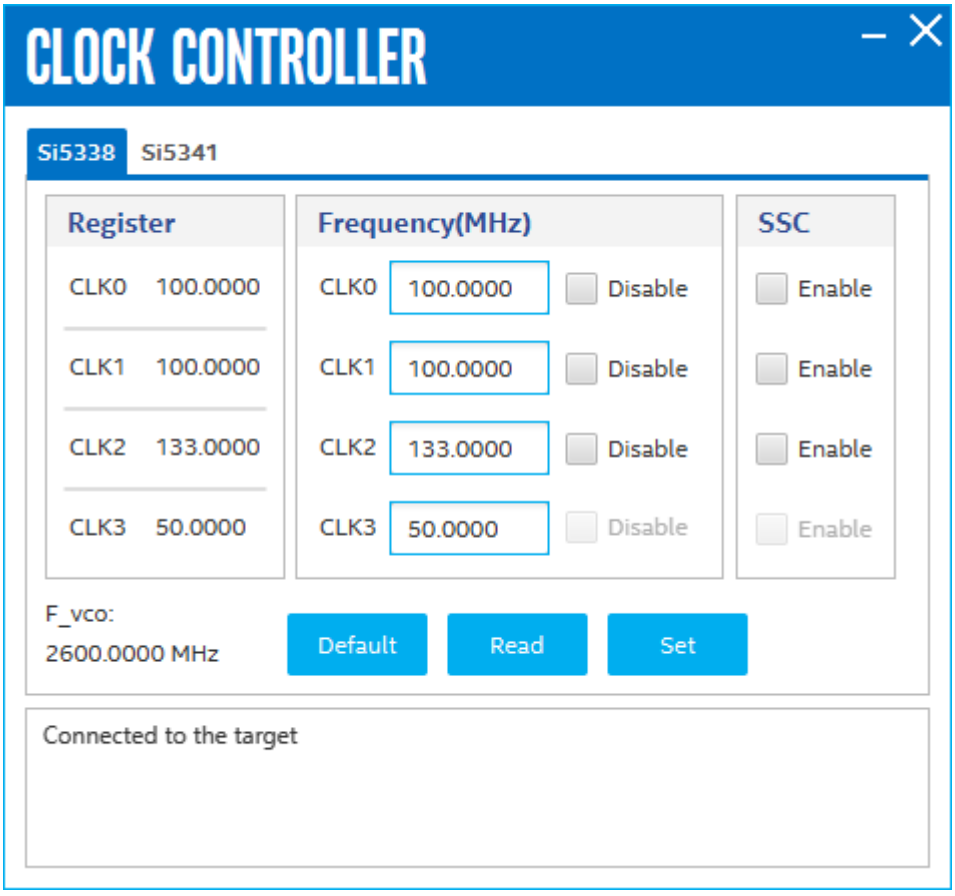
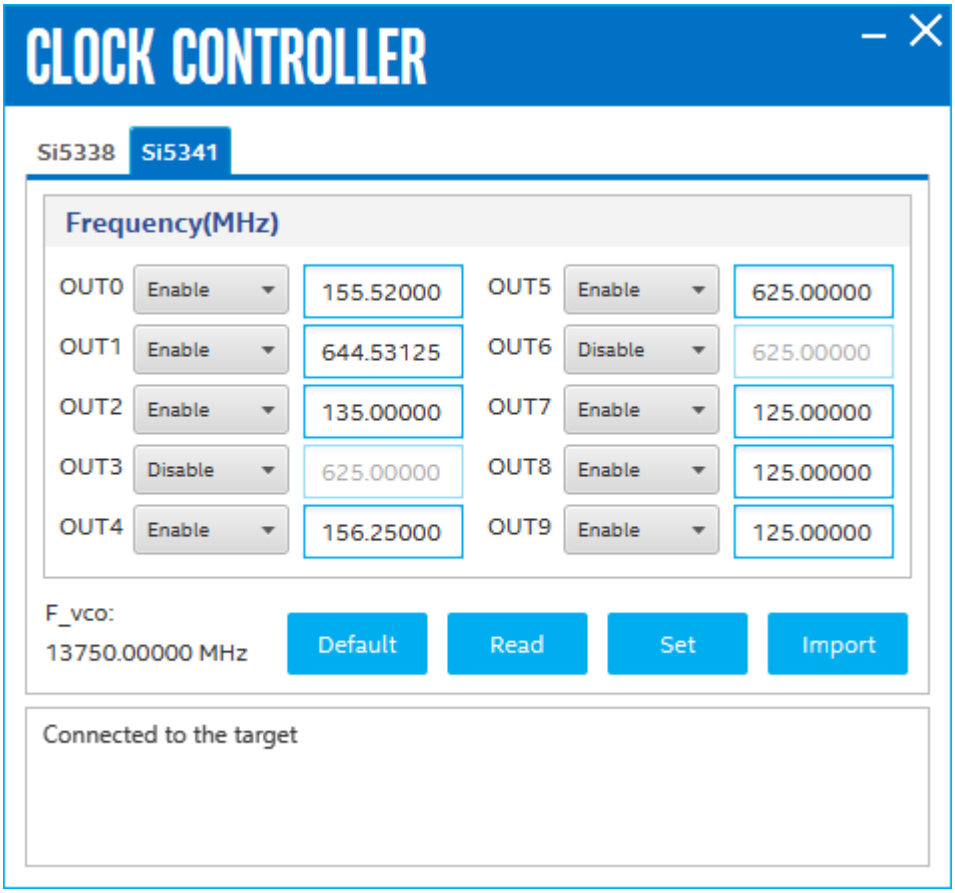


Figure 33. Clock Controller - Si5341



Si5338 tab and Si5341 tab display the same GUI controls for each clock generators. Each tab allows for separate control. The Si5338 is capable of synthesizing four independent user-programmable clock frequencies up to 710 MHz.

The controls of the clock controller are described below:

F_vco

Displays the generating signal value of the voltage-controlled oscillator.

Registers

Display the current frequencies for each oscillator.

Frequency

Allows you to specify the frequency of the clock MHz.

SSC

Set enable or disable Spread Spectrum Clocking.

Read

Reads the current frequency setting for the oscillator associated with the active tab.

Default

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

Set Freq

Sets the programmable oscillator frequency for the selected clock to the value in the CLK0 to CLK3 controls for the Si5338. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Intel recommends resetting the FPGA logic after changing frequencies.

Import

Import register map file generated from Silicon Laboratories ClockBuilder Desktop.

6.4. Smart VID Setting

If you are creating your own design and want to generate programming **.sof** file, you must add the correct Smart VID Setting into the Intel Quartus Prime project for successfully configuring the Intel Stratix 10 GX FPGA Development Kit. Before you add the following Smart VID setting into the **.qsf** file, you must change the configuration scheme to Avalon® streaming interface x16 for your project. You can also extract the Smart VID setting from the Golden Top file.

```
set_global_assignment -name USE_PWRMGT_SCL SDM_IO14
set_global_assignment -name USE_PWRMGT_SDA SDM_IO11
set_global_assignment -name USE_CONF_DONE SDM_IO16
set_global_assignment -name USE_INIT_DONE SDM_IO0
set_global_assignment -name VID_OPERATION_MODE "PMBUS MASTER"
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "400 KHZ"
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE LTM4677
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 4F
set_global_assignment -name PWRMGT_SLAVE_DEVICE1_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE2_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE3_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE4_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE5_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE6_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE7_ADDRESS 00
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE ON
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "AUTO DISCOVERY"
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
```

Figure 34. Power Management & VID

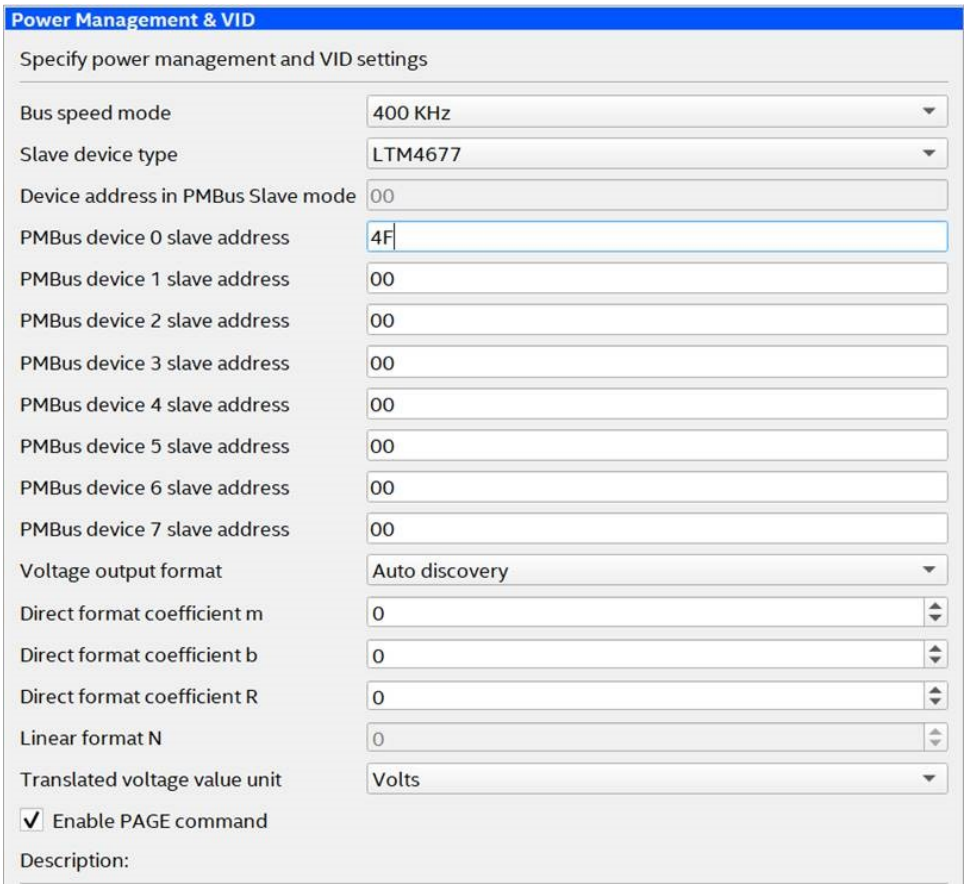
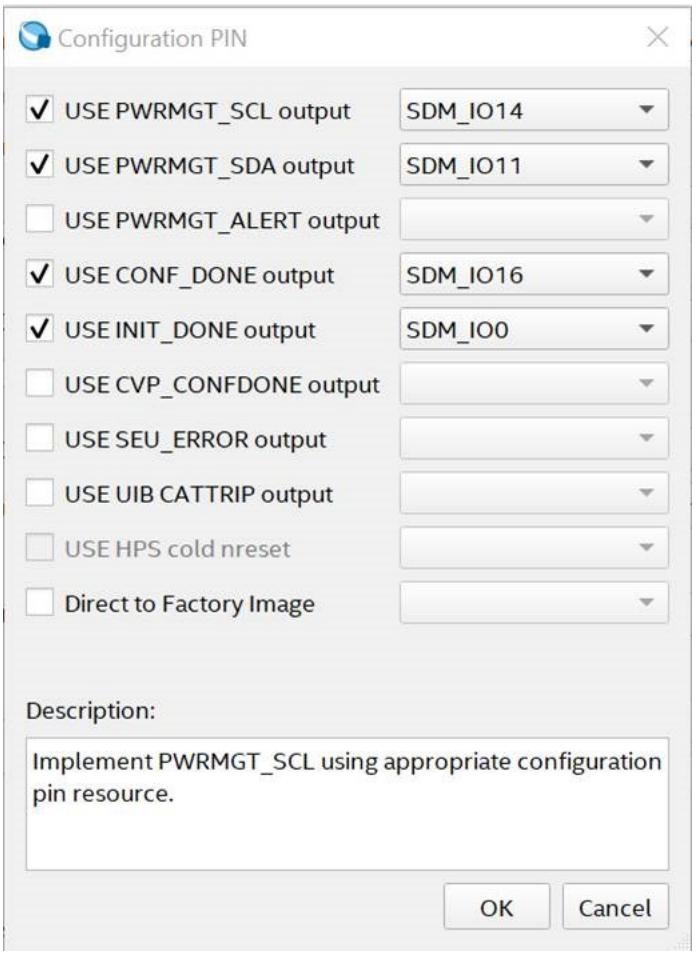


Figure 35. Configuration PIN



A. Additional Information

A.1. Safety and Regulatory Information

ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

A.1.1. Safety Warnings

Power Supply Hazardous Voltage

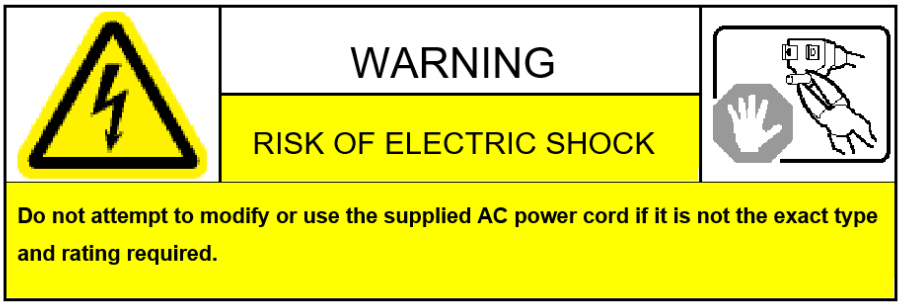
AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment that attaches to this product is also connected to properly wired and grounded receptacles.



Power Cord Requirements

The connector that plugs into the wall outlet must be a grounding-type male plug designed for use in your region. It must have marks showing certification by an agency in your region. The connector that plugs into the AC receptacle on the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord and do not use it with adapters.

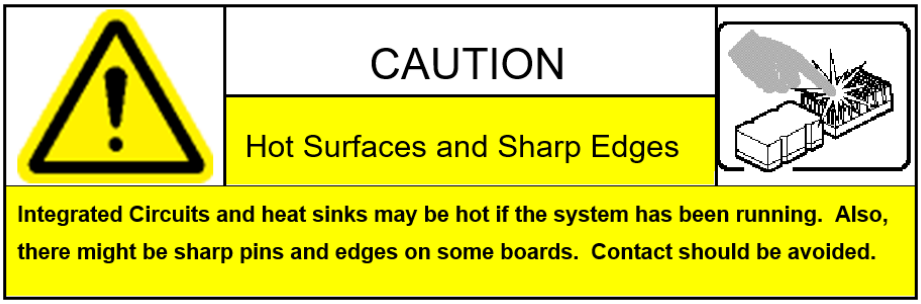
Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

A.1.2. Safety Cautions



Caution: Hot Surfaces and Sharp Edges. Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp edges on some boards. Contact should be avoided.

Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.

Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interfence to radio or television reception, which can be determined by turning the equipment on and off, the user is required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.

Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

Attention: Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

A.2. Compliance and Conformity Statements

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2004/108/EC. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

CE

B. Revision History

Table 40. Revision History for the Intel Stratix 10 GX FPGA Development Kit User Guide

Document Version	Changes
2020.04.02	Added Smart VID Setting on page 88
2019.09.20	Updated: • Updated *Table: PCI Express Pin Assignments, Schematic Signal Names and Functions* in PCI Express on page 28 • Updated *Figure: Intel Stratix 10 GX FPGA Board - Clock Inputs and Default Frequencies* in On-Board Oscillators on page 46
2019.06.11	Updated Table *SW1 DIP Switch Default Settings (Board TOP)* in the section Default Switch and Jumper Settings on page 10 to clarify that MSEL [0] is tied to Vcc
2019.03.29	• Added featured device information in *Table: Intel Stratix 10 GX FPGA Development Kit Versions*. • Renamed the USB-Blaster to Intel FPGA Download Cable II. • Labeled the components of the board in the following: — *Figure: Intel Stratix 10 GX FPGA Development Board Image - Front* — *Figure: Intel Stratix 10 GX FPGA Development Board Image - Rear*
2018.11.27	Updated figure in Default Switch and Jumper Settings on page 10. Default position representation of M5JTAG_BYPASSn signal in switch SW6 is corrected to OFF position to ensure it matches the table description
2018.07.20	Added FPGA device variant GX to the document title
2017.12.28	Corrected errors in pin table in HiLo External Memory Interface on page 31
2017.12.22	Updated tables in HiLo External Memory Interface on page 31, QSFP on page 41 and DisplayPort on page 43
2017.10.11	• Corrected errors in Pin tables for PCI Express on page 28, HiLo External Memory Interface on page 31, FMC on page 36, QSFP on page 41 and DisplayPort on page 43 • Reorganized Revision History as a separate Appendix
2017.04.17	Engineering Silicon (ES) Release
2016.12.23	Preliminary Release