DATASHEET

ISL8023, ISL8024

Compact Synchronous Buck Regulator

FN7812
Rev 3.00
March 24, 2014

The ISL8023, ISL8024 are highly efficient, monolithic, synchronous step-down DC/DC converters that can deliver 3A (ISL8023) or 4A (ISL8024) of continuous output current from a 2.7V to 5.5V input supply. The devices use current mode control architecture to deliver very low duty cycle operation at high frequency with fast transient response and excellent loop stability.

The ISL8023 and ISL8024 integrate a very low On-resistance P-Channel (45mΩ) high side FET and N-Channel (19mΩ) low side FET to maximize efficiency and minimize external component count. The 100% duty-cycle operation allows less than 200mV dropout voltage at 4A output current. The operation frequency of the pulse-width modulator (PWM) is adjustable from 500kHz to 4MHz. The default switching frequency of 1MHz is set by connecting the FS pin high, which allows for the use of small external components.

The ISL8023, ISL8024 can be configured for discontinuous or forced continuous operation at light load. Forced continuous operation reduces noise and RF interference while discontinuous mode provides higher efficiency by reducing switching losses at light loads.

Fault protection is provided by internal hiccup mode current limiting during short circuit and overcurrent conditions. Other protection, such as overvoltage and over-temperature are also integrated into the device. A power-good output voltage monitor indicates when the output is in regulation.

The ISL8023, ISL8024 offer a 1ms Power-Good (PG) timer at power-up. When in shutdown, ISL8023, ISL8024 discharges the output capacitor through an internal soft-stop switch. Other features include internal fixed or adjustable soft-start and internal/external compensation.

The ISL8023 and ISL8024 are offered in a space saving 16 Ld 3x3 Pb-free QFN package with an exposed pad for improved thermal performance and 1mm maximum height. The complete converter occupies less than 0.22 in^2 area.

Various fixed output voltages are available upon request. See the “Ordering Information” on page 4 for more details.

Features

- 2.7V to 5.5V input voltage range
- Very low on-resistance FET’s - P-Channel 45mΩ and N-Channel 19mΩ typical values
- High efficiency synchronous buck regulator with up to 95% efficiency
- 0.8% reference accuracy over-temperature/load/line
- Complete BOM with as few as 3 external parts
- Start-up with pre-biased output
- Internal soft-start - 1ms or adjustable
- Soft-stop output discharge during disabled
- Adjustable frequency from 500kHz to 4MHz - default at 1MHz (8023/24), 2MHz (8023A/24A)
- External synchronization up to 4MHz
- Over-temperature, Overcurrent, Overvoltage and negative overcurrent protection
- Tiny 3x3 QFN package

Applications

- DC/DC POL modules
- μC/μP, FPGA and DSP power
- Plug-in DC/DC modules for routers and switchers
- Portable instruments
- Test and measurement systems
- Li-ion battery powered devices

Related Literature

- See AN1759, “3A/4A Low Quiescent Current High Efficiency Synchronous Buck Regulator”

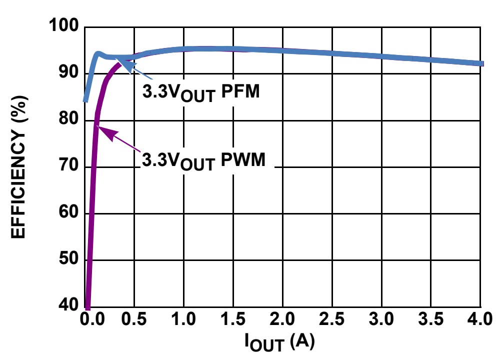
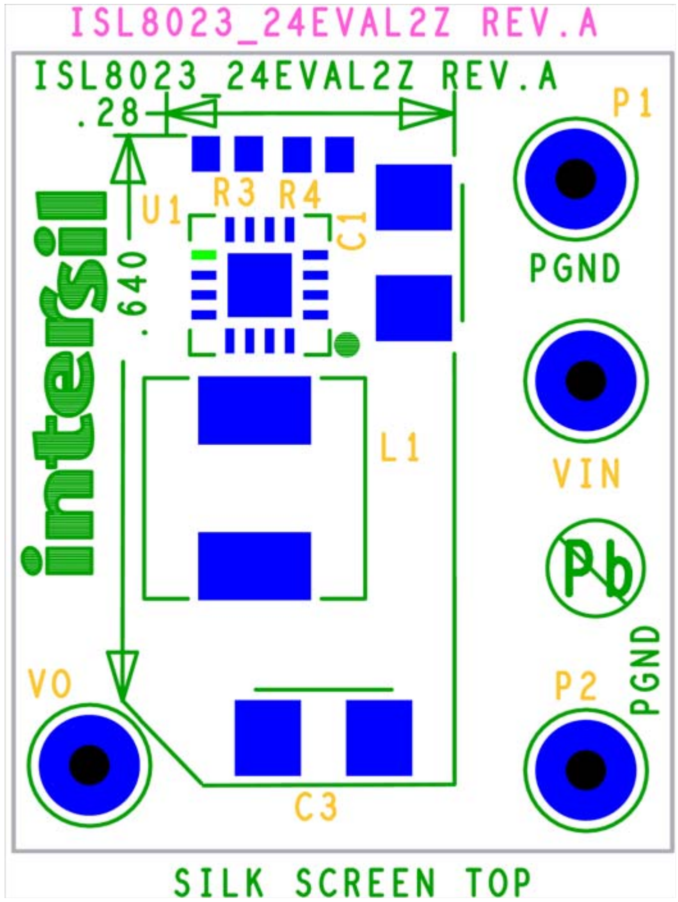


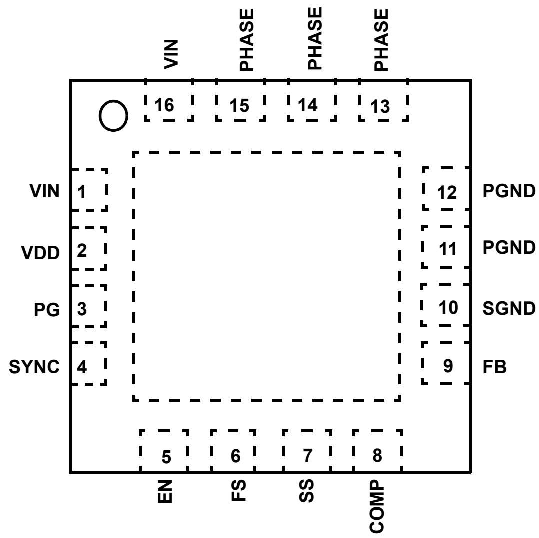
FIGURE 1. EFFICIENCY T = +25°C, V_{IN} = 5V



NOTE: Full solution in size board. The full schematic and Gerber files are available for down load from Intersil.com.

Pin Configuration

ISL8023, ISL8024
(16 LD TQFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1, 16	VIN	Input supply voltage. Connect two 22µF ceramic capacitors to power ground.
2	VDD	Input supply voltage for the logic. Connect VIN PIN.
3	PG	Power-good is an open-drain output. Use 10kΩ to 100kΩ pull-up resistor connecting between VIN and PG. At power-up or EN HI, PG rising edge is delayed by 1ms upon output reached within regulation.
4	SYNC	Mode Selection pin. Connect to logic high or input voltage VIN for PWM mode. Connect to logic low or ground for PFM mode. Connect to an external function generator for synchronization with the positive edge trigger. There is an internal 1MΩ pull-down resistor to prevent an undefined logic state in case of SYNIN pin float.
5	EN	Regulator enable pin. Enable the output when driven to high. Shutdown the chip and discharge output capacitor when driven to low. There is an internal 1MΩ pull-down resistor to prevent an undefined logic state in case of EN pin float.
6	FS	This pin sets the oscillator switching frequency, using a resistor, RFS, from the FS pin to GND. The frequency of operation may be programmed between 500kHz to 4MHz. The default frequency is 1MHz and configured for internal compensation if FS is connected to VIN.
7	SS	SS is used to adjust the soft-start time. Set to SGND for internal 1ms rise time. Connect a capacitor from SS to SGND to adjust the soft-start time. Do not use more than 33nF per IC.
8, 9	COMP, FB	The feedback network of the regulator, VFB, is the negative input to the transconductance error amplifier. COMP is the output of the amplifier if FS resistor is used. Otherwise COMP is disconnected thru a MOSFET for internal compensation. Recommend connecting COMP to SGND in internal compensation mode. The output voltage is set by an external resistor divider connected to VFB. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.6V reference. There is an internal compensation to meet a typical application. Additional external network across COMP and SGND might be required to improve the loop compensation of the amplifier operation. In addition, the regulator power-good and undervoltage protection circuitry use VFB to monitor the regulator output voltage.
10	SGND	Signal ground.
11, 12	PGND	Power ground.
13, 14, 15	PHASE	Switching node connection. Connect to one terminal of the inductor.
Exposed Pad	-	The exposed pad must be connected to the SGND pin for proper electrical performance. Place as much vias as possible under the pad connecting to SGND plane for optimal thermal performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	OUTPUT VOLTAGE (V)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL8023IRTAJZ	023A	Adjustable	-40 to +85	16 Ld 3x3 TQFN	L16.3x3D
ISL8024IRTAJZ	024A	Adjustable	-40 to +85	16 Ld 3x3 TQFN	L16.3x3D
ISL8023AIRTAJZ	23AA	Adjustable	-40 to +85	16 Ld 3x3 TQFN	L16.3x3D
ISL8024AIRTAJZ	24AA	Adjustable	-40 to +85	16 Ld 3x3 TQFN	L16.3x3D
ISL8023EVAL3Z	Evaluation Board				
ISL8024EVAL3Z	Evaluation Board				
ISL8023AEVAL3Z	Evaluation Board				
ISL8024AEVAL3Z	Evaluation Board				

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL8023, ISL8024. For more information on MSL, please see tech brief TB363.

Typical Application Diagram

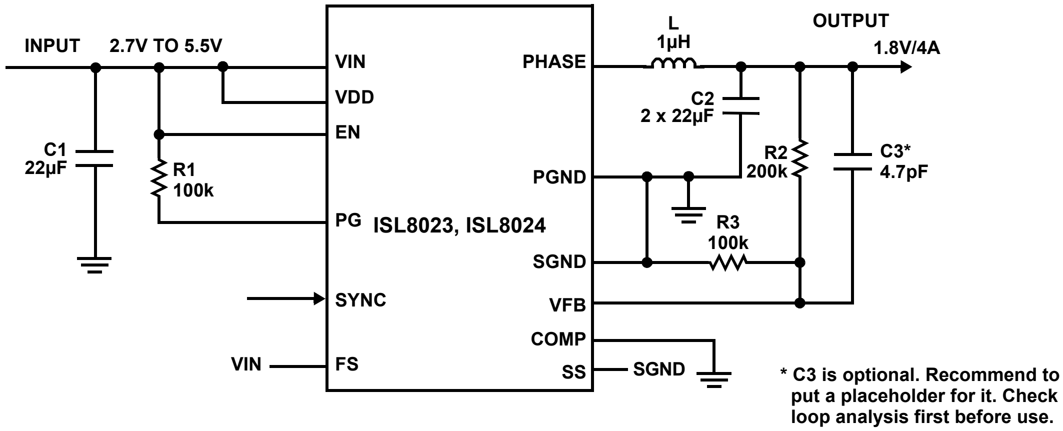


FIGURE 2. TYPICAL APPLICATION DIAGRAM

TABLE 1. COMPONENT SELECTION TABLE

V_{OUT}	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	3.6
C1	22µF	22µF	22µF	22µF	22µF	22µF	22µF
C2	4X22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF
C3	4.7pF	4.7pF	4.7pF	4.7pF	4.7pF	4.7pF	4.7pF
L1	0.47~1µH	0.47~1µH	0.47~1µH	0.68~1.5µH	0.68~1.5µH	1~2.2µH	1~2.2µH
R2	33k	100k	150k	200k	316k	450k	500k
R3	100k	100k	100k	100k	100k	100k	100k

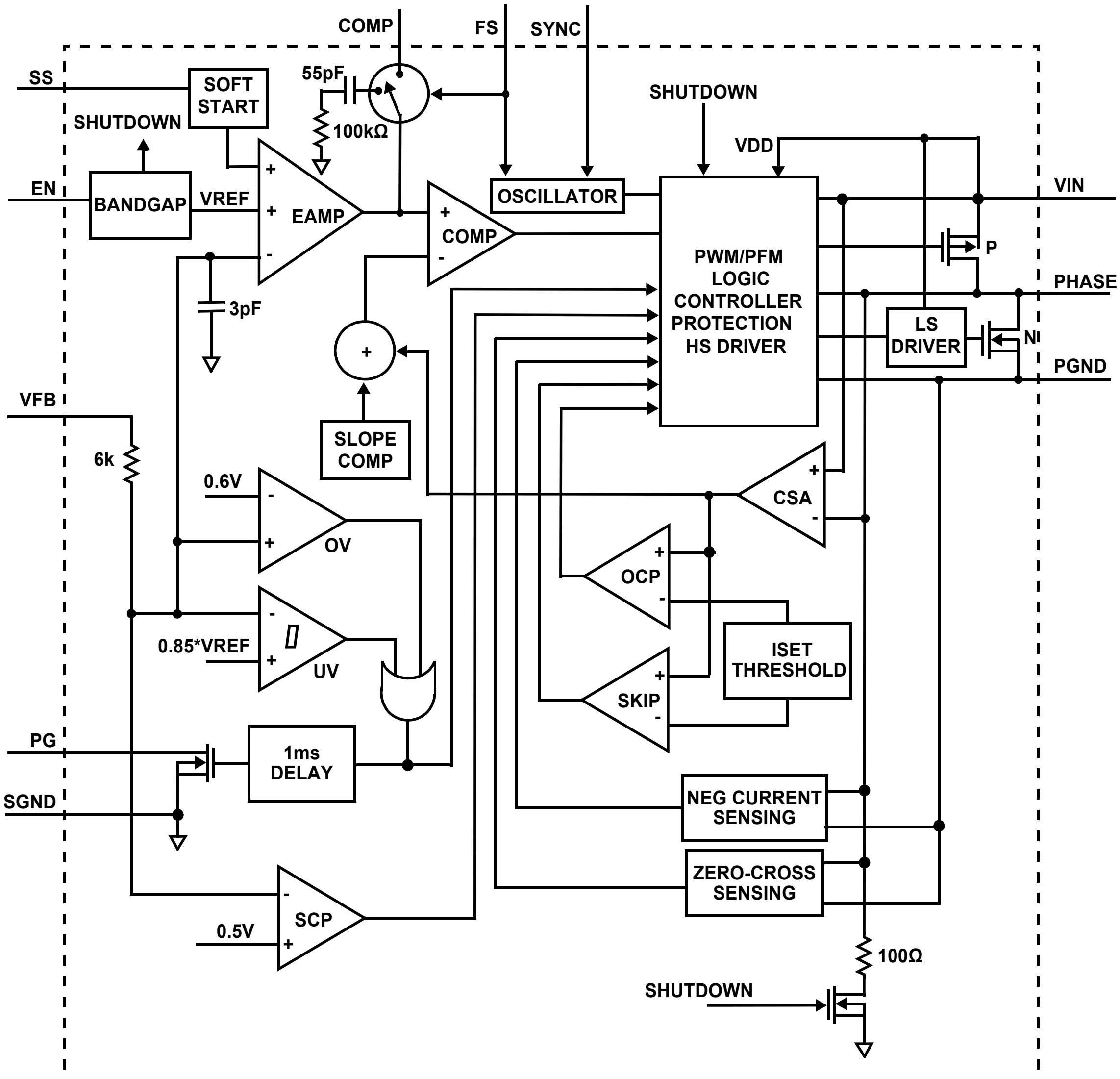


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Absolute Maximum Ratings (Reference to GND)

VIN . . . . -0.3V to 6.5V (DC) or 7V (20ms)
EN, FS, PG, SYNC, VFB . . . . -0.3V to VIN + 0.3V
PHASE . . . . -3V (100ns)/(DC) to 6.5V (DC)
COMP, SS. . . . . -0.3V to 2.7V

Recommended Operating Conditions

VIN Supply Voltage Range . . . . 2.7V to 5.5V
Load Current Range . . . . 0A to 4A
Ambient Temperature Range . . . . -40°C to +85°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 LD TQFN Package (Notes 4, 5)	45	6.5

Junction Temperature Range . . . . -55°C to +125°C
Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. θ_{JC}, “case temperature” location is at the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, all parameter limits are established over the recommended operating conditions and the typical specification are measured at the following conditions: T_A = -40°C to +85°C, V_{IN} = 3.6V, EN = V_{IN}, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
INPUT SUPPLY						
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising, no load		2.5	**2.7**	V
		Falling, no load	**2.2**	2.4		V
Quiescent Supply Current	I_{VIN}	SYNC = GND, no load at the output		50		µA
		SYNC = GND, no load at the output and no switches switching		50	**60**	µA
		SYNC = V_{IN}, F_S = 1MHz, no load at the output		8	**15**	mA
Shutdown Supply Current	I_{SD}	SYNC = GND, V_{IN} = 5.5V, EN = low		5	**7**	µA
OUTPUT REGULATION						
Reference Voltage - ISL8023IRZ, ISL8024IRZ	V_{REF}		**0.595**	0.600	**0.605**	V
VFB Bias Current - ISL8023IRZ, ISL8024IRZ	I_{VFB}	VFB = 0.75V		0.01		µA
Line Regulation		V_{IN} = V_O + 0.5V to 5.5V (minimal 2.7V)		0.2		%/V
Soft-Start Ramp Time Cycle		SS = SGND		1		ms
Soft-Start Charging Current	I_{SS}	V_{SS} = 0.1V	**1.2**	1.6	**2.0**	µA
OVERCURRENT PROTECTION						
Current Limit Blanking Time	t_{OCON}			17		Clock pulses
Overcurrent and Auto Restart Period	t_{OCOFF}			8		SS cycle
Positive Peak Current Limit	I_{PLIMIT}	4A application	**5.2**	6.5	**7.8**	A
		3A application	**3.9**	4.8	**5.9**	A
Peak Skip Limit	I_{SKIP}	4A application (test at 3.6V)	**0.9**	1.2	**1.5**	A
		3A application (test at 3.6V)	**0.65**	0.9	**1.15**	A
Zero Cross Threshold			**-200**		**200**	mA
Negative Current Limit	I_{NLIMIT}		**-3.0**	-2.4	**-1.8**	A

Electrical Specifications Unless otherwise noted, all parameter limits are established over the recommended operating conditions and the typical specification are measured at the following conditions: T_A = -40°C to +85°C, V_{IN} = 3.6V, EN = V_{IN}, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
COMPENSATION						
Error Amplifier Trans-Conductance		FS = VIN		80		µA/V
		FS with Resistor		150		µA/V
Trans-Resistance	RT		**0.15**	0.2	**0.25**	Ω
PHASE						
P-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA	**35**	45	**55**	mΩ
		V_{IN} = 2.7V, I_O = 200mA	**50**	70	**90**	mΩ
N-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA	**12**	19	**25**	mΩ
		V_{IN} = 2.7V, I_O = 200mA	**20**	28	**37**	mΩ
PHASE Maximum Duty Cycle				100		%
PHASE Minimum On-Time		SYNC = High			**140**	ns
OSCILLATOR						
Nominal Switching Frequency	Fsw	FS = VIN	**800**	1000	**1200**	kHz
		FS with RS = 402kΩ		490		kHz
		FS with RS = 42.2kΩ		4200		kHz
SYNC Logic Low to High Transition Range			**0.70**	0.75	**0.80**	V
SYNC Hysteresis				0.15		V
SYNC Logic Input Leakage Current		V_{IN} = 3.6V		3.6	**5**	µA
PG						
Output Low Voltage					**0.3**	V
Delay Time (Rising Edge)			**0.5**	1	**2**	ms
PG Pin Leakage Current				0.01	**0.1**	µA
OVP PG Rising Threshold				0.80		V
UVP PG Rising Threshold			**80**	85	**90**	%
UVP PG Hysteresis				5		%
PGOOD Delay Time (Falling Edge)				15		µs
EN						
Logic Input Low					**0.4**	V
Logic Input High			**0.9**			V
EN Logic Input Leakage Current				0.1	**1**	µA
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				25		°C

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 4A.

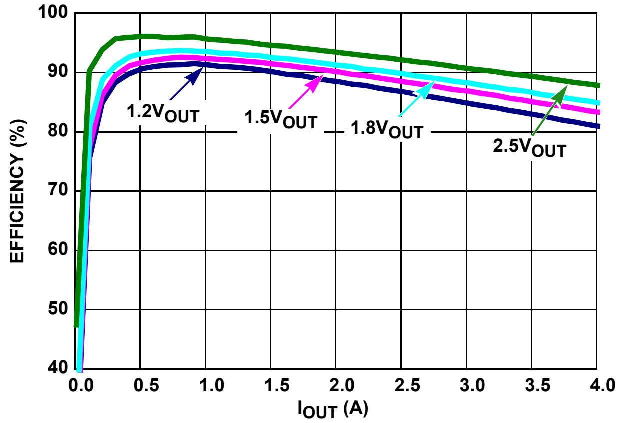


FIGURE 4. EFFICIENCY vs LOAD (1MHz 3.3 V_{IN} PWM)

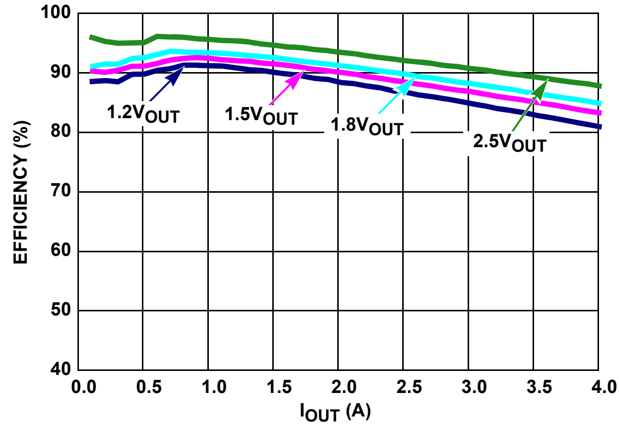


FIGURE 5. EFFICIENCY vs LOAD (1MHz 3.3 V_{IN} PFM)

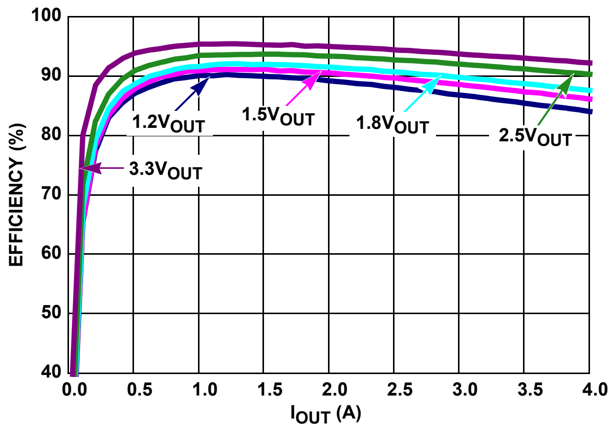


FIGURE 6. EFFICIENCY vs LOAD (1MHz 5V_{IN} PWM)

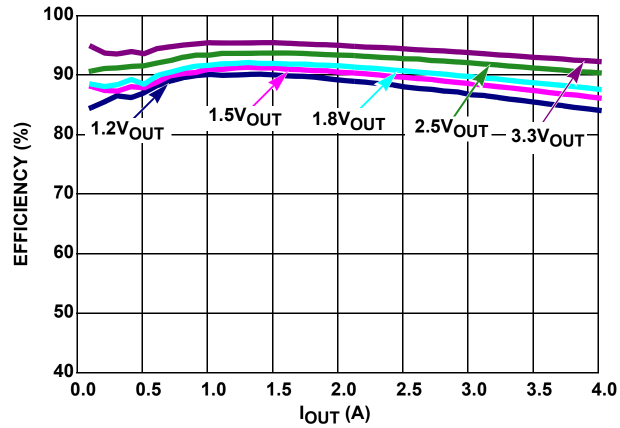


FIGURE 7. EFFICIENCY vs LOAD (1MHz 5V_{IN} PFM)

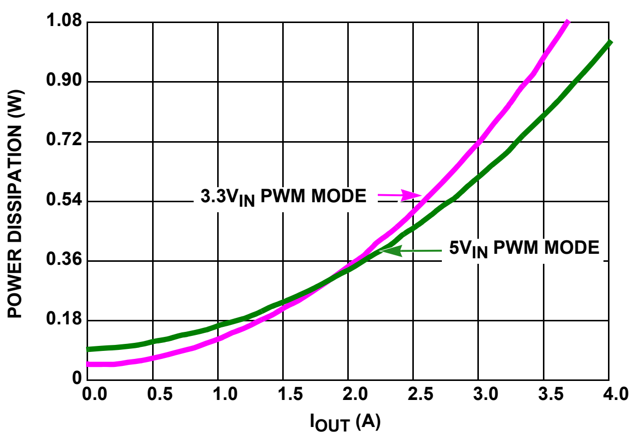


FIGURE 8. POWER DISSIPATION vs LOAD (1MHz, V_{OUT} = 1.8V)

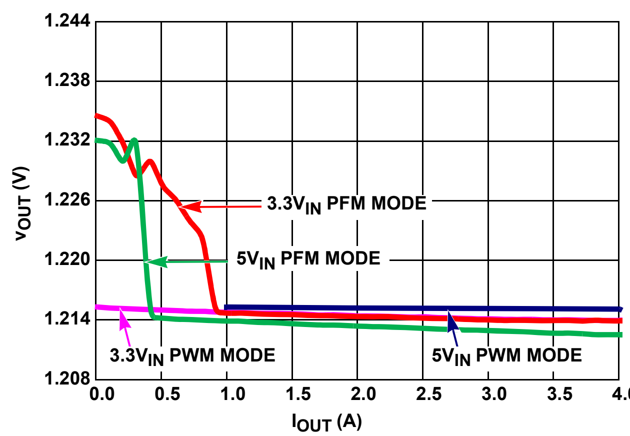


FIGURE 9. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.2V)

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 4A. **(Continued)**

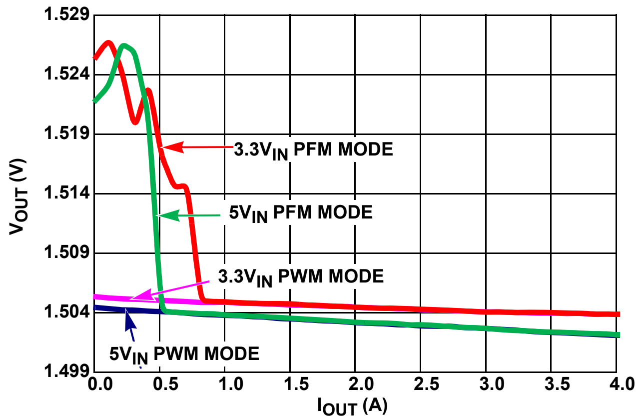


FIGURE 10. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.5V)

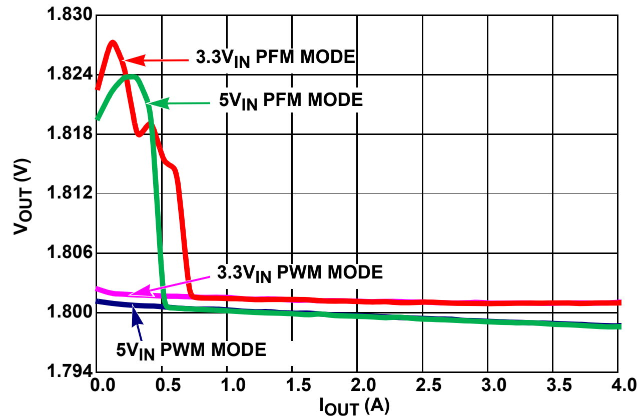


FIGURE 11. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.8V)

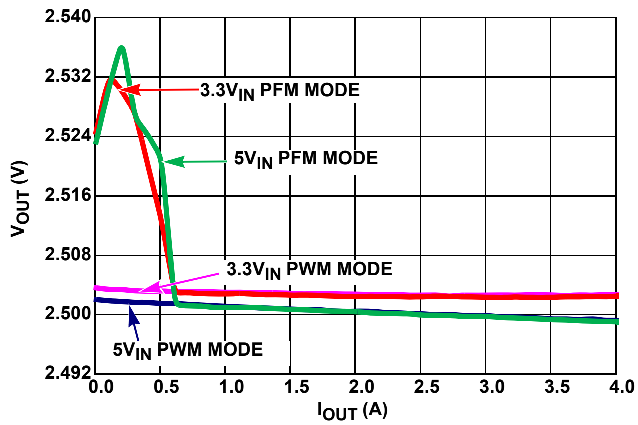


FIGURE 12. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 2.5V)

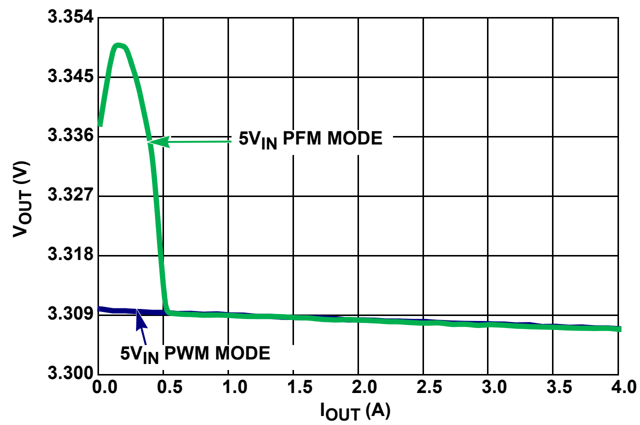


FIGURE 13. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 3.3V)

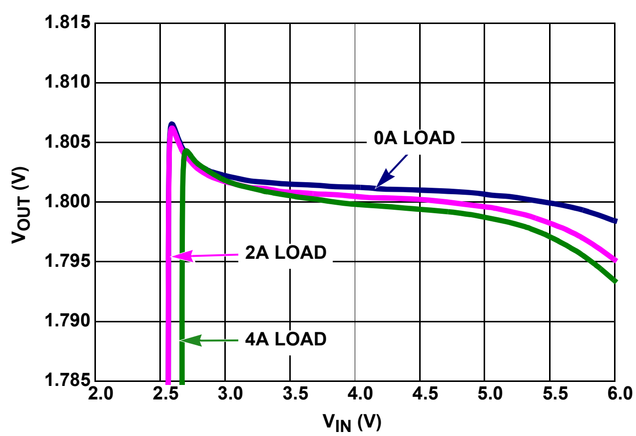


FIGURE 14. OUTPUT VOLTAGE REGULATION vs V_{IN} (PWM V_{OUT} = 1.8)

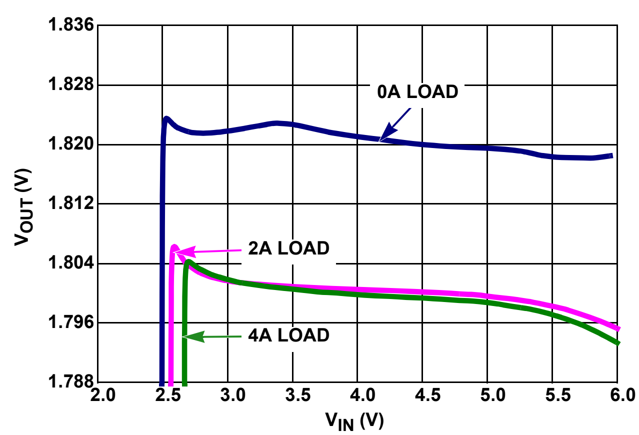


FIGURE 15. OUTPUT VOLTAGE REGULATION vs V_{IN} (PFM V_{OUT} = 1.8V)

Typical Operating Performance

Unless otherwise noted, operating conditions are: $T_A = +25°C$, $V_{VIN} = 5V$, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 4A. **(Continued)**

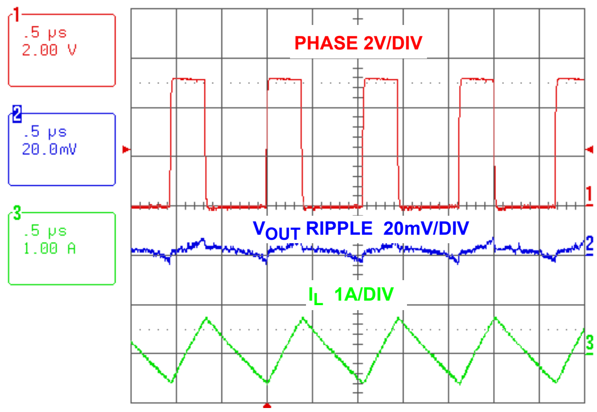


FIGURE 16. STEADY STATE OPERATION AT NO LOAD (PWM)

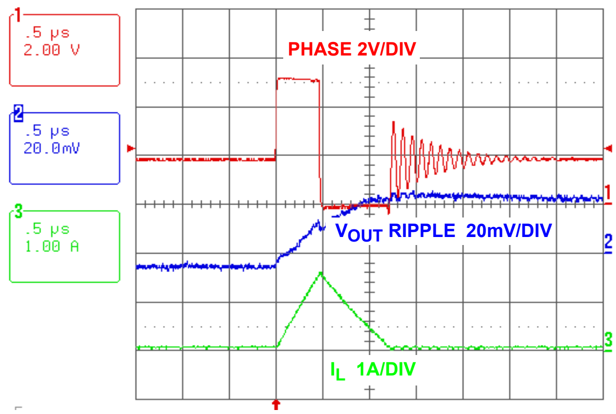


FIGURE 17. STEADY STATE OPERATION AT NO LOAD (PFM)

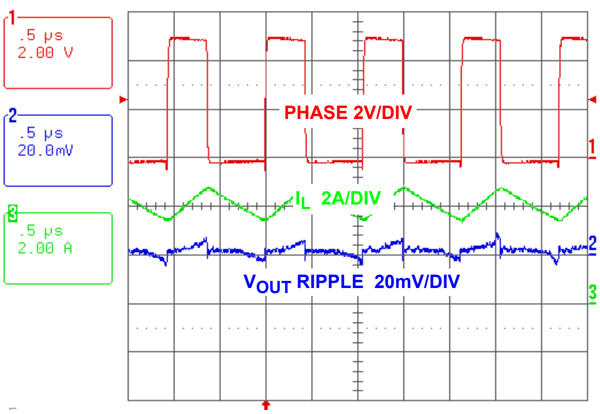


FIGURE 18. STEADY STATE OPERATION WITH FULL LOAD

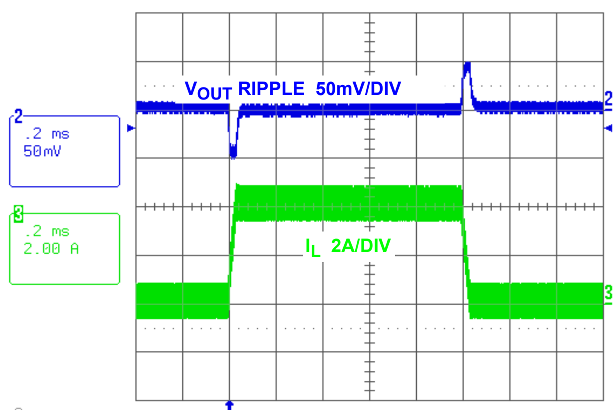


FIGURE 19. LOAD TRANSIENT (PWM)

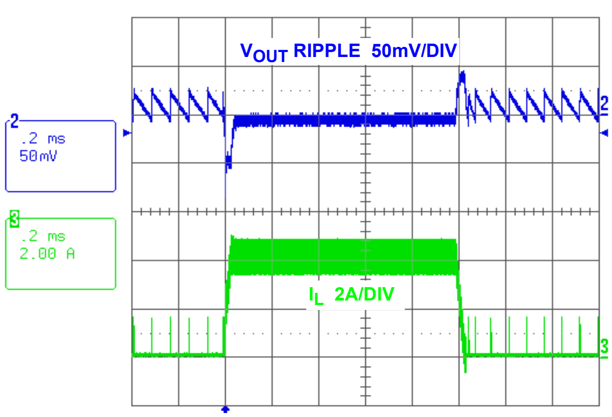


FIGURE 20. LOAD TRANSIENT (PFM)

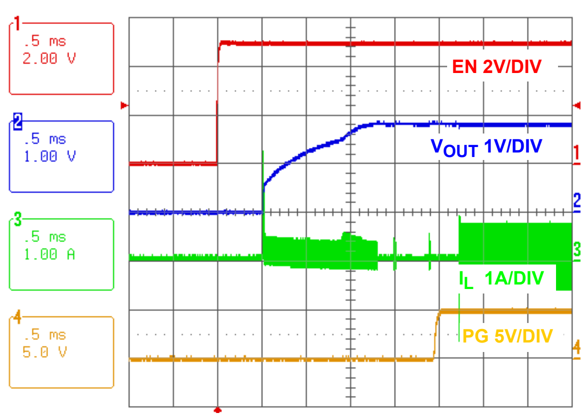


FIGURE 21. SOFT-START WITH NO LOAD (PWM)

Typical Operating Performance

Unless otherwise noted, operating conditions are: $T_A = +25°C$, $V_{VIN} = 5V$, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 4A. **(Continued)**

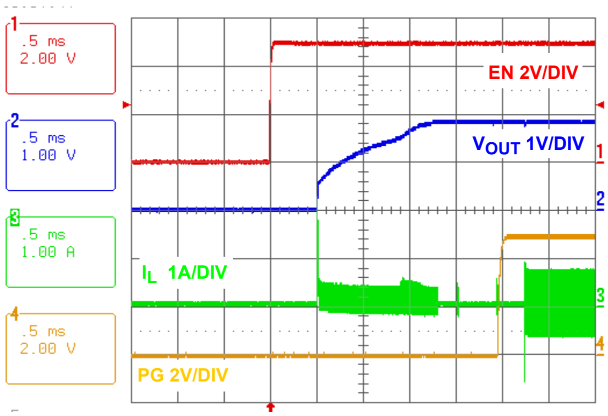


FIGURE 22. SOFT-START AT NO LOAD (PFM)

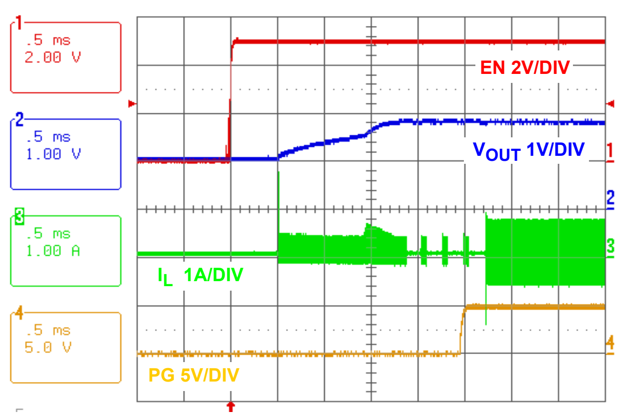


FIGURE 23. SOFT-START WITH PRE-BIASED 1V

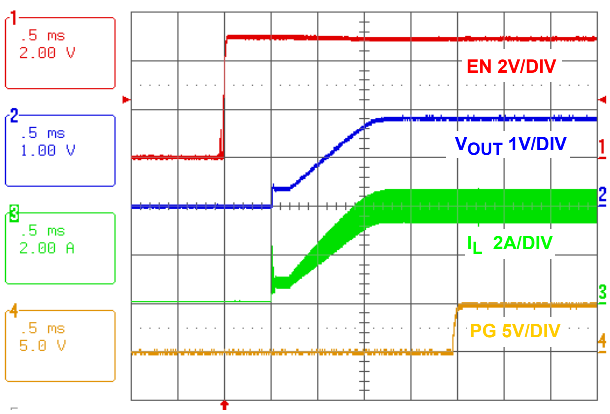


FIGURE 24. SOFT-START AT FULL LOAD

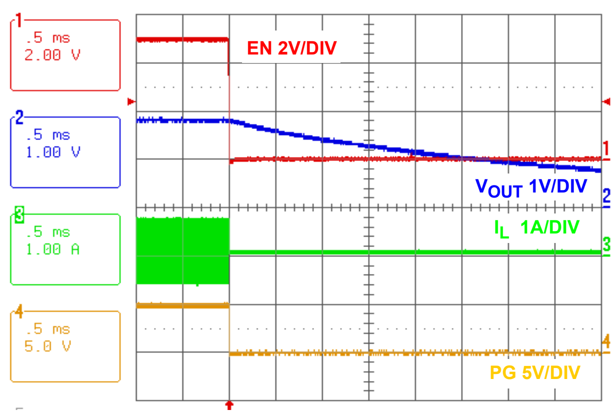


FIGURE 25. SOFT-DISCHARGE SHUTDOWN

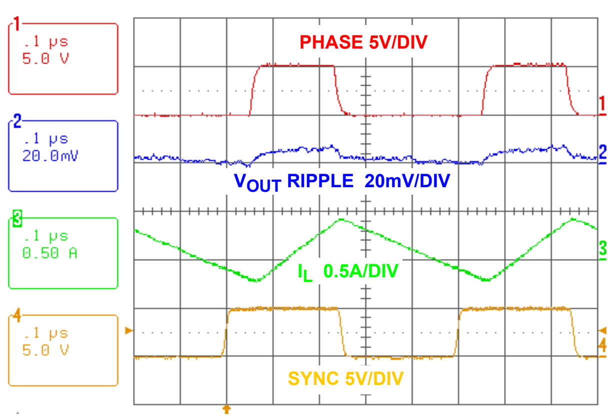


FIGURE 26. STEADY STATE OPERATION AT NO LOAD WITH FREQUENCY = 2MHz

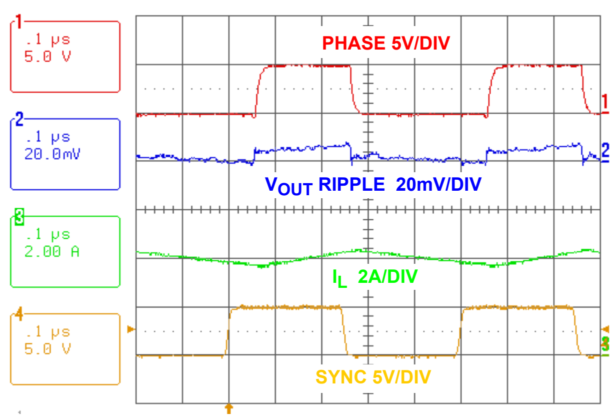


FIGURE 27. STEADY STATE OPERATION AT FULL LOAD WITH FREQUENCY = 2MHz

Typical Operating Performance

Unless otherwise noted, operating conditions are: $T_A = +25°C$, $V_{VIN} = 5V$, $EN = V_{IN}$, $SYNC = V_{IN}$, $L = 1.0µH$, $C_1 = 22µF$, $C_2 = 2 \times 22µF$, $I_{OUT} = 0A$ to $4A$. **(Continued)**

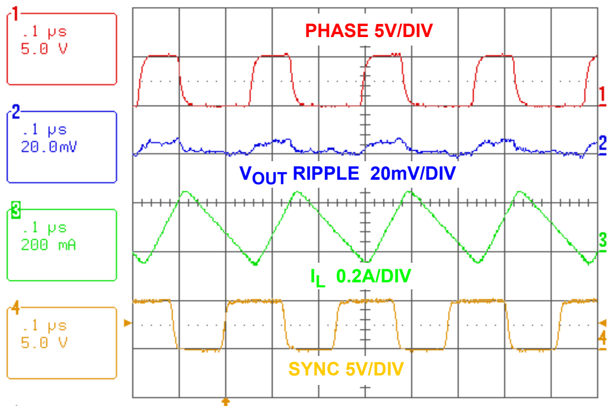


FIGURE 28. STEADY STATE OPERATION AT NO LOAD WITH FREQUENCY = 4MHz

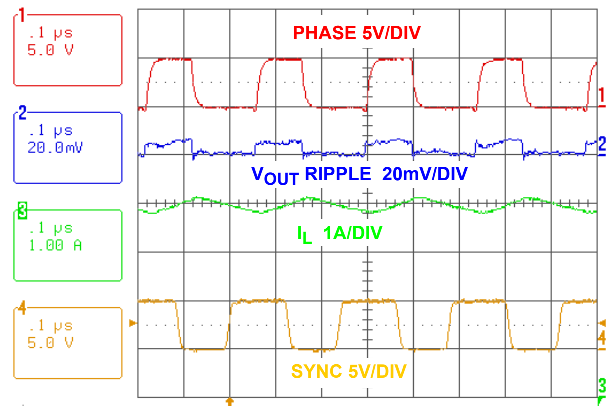


FIGURE 29. STEADY STATE OPERATION AT FULL LOAD (PWM) WITH FREQUENCY = 4MHz

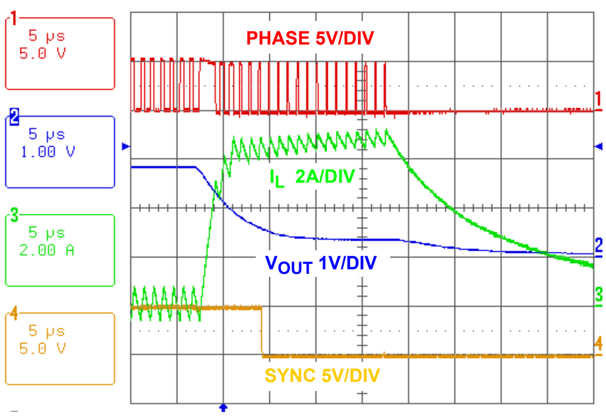


FIGURE 30. OUTPUT SHORT CIRCUIT

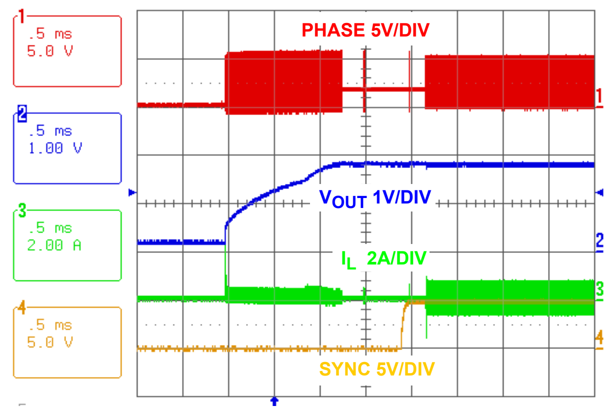


FIGURE 31. OUTPUT SHORT CIRCUIT RECOVERY

Typical Operating Performance for A Part

Unless otherwise noted, operating conditions are: $T_A = +25°C$, $V_{VIN} = 5V$, $EN = V_{IN}$, $SYNC = V_{IN}$, $L = 1.0µH$, $C_1 = 22µF$, $C_2 = 2 \times 22µF$, $I_{OUT} = 0A$ to $4A$.

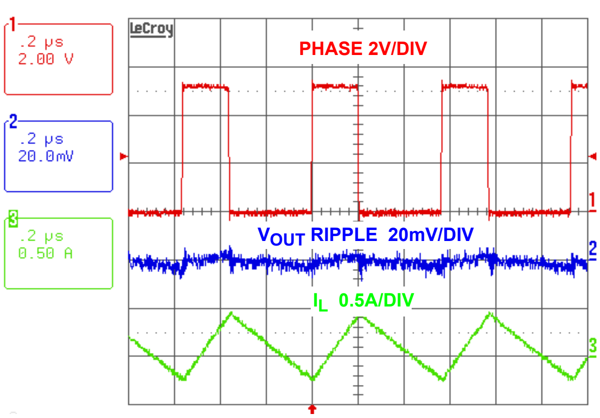


FIGURE 32. STEADY STATE OPERATION AT NO LOAD (PWM)

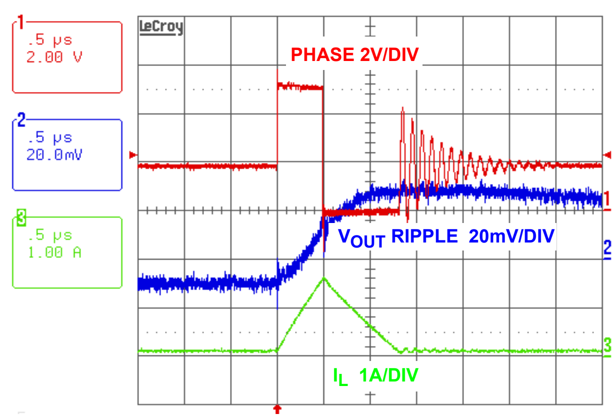


FIGURE 33. STEADY STATE OPERATION AT NO LOAD (PFM)

Typical Operating Performance for A Part

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 4A. **(Continued)**

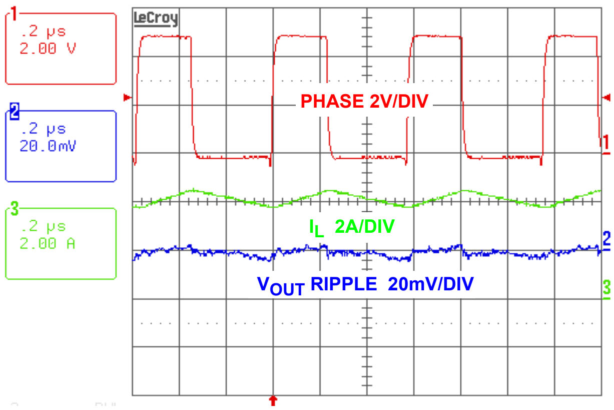


FIGURE 34. STEADY STATE OPERATION WITH FULL LOAD

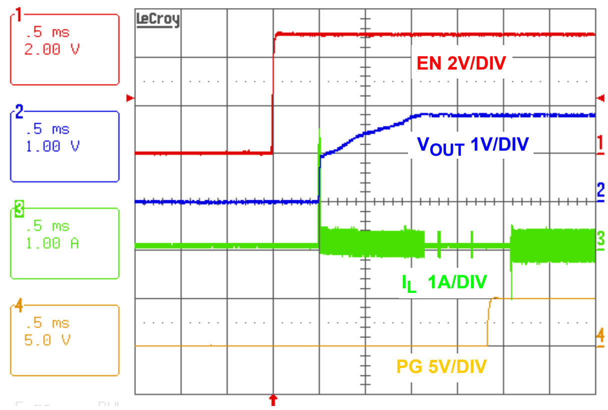


FIGURE 35. SOFT-START WITH NO LOAD (PWM)

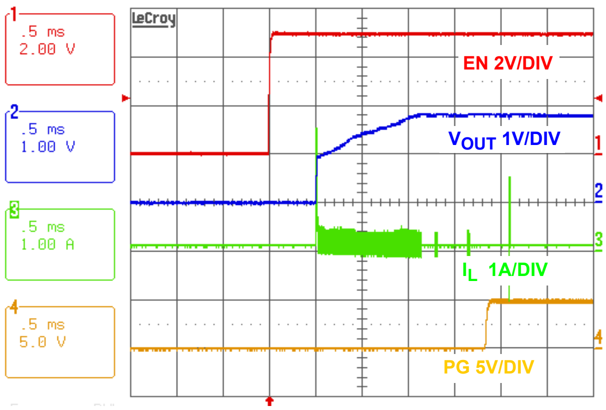


FIGURE 36. SOFT-START AT NO LOAD (PFM)

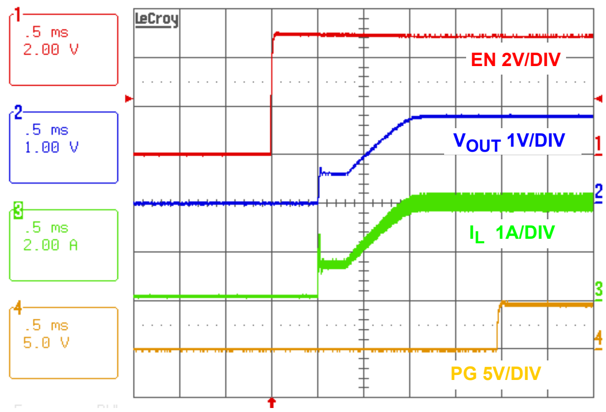


FIGURE 37. SOFT-START AT FULL LOAD

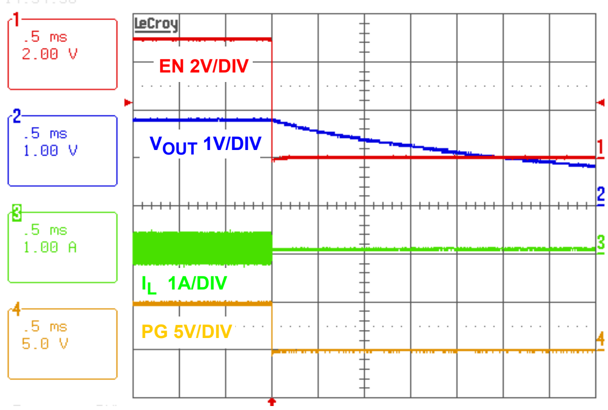


FIGURE 38. SOFT-DISCHARGE SHUTDOWN

Theory of Operation

The ISL8023, ISL8024 is a step-down switching regulator optimized for battery-powered handheld applications. The regulator operates at 1MHz fixed default switching frequency, when FS is connected to VIN, under heavy load conditions to allow smaller external inductors and capacitors to be used for minimal printed-circuit board (PCB) area. By connecting a resistor from FS to SGND, the operational frequency adjustable range is 500kHz to 4MHz. At light load, the regulator reduces the switching frequency, unless forced to the fixed frequency, to minimize the switching loss and to maximize the battery life. The quiescent current when the output is not loaded is typically only 50µA. The supply current is typically only 5µA when the regulator is shutdown.

PWM Control Scheme

Pulling the SYNC pin HI (>0.8V) forces the converter into PWM mode, regardless of output current. The ISL8023, ISL8024 employs the current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Figure 3 on page 5 shows the Functional Block Diagram. The current loop consists of the oscillator, the PWM comparator, current sensing circuit and the slope compensation for the current loop stability. The slope compensation is 440mV/Ts, which changes with frequency. The gain for the current sensing circuit is typically 200mV/A. The control reference for the current loops comes from the error amplifier's (EAMP) output.

The PWM operation is initialized by the clock from the oscillator. The P-Channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA and the slope compensation reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-FET and turn on the N-Channel MOSFET. The N-FET stays on until the end of the PWM cycle. Figure 39 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the current-sense amplifier's CSA output.

The output voltage is regulated by controlling the V_{EAMP} voltage to the current loop. The bandgap circuit outputs a 0.6V reference voltage to the voltage loop. The feedback signal comes from the VFB pin. The soft-start block only affects the operation during the start-up and will be discussed separately. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 55pF and 100kΩ RC network. The maximum EAMP voltage output is precisely clamped to 1.6V.

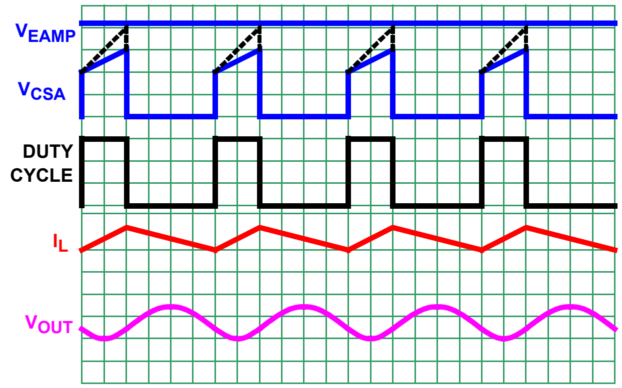


FIGURE 39. PWM OPERATION WAVEFORMS

SKIP Mode

Pulling the SYNC pin LO (<0.4V) forces the converter into PFM mode. The ISL8023, ISL8024 enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 40 illustrates the skip-mode operation. A zero-cross sensing circuit shown in Figure 3 on page 5 monitors the N-FET current for zero crossing. When 8 consecutive cycles of the inductor current crossing zero are detected, the regulator enters the skip mode. During the eight detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

Once the skip mode is entered, the pulse modulation starts being controlled by the SKIP comparator shown in Figure 3 on page 5. Each pulse cycle is still synchronized by the PWM clock. The P-FET is turned on at the clock's rising edge and turned off when the output is higher than 1.5% of the nominal regulation or when its current reaches the peak Skip current limit value. Then the inductor current is discharging to 0A and stays at zero. The internal clock is disabled. The output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-FET will be turned on again at the rising edge of the internal clock as it repeats the previous operations.

The regulator resumes normal PWM mode operation when the output voltage drops 1.5% below the nominal voltage.

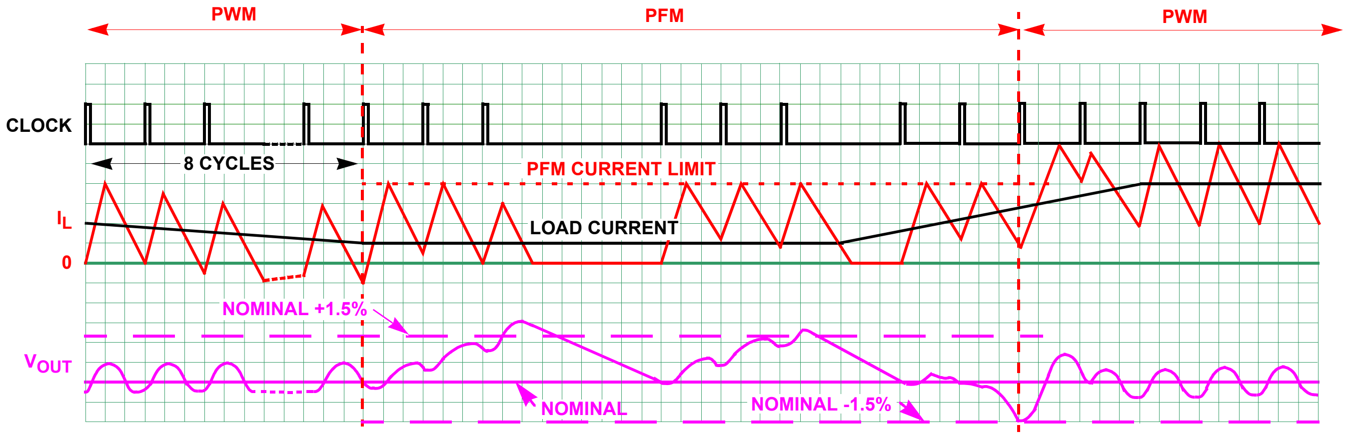


FIGURE 40. SKIP MODE OPERATION WAVEFORMS

Frequency Adjust

The frequency of operation is fixed at 1MHz and internal compensation when FS is tied to VIN. Adjustable frequency range from 500kHz to 4MHz via simple resistor connecting FS to SGND according to Equation 1:

$$R_T[k\Omega] = \frac{220 \cdot 10^3}{f_{OSC}[kHz]} - 14 \quad \text{(EQ. 1)}$$

Overcurrent Protection

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in Figure 3. The current sensing circuit has a gain of 200mV/A, from the P-FET current to the CSA output. When the CSA output reaches the threshold, the OCP comparator is trippled to turn off the P-FET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFET.

Upon detection of an overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the overcurrent fault counter is set to 1. If, on the subsequent cycle, another overcurrent condition is detected, the OC fault counter will be incremented. If there are 17 sequential OC fault detections, the regulator will be shutdown under an overcurrent fault condition. An overcurrent fault condition will result in the regulator attempting to restart in a hiccup mode within the delay of eight soft-start periods. At the end of the eight soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away during the delay of eight soft-start periods, the output will resume back into regulation point after hiccup mode expires.

Negative Current Protection

Similar to the overcurrent, the negative current protection is realized by monitoring the current across the low-side N-FET, as shown in Figure 3 on page 5. When the valley point of the inductor current reaches -3A for 4 consecutive cycles, both P-FET and N-FET are off. The 100Ω in parallel to the N-FET will activate discharging the output into regulation. The control will begin to switch when output is within regulation. The regulator will be in PFM for 20µs before switching to PWM if necessary.

PG

PG is an open-drain output of a window comparator that continuously monitors the buck regulator output voltage. PG is actively held low when EN is low and during the buck regulator soft-start period. After 1ms delay of the soft-start period, PG becomes high impedance as long as the output voltage is within nominal regulation voltage set by VFB. When VFB drops 15% below or raises 0.8V above the nominal regulation voltage, the ISL8023, ISL8024 pulls PG low. Any fault condition forces PG low until the fault condition is cleared by attempts to soft-start. For logic level output voltages, connect an external pull-up resistor, R_1, between PG and VIN. A 100kΩ resistor works well in most applications.

UVLO

When the input voltage is below the undervoltage lock-out (UVLO) threshold, the regulator is disabled.

Soft Start-Up

The soft start-up reduces the in-rush current during the start-up. The soft-start block outputs a ramp reference to the input of the error amplifier. This voltage ramp limits the inductor current as well as the output voltage speed so that the output voltage rises in a controlled fashion. When VFB is less than 0.1V at the beginning of the soft-start, the switching frequency is reduced to 200kHz so that the output can start-up smoothly at light load condition. During soft-start, the IC operates in the SKIP mode to support pre-biased output condition.

Tie SS to SGND for internal soft-start approximately 1ms. Connect a capacitor from SS to SGND to adjust the soft-start time. This capacitor, along with an internal 1.6µA current source, sets the soft-start interval of the converter, T_{SS} as shown by Equation 2.

$$C_{SS}[\mu F] = 3.33 \cdot T_{SS}[s] \qquad \text{(EQ. 2)}$$

C_{SS} must be less than 33nF to insure proper soft-start reset after fault condition.

Enable

The enable (EN) input allows the user to control the turning on or off the regulator for purposes such as power-up sequencing. When the regulator is enabled, there is typically a 600µs delay for waking up the bandgap reference and then the soft-start-up begins.

Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs or the VIN UVLO is set, the outputs discharge to GND through an internal 100Ω switch.

Power MOSFETs

The power MOSFETs are optimized for best efficiency. The ON-resistance for the P-FET is typically 45mΩ and the ON-resistance for the N-FET is typically 19mΩ.

100% Duty Cycle

The ISL8023, ISL8024 features 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the ISL8023, ISL8024 can no longer maintain the regulation at the output, the regulator completely turns on the P-FET. The maximum dropout voltage under the 100% duty-cycle operation is the product of the load current and the ON-resistance of the P-FET.

Thermal Shut-Down

The ISL8023, ISL8024 has built-in thermal protection. When the internal temperature reaches +150°C, the regulator is completely shutdown. As the temperature drops to +125°C, the ISL8023, ISL8024 resumes operation by stepping through the soft-start.

Applications Information

Output Inductor and Capacitor Selection

To consider steady state and transient operations, ISL8023, ISL8024 typically uses a 1.0µH output inductor. The higher or lower inductor value can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V application, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased. It is recommended to set the ripple inductor current approximately 30% of the maximum output current for optimized performance. The inductor ripple current can be expressed as shown in Equation 3:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_S} \qquad \text{(EQ. 3)}$$

The inductor's saturation current rating needs to be at least larger than the peak current. The ISL8023, ISL8024 protects the typical peak current 4.8A/6.5A. The saturation current needs be over 7A for maximum output current application.

ISL8023, ISL8024 uses internal compensation network and the output capacitor value is dependent on the output voltage. The ceramic capacitor is recommended to be X5R or X7R. The recommended X5R or X7R minimum output capacitor values are shown in Table 1.

In Table 1, the minimum output capacitor value is given for the different output voltage to make sure that the whole converter system is stable. Additional output capacitance should be added for better performances in applications where high load transient or low output ripple is required. It is recommended to check the system level performance along with the simulation model.

Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider that is used to scale the output voltage relative to the internal reference voltage and feed it back to the inverting input of the error amplifier. Refer to Figure 2.

The output voltage programming resistor, R_2, will depend on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor is typically between 10kΩ and 100kΩ, as shown in Equation 4.

$$R_2 = R_3\left(\frac{V_O}{VFB} - 1\right) \qquad \text{(EQ. 4)}$$

If the output voltage desired is 0.6V, then R_3 is left unpopulated and R_2 is shorted. There is a leakage current from VIN to PHASE. It is recommended to preload the output with 10µA minimum. For better performance, add 15pF in parallel with R_2 (100kΩ). Check loop analysis before use in application.

Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current flowing back to the battery rail. At least two 22µF X5R or X7R ceramic capacitors are a good starting point for the input capacitor selection.

Loop Compensation Design

When there is an external resistor connected from FS to SGND, the COMP pin is active for external loop compensation. The ISL8023, ISL8024 uses constant frequency peak current mode control architecture to achieve fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant, and the system becomes single order system. It is much easier to design a type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has inherent input voltage feed-forward function to achieve good line regulation. Figure 41 shows the small signal model of the synchronous buck regulator.

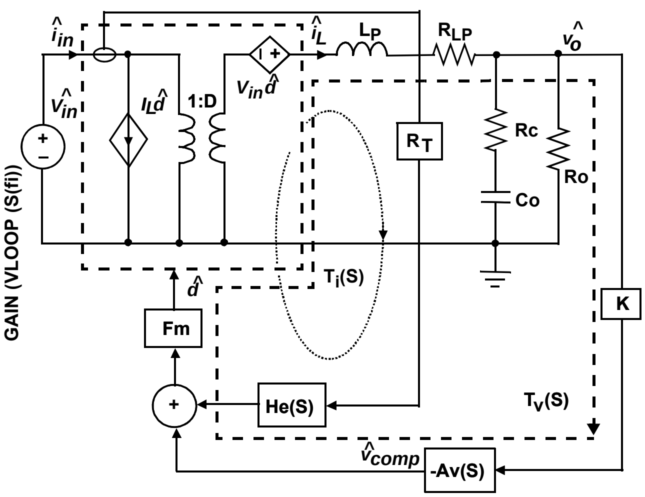


FIGURE 41. SMALL SIGNAL MODEL OF SYNCHRONOUS BUCK REGULATOR

PWM Comparator Gain F_m:

The PWM comparator gain F_m for peak current mode control is given by Equation 5:

$$F_m = \frac{\hat{d}}{\hat{v}_{comp}} = \frac{1}{(S_e + S_n)T_s} \qquad \text{(EQ. 5)}$$

Where S_e is the slew rate of the slope compensation and S_n is given by Equation 6:

$$S_n = R_t\frac{V_{in} - V_o}{L_P} \qquad \text{(EQ. 6)}$$

where R_t is trans-resistance, which is the gain of the current amplifier.

CURRENT SAMPLING TRANSFER FUNCTION $H_e(S)$:

In current loop, the current signal is sampled every switching cycle. It has the following transfer function in Equation 7:

$$H_e(S) = \frac{S^2}{\omega_n^2} + \frac{S}{\omega_n Q_n} + 1 \qquad \text{(EQ. 7)}$$

where Q_n and ω_n are given by $Q_n = -\frac{2}{\pi}$, $\omega_n = \pi f_s$

Power Stage Transfer Functions

Transfer function $F_1(S)$ from control to output voltage is:

$$F_1(S) = \frac{\hat{v}_o}{\hat{d}} = V_{in}\frac{1 + \frac{S}{\omega_{esr}}}{\frac{S^2}{\omega_o^2} + \frac{S}{\omega_o Q_p} + 1} \qquad \text{(EQ. 8)}$$

Where $\omega_{esr} = \frac{1}{R_c C_o}, Q_p \approx R_o\sqrt{\frac{C_o}{L_P}}, \omega_o = \frac{1}{\sqrt{L_P C_o}}$

Transfer function $F_2(S)$ from control to inductor current is given by Equation 9:

$$F_2(S) = \frac{\hat{I}_o}{\hat{d}} = \frac{V_{in}}{R_o + R_{LP}} \frac{1 + \frac{S}{\omega_z}}{\frac{S^2}{\omega_o^2} + \frac{S}{\omega_o Q_p} + 1} \qquad \text{(EQ. 9)}$$

where $\omega_z = \frac{1}{R_o C_o}$.

Current loop gain $T_i(S)$ is expressed as Equation 10:

$$T_i(S) = R_t F_m F_2(S) H_e(S) \qquad \text{(EQ. 10)}$$

The voltage loop gain with open current loop is Equation 11:

$$T_v(S) = K F_m F_1(S) A_v(S) \qquad \text{(EQ. 11)}$$

The Voltage loop gain with current loop closed is given by Equation 12:

$$L_v(S) = \frac{T_v(S)}{1 + T_i(S)} \qquad \text{(EQ. 12)}$$

Where $K = \frac{V_{FB}}{V_o}$, V_{FB} is the feedback voltage of the voltage error amplifier. If $T_i(S)>>1$, then Equation 12 can be simplified as Equation 13:

$$L_v(S) = \frac{V_{FB}}{V_o}\frac{R_o + R_{LP}}{R_t}\frac{1 + \frac{S}{\omega_{esr}}}{1 + \frac{S}{\omega_p}}\frac{A_v(S)}{H_e(S)}, \omega_p \approx \frac{1}{R_o C_o} \qquad \text{(EQ. 13)}$$

Equation 13 shows that the system is a single order system, which has a single pole located at ω_p before the half switching frequency. Therefore, a simple type II compensator can be easily used to stabilize the system.

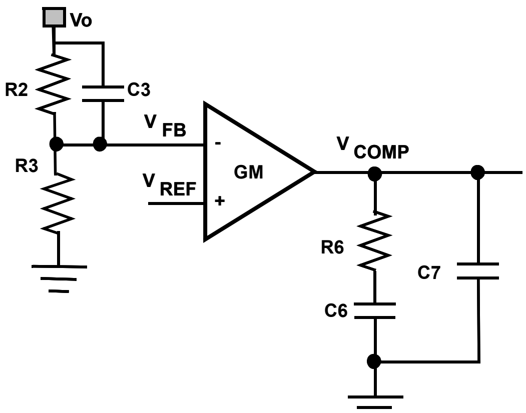


FIGURE 42. TYPE II COMPENSATOR

Figure 42 shows the type II compensator and its transfer function is expressed as Equation 14:

$$A_V(S) = \frac{\hat{v}_{comp}}{\hat{v}_{FB}} = \frac{GM}{C_6 + C_7} \frac{\left(1 + \frac{S}{\omega_{cz1}}\right)\left(1 + \frac{S}{\omega_{cz2}}\right)}{S\left(1 + \frac{S}{\omega_{cp}}\right)} \quad \text{(EQ. 14)}$$

where,

$$\omega_{cz1} = \frac{1}{R_6 C_6}, \quad \omega_{cz2} = \frac{1}{R_2 C_3}, \omega_{cp} = \frac{C_6 + C_7}{R_6 C_6 C_7}$$

Compensator design goal:

High DC gain

Loop bandwidth f_c: $\left(\frac{1}{4} \text{to} \frac{1}{10}\right) f_s$

Gain margin: >10dB

Phase margin: 40°

The compensator design procedure is as follows:

Put compensator zero $\omega_{cz1} = (1\text{to}3)\frac{1}{R_o C_o}$

Put one compensator pole at zero frequency to achieve high DC gain, and put another compensator pole at either ESR zero frequency or half switching frequency, whichever is lower. An optional zero can boost the phase margin. ω_{CZ2} is a zero due to R_2 and C_3.

Put compensator zero $\omega_{cz2} = (5\text{to}8)\frac{1}{R_2 C_3}$

The loop gain $T_v(S)$ at crossover frequency of f_c has unity gain. Therefore, the compensator resistance R_6 is determined by Equation 15.

$$R_6 = \frac{2\pi f_c V_o C_o R_t}{GM \cdot V_{FB}} \quad \text{(EQ. 15)}$$

where GM is the sum of the trans-conductance, g_m, of the voltage error amplifier in each phase. Compensator capacitor C6 is then given by Equation 16.

$$C_6 = \frac{1}{R_6 \omega_{cz1}}, \; C_7 = \frac{1}{2\pi R_6 f_{esr}} \quad \text{(EQ. 16)}$$

Example: V_{IN} = 5V, V_o = 1.8V, I_o = 4A, f_s = 1MHz, C_o = 2X22µF/3mΩ, L = 1µH, GM = 150µs, R_t = 0.20V/A, V_{FB} = 0.6V, S_e = 440mV/µs, S_n = 6.4×10^{5}V/s, f_c = 100kHz, then compensator resistance R_6 = 100kΩ.

Put the compensator zero at 8kHz, and put the compensator pole at either half of switching frequency or ESR zero. We choose 500kHz here, then the compensator capacitors are:

C_6 = 220pF, C_7 = 3pF (There is approximately 3pF parasitic capacitance from V_{COMP} to GND; Therefore, C_7 optional).

Figure 43 shows the simulated voltage loop gain. It is shown that it has 90kHz loop bandwidth with 70° phase margin and 10dB gain margin.

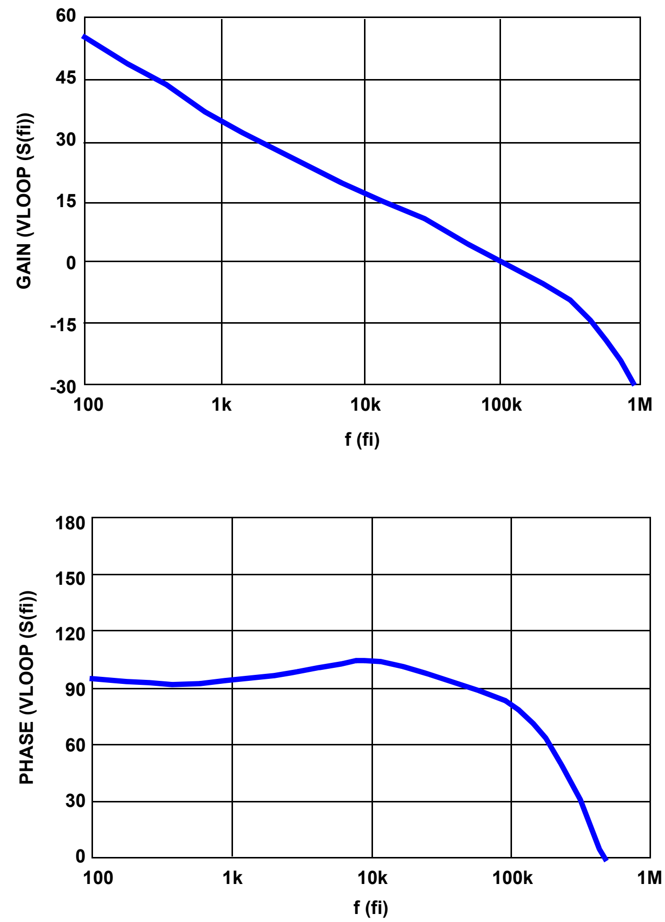


FIGURE 43. SIMULATED LOOP GAIN

PCB Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well. For ISL8023, ISL8024, the power loop is composed of the output inductor L's, the output capacitor C_{OUT}, the PHASE's pins, and the PGND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide. The switching node of the converter, the PHASE pins, and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The input capacitor should be placed as close as possible to the VIN pin. The ground of input and output capacitors should be connected as closely as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. It is recommended to add at least 5 vias ground connection within the pad for the best thermal relief.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
March 24, 2014	FN7812.3	Electrical spec table: "OUTPUT REGULATION" on page 6, under VFB Bias Current section, changed the typical value from 0.1µA to 0.01µA. Added ISL8023EVAL3Z, ISL8024EVAL3Z and ISL8023AEVAL3Z, ISL8024AEVAL3Z Evaluation Boards to Ordering Information table on page 4.
May 7, 2012	FN7812.2	Page 2: Updated with new silkscreen to show the correct placement of U1-Pin1. Page 3: Pin Descriptions , COMP, FB Changed the description from "Must connect COMP to SGND in internal compensation mode " to "Recommend connect COMP to SGND in internal compensation mode". Updated Figure 2 to show the COMP pin tied to GND Page 18: Put compensator zero ωcz2 = (5to8) R0C0" changed to "..... R2C3" Figure 43, Simulated Loop Gain: Added Y-axis title to the top graph: GAIN (VLOOP(S(fi)))
February 15, 2012	FN7812.1	In the "Absolute Maximum Ratings" on page 6, changed "VIN" from "-0.3V" to "-0.3V to 6.5V (DC) or 7V (20ms)"
February 1, 2012		Revised description, Features and Applications on page 1. Added Figure 2.
December 22, 2011	FN7812.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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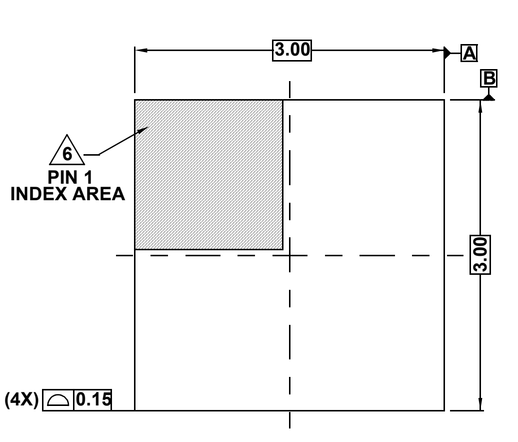
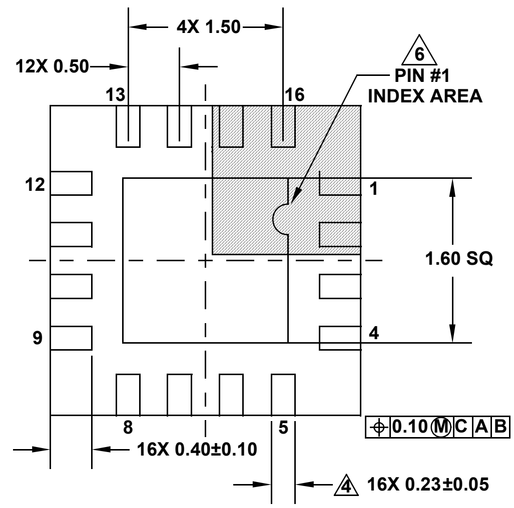
Package Outline Drawing

L16.3x3D

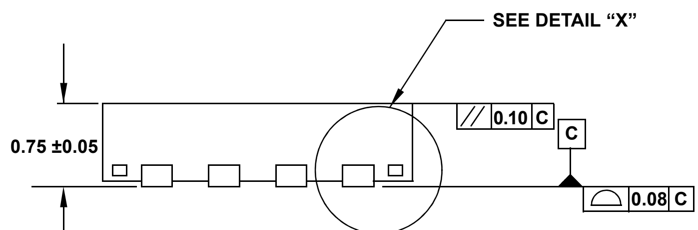
16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 3/10



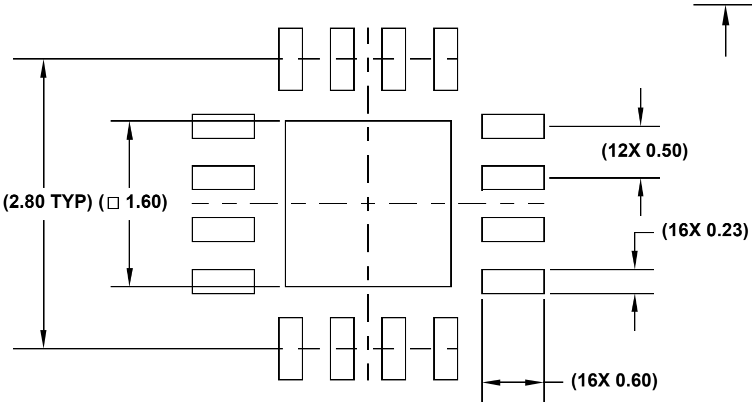
TOP VIEW



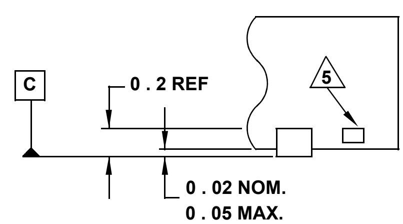
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220 WEED.