EZ6303QI Triple Output Module

2.2A DC-DC Buck Module with 2 x 300mA LDOs

DESCRIPTION

The EZ6303QI is a triple output PowerSoC with one buck and two low drop-out (LDO) regulators. It has three separated inputs and outputs. The DC-DC buck can support up to 2.2A of continuous output current while the other two outputs are separated 300mA LDOs.

The EZ6303QI employs Intel Enpirion's lateral MOSFET technology for monolithic integration and very low switching loss. The DC-DC switches at 2.5MHz in fixed PWM operation to eliminate the low frequency noise that is created by pulse frequency modulation operating modes. The MOSFET ratios are optimized to offer high conversion efficiency for lower VOUT settings.

The Intel Enpirion power solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of vendors required for the complete power solution helps to enable an overall system cost savings.

All Enpirion products are ROHS compliant and lead-free manufacturing environment compatible.

FEATURES

- Integrated 2.2A Buck Module with 2x300mA LDO
- Tiny 7mm x 4mm x 1.85mm QFN Package
- High Efficiency Buck (Up to 96 %)
- Optimized Total Solution Size (120 mm^2)
- Input Voltage Range
  - Buck (2.7V to 3.6V)
  - LDO (1.6V to 3.6V)
- Output Voltage Range
  - Buck (0.6V to 3.0V)
  - LDO (0.9V to 3.3V)
- Independent Input and Output Terminals
- Independent Output Enables and Power OK Flags
- Programmable Soft-Start (buck)
- Over-Current, Short Circuit, Under-Voltage, Thermal and Pre-Bias Protections
- Pin Compatible with EZ6301QI
- RoHS Compliant, MSL Level 3, 260 °C Reflow

APPLICATIONS

- Intel FPGAs (MAX, ARRIA, CYCLONE, STRATIX)
- All SERDES and IO Supplies Requiring Low Noise
- Low Power/Space Constraint Applications
- Applications Needing High Reliability

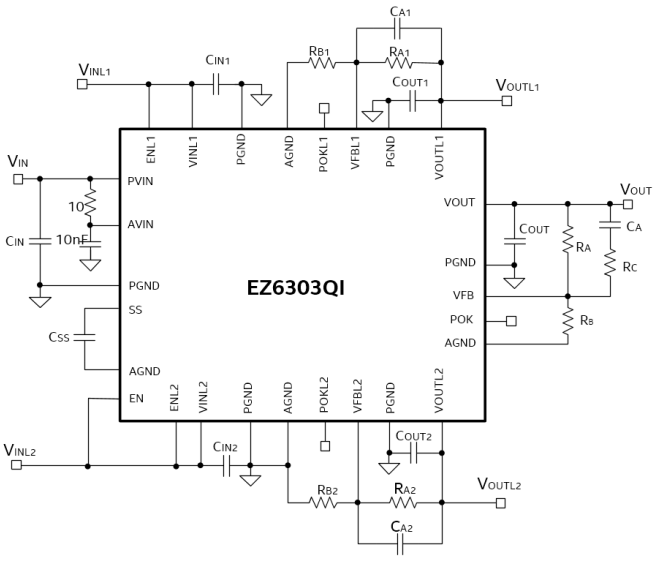


Figure 1: Simplified Applications Circuit

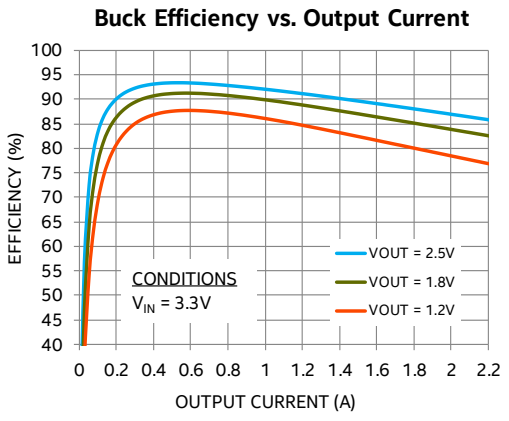


Figure 2: Efficiency at V_{IN} = 3.3V

ORDERING INFORMATION

Part Number	Package Markings	T_A Rating (°C)	Package Description
EZ6303QI	EZ6303QI	-40 to +85	40-pin (4mm x 7mm x 1.85mm) QFN
EVB-EZ6303QI	EZ6303QI	QFN Evaluation Board	

Packing and Marking Information: https://www.intel.com/support/quality-and-reliability/packing.html

PIN FUNCTIONS

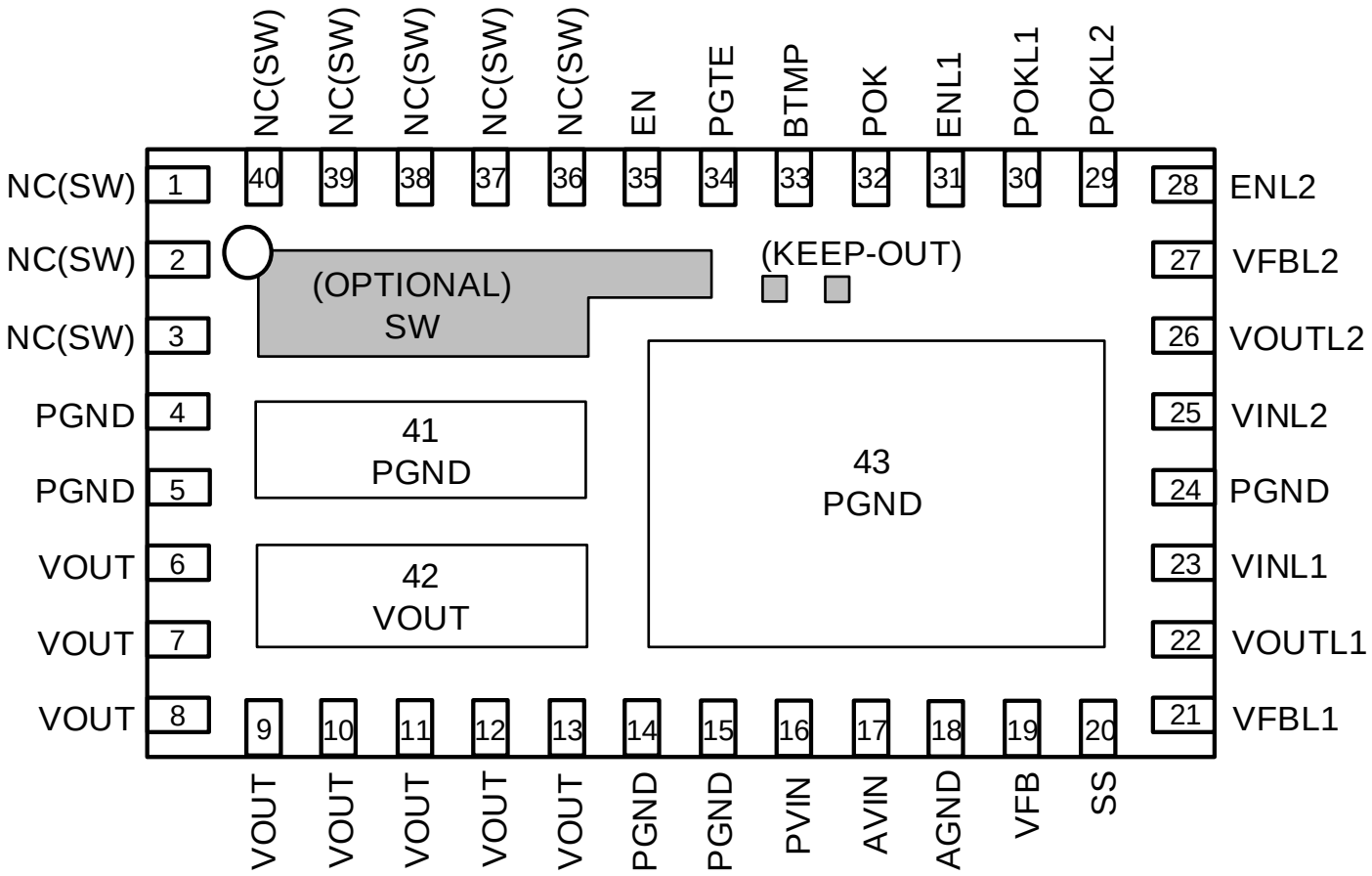


Figure 3: Pin Diagram (Top View)

NOTE A: Optional pads do not need to be electrically connected or soldered to the PCB, but may be done for Board Level Reliability (BLR).

NOTE B: The dot on top left is pin 1 indicator on top of the device package.

NOTE C: Keep-Out are No Connect pads that should not to be electrically connected to each other or to any external signal, ground or voltage. They do not need to be soldered to the PCB.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1, 2, 3, 36-40	NC(SW)	-	No Connect. These pins are internally connected to the common switching node of the internal MOSFETs. They must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage.
4, 5, 14, 15, 24	PGND	Ground	Power ground. Noisy ground for the power stages.
6-13	VOUT	Power	Regulated switching converter output. VOUT needs to be decoupled towards PGND.
16	PVIN	Power	Input power supply. Connect to input power supply; needs to be decoupled to PGND.
17	AVIN	Power	Analog Input voltage. This pin has to be connected to PVIN through a 10Ω resistor and decoupled towards AGND.
18	AGND	Power	Analog ground. The quiet ground for the control circuits.
19	VFB	Analog	Feedback input pin for switching converter. The compensation network and resistor divide are connected to this pin. The output voltage regulation is based on the VFB node voltage equal to 0.6V.
20	SS	Analog	Soft start pin. A soft-start capacitor is connected between this pin and AGND. The value of the capacitor controls the soft-start slew rate for the DC-DC regulator.
21	VFBL1	Analog	LDO1 feedback pin. The compensation/divider network from the LDO output to ANGD, having the feedback node as mid point. The output voltage regulation is based on the VFBL1 node voltage equal to 0.9V.
22	VOUTL1	Power	LDO1 regulated converter output. Connect to the load and place output filter capacitor(s) between these pins and PGND pins.
23	VINL1	Power	LDO1 input power supply. The power supply connected to this pin needs to be decoupled to PGND.
25	VINL2	Power	LDO2 input power supply. The power supply connected to this pin needs to be decoupled to PGND.
26	VOUTL2	Power	LDO2 regulated converter output. Connect to the load and place output filter capacitor(s) between these pins and PGND pins.
27	VFBL2	Analog	LDO2 feedback pin. The compensation/divider network from the LDO output to ANGD, having the feedback node as mid point. The output voltage regulation is based on the VFBL2 node voltage equal to 0.9V.
28	ENL2	Analog	LDO2 input enable. Applying logic high enables the output and initiates soft-start. Applying logic low disables the output.
29	POKL2	Digital	LDO2 Power OK. POKL2 is open drain logic used for power system state indication. POKL2 is logic high when VOUT is within ±10% of nominal.

PIN	NAME	TYPE	FUNCTION
30	POKL1	Digital	LDO1 Power OK. POKL1 is open drain logic used for power system state indication. POKL1 is logic high when VOUT is within ±10% of nominal.
31	ENL1	Analog	LDO1 input enable. Applying logic high enables the output and initiates a soft-start. Applying logic low disables the output.
32	POK	Digital	Switcher power OK. POK is open drain logic used for power system state indication. POK is logic high when VOUT is within ±10% of nominal.
33	BTMP	-	Bottom Plate connection for internal PGTE. This pin has to be soldered to the PCB but has to be left floating.
34	PGTE	-	PMOS Gate. This pin has to be soldered to the PCB but has to be left floating.
35	EN	Analog	Switcher Enable. Applying logic high enables the output and initiates a soft-start. Applying logic low disables the output.
41, 43	PGND	Ground	Not perimeter pins. Device thermal pads to be connected to the system GND plane for heat-sinking purposes. Covered in the Layout Recommendation section.
42	VOUT		Not perimeter pins. Device thermal pads to be connected to the system VOUT plane for heat-sinking purposes. Covered in the Layout Recommendation section.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
PVIN, AVIN, VINL1, VINL2, VOUTL1, VOUTL2		-0.3	7.0	V
EN, ENL1, ENL2, POK, POKL1, POKL2		-0.3	V_{IN}+0.3	V
VFB, SS		-0.3	2.7	V
PGTE		VIN – 2.7V	VIN	-
BTMP		0	2.7	V
NC(SW) Voltage DC	V_{SW}		7.0	V
NC(SW) Voltage Peak < 5ns	V_{SW_PEAK}	-2.0	10.5	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V
CDM (Charged Device Model)		±500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Switcher Input Voltage Range	V_{IN}	2.7	3.6	V
LDO Input Voltage Range	$V_{INL1,2}$	1.6	3.6	V
DC-DC Output Voltage Range	V_{OUT}	0.6	$V_{IN} - V_{DO}$ (1)	V
LDO Output Voltage Range	$V_{OUTL1/2}$	0.9	3.3	V
DC/DC Output Current Range	I_{OUT}		2.2	A
LDO1/2 Output Current Range	I_{OUT_LDO}		0.3	A
Operating Ambient Temperature Range	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	155	°C
Thermal Shutdown Hysteresis	T_{SDH}	20	°C
Thermal Resistance: Junction to Ambient (0 LFM) (2)	θ_{JA}	11.5	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	1	°C/W

(1) VDO (dropout voltage) is defined as (ILOAD x Droput Resistance). Please refer to Electrical Characteristics Table.

(2) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

NOTE: V_{IN} = 3.3V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25 °C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage (Switcher)	V_{IN}	PVIN = AVIN	2.7		3.6	V
Under Voltage Lock-Out – V_{IN} Rising	V_{UVLOR}	Voltage above which UVLO is not asserted	2	2.3	2.6	V
Under Voltage Lock-Out – V_{IN} Falling	V_{UVLOF}	Voltage below which UVLO is asserted	1.7	2.1	2.5	V
Under Voltage Lock-Out Hysteresis				250		mV
Buck Shut-Down Current	I_S	EN = ENL1 = ENL2 = 0V	500	680	900	µA
Operating Quiescent Current	I_Q	AVIN only			14	mA
No Load Quiescent Current	I_{VINQ}	PVIN and AVIN V_{OUT} = 1.2V		24		mA
DC-DC Initial VFB Pin [3] Voltage Accuracy	V_{FB}	No Load T_A = 25°C	0.597	0.6	0.603	V
DC-DC VFB Pin [3] Voltage (Line, Load and Temperature)	V_{FB}	2.7V ≤ VIN ≤ 3.6V 0A ≤ I_{LOAD} ≤ 2.2A -40°C ≤ T_A ≤ 85°C	0.591	0.6	0.609	V
Feedback Pin Input Leakage Current [4]	I_{FB}	VFB pin input leakage current	-10		10	nA
V_{OUT} Rise Time Range [4]	t_{RISE}	Capacitor programmable	0.65		6.5	ms
Soft Start Capacitance Range [4]	C_{SS_RANGE}		10		100	nF
Soft-Start Charging Current	I_{SS}			9		µA
Buck Dropout Resistance [4]	R_{DO}	Input to output resistance		170	255	mΩ
Drop-Out Voltage[4]	V_{DO}	V_{INMIN}-V_{OUT} at full load (2.2A)		374	561	mV
DC-DC Continuous Output Current	I_{OUT}		0		2.2	A

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Buck Over Current Trip Level	I_{OCP}	V_{IN} = 3.3V, V_{OUT} = 1.2V	2.4	2.9	3.4	A
Current Limit Retry Time	T_{CL_TRY}			6.5		ms
Precision Disable Threshold	$V_{DISABLE}$	EN pin logic going low	0.97	1.03	1.07	V
Precision Enable Threshold	V_{ENABLE}	EN pin logic going high	1.1	1.14	1.17	V
Enable Hysteresis	EN_{HYS}			110		mV
EN Pin Input Current	I_{EN}	EN pin has 159kΩ pull-down		45		µA
Switching Frequency (Free Running)	F_{SW}	Free running frequency of oscillator	2.25	2.5	2.75	MHz
POK High Range	POK_{RANGE}	Typical percentage range within V_{OUT} nominal when POK is asserted high		±10		%
POK Low Voltage	V_{POKL_B}	With 4mA current sink into POK			0.4	V
POK High Voltage	V_{POKH_B}	2.5V ≤ V_{IN} ≤ 3.6V			V_{IN}	V
POK Pin Leakage Current [(4)]	I_{POKH_B}	POK is high			1	µA
Linear Regulators						
Operating Input Voltage (LDO)	V_{IN}	PVIN = AVIN	1.6		3.6	V
LDO Shut-Down Supply Current	I_{SL}	EN = ENL1 = ENL2 = 0V		30	40	µA
LDO Quiescent Current (LDO1 or LDO2)	I_{QLDO}	No resistor divider on the output.		200	450	µA
LDO Dropout Resistance [(4)]	R_{DOL}	Input to output resistance		250		mΩ
LDO Drop-Out Voltage[(4)]	V_{LDO_DO}	V_{INMIN}-V_{OUT} at full load (300mA)		75		mV
LDO Over Current Trip Level	I_{OCPL}	V_{IN} = 3.3V, V_{OUT} = 1.2V	400	600	800	mA
LDO VFBL1,2 Pin Voltage (Line, Load and Temperature)	$V_{FBL1,2}$	1.6V ≤ VIN ≤ 3.6V 0A ≤ I_{LOAD} ≤ 0.3A	0.8865	0.9	0.9135	V

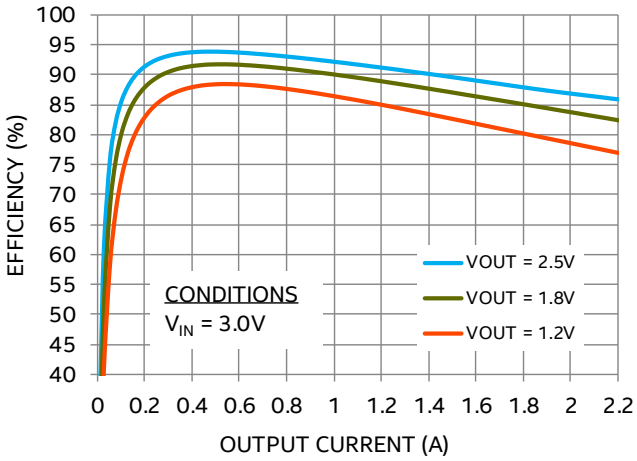
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LDO Precision Disable Threshold	$V_{DISABLEL}$	EN pin logic going low	0.97	1.03	1.07	V
LDO Precision Enable Threshold	$V_{ENABLEL}$	EN pin logic going high	1.1	1.14	1.17	V
LDO Enable Hysteresis	EN_{HYSL}			110		mV
LDO ENL1 or ENL2 Input Current	I_{ENL1}, I_{ENL2}	ENL1,2 pin has 159kΩ pull-down		45		µA
LDO POK High Range	$POKL_{RANGE}$	Typical percentage range within V_{OUT} nominal when POK is asserted high		±10		%
LDO POK Low Voltage	V_{POKL_L}	With 4mA current sink into POK			0.4	V
LDO POK High Voltage	V_{POKH_L}	2.5V ≤ V_{IN} ≤ 3.6V			V_{IN}	V
LDO POK Pin Leakage Current (4)	I_{POKH_L}	POK is high			1	µA
LDO PSRR(4)	PSRR	100Hz		48		dB
		10kHz		34		dB
		50kHz		20		dB

(3) The VFB pin is a sensitive node. Do not touch VFB while the device is in regulation.

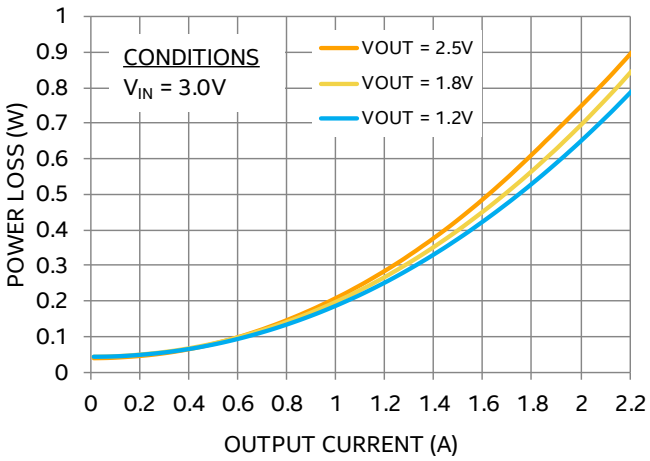
(4) Parameter not production tested but is guaranteed by design.

TYPICAL PERFORMANCE CURVES

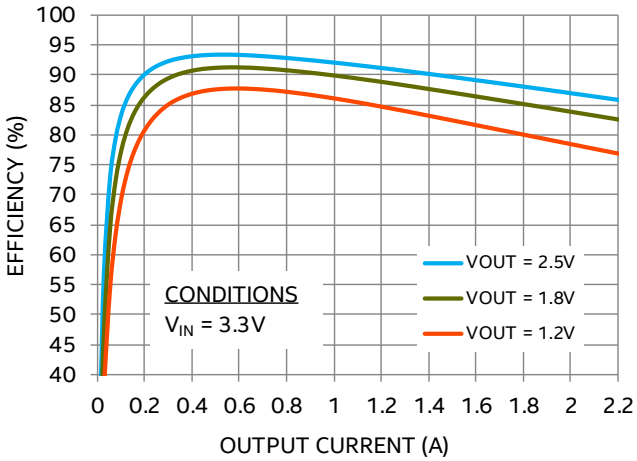
Buck Efficiency vs. Output Current



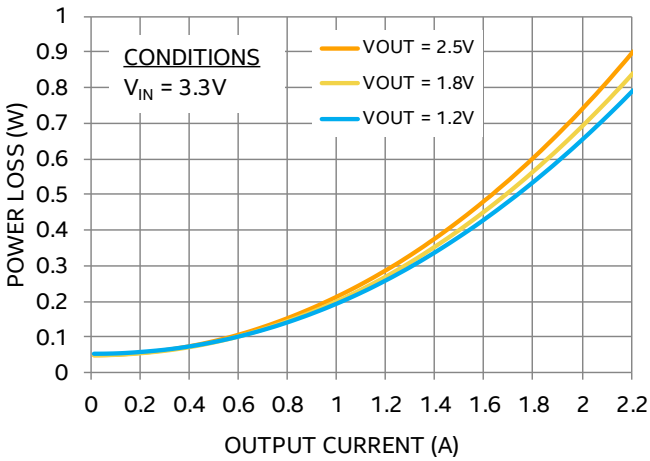
Buck Power Loss VIN = 3.0V



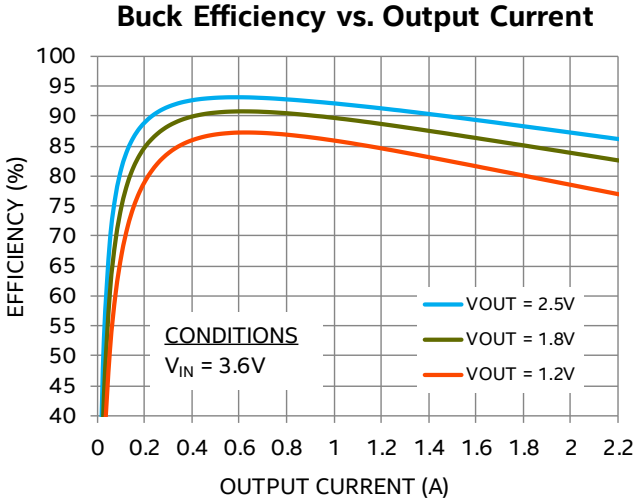
Buck Efficiency vs. Output Current



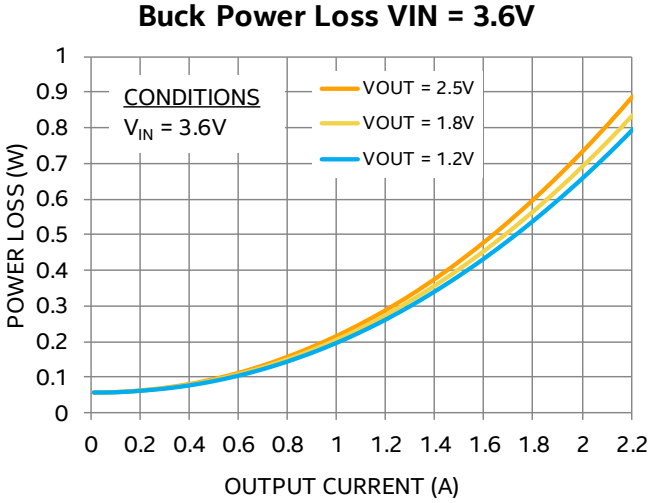
Buck Power Loss VIN = 3.3V



Buck Efficiency vs. Output Current

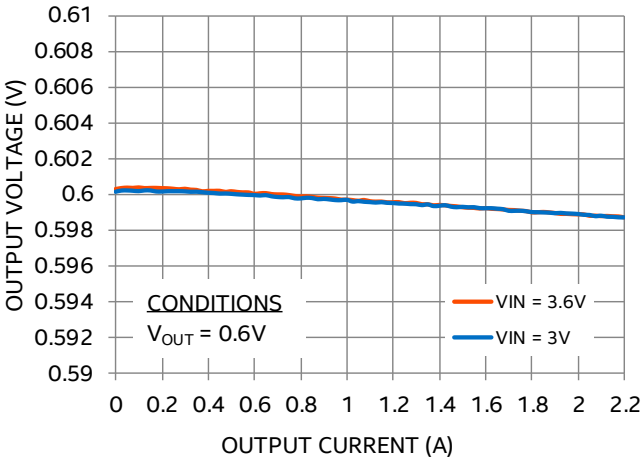


Buck Power Loss VIN = 3.6V

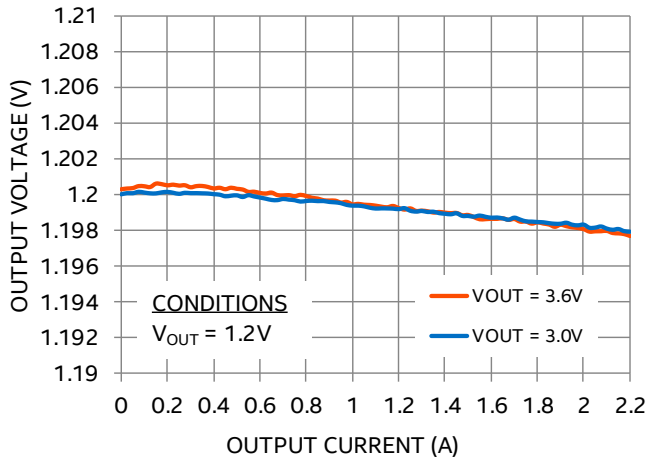


TYPICAL PERFORMANCE CURVES (CONTINUED)

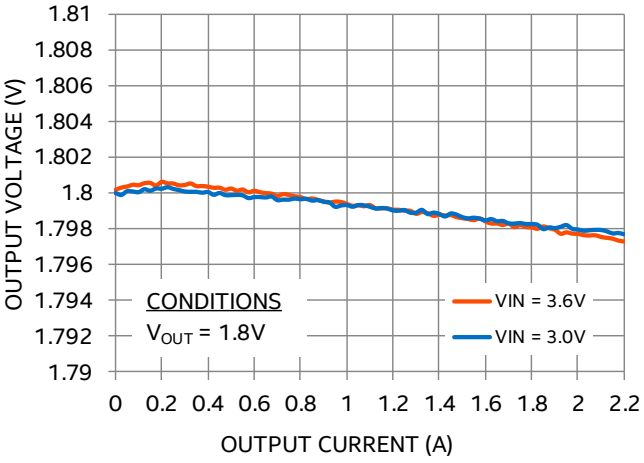
Buck VOUT vs. Output Current



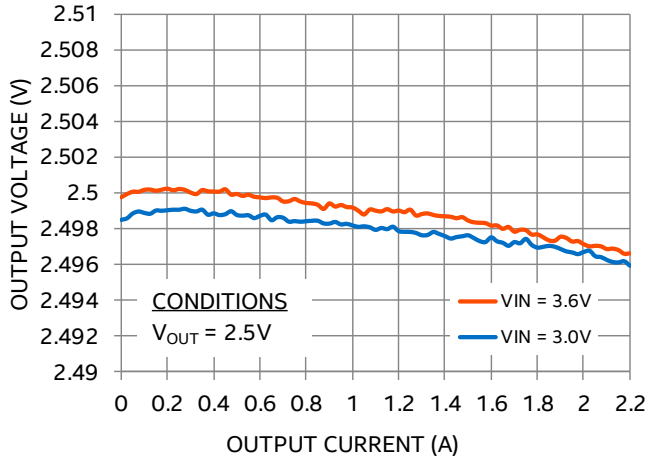
Buck VOUT vs. Output Current



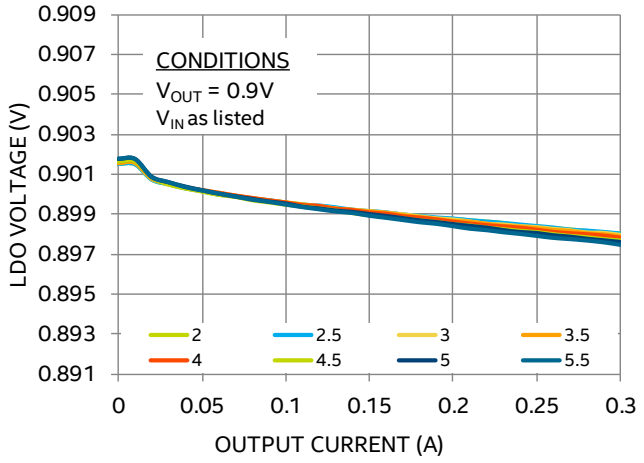
Buck VOUT vs. Output Current



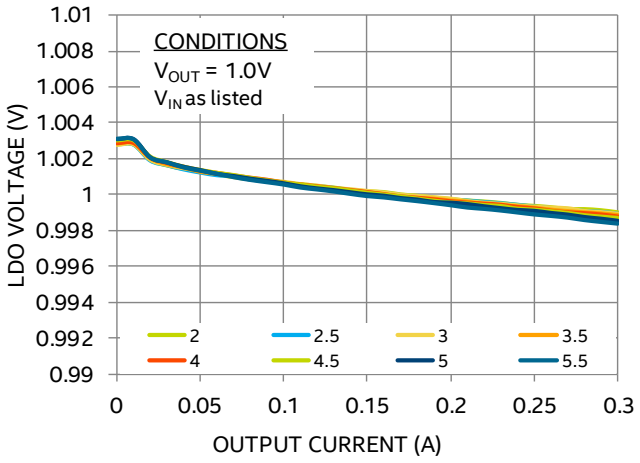
Buck VOUT vs. Output Current



LDO VOUT vs. Output Current

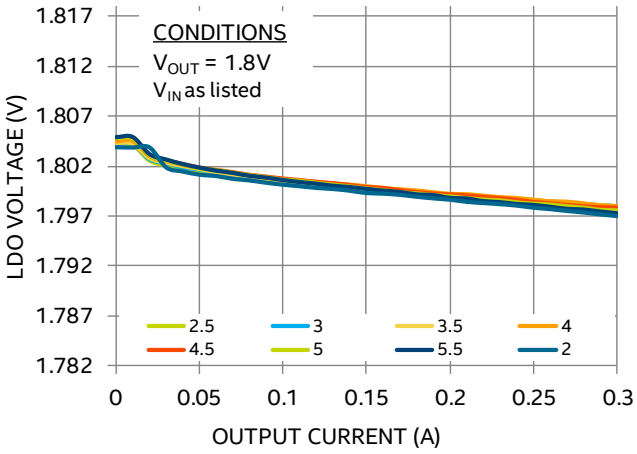


LDO VOUT vs. Output Current

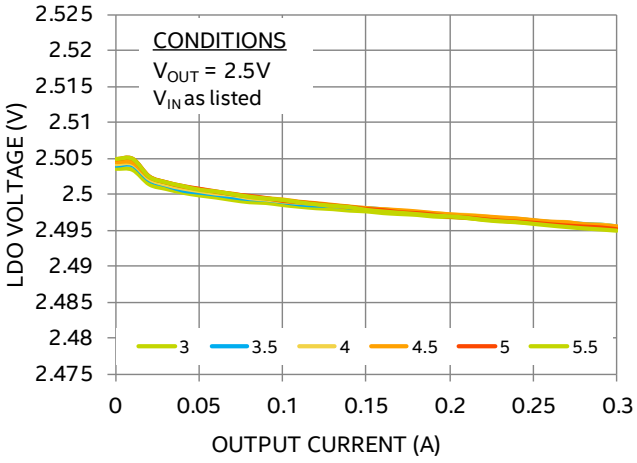


TYPICAL PERFORMANCE CURVES (CONTINUED)

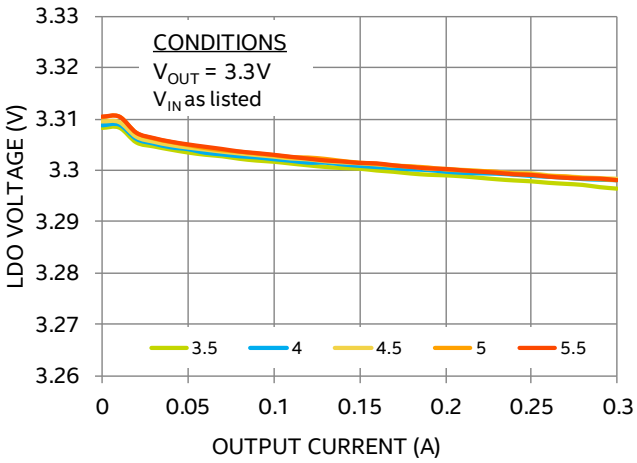
LDO VOUT vs. Output Current



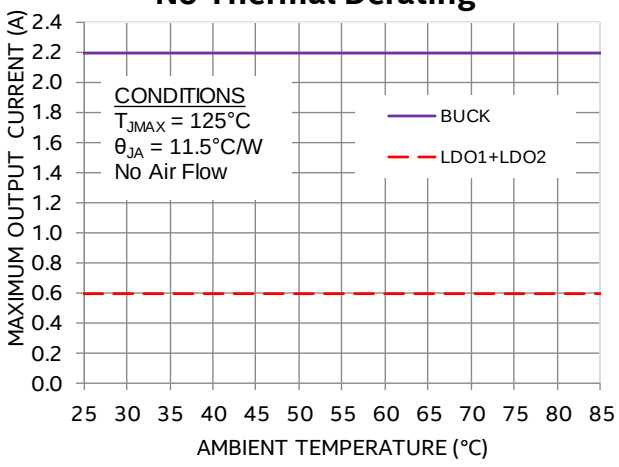
LDO VOUT vs. Output Current



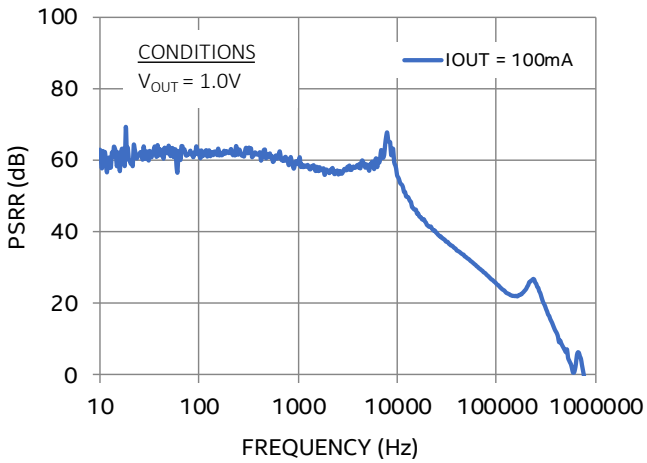
LDO VOUT vs. Output Current



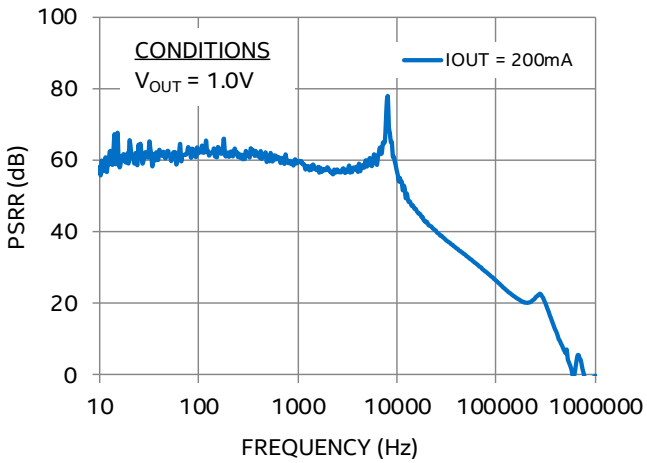
No Thermal Derating



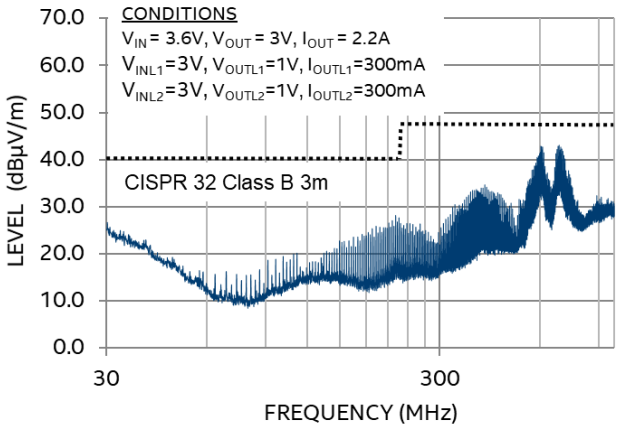
LDO PSRR VIN = 3.3V



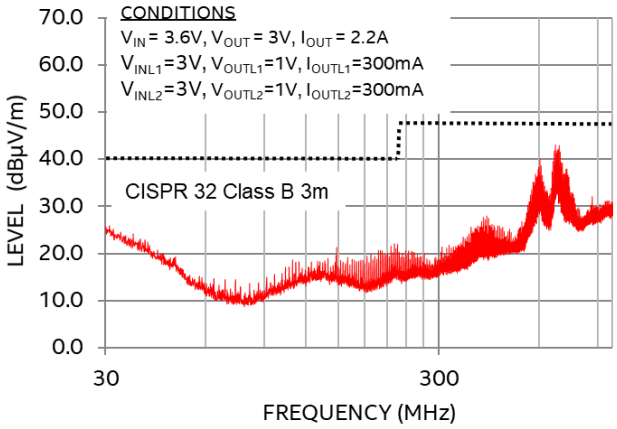
LDO PSRR VIN = 3.3V



EMI Performance (Horizontal scan)

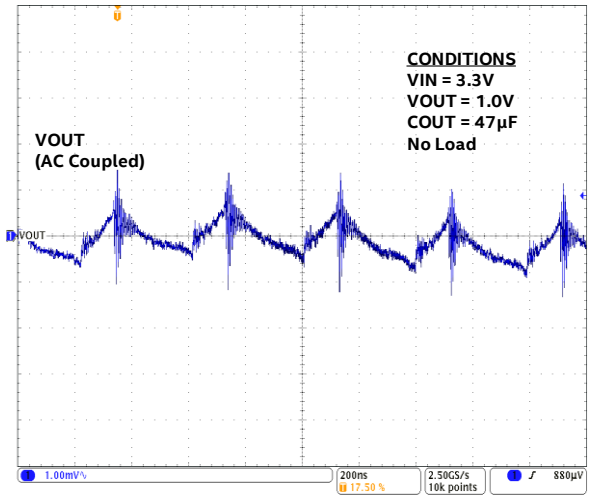


EMI Performance (Vertical scan)

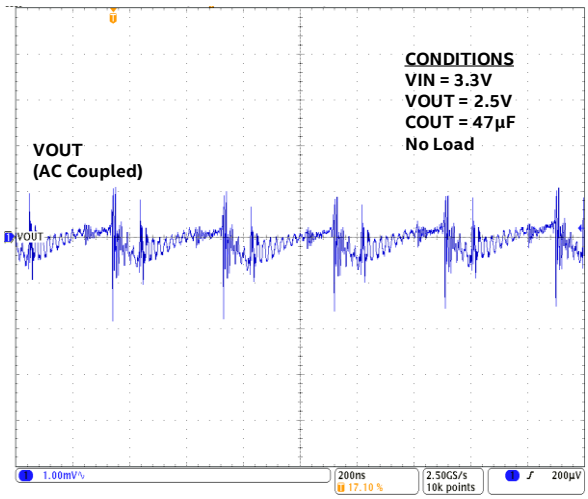


TYPICAL PERFORMANCE CHARACTERISTICS

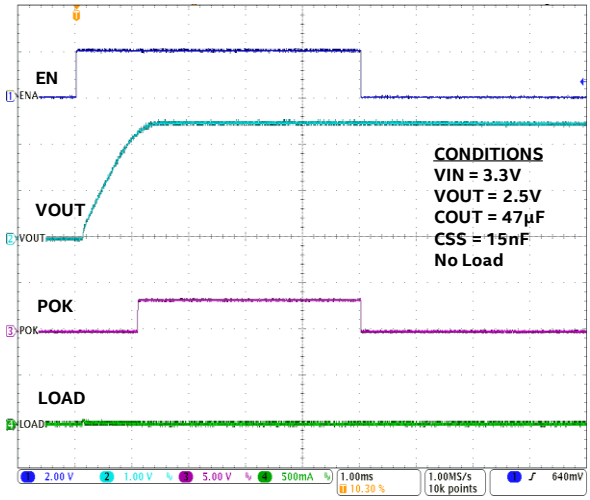
Buck Output Voltage Ripple



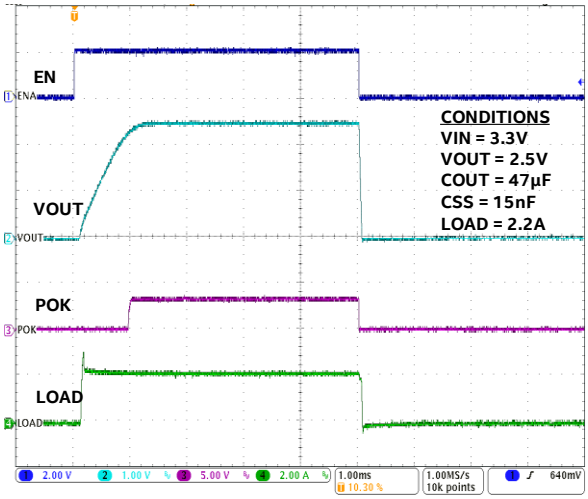
Buck Output Voltage Ripple



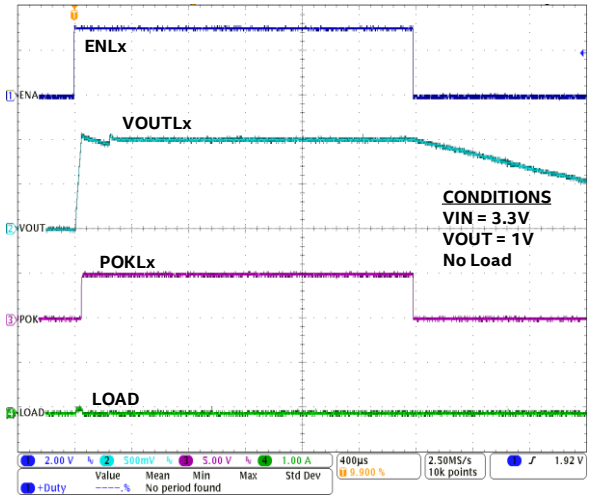
Buck Startup and Shutdown



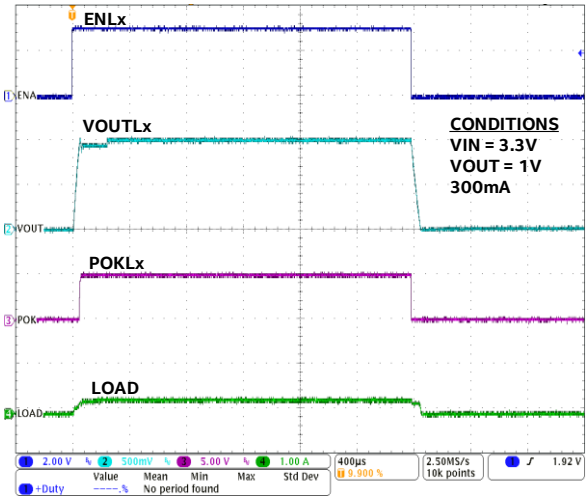
Buck Startup and Shutdown



LDO Startup and Shutdown

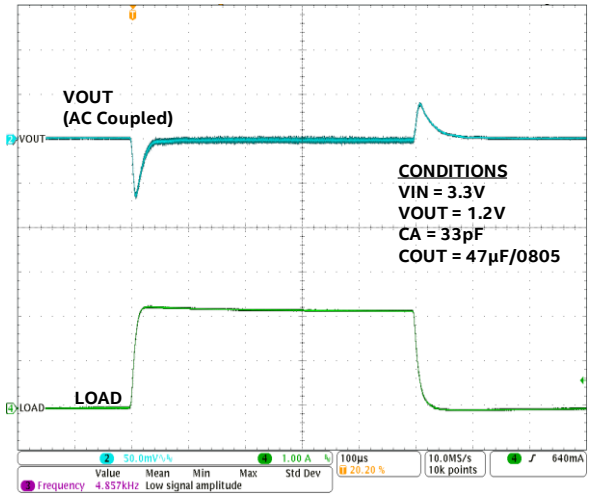


LDO Startup and Shutdown

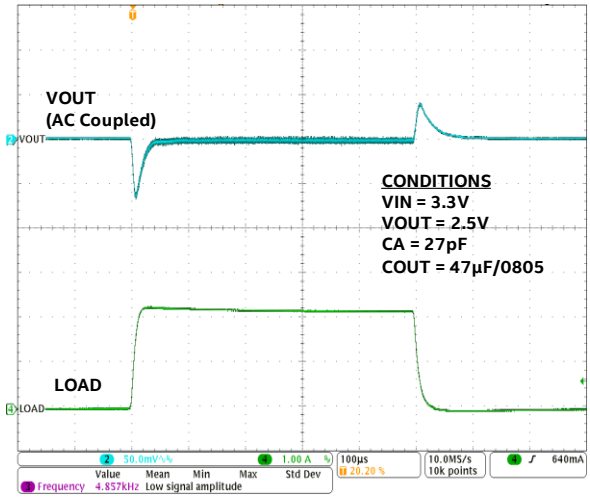


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

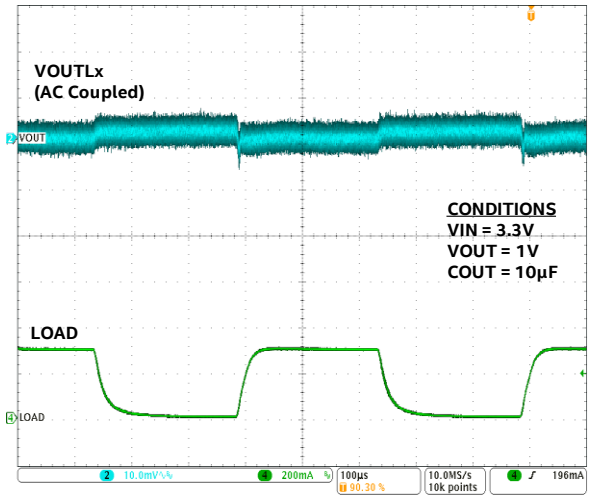
Buck Load Transient 0 to 2.2A



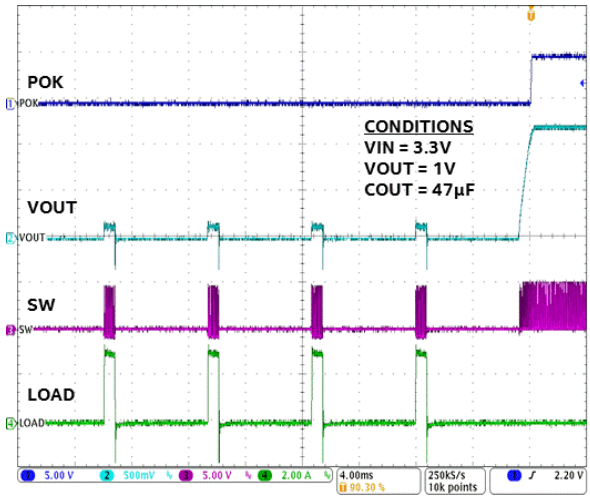
Buck Load Transient 0 to 2.2A



LDO Load Transient 0 to 300mA



Buck Short Circuit Recovery



FUNCTIONAL BLOCK DIAGRAM

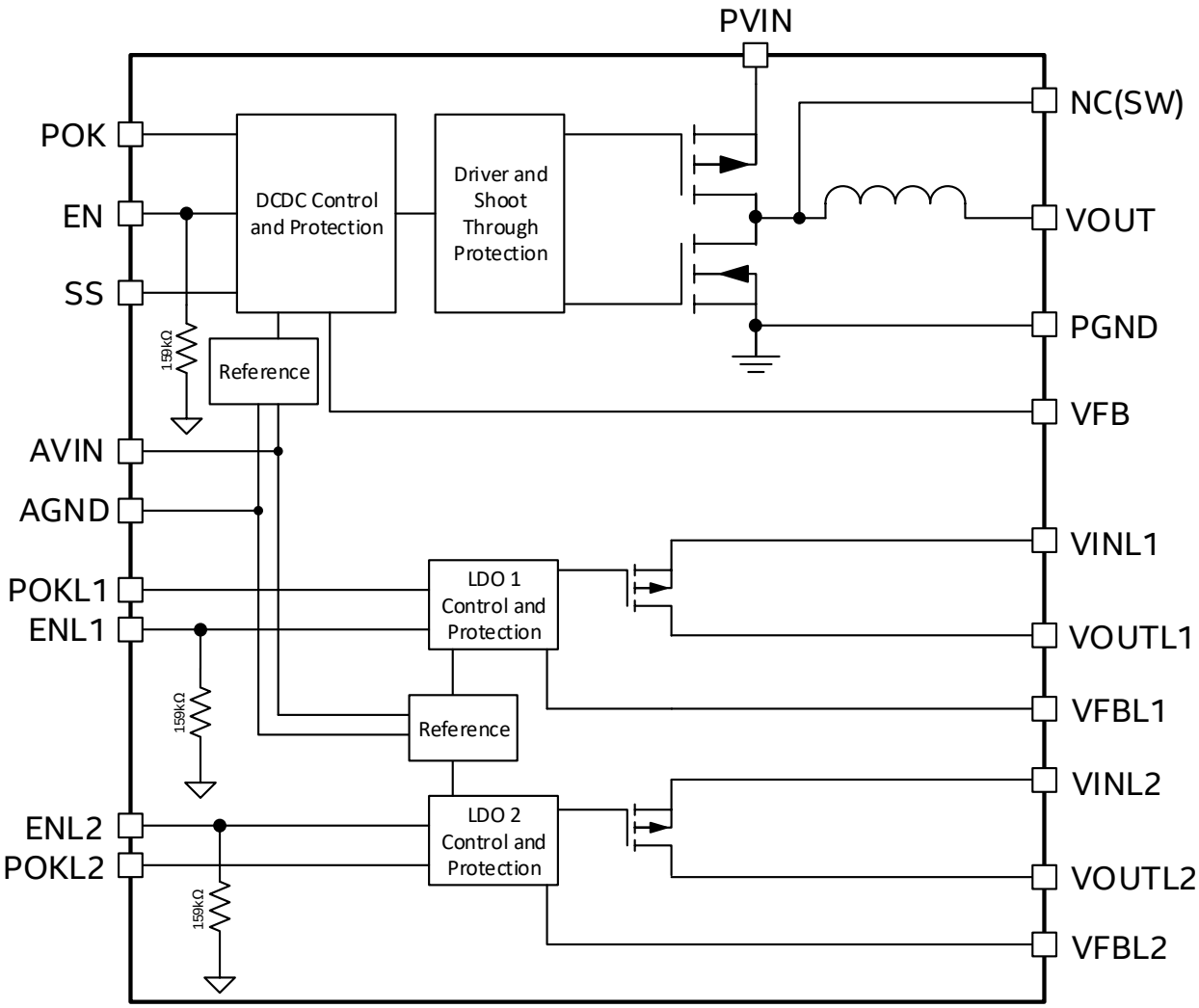


Figure 4: Functional Block Diagram

FUNCTIONAL DESCRIPTION

Synchronous Buck Converter

The EZ6303QI is a synchronous, programmable power supply with integrated power MOSFET switches, integrated inductor and two LDOs. The nominal input voltage range for the buck converter is 2.7V to 3.6V and 1.6V to 3.6V for the LDOs. The output voltage for all three rails can be programmed using external resistor divider networks. The buck converter uses a voltage-mode type III compensation network. Much of the compensation circuitry is internal to the device; however, a phase lead capacitor is required along with the output voltage feedback resistor divider to complete the type III compensation network. The device uses a low-noise PWM topology. Up to 2.2A of continuous output current can be drawn from this converter. The 2.5MHz switching frequency allows the use of small size input and output capacitors and enables wide loop bandwidth within a small foot print. The low thermal resistance of the package allows the LDOs continuous maximum current in the full temperature range.

The EZ6303QI architecture includes the following features.

Operational Features:

- Precision enable circuit with tight threshold range
- Soft-start circuit allowing controlled startup with adjustable soft-start capacitance for buck converter and built-in soft-start for LDOs
- Power good circuits on all rails indicating the output voltage is within ±10% of programmed value

Protection Features:

- Over-current protection with hiccup and reverse current protection for the buck converter
- Over-current protection with fold-back for the LDOs
- Thermal shutdown with hysteresis
- Under-voltage lockout circuit to disable switching until the input is adequate

Precision Enable Operation

The enable (EN, ENL1, ENL2) pins provide means to startup or to shutdown the device. When the enable pin is asserted high, the device will undergo a normal soft-start where the output will rise monotonically into regulation. Asserting a logic low on this pin will deactivate the device by turning off the internal power switches and the POK flag will also be pulled low. Precision voltage reference and comparator circuits are kept powered up even when the device is disabled. The precision enable circuit ensures the device will enable or disable within a tight voltage range for both high or low logic. This precision allows accurate sequencing for multiple power supplies. In order to ensure a known state, the enable pin should be pulled high or low while the device's input voltage is above UVLO. When input voltage decays slowly and the device is operating below the minimum operating voltage, switching chatter may occur due to insufficient voltage. In order to avoid chatter during power down, a resistor divider may be connected on the enable pin to power down the switching DC-DC regulator.

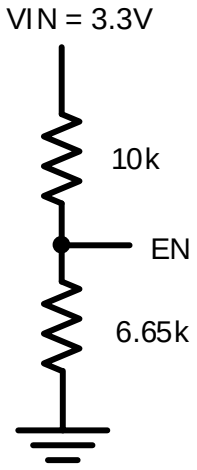


Figure 5: Sample Enable Resistor Divider Circuit

The resistor divider circuit in Figure 5 may be used to disable the regulator at around 2.6V, but be sure to have sufficient voltage for startup when choosing divider values. See the Electrical Characteristics Table for technical specifications for the enable pins for the switcher and LDOs.

Soft-Start Operation

DC-DC Buck:

The soft-start circuitry will reduce inrush current during startup as the regulator charges the output voltage up to nominal level gradually. The DC-DC buck output rise time is controlled by the soft-start capacitor, which is placed between the SS pin and the AGND pin. When the part is enabled, the soft-start (SS) current generator charges the SS capacitor in a linear manner. Once the voltage on the SS capacitor reaches 0.6V, the controller selects the intenral bandgap voltage as the reference. The voltage across the SS capacitor will continue ramping up until it reaches around 1.27V. The rise time is defined as the time needed by the output voltage to go from zero to the programmed value. The rise time (t_{RISE}) is given by the following equation:

$$t_{RISE}\ [ms] = C_{ss}\ [nF] \times 0.065$$

With a 10nF soft-start capacitance on the SS pin, the soft-start rise time will be set to 0.65ms. The recommended range for the value of the SS capacitor is between 10nF and 100nF. Note that excessive bulk capacitance on the output can cause an over current event on startup if the soft-start time is too low. Refer to the Compensation and Transient Response section for details on proper bulk capacitance usage.

LDO:

The LDOs have fixed internal soft-start. When enabled, the output will rise into regulation in a controlled manner.

POK Operation

The POK signals (POK, POKL1, POKL2) are open drain signals to indicate if the output voltage is within the specified range. They each require an external pull-up (10k-100k) to VIN. POK is asserted high when the rising output voltage exceeds 90% of the programmed output voltage. If the nominal output voltage falls outside the set range (typically 90% to 110% of nominal) the POK signal will be asserted low by an internal 4mA pull-down transistor.

Over-Current Protection

DC-DC Buck:

The current limit function is achieved by sensing the current flowing through the High Side Switch. When the sensed current exceeds the over current trip point, both power FETs are turned off for the remainder of the switching cycle. If the over-current condition is removed, the over-current protection circuit will enable normal PWM operation. In the event the OCP circuit trips for a given number of consecutive PWM cycles, the device enters hiccup mode; the device is disabled for about 6.5ms and restarted with a normal soft-start. This cycle can continue indefinitely as long as the over current condition persists.

LDO:

The LDOs have foldback current limit. When an over-current event is detected, the LDO will limit the amount of output current that is allowed in order to reduce power dissipation. The foldback current is typically 50% of the nominal current limit.

Thermal Protection

The thermal shutdown circuit disables the device operation (transistors turn off) when the junction temperature exceeds 155°C. When the junction temperature drops by approximately 25°C, the converters will re-start with a normal soft-start. By preventing operation at excessive temperatures, the thermal shutdown circuit will protect the device from overstress.

Pre-Bias Start-up

DC-DC buck regulator supports startup into a pre-biased output. A proprietary circuit ensures the output voltage rises from the pre-bias voltage level to the programmed output voltage on startup. During this soft-start period, the voltage rise is monotonic for output voltage range from 0% to 90% of nominal. If the pre-bias voltage is above 90% on startup, there might be a slight dip (~3%) in output voltage before it rises monotonically. If the pre-bias voltage is above 100% of nominal during startup, the device will not switch until the output voltage decays below the target voltage. Note that when the device begins switching and the pre-bias output voltage is higher than nominal, the bottomside NFET will discharge the output quickly (but limited to 2-cycles to prevent excessive current) to bring the voltage back into regulation. The pre-bias protection circuit is designed to prevent improper behavior on startup regardless of pre-bias output voltage during soft-start.

Input Under-Voltage Lock-Out

When the device input voltage falls below UVLO, switching is disabled to prevent operation at insufficient voltage levels. During startup, the UVLO circuit ensures that the converter will not start switching until the input voltage is above the specified minimum voltage. Hysteresis and input de-glitch circuits are incorporated in order to ensure high noise immunity and prevent a false trigger in the UVLO voltage region.

APPLICATION INFORMATION

Each output rail on the EZ6303QI can be programmed using the feedback reference voltage and a simple resistor divider network (R_A and R_B). The DC-DC buck regulator feedback reference voltage is 0.6V and the LDO feedback reference voltage is 0.9V (V_{FB} = 0.6V, V_{FBL1} = V_{FBL2} = 0.9V).

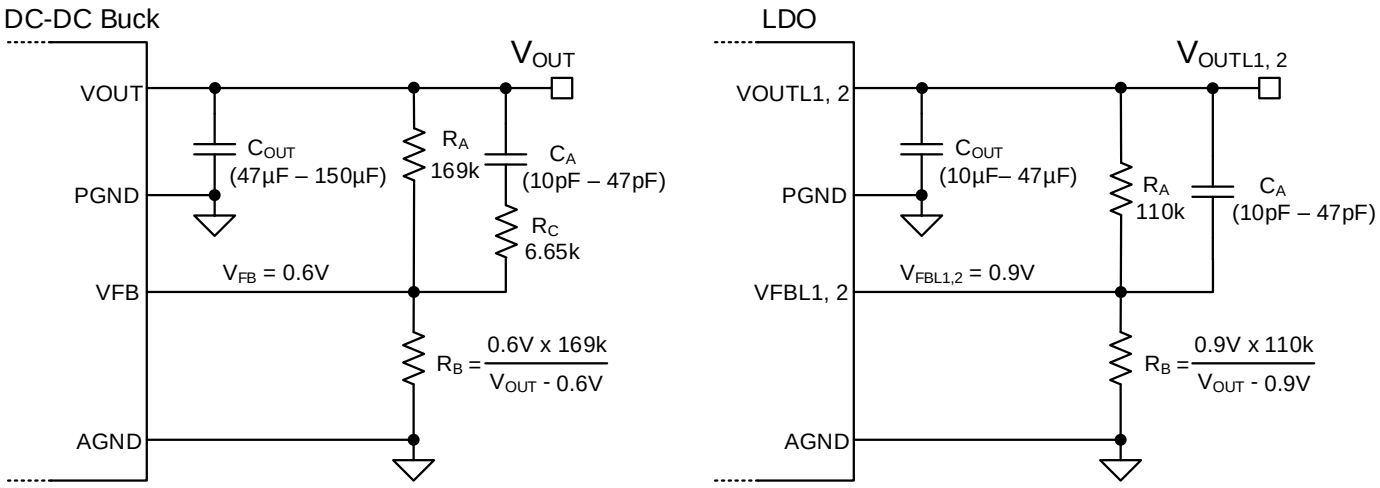


Figure 6: Output Voltage Setting (Buck left, LDO right)

The recommended R_A resistor value is shown in Figure 6 and Table 1 for each regulator. Depending on the output voltage (V_{OUT}), the R_B resistor value may be calculated as shown in Figure 6. Since the accuracy of the output voltage setting is dependent upon the feedback voltage and the external ressitors, 1% or better resistors are recommended. The recommended external compensation values are shown in Table 1.

Table 1: External Compensation Recommendations

Rail	V_{OUT}	R_B	C_A	R_A	R_C	C_{OUT}
DC-DC	0.6V	OPEN	33pF	169kΩ	6.65kΩ	47µF or 2 x 22µF
	0.9V	340kΩ	33pF			
	1.0V	255kΩ	33pF			
	1.2V	169kΩ	33pF			
	1.5V	113kΩ	27pF			
	1.8V	84.5kΩ	27pF			
	2.5V	53.6kΩ	27pF			
	3.3V	37.4kΩ	27pF			
LDO	1.0V	1MΩ	33pF	110kΩ	0	47µF or 2 x 22µF
	1.2V	332kΩ	33pF			
	1.5V	165kΩ	27pF			
	1.8V	110kΩ	27pF			
	2.5V	61.9kΩ	27pF			
	3.3V	41.2kΩ	27pF			

Compensation

Most of the DC-DC regulator's compensation is internal, which simplifies the design. In some applications, improved transient performance may be desired with additional output capacitors (C_{OUT}). In such an instance, the phase-lead capacitor (C_A) can be adjusted depending on the total output capacitance. Using Table 1 as the reference for C_A, if C_{OUT} is increased, then the C_A should also be increased. The relationship is linearly shown below:

$$\Delta C_{OUT} \approx +50\mu F \rightarrow \Delta C_A \approx +5pF$$

As C_{OUT} increases and the C_A value is adjusted, the device bandwidth will reach its optimization level (at around $1/10^{th}$ of the switching frequency). The limitation for adjusting the compensation is based on diminished return. Significant increases in C_{OUT} and C_A may not yield better transient response or in some situations cause lower gain and phase margin. Over compensating with excessive output capacitance may also cause the device to trigger current limit on startup due to the energy required to charge the output up to regulation level. Due to such limitations, the recommended maximum output capacitance (C_{OUT_MAX}) is 150µF and the recommended maximum phase-lead capacitance (C_{A_MAX}) is 47pF.

Input Capacitor Selection

The input of synchronous buck regulators can be very noisy and should be decoupled properly in order to ensure stable operation. In addition, input parasitic line inductance can attribute to higher input voltage ripple. The EZ6303QI requires a minimum of 10µF input capacitor on each of the rails. As the distance of the input power source to the input is increased, it is recommended to increase input capacitance in order to mitigate the line inductance from the source. Low-ESR ceramic capacitors should be used. The dielectric must be X5R or X7R rated and the size must be at least 0805 (EIA) due to derating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger capacitors in order to provide high frequency decoupling. Larger electrolytic or tantalum bulk capacitors may be used in conjunction to increase total input capacitance but should not be used solely as a replacement for the ceramic capacitors.

Table 2: Recommended Input Capacitors

Description	MFG	P/N
10 µF, 10V, 10% X7R, 1206	Murata	GRM31CR71A106KA01L
	Taiyo Yuden	LMK316B7106KL-T
22 µF, 10V, 20% X5R, 1206	Murata	GRM31CR61A226ME19L
	Taiyo Yuden	LMK316BJ226ML-T

Output Capacitor Selection

The output ripple of a synchronous buck converter can be attributed to its inductance, switching frequency and output decoupling. The EZ6303QI requires a minimum of 47µF output capacitance for the DC-DC buck regulator and 10µF for each of the LDOs. Low ESR ceramic capacitors should be used. The dielectric must be X5R or X7R rated and the size must be at least 0805 (EIA) due to derating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.

Table 3: Recommended Output Capacitors

Description	MFG	P/N
47µF, 6.3V, 20% X5R, 1206	Murata	GRM31CR60J476ME19L
	Taiyo Yuden	JMK316BJ476ML-T
	Taiyo Yuden	LMK316BJ226ML-T

Output ripple voltage is determined by the aggregate output capacitor impedance. Output impedance, denoted as Z, is comprised of effective series resistance (ESR) and effective series inductance (ESL):

$$Z = ESR + ESL$$

The resonant frequency of a ceramic capacitor is inversely proportional to the capacitance. Lower capacitance corresponds to higher resonant frequency. When two capacitors are placed in parallel, the benefit of both are

combined. It is beneficial to decouple the output with capacitors of various capacitance and size. Placing them all in parallel reduces the impedance and will hence result in lower output ripple.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

THERMAL CONSIDERATIONS

Thermal considerations are important elements of power supply design. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be taken into account. The Intel Enpirion PowerSoC technology helps alleviate some of those concerns.

The EZ6303QI DC-DC converter is packaged in a 4mm x 7mm x 1.85mm 40-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 155°C.

The following example and calculations illustrate the thermal performance of the EZ6303QI with the following parameters:

$V_{IN} = V_{INL1} = V_{INL2} = 3.3V$

$V_{OUT} = 2.5V$, $V_{OUTL1} = 2.5V$, $V_{OUTL2} = 1.8V$

$I_{OUT} = 2.2A$, $I_{OUTL1} = 300mA$, $I_{OUTL2} = 300mA$

First, calculate the total output power based on all rails.

$P_{OUT} = V_{OUT} \times I_{OUT} = 2.5V \times 2.2A = 5.5W$

$P_{OUTL1} = V_{OUTL1} \times I_{OUTL1} = 2.5V \times 300mA = 0.75W$

$P_{OUTL2} = V_{OUT} \times I_{OUT} = 1.8V \times 300mA = 0.54W$

Next, determine the input power. For the DC-DC buck regulator we can use the efficiency (η) shown in Figure 7 to determine the input power.

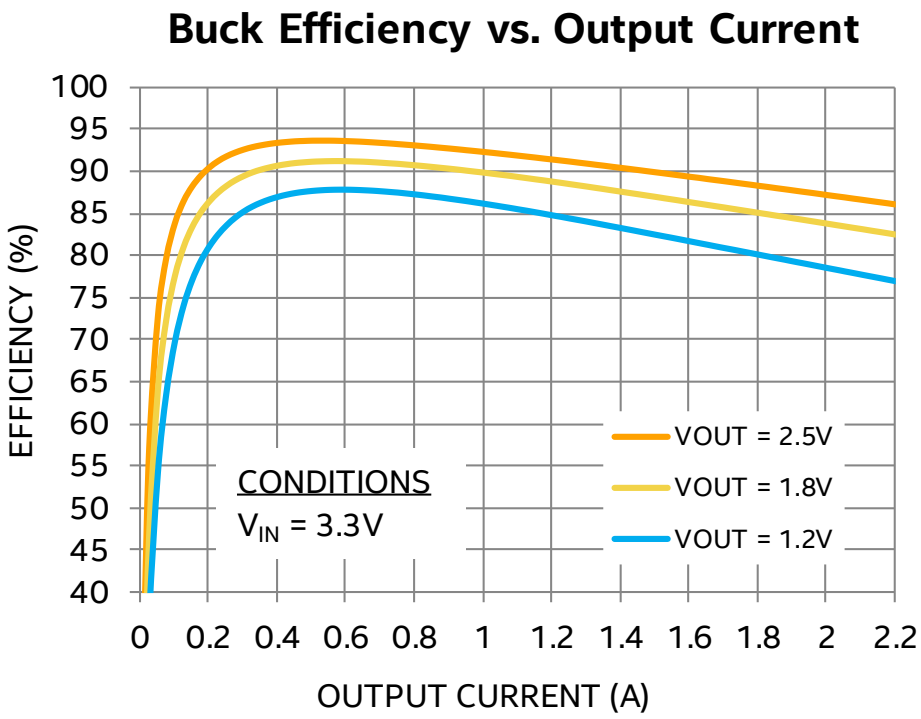


Figure 7: Efficiency vs. Output Current

For the DC-DC buck regulator, V_{IN} = 3.3V, V_{OUT} = 2.5V at 2.2A, η ≈ 86%

$\eta = P_{OUT} / P_{IN} = 86\% = 0.86$

$P_{IN} = P_{OUT} / \eta$

$P_{IN} \approx 5.5W / 0.86 \approx 6.4W$

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

$P_D = P_{IN} – P_{OUT}$

$= 6.4W – 5.5W \approx 0.9W$

For the LDOs, the input current is approximately equal to the output current (note that the quiescent current of the LDO is assumed to be negligible).

$P_{DL1} = P_{INL1} – P_{OUTL1}$

$P_{DL1} = 3.3V \times 300mA – 2.5V \times 300mA = 0.24W$

$P_{DL2} = 3.3V \times 300mA – 1.8V \times 300mA = 0.45W$

The total power loss is the sum of all losses on all rails.

$P_{DTOTAL} = P_D + P_{DL1} + P_{DL2}$

$P_{DTOTAL} = 0.9W + 0.24W + 0.45W$

$P_{DTOTAL} = 1.59W$

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EZ6303QI has a θ_{JA} value of 11.5°C/W without airflow.

Determine the change in temperature (ΔT) based on P_D and θ_{JA}.

$$\Delta T = P_{DTOTAL} \times \theta_{JA}$$

$$\Delta T \approx 1.59W \times 11.5°C/W \approx 18.3°C$$

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

$$T_J = T_A + \Delta T$$

$$T_J \approx 25°C + 18.3°C \approx 43.3°C$$

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

$$T_{AMAX} = T_{JMAX} – P_{DTOTAL} \times \theta_{JA}$$

$$\approx 125°C – 18.3°C \approx 106.7°C$$

The maximum ambient temperature the device can reach is 106.7°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.

APPLICATION SCHEMATIC

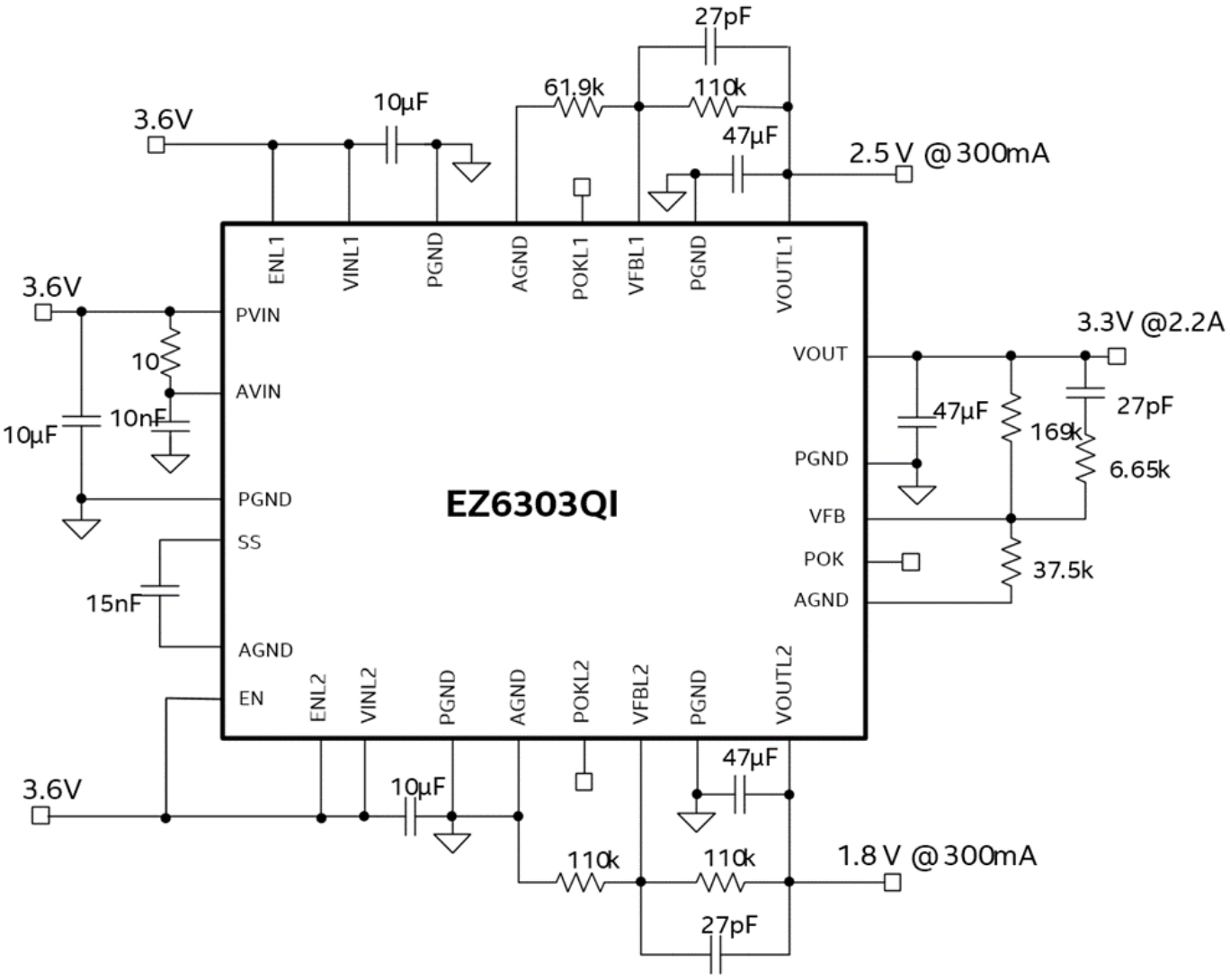


Figure 8: Application Schematic for V_{OUT} = 3.3V, V_{OUTL1}=2.5V, V_{OUTL2} = 1.8V

LAYOUT RECOMMENDATIONS

Figure 9 shows critical components and layer 1 traces of a recommended minimum footprint EZ6303QI layout. ENABLE and other small signal pins need to be connected and routed according to specific customer application. Visit the Enpirion Power Solutions website at www.altera.com/powersoc for more information regarding layout. Please refer to this Figure 9 while reading the layout recommendations in this section.

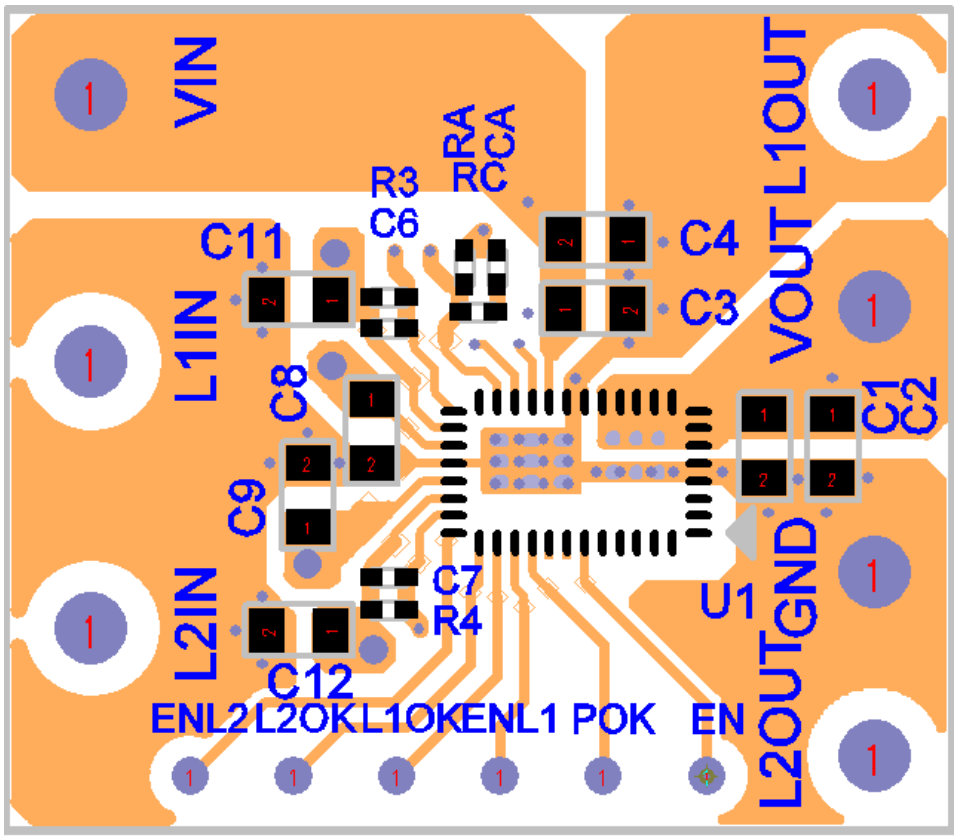


Figure 9: Top PCB Layer Critical Components and Copper for Minimum Footprint (Top View)

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EZ6303QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The Voltage and GND traces between the capacitors and the EZ6303QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The system ground plane should be on the 2nd layer (below the surface layer). This ground plane should be continuous and un-interrupted.

Recommendation 3: The large thermal pad underneath the device must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1-oz. copper plating on the inside wall, making the finished hole size around 0.2mm to 0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter. Please see Figure 9.

Recommendation 4: Multiple small vias (the same size as the thermal vias discussed in recommendation 4 should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. Put the vias under the capacitors along the edge of the GND copper closest to the Voltage copper. Please see Figure 9. These vias connect the input/output filter capacitors to the GND plane, and help reduce

parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND slit separating the two components. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

Recommendation 5: AVIN is the power supply for the internal small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 9 this connection is made at the input capacitor furthest from the PVIN pin and on the input source side. Avoid connecting AVIN near the PVIN pin even though it is the same node as the input ripple is higher there.

Recommendation 6: The V_{OUT} sense point should be connected at the last output filter capacitor furthest from the VOUT pins. Keep the sense trace as short as possible in order to avoid noise coupling into the control loop.

Recommendation 7: Keep R_A, C_A, R_C and R_B close to the VFB pin (see Figure 9). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane. The AGND should connect to the PGND at a single point from the AGND pin to the PGND plane on the 2nd layer.

Recommendation 8: The layer 1 metal under the device must not be more than shown in Figure 9. See the following section regarding Exposed Metal on Bottom of Package. As with any switch-mode DC-DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

DESIGN CONSIDERATIONS FOR LEAD-FRAME BASED MODULES

Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package, as shown in Figure 10.

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EZ6303QI should be clear of any metal (copper pours, traces, or vias) except for the thermal pads. The “shaded-out” area in Figure 10 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the shaded-out area runs the risk of undesirable shorted connections even if it is covered by soldermask.

The solder stencil aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package.

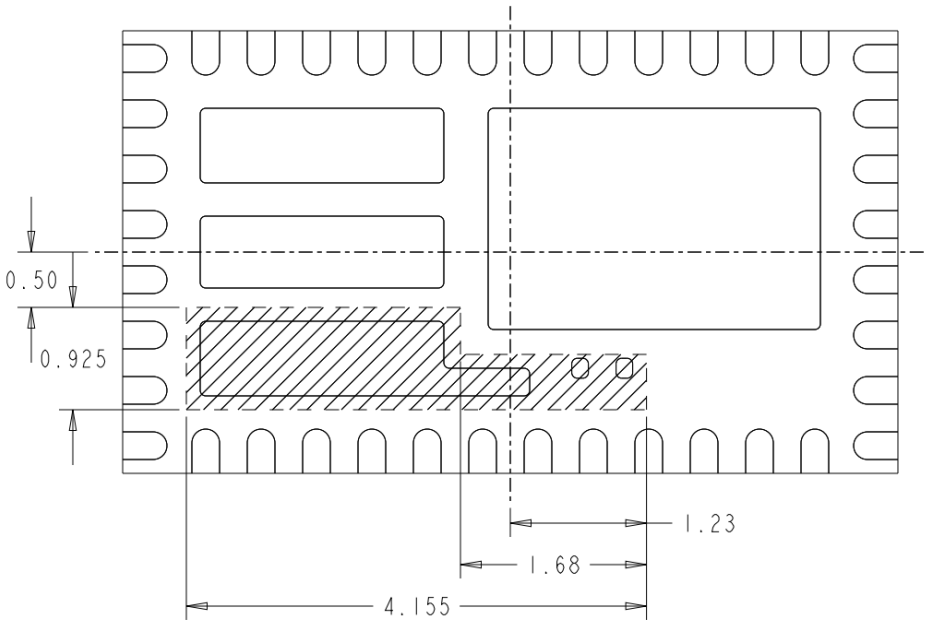


Figure 10: Lead-Frame exposed metal (Bottom View)

Shaded area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

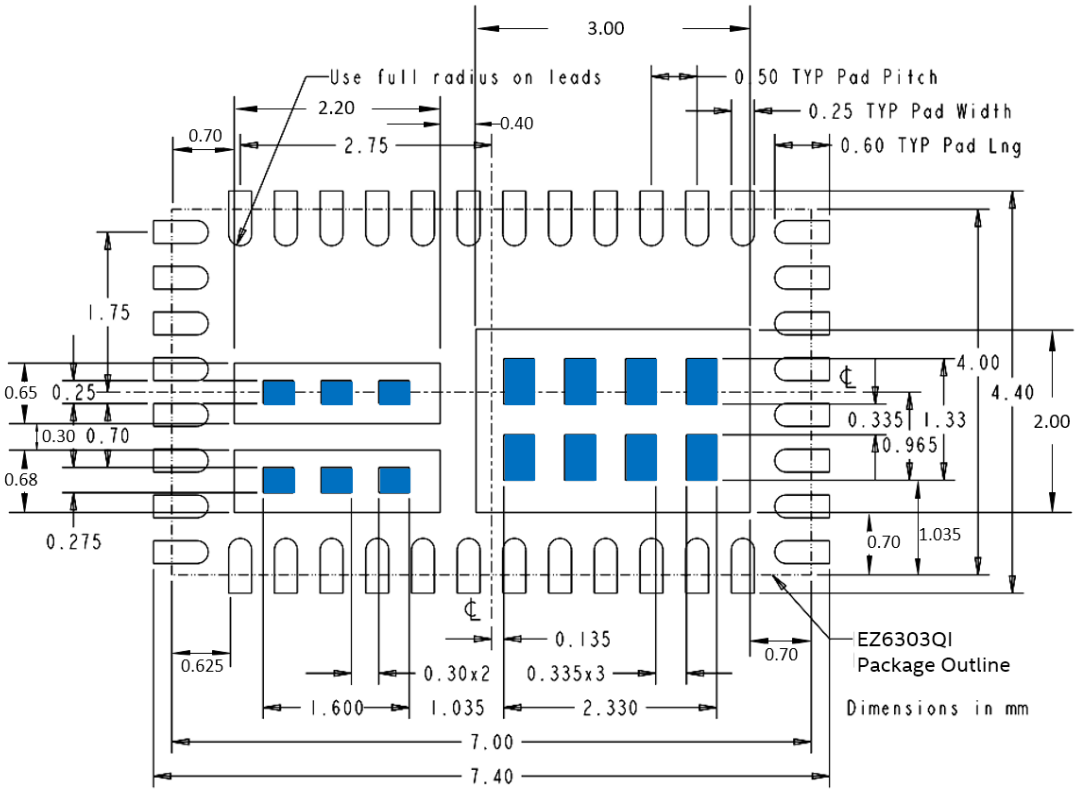


Figure 11: EZ6303QI Landing Pattern with Solder Stencil (Top View)

The solder stencil aperture for the underneath pads is shown in Figure 11 and is based on Enpirion power product manufacturing specifications.

PACKAGE DIMENSIONS

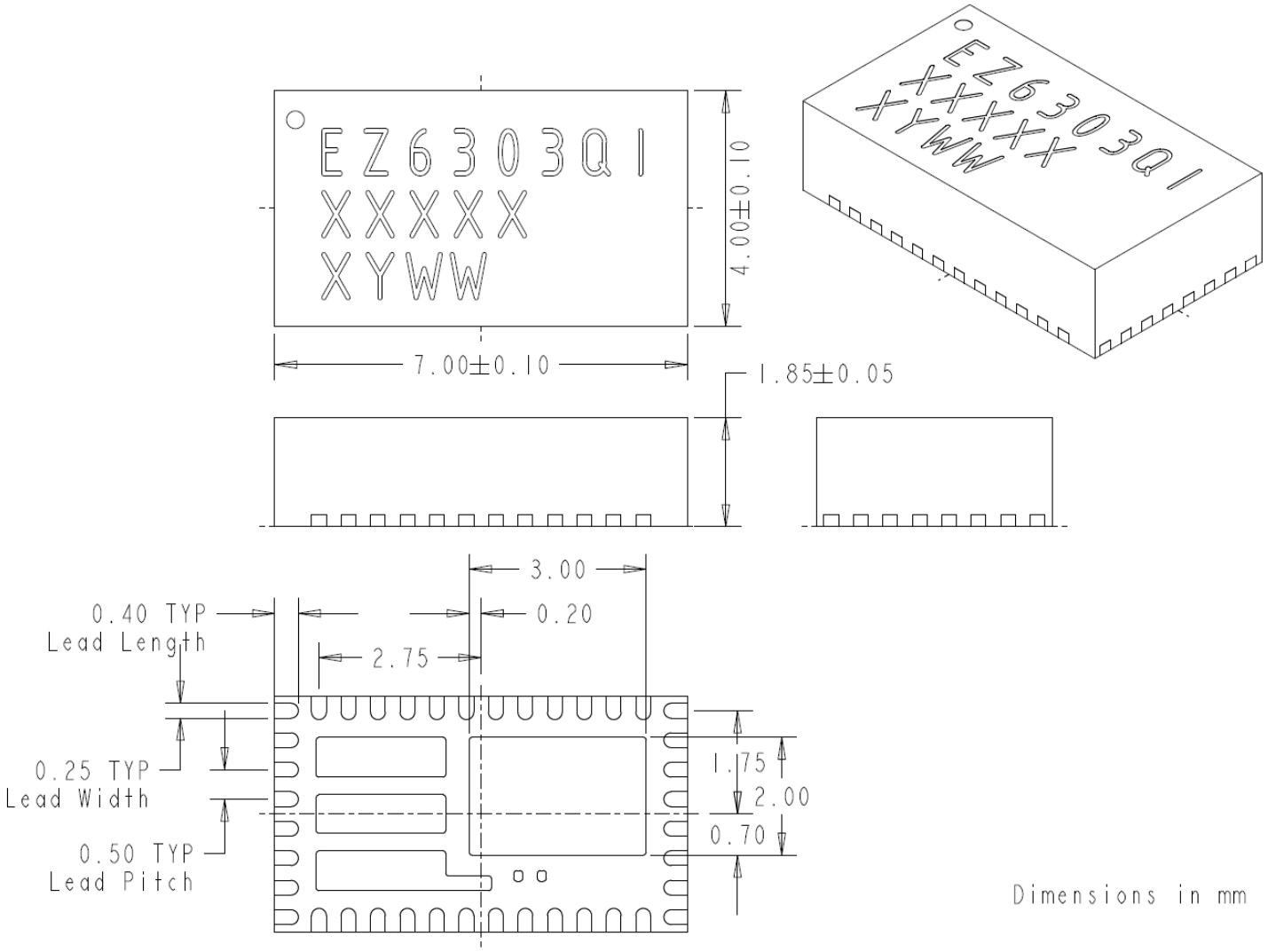


Figure 12: EZ6303QI Package Dimensions

Packing and Marking Information: www.Intel.com/support/reliability/packing/rel-packing-and-marking.html

REVISION HISTORY

Rev	Date	Change(s)
A	December, 2017	• Initial Release
B	April, 2018	• Corrected typo on Pin Configuration pad number for 42 and 43 • Changed Note A to discuss Optional pads to improve BLR • Updated Layout Recommendations image to reflect latest layout
C	September, 2018	• Added EMI performance curves • Corrected maximum C_A range on Figure 6
D	May, 2019	• Corrected Solder stencil on Figure 11
E	June, 2019	• Update the application schematic on Figure 8 • Formatting changes
F	July, 2019	• Updated the footprint missing dimensions on Figure 11

WHERE TO GET MORE INFORMATION

For more information about Intel and Intel Enpirion PowerSoCs, visit https://www.intel.com/enpirion

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