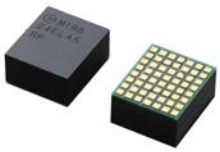
MYMGM1R824ELA5RP

MonoBK™, 2 Modules Multi Phase 40A DC-DC Converter



Typical unit of 1 module

FEATURES

- Settable output voltage from 0.7 to 1.2Vdc
- Up to 40A of output current with 2 modules by multi Phase Operation
- Quick response to load change
- Ultra small surface mount package 10.5 x 9.0 x 5.0mm per 1 module
- High efficiency of 91.0% max total.
- Outstanding thermal derating performance
- Over Current (OC) /Voltage (OV) ,Under Voltage (UV) protection and Over Temperature protection (OT).
- ON/OFF control (Positive logic)
- Power Good (PWGOOD) signal
- High Reliability / Heat Shock Testing 700cycle (-40 to +125degC)
- PMBus™ interface available
- PMBus™ 1.3 ready
- Minimum Vout setting resolution 2mV/bit

PRODUCT OVERVIEW

The MYMGM1R824ELA5RP is miniature MonoBK™ called "Mono Block", non-isolated Point-of-Load (PoL) DC-DC power converters for embedded applications. The small form factor measures only 10.5 x 9.0 x 5.0 mm per 1 module. Applications include powering FPGA/CPU's, data-com/telecom systems, Distributed Bus Architectures (DBA), programmable logic and mixed voltage systems.

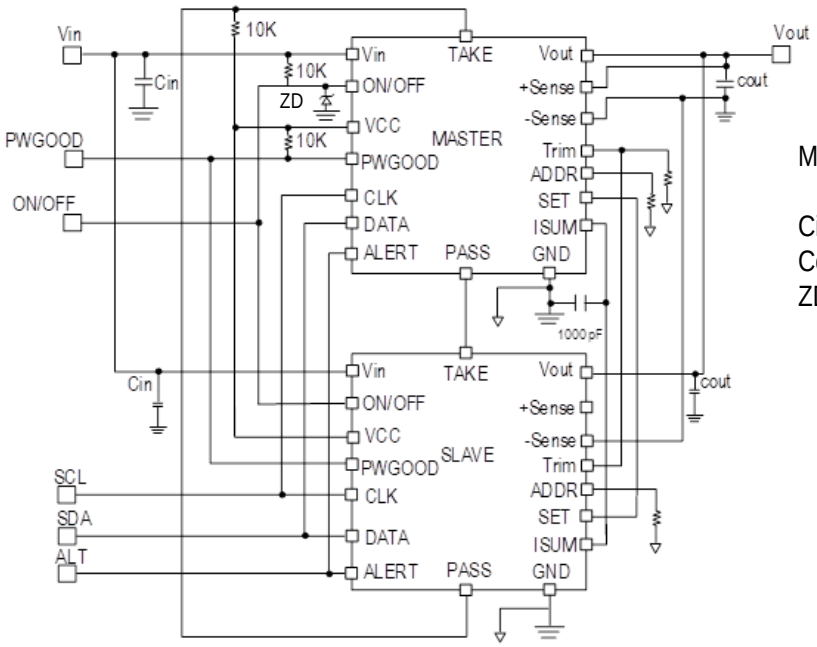
The product has input voltage ranges of 7.5 to 15Vdc and a maximum output current up to 40A with 2 modules. (This product cannot be used 1 module. Please use 2 modules together.) Based on a fixed frequency synchronous buck converter switching topology, this high power conversion efficient PoL module features settable output voltage 0.7 to 1.2Vdc, ON/OFF control, Power Good (PWGOOD) signal output and PMBus™ ALERT output.

This product also includes under voltage lock out (UVLO), output short circuit protection, over-current protection (OC), over-voltage protection (OV). under-voltage protection (UV) and over-temperature protection (OT).

Moreover this product has PMBus™ interface so various parameters can be handled and monitored by digital signals.

SIMPLIFIED APPLICATION

MYMGM1R824ELA5RP 2 modules multi phase operation



MYMGM1R824ELA5RP x 2

Cin : 22uF/25V x 2pcs for each 1 module
Cout : 220uF/4V x 3pcs for each 1 module
ZD : EDZV 3.3B (ROHM)

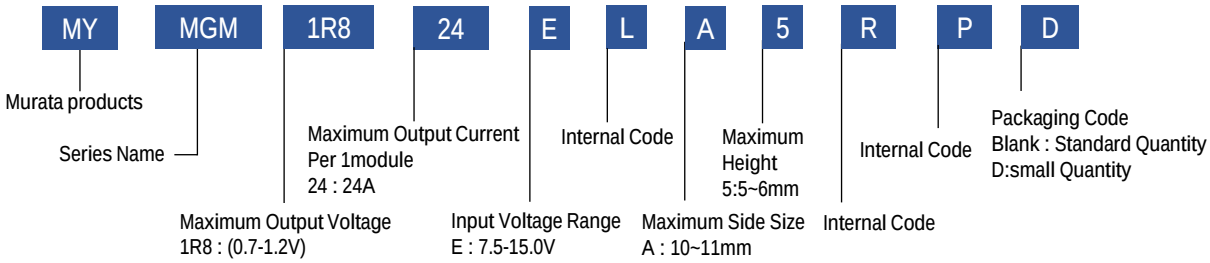
(Typical topology is shown. Murata recommends an external input fuse.)

PERFORMANCE SPECIFICATIONS SUMMARY AND ORDERING GUIDE (Including series products)

PART NUMBER	OUTPUT						INPUT				Efficiency (%)	ON/OFF	PACKAGE (Per 1 module)
	Vout (V)	Iout (A,max.)	Power (W)	R/N typ. (% of Vout)	Regulation(max.) Line(%)	Regulation(max.) Load(%)	Vin typ. (V)	Range (Vdc)	Iin no load (mA)	Iin full load (A)			(mm)
MYMGM1R824ELA5RP	0.7-1.2	40	48	1.5	±0.5	±0.5	12	7.5-15.0	110	4.62	86.1	Yes (Positive)	10.5 x 9.0 x 5.0
MYMGM1R824ELA5RPD	0.7-1.2	40	48	1.5	±0.5	±0.5	12	7.5-15.0	110	4.62	86.1	Yes (Positive)	10.5 x 9.0 x 5.0

1.All specifications are at typical line voltage, Vout = 1.2V and full load, +25degC unless otherwise noted. And the values are for 2 modules used together. Output capacitors are 220uF x 3 (Per 1 module) ceramic. Input capacitors is 22uF x 2 ceramic (Per 1 module) and plenty electrolytic capacitors. See detailed specifications. Input and Output capacitors are necessary for our test equipment.
2.Use adequate ground plane and copper thickness adjacent to the converter.

PART NUMBER STRUCTURE

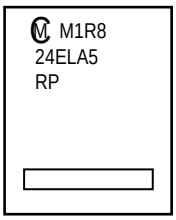


Product Marking

Because of the small size of these products, the product marking contains a character-reduced code to indicate the model number and manufacturing date code. Not all items on the marking are always used. Please note that the marking differs from the product photograph. Here is the layout of the Marking.

Part Number	Product Code
MYMGM1R824ELA5RP	M1R824ELA5RP
MYMGM1R824ELA5RPD	M1R824ELA5RP

Layout (reference)



Codes(reference)

1Pin Marking

M1R824ELA5RP Product code
(Please see product code table beside)

☐ Internal Manufacturing code

FUNCTIONAL SPECIFICATIONS OF MYMGM1R824ELA5RP (Note 1)

ABSOLUTE MAXIMUM RATINGS	Conditions	Minimum	Typical	Maximum	Units
Input Voltage		-0.3		16	Vdc
ON/OFF,PWGOOD,CLK,DATA,ADDR,ALERT Pins	Power on, referred to -Vin	-0.3		3.9	Vdc
Trim Pin	Power on, referred to -Vin			3.9	Vdc
Vout		0.7		1.32	Vdc
Output Current	Current-limited, no damage, short-circuit protected	0		40	A
Storage Temperature Range	Vin = Zero (no power)	-40		125	degC
Absolute maximums are stress ratings. Exposure of devices to greater than any of these conditions may adversely affect long-term reliability. Proper operation under conditions other than those listed in the Performance/Functional Specifications Table is not implied or recommended.					
INPUT	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Operating Voltage Range		7.5	12	15	Vdc
Start-up Threshold	Rising input voltage		7.25		Vdc
Under Voltage Shutdown (Note 12)	Falling input voltage		6.75		Vdc
Internal Filter Type			Capacitive		
Input Current					
Full Load Conditions	Vin = 12.0V, Vout = 1.2V, Iout = 40A		4.62		A
Low Line	Vin = 7.5V, Vout = 1.2V, Iout = 40A		7.36		A
No Load Current	Iout=0A, unit = ON		110		mA
Shut-Down Mode Input Current			5		mA
GENERAL and SAFETY	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Efficiency	Vin = 12.0V, Vout = 1.2V, Iout = 40A		86.1		%
	Vin = 12.0V, Vout = 0.7V, Iout = 40A		79.8		
Calculated MTBF (Note 3)	'+40degC, Vin = 12.0V, Vout = 1.2V, Iout = 50%		$4x10^6$		hours
DYNAMIC CHARACTERISTICS	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Fixed Switching Frequency per 1 module			400		kHz
Startup Time (Vin ON)	Vout = 1.2V (Vout = 5% to 90% of Vout)		2		ms
Startup Time (Remote ON)	Vout = 1.2V (Vout = 5% to 90% of Vout)		2		ms
Dynamic Load Response	50-100% load step, di/dt		2		A/us
Dynamic Load Peak Deviation (Note 16)	Vin = 12V, Vout = 1.0V, Iout = 50-100%		±3.0%		Voset
FUNCTIONS	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Remote ON/OFF Control (Note 4)					
Logic					
ON State Range		2.15		3.6	V
OFF Stage Range		-0.3		1.2	V
Control Current	Open collector/drain			-	mA
Power-Good (PWGOOD) Output					
PWGOOD TRUE (HI)		(Voset x 90%) < Vout < (Voset x 115%)			
PWGOOD FALSE (LO)		Out of above range			
OUTPUT	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Total Output Power	See Derating	0		48	W
Voltage					
Output Voltage Range (Note 10)		0.7		1.2	Vdc
Minimum Loading			Note		
Accuracy (50% load, untrimmed)	Vin = 12V, Vout = 1.2V, Cout = 1320uF, Ta = 25degC	±1			% of Vout
Over Voltage Protection (Note 13)		>120%			Vout
Under Voltage Protection		<70%			Vout
Current					
Total Output Current Range (Note 2)		0		40	A
Each Phase Current Limit Inception	After warmup		32		A
Output Maximum Current Per 1 module (Note 2, 17)		0		24	A
Short Circuit					
Short Circuit Duration (remove short for recovery)	Output shorted to ground, no damage		Continuous		
Short Circuit Protection Method (Note 5)			Hiccup		
Pre-bias Start-up		Converter will start up if the external output voltage is less than set Vout.			
Regulation (Note 8)					
Line Regulation (Note 17)	Vin = min. to max. Ta = min. to max.			±1.0	% of Vout
Temperature variation			±1.5		% of Vout
Total output voltage variation (Note 17)	Iout = min. to max.			±3.0	%
Ripple and Noise (20MHz bandwidth) (Note 6)			10		mV pk-pk
External Output Capacitance Range (Note 11)		1320		5000	uF

COMMON SPECIFICATION

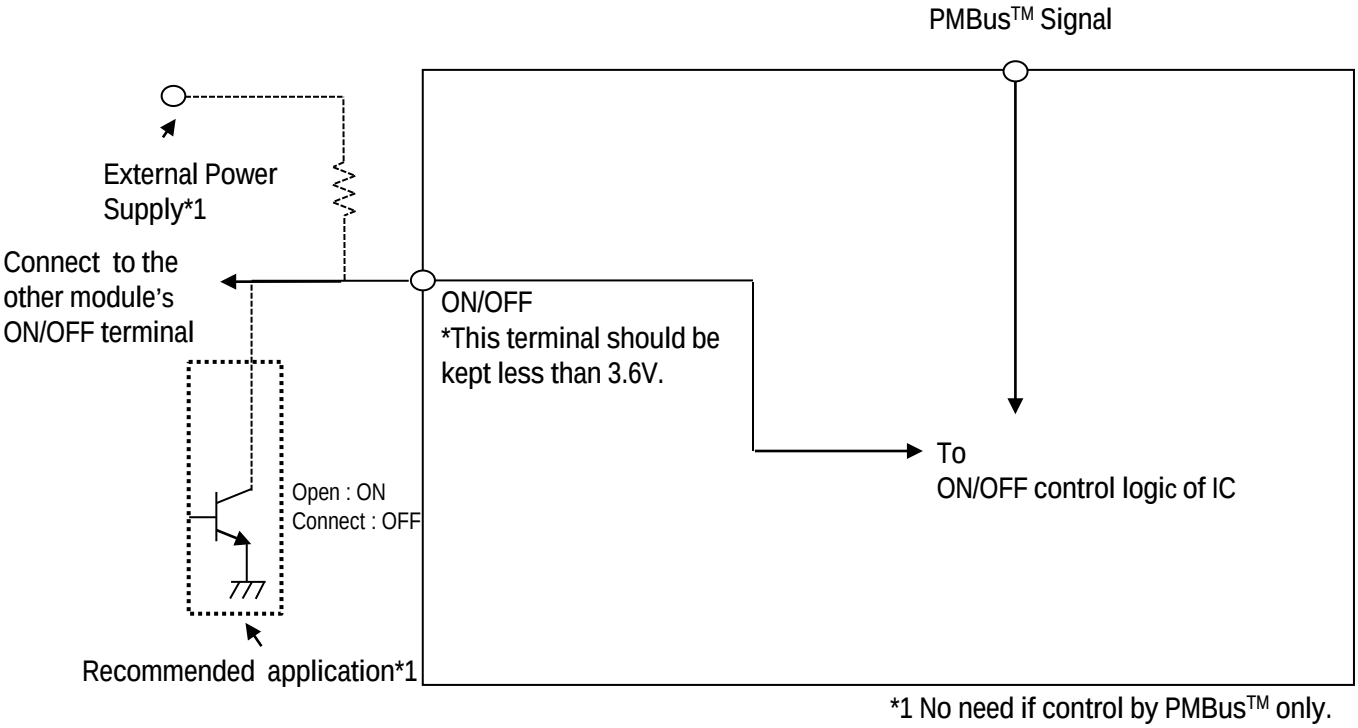
MECHANICAL(Common)	Conditions	Minimum	Typical	Maximum	Units
Mechanical Dimension of 1 module	L x W x H		10.5(typ.) x 9.0(typ.) x 5.0(max.)		mm
Weight of 1 module			1.5		grams
ENVIRONMENTAL(Common)	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Operating Ambient Temperature Range (Note 2, 7)	With Derating	-40		105	degC
Storage Temperature Range	Vin = Zero (no power)	-40		125	degC
Thermal Resistance(Reference data) Ψjt (Note 15)	Vin=12V, Vout=1.2V, Iout=20A (Per 1 module)		1.6		degC/W
	Vin=12V, Vout=1.2V, Iout=10A (Per 1 module)		2.5		degC/W
Maximum Junction Temperature				125	degC
Thermal Protection/Shutdown (Note 9, 14)	Measured in module		155		degC
Thermal Protection/Shutdown (Recovery) (Note 9, 14)	Measured in module		135		degC
Moisture Sensitivity Level			3		

Specification Notes

(1)Specifications are typical at +25degC, Vin=typical (+12.0V), Vout=typical (+1.2V), full load (40A), external caps and natural convection with 2 modules, unless otherwise indicated. This model is tested and specified with external 220uF x 3 ceramic output capacitors per 1 module, 22uF x 2 ceramic and plenty electrolytic external input capacitors per 1 module. All capacitors are low ESR types. These capacitors are necessary to accommodate our test equipment and may not be required to achieve specified performance in your applications. However, Murata recommends installation of these capacitors. Several parameters can be changed by PMBus.(See PMBus interface later)
(2)Note that Maximum Power Derating curves indicate an average current at typical input voltage. At higher temperatures and/or no airflow, the converter will tolerate brief full current outputs if the total RMS current over time does not exceed the Derating curve.
(3)Mean Time Between Failure is calculated using the Telcordia SR-332 method, +40degC, half output load, natural air convection.
(4)The ON/OFF Control Input should use a switch or an open collector/open drain transistor referenced to GND. A logic gate may also be used by applying appropriate external voltages which do not exceed absolute maximum ratings.
(5)"Hiccup" overcurrent operation repeatedly attempts to restart the converter with a brief, full-current output. If the overcurrent condition still exists, the restart current will be removed and then tried again. This short current pulse prevents overheating and damaging the converter. Once the fault is removed, the converter immediately recovers normal operation.
(6)Output noise may be further reduced by adding an external filter. At zero output current, the output may contain low frequency components which exceed the ripple specification. The output may be operated indefinitely with no load.
(7)All models are fully operational and meet published specifications, including "cold start" at -40degC.
(8)Regulation specifications describe the deviation as the line input voltage or output load current is varied from a midpoint value to either extreme.
(9)Thermal Protection/Shutdown temperature is measured with the sensor in the each module.
(10)Do not exceed maximum power specifications when adjusting the output trim.
(11)The maximum output capacitive loads depend on the Equivalent Series Resistance (ESR) of the external output capacitor and, to a lesser extent, the distance and series impedance to the load. Larger caps will reduce output noise but may change the transient response. Newer ceramic caps with very low ESR may require lower capacitor values to avoid instability. Thoroughly test your capacitors in the application.
(12)Do not allow the input voltage to degrade lower than the input under voltage shutdown voltage at all times. Otherwise, you risk having the converter turn off. The under voltage shutdown is not latching and will attempt to recover when the input is brought back into normal operating range.
(13)The outputs are intended to sink appreciable reverse current.
(14)When the temperature decreases below the turn-on threshold, the converter will automatically restart.
(15)The thermal resistances are measured only about single module as reference data, and they are measured with our evaluation board as below. 50.8mm x 60.0mm x 1.6mm (8 Layer, 2oz copper each)FR-4.
(16)About di/dt condition, please refer to the table described later.
(17)Ensured by design. Not production tested.

Internal Circuit Diagrams

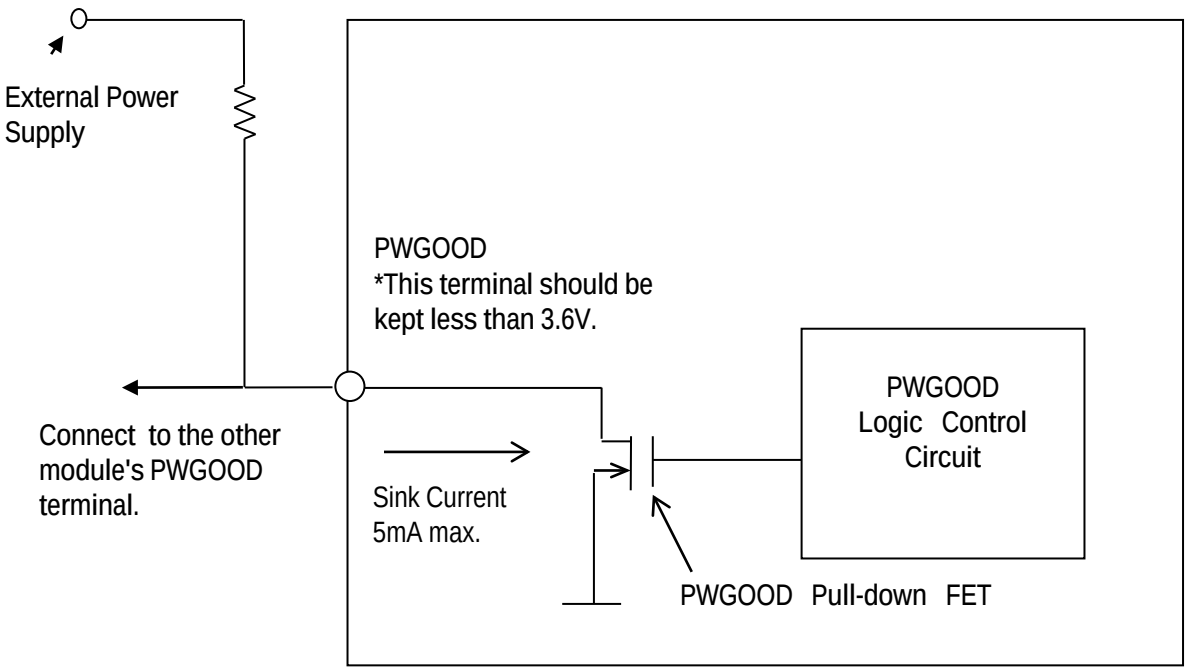
ON/OFF internal circuit diagram and using guide



*1 No need if control by PMBus™ only.

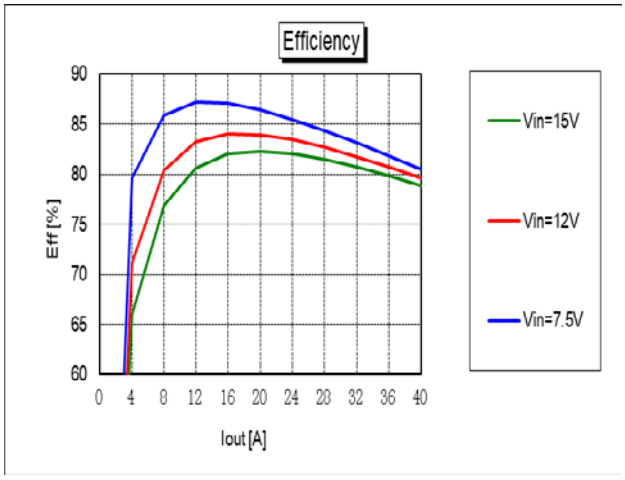
PWGOOD (P.G) internal circuit diagram and using guide

This product needs pulling this terminal.

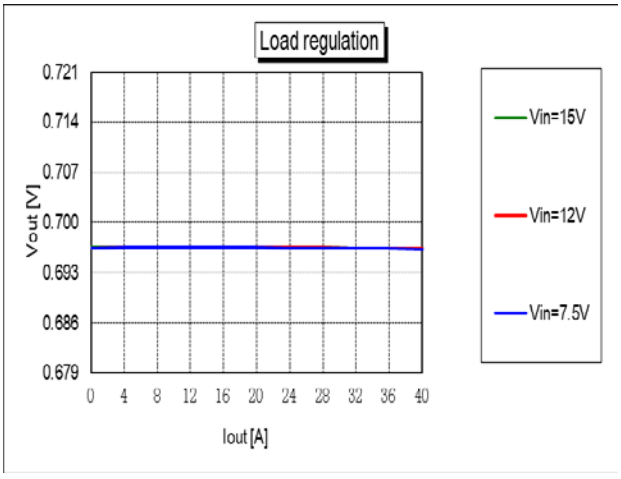


PERFORMANCE DATA AND OSCILLOGRAMS OF MYMGM1R824ELA5RP

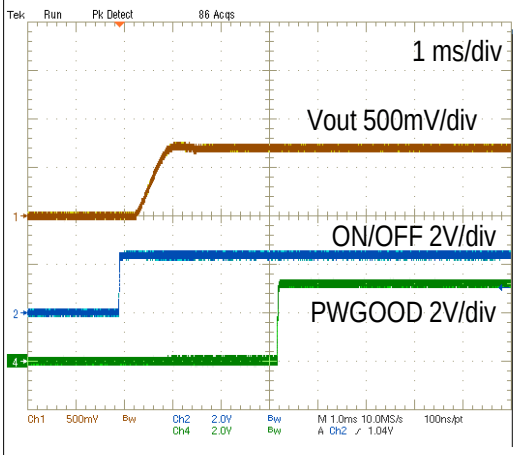
Efficiency vs. Line Voltage and Load Current @ +25degC. (Vout = 0.7V)



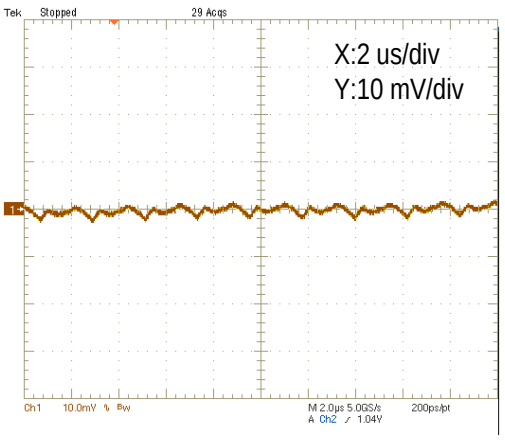
Vout vs. Line Voltage and Load Current @ +25degC. (Vout = 0.7V)



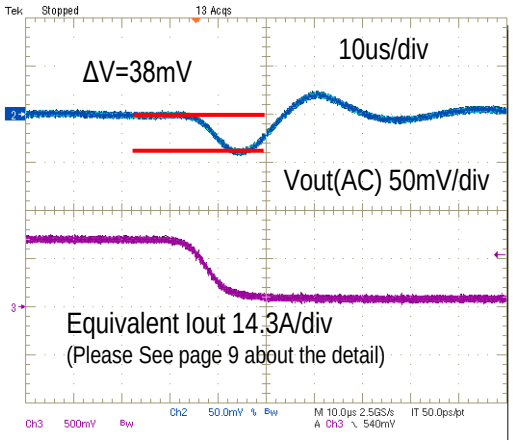
ON/OFF Enable Delay (Vin=12V, Vout=0.7V, Iout=40A, Cload=660uF per 1 module)



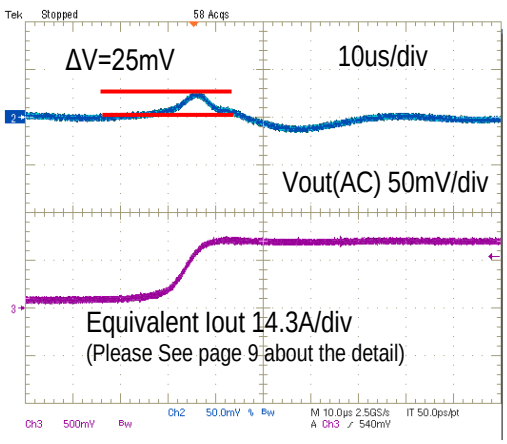
Output Ripple and Noise
(Vin=12V, Vout=0.7V, Iout=40A, Cload=660uF per 1 module, Scope BW=20MHz)



Step Load Transient Response
(Vin=12V, Vout=0.7V, Cload=660uF per 1 module, Iout=20A to 40A 2A/us)

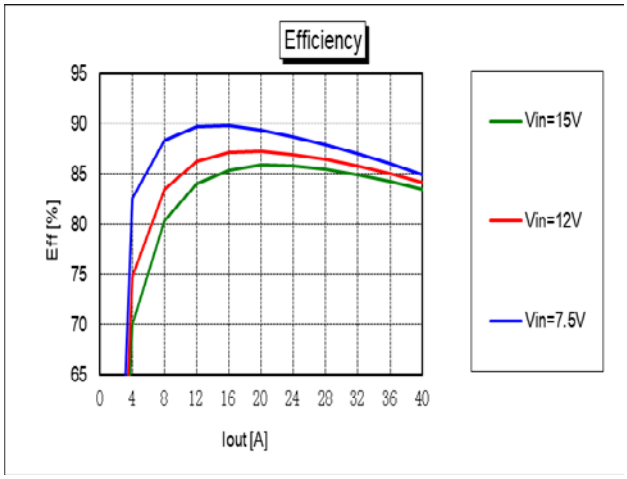


Step Load Transient Response
(Vin=12V, Vout=0.7V, Cload=660uF per 1 module, Iout=40A to 20A 2A/us)

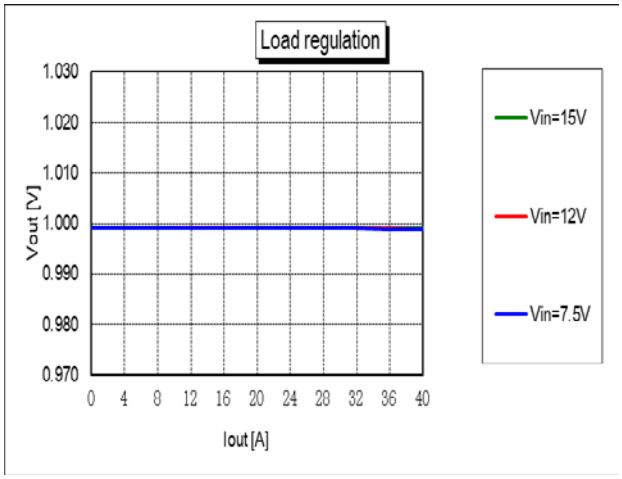


PERFORMANCE DATA AND OSCILLOGRAMS OF MYMGM1R824ELA5RP

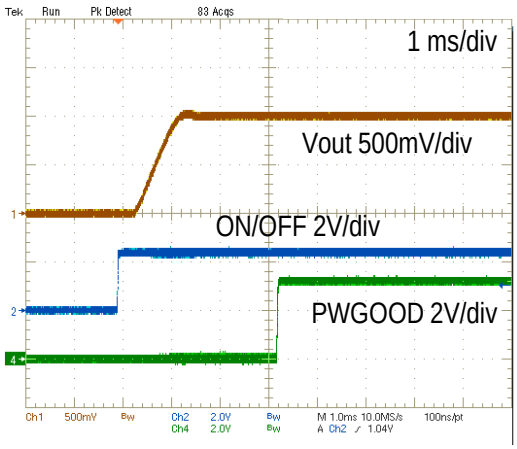
Efficiency vs. Line Voltage and Load Current @ +25degC. (Vout = 1.0V)



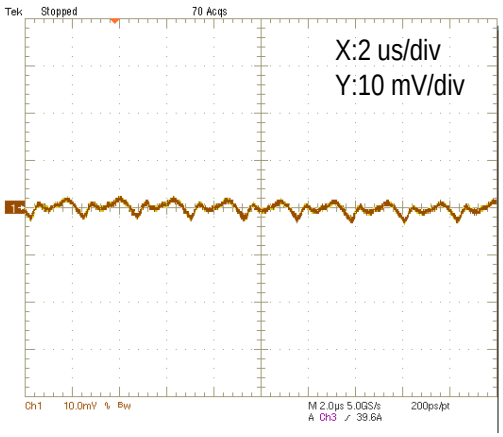
Vout vs. Line Voltage and Load Current @ +25degC. (Vout = 1.0V)



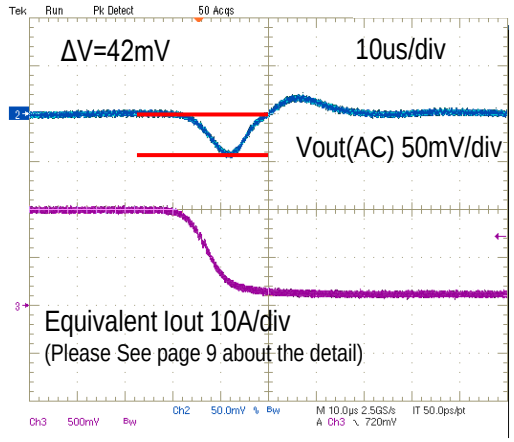
ON/OFF Enable Delay (Vin=12V, Vout=1.0V, Iout=40A, Cload=660uF per 1 module)



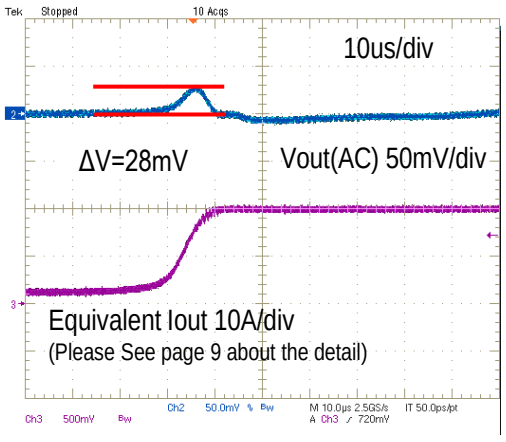
Output Ripple and Noise
(Vin=12V, Vout=1.0V, Iout=40A, Cload=660uF per 1 module, Scope BW=20MHz)



Step Load Transient Response
(Vin=12V, Vout=1.0V, Cload=660uF per 1 module, Iout=20A to 40A 2A/us)

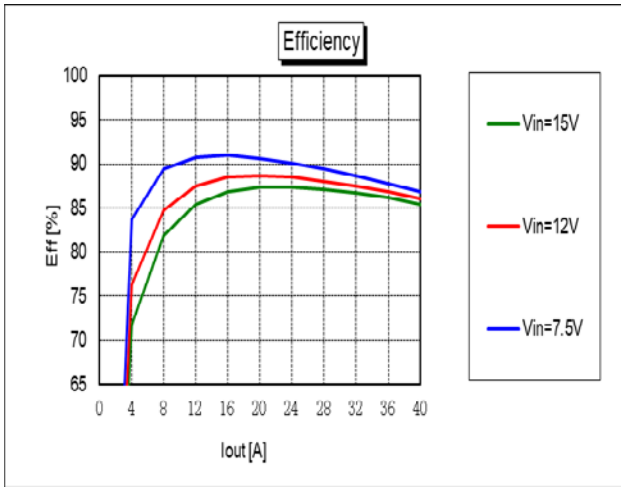


Step Load Transient Response
(Vin=12V, Vout=1.0V, Cload=660uF per 1 module, Iout=40A to 20A 2A/us)

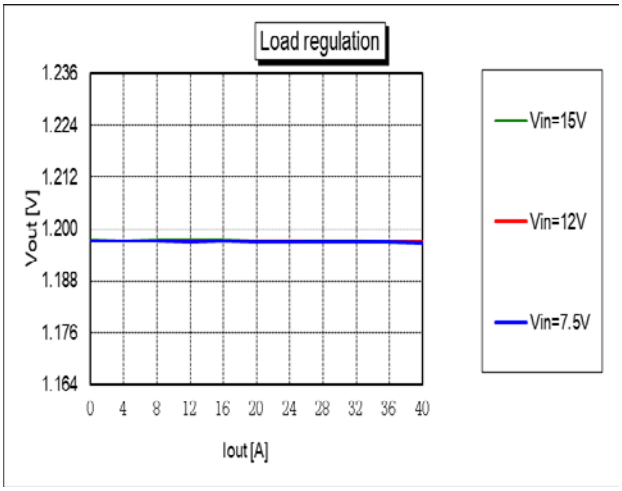


PERFORMANCE DATA AND OSCILLOGRAMS OF MYMGM1R824ELA5RP

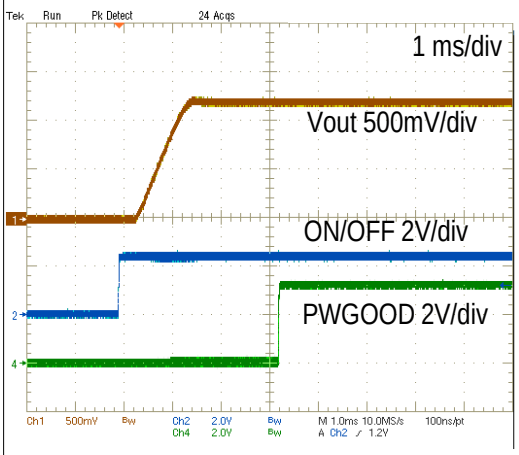
Efficiency vs. Line Voltage and Load Current @ +25degC. (Vout = 1.2V)



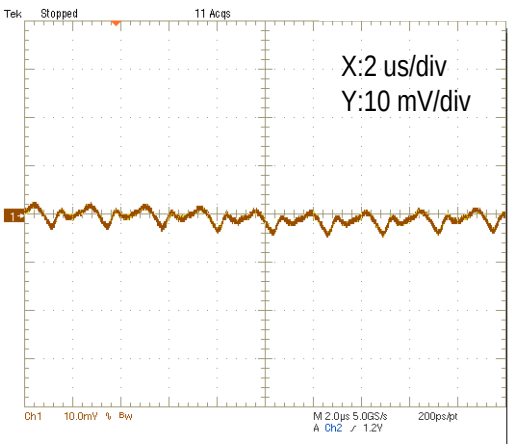
Vout vs. Line Voltage and Load Current @ +25degC. (Vout = 1.2V)



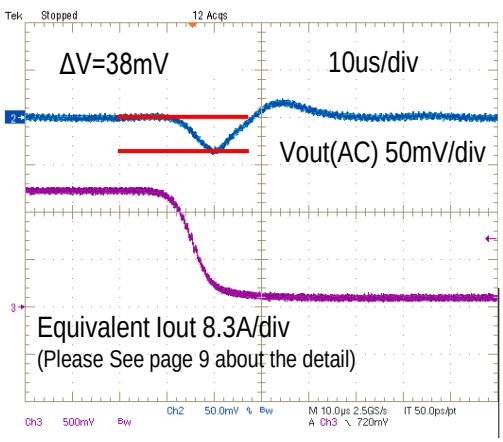
ON/OFF Enable Delay (Vin=12V, Vout=1.2V, Iout=40A, Cload=660uF per 1 module)



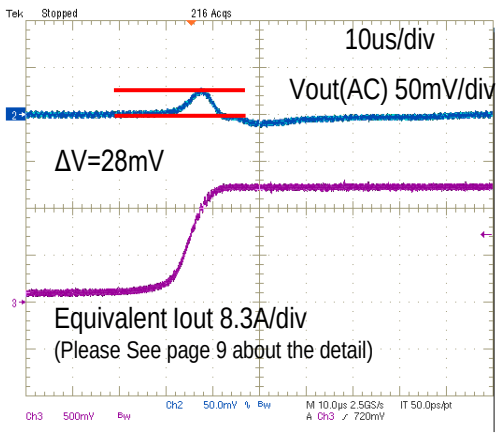
Output Ripple and Noise
(Vin=12V, Vout=1.2V, Iout=40A, Cload=660uF per 1 module, Scope BW=20MHz)



Step Load Transient Response
(Vin=12V, Vout=1.2V, Cload=660uF per 1 module, Iout=20A to 40A 2A/us)

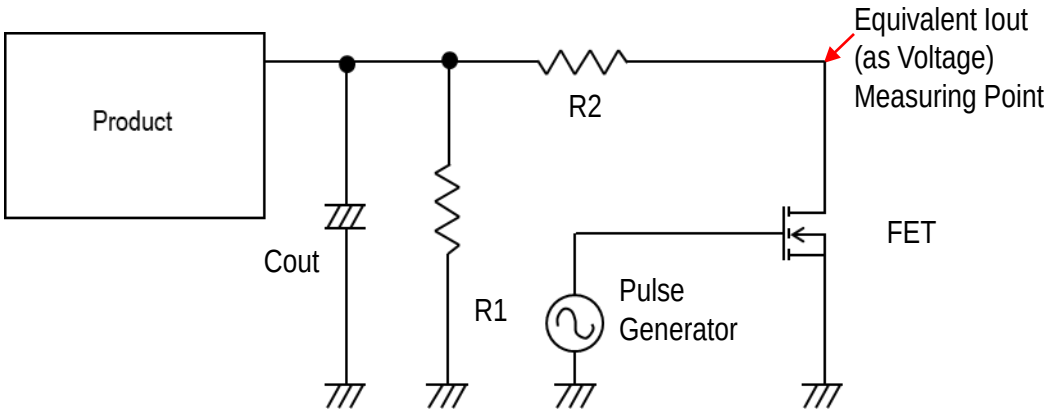


Step Load Transient Response
(Vin=12V, Vout=1.2V, Cload=660uF, Iout=40A to 20A 2A/us)



Step Load Transient Response Measuring Circuit and Condition.

Circuit



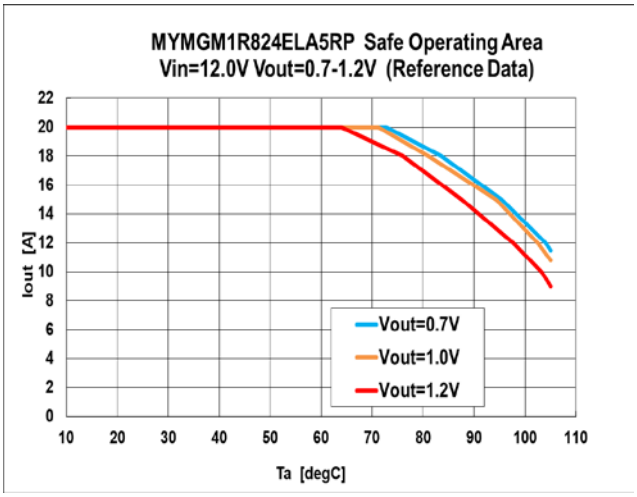
Condition

Vout Setting (V)	R1 (mohm)	R2 (mohm)	FET Ron (mohm)
0.7	35	30	5
1.0	50	45	5
1.2	60	55	5

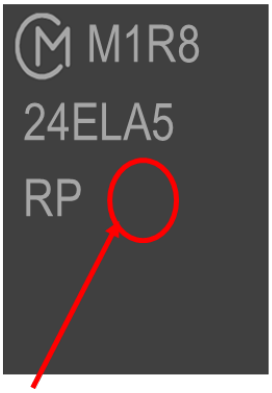
THERMAL DERATINGS OF MYMGM1R824ELA5RP

MYMGM1R824ELA5RP

Maximum Current Temperature Derating at Sea Level Per 1 Module



Temperature Measuring Area



Temperature Measuring Area (Reference)
Position : Center of the Module
Radius: 1mm

Thermal deratings are evaluated in following condition.
・The product is mounted on 50.8mm x 60.0mm x 1.6mm (8 Layer, 2oz copper each) FR-4 board respectively.
・No forced air flow.
Surface(Top of the coil) temperature of the product : 110degC max

TRANSIENT RESPONSE DATAS OF MYMGM1R824ELA5RP

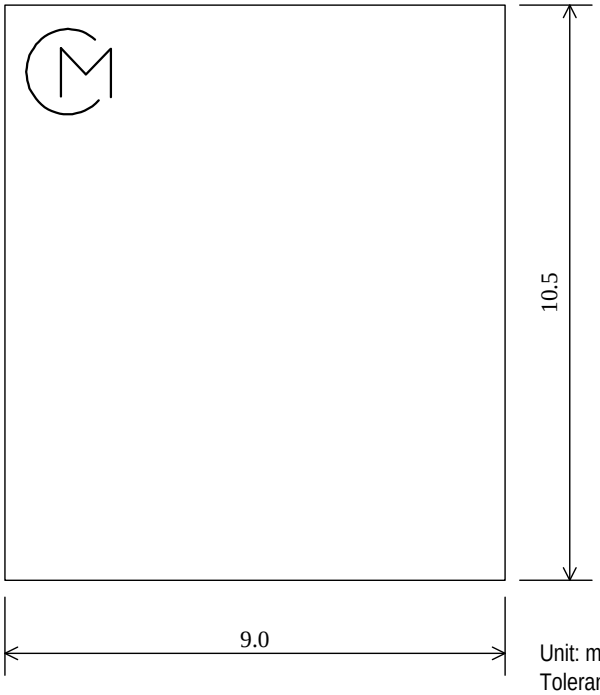
Transient response data at various conditions are showed in following table.
Minimum output capacitance can serve less than 3% x Vout of deviation for 20A load change(1A/us).

Vout(V)	Vin(V)	Total Cout(uF)	Voltage Deviation(mV)
			20-40A Load Step (1A/us)
0.7	12	1320	21
1			30
1.2			30

MECHANICAL SPECIFICATIONS

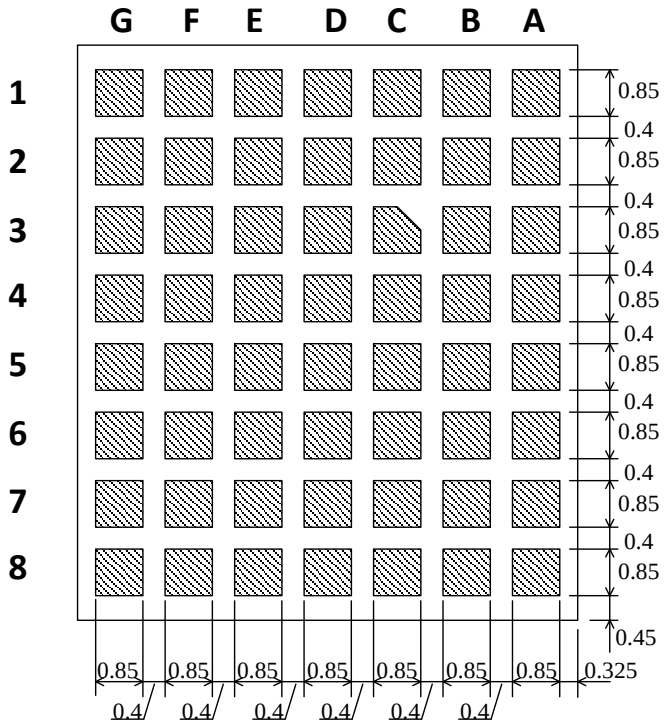
Dimension and Pin Assignment of each 1 module

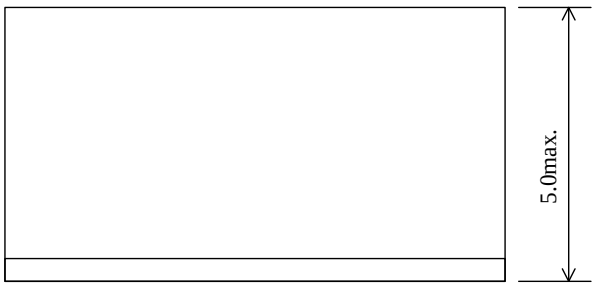
< Top View >



Unit: mm
Tolerances
± 0.15mm

< Bottom View >





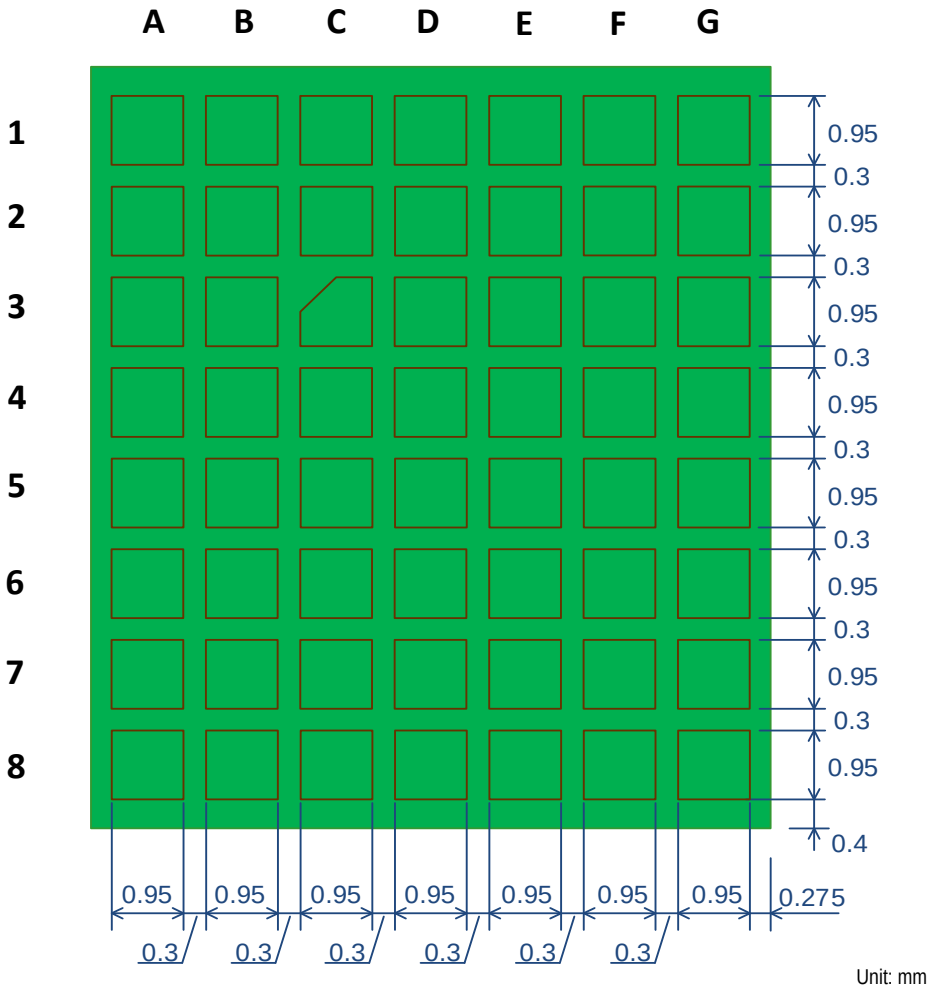
< Side View >

Pin Assignment			
Pin No.	Name	Pin No.	Name
A1	CLK	D7,D8	Vout
A2	DATA	E1,E2	Vin
A3	ALERT	E3-E8	GND
A4	ON/OFF	F1,F2	Vin
A5	PWGOOD	F3-F8	GND
A6	PASS	G1	VCC
A7	TAKE	G2	-Sense
A8	Vout	G3	Trim
B1-B6	GND	G4	+Sense
B7,B8	Vout	G5	ISUM
C1-C6	GND	G6	ADDR
C7,C8	Vout	G7	No Connection
D1,D2	Vin	G8	SET
D3-D6	GND		

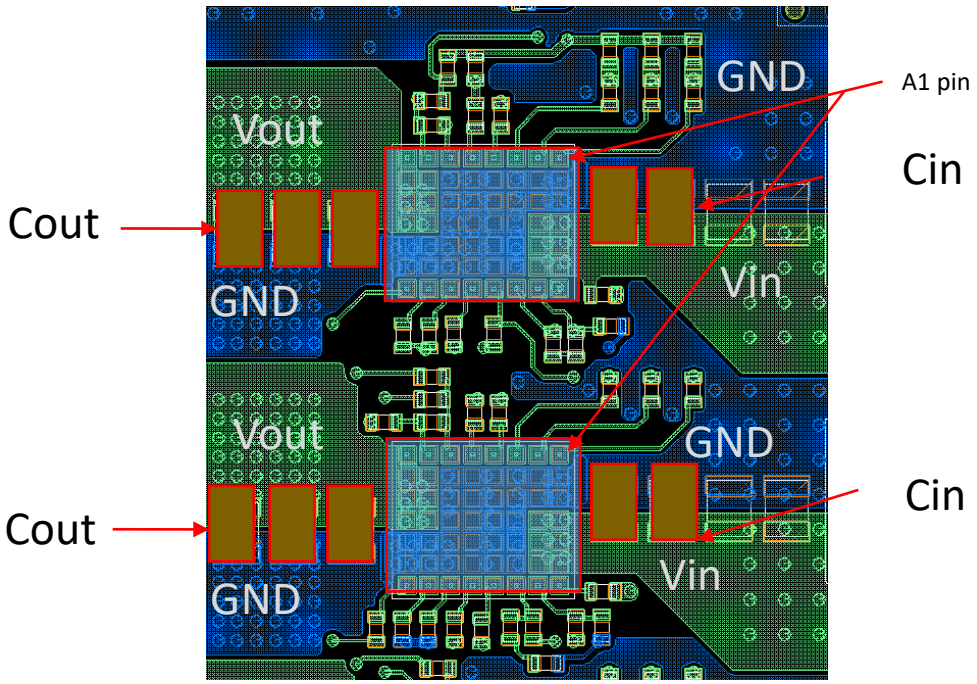
Pin Function & Descriptions

INPUT/OUTPUT Pins Functions & Descriptions		
Pin No.	Name	Function & Description
A1	CLK	PMBus™ Clock.
A2	DATA	PMBus™ data.
A3	ALERT	PMBus™ alert pin. ALT is active low. A pull-up resistor connected to 3.3V is required if the ALT function is needed.
A4	ON/OFF	PMBus™ control pin. ON/OFF is a digital input that turns the converter on or off with proper ON_OFF_CONFIG (02h) configuration. Drive ON/OFF high to turn on the regulator. Drive ON/OFF low to turn off the regulator. Do not float ON/OFF.
A5	PWGOOD	Power good output. The output of PWGOOD is an open-drain signal. PWGOOD requires a pull-up resistor connected to a DC voltage to indicate high if the output voltage is higher than 90% of the nominal voltage. There is a PWGOOD delay from low to high. PWGOOD must be pulled high to ensure proper operation.
A6	PASS	Passes RUN signals to the next phase.
A7	TAKE	Receives RUN signals from the previous phase. TAKE is used for master detection during the initial power-up. For the master phase, TAKE must be pulled high through a resistor. For the slave phase, TAKE is connected to the PASS of the previous phase.
A8, B7, B8, C7, C8, D7, D8	Vout	Power output voltage.
B1-B6, C1-C6, D3-D6, E3-E8, F3-F8	GND	Power Ground.
D1, D2, E1, E2, F1, F2	Input Voltage	Power input voltage.
G1	VCC	Internal 3.3V LDO output. VCC powers the analog and digital control circuits. This VCC pin does not accept external voltage bias. Connect the VCC pins of each phase together.
G2	-Sense	Output voltage sense negative return. Vout -Sense is tied to the GND sense point of the load directly. Connect Vout -Sense to GND closely if the remote sense is not used.
G3	Trim	Output voltage setting pin. The divider resistor must be locate between GND to set output voltage correctly. Tie the Trim pins of each phase together.
G4	+Sense	Output voltage sense positive return. Connect Vout +Sense of master phase to the output voltage sense of the load directly. Left Vout +Sense pin of slave phase open. Connect Vout +Sense to Vout closely if the remote sense is not used.
G5	ISUM	Current sense output. Tie the ISUM pins of each phase together for current sharing. Insert ceramic capacitor between ISUM and GND.
G6	ADDR	PMBus™ slave address-setting pin. Connect a resistor from ADDR to GND to set the address of this device.
G7	No Connection	Keep floating.
G8	SET	PWM signal. Tie the SET pins of each phase together.

Recommended Board Land Pattern for 1 module (Top View)

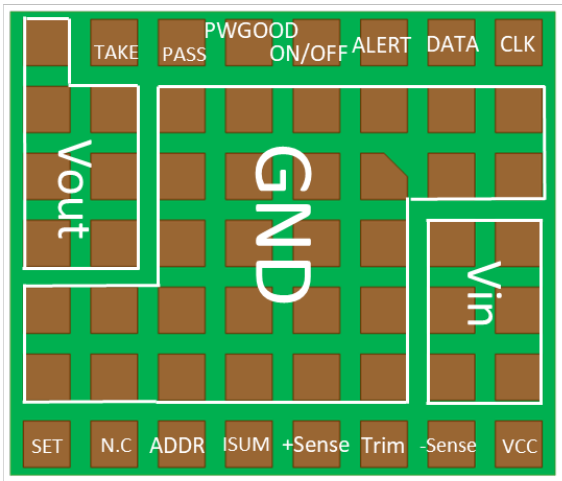


Example of Pattern Layout (Top View)



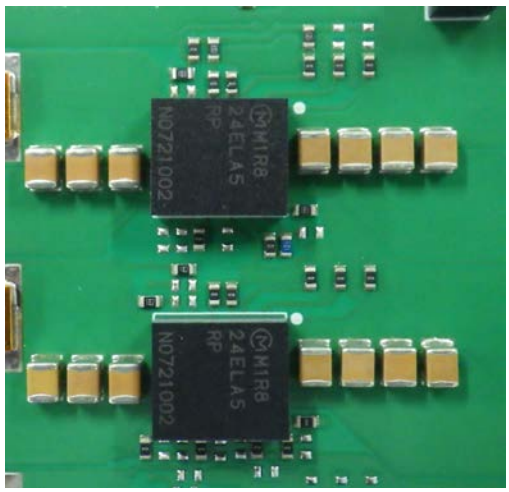
Pin Layout

TOP VIEW



Picture

TOP VIEW



Layout & Operation Guidelines

(1) When using parallel operation, the temperature of some parts may increase in one of the module because there are some differences in the operating conditions between the first and second module. For this reason, please check the temperature of the modules in your application.

(2) It is necessary to install Cin and Cout (ceramic capacitor) for each module.

(3) To avoid Over Current Protection, Over Voltage Protection and Under Voltage protection malfunction, please set same values of Vout of each module and place each module isometric alignment for Vin and Load.
And it is recommended that the load may be started after PWGOOD signal “High” because of the same reason.

(4) Parallel operation can be available among same parts No. only.

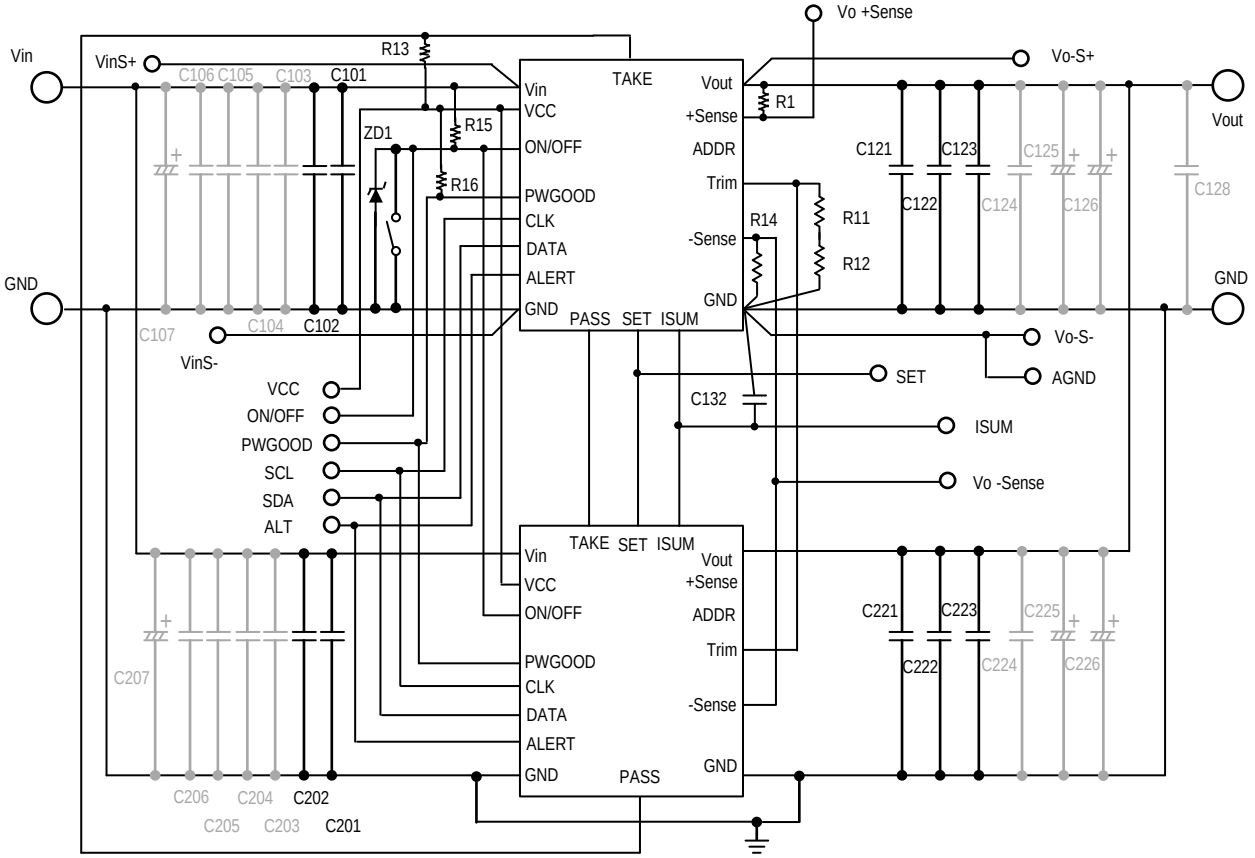
(5) There is no redundancy function.

(6) Please shield well from any noise, especially Trim, ISUM, +Sense, and -Sense lines to avoid any unexpected interference during operation.
- It is recommended to make capacitor land and set about 1000pF between ISUM-GND to avoid unexpected oscillation.
- +Sense and -Sense lines strongly recommended short.

(7) Be careful for drawing of TAKE, PASS and SET lines, because these lines have large amplitude of voltage pulse wave form.

(8) Please set same PMBus™ address about 2 modules.

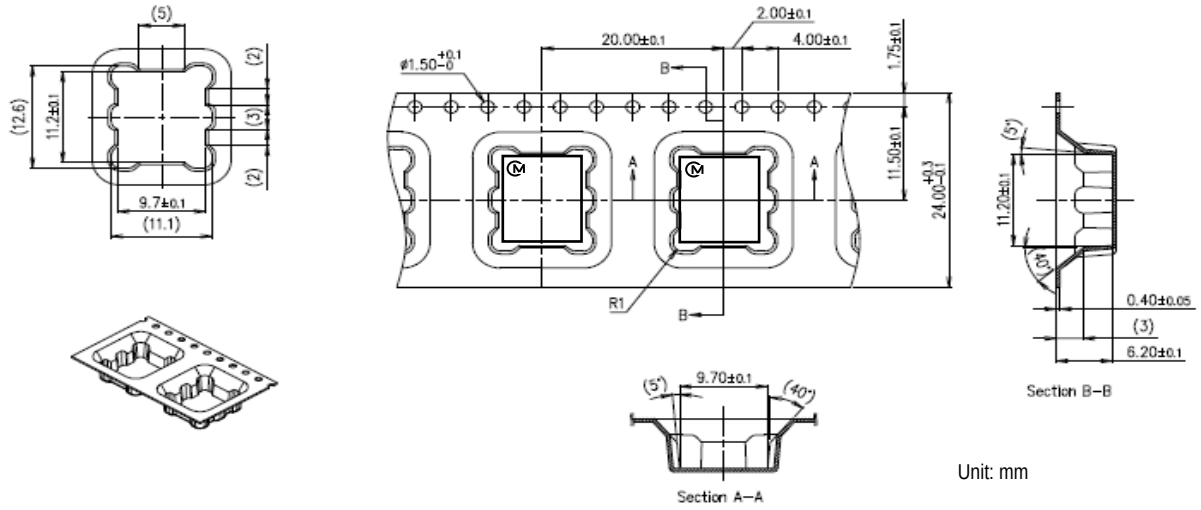
Application Circuit & BOM list (Evaluation Board Default)



Reference No.	Part Name
C101,C102 C201,C202	22uF/25V GRM32ER71E226KE15 (Murata)
C121, C122, C123,C221, C222,C223	220uF/4V GRM32EC80G227ME05 (Murata)
C132	1000pF/50V GRM1552C1H102JA01 (Murata)
R1,R14	1005, Chip resister, 0 ohm
R11, R12	1005, Chip resister
R13,R15,R16	1005, Chip resister, 10 kohm
ZD1	EDZV3.3B (Rohm)
The others	No Mount

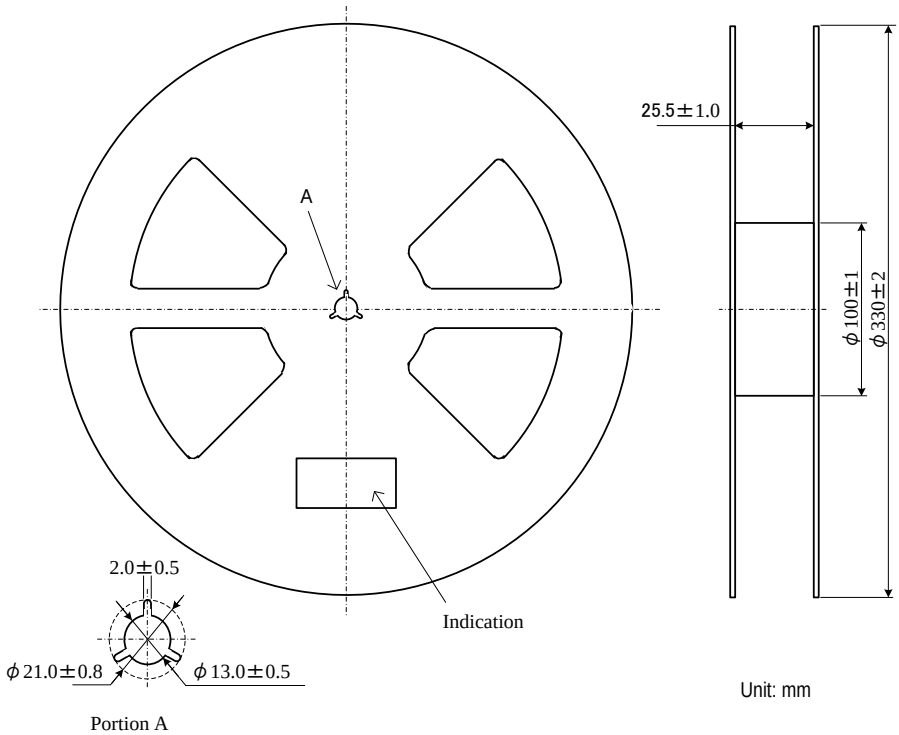
TAPE AND REEL INFORMATION

Tape Dimension



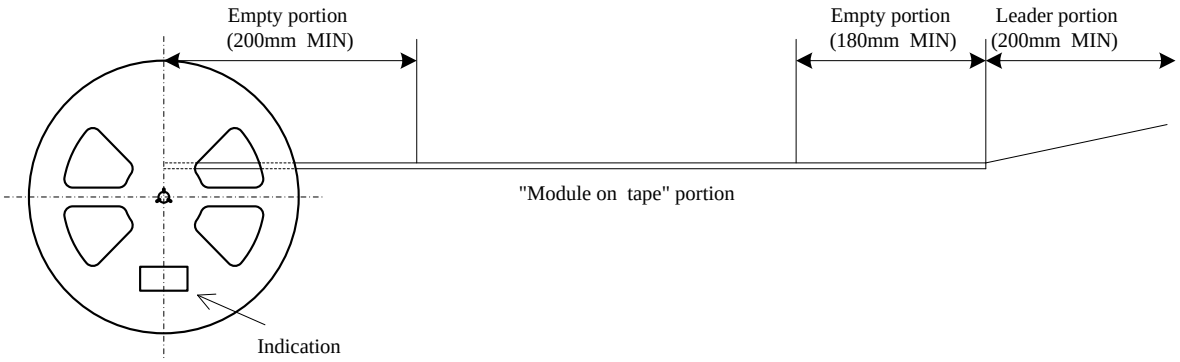
Unit: mm

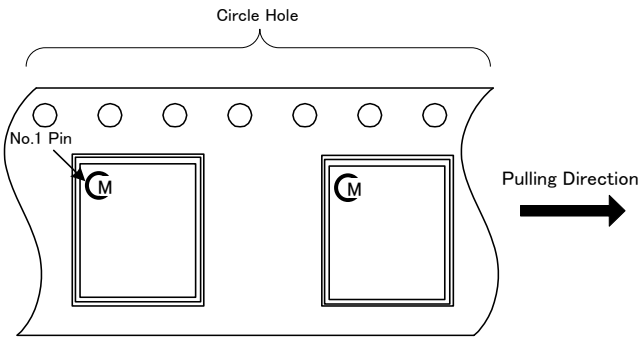
Reel Dimension



Unit: mm

TAPE SPECIFICATIONS





Note

1. The adhesive strength of the protective tape must be within 0.1-1.3N.
2. Each reel contains the quantities such as the table below.
3. Each reel set in moisture-proof packaging because of MSL 3.
4. No vacant pocket in “Module on tape” section.
5. The reel is labeled with Murata part number and quantity.
6. The color of reel is not specified.

Part Number	Qty(pcs)
MYMGM1R824ELA5RP	400
MYMGM1R824ELA5RPD	100

TECHNICAL NOTES

Multi Phase Operation

This module is a fully integrated, synchronous, step-down, switch-mode converter that uses multi-phase operation.

CAUTION

Two modules are always required for operation.

Master/Slave Auto-Detection

One master phase is needed for operation. To be configured as a master phase, the TAKE pin of the phase must be pulled high to a voltage source. The PASS/TAKE pins of all phases are connected in a daisy chain configuration. The PASS pin of the last phase is connected back to the TAKE pin of the first (master) phase. After power-up, the master phase is determined, and the other is slave phase.

Operation (Master)

The master phase has the following functions:

- Accept both write and read commands through the PMBus™ from the system.
- Generate the SET signals.
- Manage start-up, shut-off, and all protections.
- Monitor fault alerts from the slave phases through the PG pin.
- Start the first on pulse.
- Start the on pulse when receiving RUN and SET signals.
- Determine the on pulse width of its own phase based on the per-phase and total current.
- Carry on the PASS/TAKE signal.

Operation (Slave)

The slave phase has the following functions:

- Accept write commands through the PMBus™ from the system.
- Take the SET signal from the master.
- Send an OV/UV/OT alert to the master through PWGood
- Start the on pulse when receiving RUN and SET signals.
- Determine the on pulse width of its own phase based on the per-phase and total current.
- Carry on the PASS/TAKE signal.

Input Fuse

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Fuses should also be used when there is the possibility of sustained input voltage reversal which is not current limited. For greatest safety, we recommend a fast blow fuse installed in the ungrounded input supply line. The installer must observe all relevant safety standards and regulations. For safety agency approvals, install the converter in compliance with the end-user safety standard.

Input Under-Voltage Shutdown and Start-Up Threshold

Under normal start-up conditions, converter will not begin to regulate properly until the ramping-up input voltage exceeds and remains at the Start-Up Threshold Voltage (see Specifications). Once operating, converter will not turn off until the input voltage drops below the Under-Voltage Shutdown Limit. Subsequent restart will not occur until the input voltage rises again above the Start-Up Threshold. This built-in hysteresis prevents any unstable on/off operation at a single input voltage.

Users should be aware however of input sources near the Under-Voltage Shutdown whose voltage decays as input current is consumed (such as capacitor inputs), the converter shuts off and then restarts as the external capacitor recharges. Such situations could oscillate. To prevent this, make sure the operating input voltage is well above the UV Shutdown voltage at all times.

Start-Up Time

Assuming that the output current is set at the rated maximum, the Vin to Vout Start-Up Time (see Specifications) is the time interval between the point when the ramping input voltage crosses the Start-Up Threshold and the fully loaded regulated output voltage enters and remains within its specified accuracy band. Actual measured times will vary with input source impedance, external input capacitance, input voltage slew rate and final value of the input voltage as it appears at the converter.

This converter includes a soft start circuit to moderate the duty cycle of its PWM controller at power up, thereby limiting the input inrush current. The ON/OFF Remote Control interval from On command to Vout regulated assumes that the converter already has its input voltage stabilized above the Start-Up Threshold before the On command. The interval is measured from the On command until the output enters and remains within its specified accuracy band. The specification assumes that the output is fully loaded at maximum rated current. Similar conditions apply to the On to Vout regulated specification such as external load capacitance and soft start circuitry.

Recommended Input Filtering

The user must assure that the input source has low AC impedance to provide dynamic stability and that the input supply has little or no inductive content, including long distributed wiring to a remote power supply. For best performance, we recommend installing a low-ESR capacitor immediately adjacent to the converter's input terminals.

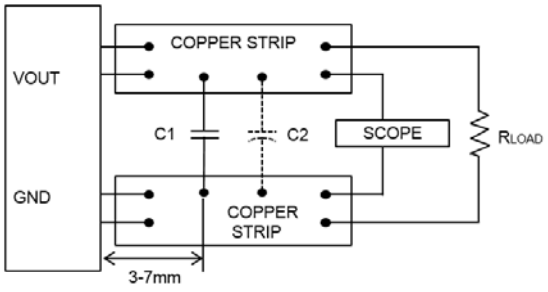
The capacitor should be a ceramic type such as the Murata GRM32 series and a electrolytic type such as Panasonic OS-CON series. Initial suggested capacitor values are 22uF x 2 ceramic type and 1000uF x 1 electrolytic type per 1 module, rated at twice the expected maximum input voltage. Make sure that the input terminals do not go below the under voltage shutdown voltage at all times. More input bulk capacitance may be added in parallel (either electrolytic or tantalum) if needed.

Recommended Output Filtering

The converter will achieve its rated output ripple and noise with additional external capacitor. The user may install more external output capacitance reduce the ripple even further or for improved dynamic response. Again, use low-ESR ceramic (Murata GRM32 series). Initial values of 220uF x 3 ceramic type may be tried per 1 module, either single or multiple capacitors in parallel. Mount these close to the converter. Measure the output ripple under your load conditions. Use only as much capacitance as required to achieve your ripple and noise objectives. Excessive capacitance can make step load recovery sluggish or possibly introduce instability. Do not exceed the maximum rated output capacitance listed in the specifications.

Output Noise

This converter is tested and specified for output noise using designated external output components, circuits and layout as shown in the figures below. In the figure below, the two copper strips simulate real-world printed circuit impedances between the power supply and its load. In order to minimize circuit errors and standardize tests between units, scope measurements should be made using BNC connectors or the probe ground should not exceed one half inch and soldered directly to the test circuit.



C1=220uF x 3 x2 CERAMIC
C2=OPEN
Figure : Measuring Output Ripple and Noise

Minimum Output Loading Requirements

This converter regulates within specification and are stable under no load to full load conditions. Operation under no load might however slightly increase output ripple and noise.

Thermal Shutdown

To prevent many over temperature problems and damage, this converter include thermal shutdown circuitry. If environmental conditions cause the temperature of the converter's to rise above the Operating Temperature Range up to the shutdown temperature, an on-board electronic temperature sensor will shut down the unit. When the temperature decreases below the turn-on threshold, the converter will automatically restart.

CAUTION: If you operate too close to the thermal limits, the converter may shut down suddenly without warning. Be sure to thoroughly you're your application to avoid unplanned thermal shutdown.

Temperature Derating Curves

The graph in this data sheet illustrates typical operation under a variety of conditions. The derating curves show the maximum continuous ambient air temperature. Note that these are AVERAGE measurements.

Note that the temperatures are of the ambient airflow, not the converter itself which is obviously running at higher temperature than the outside air. Also note that very low flow rates (below about 25 LFM) are similar to "natural convection," that is, not using fan-forced airflow. Murata makes Characterization measurements in a closed cycle wind tunnel with calibrated airflow. We use both thermocouples and an infrared camera system to observe thermal performance.

CAUTION: This graph is collected at slightly above Sea Level altitude. Be sure to reduce the derating for higher density altitude.

Output Current Limiting

Current limiting inception is defined as the point at which full power falls below the rated tolerance. See the Performance/Functional Specifications. Note particularly that the output current may briefly rise above its rated value in normal operation as long as the average output power is not exceeded. This enhances reliability and continued operation of your application. If the output current is too high, the converter will enter the short circuit condition.

Output Short Circuit Condition

When a converter is in current-limit mode, the output voltage will drop as the output current demand increases. Following a time-out period, the converter will restart, causing the output voltage to begin ramping up to its appropriate value. If the short-circuit condition persists, another shutdown cycle will initiate. This rapid on/off cycling is called "hiccup mode". The hiccup cycling reduces the average output current, thereby preventing excessive internal temperatures and/or component damage. A short circuit can be tolerated indefinitely.

The "hiccup" system differs from older latching short circuit systems because you do not have to power down the converter to make it restart. The system will automatically restore operation as soon as the short circuit condition is removed.

Power Good (PWGOOD)

Please refer to the Connection Diagram on page 1 for PWGOOD connection.

The Product has a power good (PWGOOD) output. PWGOOD is the open drain of a MOSFET. Connect PWGOOD to Vin or another external voltage source less than 3.6V through a pull-up resistor (Typically 100kohm). After applying the input voltage, the module turns on so that PWGOOD is pulled to GND before the soft start is ready. After the TRIM voltage reaches the threshold set internally, PWGOOD is pulled high after a delay.

When the converter encounters any fault (e.g.: UV, OV, OT, UVLO, etc.), PWGOOD is latched low and cannot be pulled high again until a new soft start is initialized.
When the convertor is configured as the multi-phase operation, the PWGOOD pin is used for fault indication. Therefore, PWGOOD must be pulled high to ensure proper operation.
The slave fault detection feature is fixed enable.
If the input supply fails to power the product, PWGOOD is clamped low.

PMBus™ Alert (ALT#)

ALT# is active low. A pull-up resistor connected to 3.3V is required if the ALT# function is needed.
If any PMBus™ warnings appears, this terminal turn to High.
The CLEAR_FAULTS command is used to reset all stored warning and fault flags.
See, Clear Faults command and any Warning commands, if need.

UVP/OVP Function

This product monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes lower than 70% of the target voltage, after 1ms, the product turns OFF. The converter restarts after a hiccup delay (about 16ms). This function is enabled 1.5ms after the soft-start is completed.
When the feedback voltage becomes higher than 120% of the target voltage, the circuit operates sink-mode to decrease output voltage. If the output voltage reaches UV threshold, the device restarts after a hiccup delay. If the OV condition remains, the converter will not start until the OV condition is removed.

Remote ON/OFF Control

Please refer to the Connection Diagram on page 1 for ON/OFF connection.
This converter is enabled when the ON/OFF pin is pulled high with respect to GND. This device is disabled when the ON/OFF pin is grounded or brought to within a low voltage (see Specifications) with respect to GND.
The ON/OFF function and operation are also controlled by using PMBus™ command OPERATION (01h) and ON_OFF_CONFIG (02h) as below.
Dynamic control of the ON/OFF function should be able to sink appropriate signal current when brought low and withstand appropriate voltage when brought high. Be aware too that there is a finite time in milliseconds (see Specifications) between the time of ON/OFF Control activation and stable, regulated output. This time will vary slightly with output load type and current and input conditions.

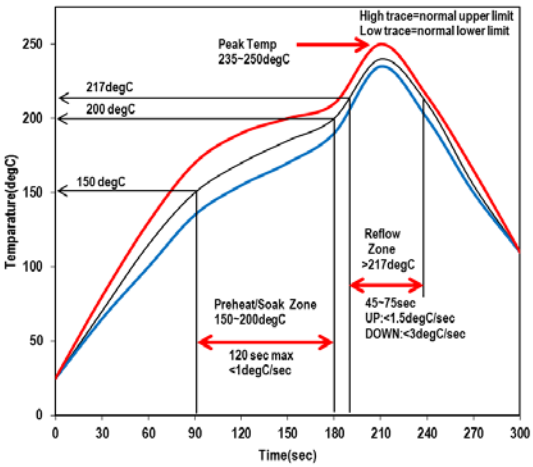
OUTPUT	OPERATION (01h) on/off bit	ON_OFF_CONFIG (02h)	ON/OFF Pin
ON	ignore	16h (Default)	H
OFF			L
ON	ON	1Ah	ignore
OFF	OFF		
ON	ON	1Eh	H
OFF	OFF		L
OFF	OFF		H
OFF	ON		L
OFF	ignore	12h	ignore
ON	ignore	0xh	ignore

Soldering Guidelines

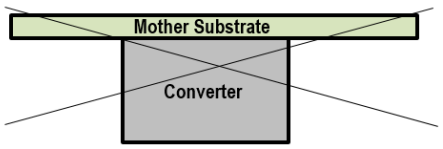
Murata recommends the specifications below when installing these converters. These specifications vary depending on the solder type. Exceeding these specifications may cause damage to the product. Your production environment may differ therefore please thoroughly review these guidelines with your process engineers.
This product can be reflowed once.

Reflow Solder Operations for surface-mount products	
For Sn/Ag/Cu based solders:	
Preheat Temperature	Less than 1degC per second
Time over Liquidus	45 to 75 seconds
Maximum Peak Temperature	250degC
Cooling Rate	Less than 3degC per second
For Sn/Pb based solders:	
Preheat Temperature	Less than 1degC per second
Time over Liquidus	60 to 75 seconds
Maximum Peak Temperature	235degC
Cooling Rate	Less than 3degC per second

Recommended Lead-free Solder Reflow Profile



CAUTION: Do not reflow the converter as follows, because the converter may fall from the substrate during reflowing.



Pb-free solder processes

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020D.
During reflow product must not exceed 250degC at any time.

Dry Pack Information

Products intended for Pb-free reflow soldering processes are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033.
(Handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices.)
Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the modules must be baked according to J-STD-033.

Output Voltage Adjustment

This product provides output voltage monitoring through the register of READ_VOUT (8Bh). In order to have correct output voltage setting and monitoring, the external voltage divider (RTrim) and the registers of VOUT_COMMAND (21h), VOUT_MARGIN_HIGH (25h), VOUT_MARGIN_LOW (26h), VOUT_SCALE_LOOP (29h) should be set correspondingly. The following shows how to set the output voltage.

1.Determin the Rtrim value using following formula.

Rtrim (kohm) = 6 /(Vout - 0.6)

Then, connect an external trim resistor (Rtrim) between the Trim pin and GND pin. The Rtrim resistor must be a 1/10W precision metal film type, ±0.5% accuracy or better with low temperature coefficient, ±100 ppm/degC.

2.Set the VOUT_COMMAND(21h) and the VOUT_SCALE_LOOP(29h) as follows.

VOUT_COMMAND : Target Voltage in hexadecimal
(Least Significant Bit is 0.002V)
VOUT_SCALE_LOOP: Set following value in hexadecimal
VOUT_SCALE_VALUE= 0.6/Target Vout
(Least Significant Bit is 0.001)

3.Set VOUT_MARGIN_HIGH (25h), VOUT_MARGIN_LOW (26h) as follows.

VOUT_MARGIN_HIGH (25h):Vout margin (high) voltage in hexadecimal.(Should be set in the range of 100~110% of target Vout)
VOUT_MARGIN_LOW (26h):Vout margin (low) voltage in hexadecimal.(Should be set in the range of 90~100% of target Vout)
(Least Significant Bit is 0.002V respectively)

The following table shows the RTrim and PMBus™ parameters at particular Vout for example.

		PMBus™ Command Parameters			
Output Voltage	Estimated Rtrim (kohm)	21h	29h	25h	26h
0.7V	30+30	0x015E (0.7V)	0x0359 (0.857)	0x0181 (0.77V)	0x013B (0.63V)
1.0V	15	0x01F4 (1.0V)	0x0258 (0.600)	0x0226 (1.1V)	0x01C2 (0.9V)
1.2V	10	0x0258 (1.2V)	0x01F4 (0.500)	0x0294 (1.32V)	0x021C (1.08V)

CAUTION

It's not recommended to change PMBus™ parameters when the power stage is enabled. Proper operation of the converter is not guaranteed to do so.
Rtrim is needed only for one tied Trim line.
(Do not need to locate Rtrim for each converter.)
Do not exceed the specified limits of the output voltage or the converter's maximum power rating when applying these resistors.

Output Voltage Remote Sense

This function is capable to compensate up the voltage drop between the output and input of load. The sense range depend on the maximum voltage allowing on the Vout Pin. The sense trace should be short as possible and shielded by GND line or else to reduce noise susceptibility. The sense line length is recommended within 10cm for output voltage stability. If the remote sense is not needed, +/-Sense Pins should be connected to Vout PIN and GND respectively.

Output Capacitive Load

Users should only consider adding capacitance to reduce switching noise and/or to handle spike current load steps. Install only enough capacitance to achieve noise objectives. Excess external capacitance may cause regulation problems, degraded transient response and possible oscillation or instability.

PMBus™ Serial Interface Description

The Power Management Bus (PMBus™) is an open-standard, power-management protocol that defines a means of communication with power conversion and other devices.
The PMBus™ is a two-wire, bidirectional, serial interface, consisting of a data line (DATA) and a clock line (CLK). The lines are externally pulled to a bus voltage when they are idle. When connecting to the lines, a master device generates the CLK signal and device address and arranges the communication sequence. This is based on the I^2C operation principles. This product is a PMBus™ slave which supports both the standard mode (100kHz) and fast modes (400kHz). The PMBus™ interface adds flexibility to the power supply solution.

Multi Address

To support multiple devices used on the same PMBus™, use the ADDR pin or PMBus™ command D3h to program the different address for each device.
To determine the PMBus™ address through PMBus™, please refer to table about PMBus™ command D3h that is described following page.
To determine by external resistor, connect a resistor between ADDR pin and GND to set the ADDR voltage. The internal ADC converts the pin voltage to set the PMBus™ address. Maximum 16 addresses can be set by ADDR pin. Following table shows the PMBus™ address for different resistor values from ADDR pin to GND.

CAUTION

For multi-phase configurations, the slave phase should be set the same address as the master. The slave phases can only accept write commands and cannot accept read commands from the PMBus™ master. The master phase can accept both write and read commands from the PMBus™ master.

R ADDR-GND(kohm)	ADDRESS
4.99	30h
15	31h
24.9	32h
34.8	33h
45.3	34h
54.9	35h
64.9	36h
75	37h
84.5	38h
95.3	39h
105	3Ah
115	3Bh
124	3Ch
133	3Dh
147	3Eh
154	3Fh

Start and Stop Conditions

The start and stop are signaled by the master device which signifies the beginning and the end of the PMBus™ transfer.
The start condition is defined as the DATA signal transitioning from high to low while the CLK is high.
The STOP condition is defined as the DATA signal transitioning from low to high while the CLK is high as shown in Figure A.
The master then generates the CLK clocks, and transmits the device address and the read/write direction bit r/w on the DATA line. Data is transferred in 8 bit bytes by DATA line. Each byte of data is to be followed by an acknowledge bit.

PMBus™ Update Sequence

This product requires a start condition, a valid PMBus™ address, a register address byte, and a data byte for a single data update.
The product acknowledges the receipt of each byte by pulling the DATA line low during the high period of a single clock pulse. A valid PMBus™ address selects the product.
The product performs an update on the falling edge of the LSB byte.

Protocol Usage

All PMBus™ transactions on device are done using defined bus protocols. The following protocols are implemented:

- Send byte with PEC
- Receive byte with PEC
- Write byte with PEC
- Read byte with PEC
- Write word with PEC
- Read word with PEC
- Block read with PEC

PMBus™ Bus message format

In the tables in Figure B, unshaded cells indicate that the bus host is actively driving the bus; shaded cells indicate that the device is driving the bus.
S = start condition
Sr = repeated start condition
P = stop condition
R = read bit
W= write bit
A = acknowledge bit (0)
A#= acknowledge bit (1)
"A" represents the ACK (acknowledge) bit. The ACK bit is typically active low (Logic 0) if the transmitted byte is successfully received by a device. However, when the receiving device is the bus master, the acknowledge bit for the last byte read is a logic 1, indicated by A#.

Packet Error Checking (PEC)

The device PMBus™ interface supports the use of the packet error checking (PEC) byte. The PEC byte is transmitted by the device during a read transaction or sent by the bus host to the device during a write transaction.
The PEC byte is used by the bus host or the device to detect errors during a bus transaction, depending on whether the transaction is a read or a write. If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read if necessary. If the device determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (does not execute it) and sets a status flag. Within a group command, the host can choose to send or not send a PEC byte as part of the message to the device.

PMBus™ Alert Response Address (ARA)

The PMBus™ alert response address (ARA) is a special address that can be used by the bus host to locate any devices that need to talk to it. A host typically uses a hardware interrupt pin to monitor the PMBus™ ALERT pins of a number of devices. When a host interruption occurs, the host issues a message on the bus using the PMBus™ receive byte or receive byte with PEC protocol. The special address used by the host is 0x0C.
Any devices that have a PMBus™ alert signal return their own 7-bit address as the seven MSBs of the data byte. The LSB value is not used and can be either 1 or 0.
The host reads the device address from the received data byte and proceeds to handle the alert condition. More than one devices may have an active PMBus™ alert signal and attempt to communicate with the host. In this case, the device with the lowest address dominates the bus and succeeds in transmitting its address to the host. The device that succeeds disables its PMBus™ alert signal. If the host sees that the PMBus™ alert signal is still low, it continues to read addresses until all devices that need to talk to it have successfully transmitted their addresses.

Data and Numerical Formats

The device uses a direct format internally to represent real-world values such as voltage, current, power and temperature. All numbers with no suffix in this document are decimals unless explicitly designated otherwise. Numbers in binary format are indicated by the prefix "n'b", where n is the binary count. For example, 5'b01010 indicates a 5-bit binary data, and the data is 01010. The suffix "h" indicates a hexadecimal format, which is generally used for the register address number in this document. The symbol "0x" indicates a hexadecimal format, which is used for the value in the register. For example, 0xA3 is a 1-byte number whose hexadecimal value is A3.

PMBus™ Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several types of the data transmission faults as listed below:
- Sending too few data
- Reading too few data
- Sending too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

PMBus™ Reporting and Status Monitoring

The device supports real-time monitoring for some operation parameters and status with PMBus™ interface. They are listed on following table.

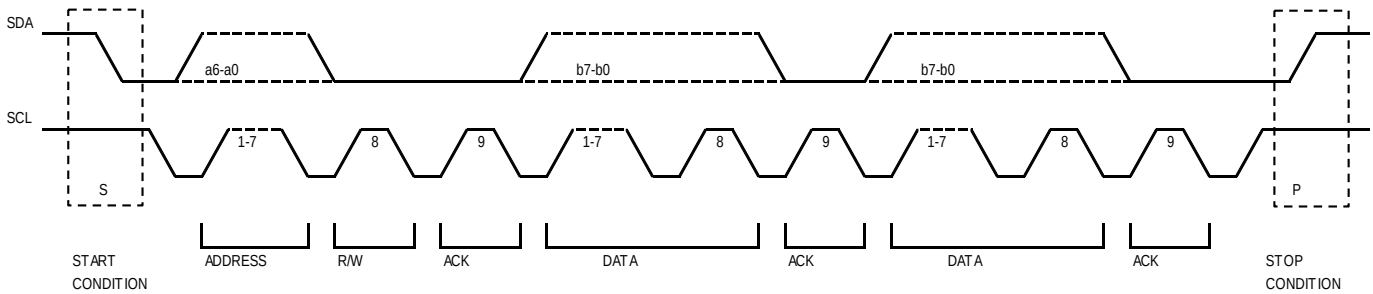


Figure. A

Communication Pattern

a) Send Byte and Send Byte with PEC

1	7	1	1	8	1	1
S	Slave Address	Wr	A	Data Byte	A	P

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Data Byte	A	PEC	A	P

b) Receive Byte and Receive Byte with PEC

1	7	1	1	8	1	1
S	Slave Address	Rd	A	Data Byte	A	P

1	7	1	1	8	1	8	1	1
S	Slave Address	Rd	A	Data Byte	A	PEC	A	P

c) Write Byte and Write Byte with PEC

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	P

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	PEC	A	P

d) Write Word and Write Word with PEC

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

1	7	1	1	8	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	PEC	A	P

e) Read Byte and Read Byte with PEC

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	A	P

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	A	PEC	A	P

f) Read Word and Read Word with PEC

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte Low	A

8	1	1
Data Byte High	A	P

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte Low	A

8	1	8	1	1
Data Byte High	A	PEC	A	P

g) Block Read with PEC

1	7	1	1	8	1	1	7	1	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Sr	Slave Address	Rd	A	Byte Count =N	A	···

8	1	8	1		8	1	1
Data Byte 1	A	Data Byte 2	A	···	Data Byte N	A	P

1	7	1	1	8	1	1	7	1	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Sr	Slave Address	Rd	A	Byte Count =N	A	···

8	1	8	1		8	1	8	1	1
Data Byte 1	A	Data Byte 2	A	···	Data Byte N	A	PEC	A	P

Figure B

PMBus™ Register Map

The following table shows the PMbus™ command list

Code	Command Name	Type	Default Value (HEX)	Default Value (actual)
01h	OPERATION	R/W w/PEC	0x80	-
02h	ON_OFF_CONFIG	R/W w/PEC	0x16	-
03h	CLEAR_FAULTS	Send byte w/PEC	-	-
10h	WRITE_PROTECT	R/W w/PEC	0x00	-
19h	CAPABILITY	R w/PEC	0xB0	-
20h	VOUT_MODE	R w/PEC	0x40	-
21h	VOUT_COMMAND	R/W w/PEC	0x015E	0.7V
25h	VOUT_MARGIN_HIGH	R/W w/PEC	0x0181	0.77V
26h	VOUT_MARGIN_LOW	R/W w/PEC	0x013B	0.63V
29h	VOUT_SCALE_LOOP	R/W w/PEC	0x0359	0.857
35h	VIN_ON	R/W w/PEC	0x001D	7.25V
36h	VIN_OFF	R/W w/PEC	0x001B	6.75V
4Ah	IOUT_OC_WARN_LIMIT	R/W w/PEC	0x0190	93.8A (Total)
51h	OT_WARN_LIMIT	R/W w/PEC	0x0091	145degC
57h	VIN_OV_WARN_LIMIT	R/W w/PEC	0x0020	16V
58h	VIN_UV_WARN_LIMIT	R/W w/PEC	0x001C	7V
60h	TON_DELAY	R/W w/PEC	0x0000	0ms
61h	TON_RISE	R/W w/PEC	0x0001	2ms
78h	STATUS_BYTE	R/W w/PEC	-	-
79h	STATUS_WORD	R/W w/PEC	-	-
7Ah	STATUS_VOUT	R/W w/PEC	-	-
7Bh	STATUS_IOUT	R/W w/PEC	-	-
7Ch	STATUS_INPUT	R/W w/PEC	-	-
7Dh	STATUS_TEMPERATURE	R/W w/PEC	-	-
7Eh	STATUS_CML	R/W w/PEC	-	-
88h	READ_VIN	R w/PEC	-	-
8Bh	READ_VOUT	R w/PEC	-	-
8Ch	READ_IOUT	R w/PEC	-	-
8Dh	READ_TEMPERATURE_1	R w/PEC	-	-
98h	PMBUS_REVISION	R/W w/PEC	-	-
D1h	MFR_CTRL_VOUT	R/W w/PEC	0x00	-
D3h	MFR_ADDR_PMBUS	R/W w/PEC	0x00	-

OPERATION (01h)

OPERATION is a paged register. The OPERATION command is used to turn the converter output on or off in conjunction with the input from the CTRL pin. OPERATION is also used to set the output voltage to the upper or lower margin voltages. The unit remains in the commanded operating mode until a subsequent OPERATION command or a change in the state of the CTRL pin instructs the converter to change to another mode. This OPERATION command is also used to re-enable the converter after a fault-triggered shutdown. Writing an off command followed by an on command clears all faults. Writing only an on command after a fault-triggered shutdown will not clear the fault registers.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r	r
Function							x	x
Default Value	1	0	0	0	0	0	x	x

Bit[7:6]	Bit[5:4]	Bit[3:2]	Bit[1:0]	On/Off	Margin state	01h
00	xx	xx	xx	Immediate off	N/A	0x00
01	xx	xx	xx	Immediate off	N/A	0x60
10	00	xx	xx	on	off	0x80
10	01	01	xx	on	Margin low (ignore fault)	0x94
10	01	10	xx	on	Margin low (act on fault)	0x98
10	10	01	xx	on	Margin high (ignore fault)	0xA4
10	10	10	xx	on	Margin high (act on fault)	0xA8

ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of the CTRL input and the PMBus™ commands to turn the converter on and off. This includes how the converter responds when an input voltage is applied.

Command	ON_OFF_CONFIG							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r
Function	x	x	x	on	op	ctrl	x	delay
Default Value	0	0	0	1	0	1	1	0

on

This on bit sets the default to either operate whenever the input voltage is present or for the on/off to be controlled by CTRL and PMBus™ commands.

Bit[4] Value	Meaning
0	Converter powers up whenever the input voltage is present regardless of state of the CTRL pin
1	Converter does not power up until commanded by the CTRL pin and OPERATION command (as programmed in bits[3:0])

op

This op bit controls how the converter responds to the OPERATION commends.

Bit[3] Value	Meaning
0	Converter ignores the “on” bit in the OPERATION command from PMBus™
1	Converter responds the “on” bit in the OPERATION command from PMBus™

ctrl

This ctrl bit controls how the converter responds to the CTRL pin.

Bit[2] Value	Meaning
0	Converter ignores the CTRL pin (on/off controlled only by the OPERATION command)
1	Converter requires the CTRL pin to be asserted to power up. Depending on bit[3] op bit, the OPERATION command may also be required to instruct the converter to power up.

delay

This delay bit sets the turn-off action when the converter is commanded off through the PMBus™. This bit is read only and cannot be modified by the end user.

Bit[0] Value	Meaning
0	TOFF_DELAY, TOFF_FALL

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to reset all stored warning and fault flags. If a fault or warning condition still remains when the CLEAR_FAULTS command is issued, the ALT# signal may not be cleared or is reasserted almost immediately. Issuing a CLEAR_FAULTS command will not cause the converter to restart in the event of a fault turn-off. The converter restart must be done by issuing an OPERATION command after the fault condition is cleared. This command uses the PMBus™ to send the byte protocol.

WRITE PROTECT (10h)

The WRITE_PROTECT command is used to control writes to the converter. This command provides protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to the converter's configuration or operation.
All the supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Bit[7:0] Value								Meaning
0	0	0	0	0	0	0	0	Enable writes to all commands
0	0	1	0	0	0	0	0	Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG and VOUT_COMMAND commands
0	1	0	0	0	0	0	0	Disable all writes except to the WRITE_PROTECT, OPERATION and PAGE commands
1	0	0	0	0	0	0	0	Disable all writes except to the WRITE_PROTECT command

CAPABILITY (19h)

The CAPABILITY command returns information about the PMBus™ functions supported by this product. This command is read with the PMBus™ read byte protocol.

Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	PEC	MAX bus speed		Alert	x	x	x	x
Default Value	1	0	1	1	0	0	0	0

Bit[6:5] Value		Meaning
0	0	Maximum supported bus speed is 100KHz
1	0	Maximum supported bus speed is 400KHz
1	1	Reserved
0	1	Not supported

VOUT_MODE (20h)

The VOUT_MODE command is used to command and read the output voltage. The three most significant bits are used to determine the data format (only direct format is supported in this product), and the rest of five bits represent the exponent used in the output voltage Read/Write commands. The default value of 20h is 0x40.

VOUT_COMMAND (21h)

The VOUT_COMMAND sets the output voltage of this product. The VOUT_COMMAND and VOUT_SCALE_LOOP together determine the feedback reference voltage: VOUT_COMMAND x VOUT_SCALE_LOOP. In the section of "Output Voltage Setting" on page 28, it shows the details about how to set the output voltage.
The value is unsigned and 1LSB = 2mV. The default value of 21h is 0x015E, which is 0.7V.

Command	VOUT_COMMAND															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				2mV/LSB											
Default Value	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1	0

VOUT_MARGIN_HIGH (25h)

Command	VOUT_MARGIN_HIGH															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				2mV/LSB											
Default Value	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1

The value is unsigned and 1LSB = 2mV. The default value is 0.77V. So the default value of 25h is 0x0181.

VOUT_MARGIN_LOW (26h)

Command	VOUT_MARGIN_LOW															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				2mV/LSB											
Default Value	0	0	0	0	0	0	0	1	0	0	1	1	1	0	1	1

The value is unsigned and 1LSB = 2mV. The default value is 0.63V. So the default value of 26h is 0x013B.

VOUT_SCALE_LOOP (29h)

VOUT_SCALE_LOOP sets the feedback resistor divider ratio and is equal to VFB/VOUT. Regardless of whether an external or internal feedback resistor divider is used, VOUT_SCALE_LOOP should match the actual feedback resistor divider used.

Command	VOUT_SCALE_LOOP															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				0.001/LSB											
Default Value	0	0	0	0	0	0	1	1	0	1	0	1	1	0	0	1

The value is unsigned and 1LSB =0.001. The default value is 0.857. So the default value of 29h is 0x0359.

VIN_ON (35h)

The VIN_ON command sets the value of the input voltage, (in V), at which the converter should start to run if all other required power-up conditions are met. The VIN_ON value can be set between 7.5V and 15V with 0.25V increment. The VIN_ON value should be always set higher than VIN_OFF value with enough margin, so that there will be no bouncing between VIN_ON and VIN_OFF during power conversion.

Command	VIN_ON															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				250mV/LSB											
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

The value is unsigned and 1LSB=250mV. The default value is 7.25V. So the default value of 35h is 0x001D.

VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage, (in V), at which the converter, once operation has started, should stop power conversion. The VIN_OFF value can be set between 7.25V and 14.75V with 0.25V increment. The VIN_OFF value should be always set lower than VIN_ON value with enough margin, so that there is no bouncing between VIN_OFF and VIN_ON during power conversion.

Command	VIN_OFF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				250mV/LSB											
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1

The value is unsigned and 1 LSB=250mV. The default value is 6.75V. So the default value of 36h is 0x001B.

IOUT_OC_WARN_LIMIT (4Ah)

The IOUT_OC_WARN_LIMIT command is used to configure or read the threshold for the over-current warning detection. If the sensed current exceeds this value, the OC warning flags are set in the STATUS BYTE (78h), STATUS_WORD (79h) respectively, and the ALT# signal is asserted.

Command	IOUT_OC_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x															
Default Value	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

The value is unsigned and 1LSB=242mA. The default value is 0190h. The corresponding value of the total output current is about 96.8A.
Caution : This parameter should be set about total output current. (Not for each module)

OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT is used to configure or read the threshold for the over-temperature warning detection. If the sensed temperature exceeds this value, an over temperature warning is triggered, the OT warning flags are set in the STATUS BYTE(78h) and STATUS_WORD(79h) respectively, and the ALT# signal is asserted. The minimum temperature warning detection time should be smaller than 20ms.

Command	OT_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x								1degC/LSB							
Default Value	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1

The value is unsigned and 1LSB=1 degC. The default value is 0x0091h. The corresponding value is 145degC. The OT_WARN_LIMIT setting value should be lower than 155degC.

VIN_OV_WARN_LIMIT (57h)

The VIN_OV_WARN_LIMIT command is used to configure or read the threshold for the input-over-voltage warning detection. If the measured value of VIN rises above the value in this register, VIN OV warning flags are set in the respective registers, and the ALT# signal is asserted.

Command	VIN_OV_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				500mV/LSB											
Default Value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

The value is unsigned and 1LSB=500mV. The default value is 0x20. The corresponding value is 16V. The VIN_OV_WARN_LIMIT setting value should not be higher than 16V.

VIN_UV_WARN_LIMIT (58h)

The VIN_UV_WARN_LIMIT command is used to configure or read the threshold for the input-under-voltage warning detection. If the measured value of VIN falls below the value in this register, VIN UV warning flags are set in the respective registers, and the ALT# signal is asserted.

Command	VIN_UV_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x				250mV/LSB											
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0

The value is unsigned and 1LSB=250mV. The default value is 0x1C. The corresponding value is 7.0V. The VIN_UV_WARN_LIMIT setting value should be higher than 7.0V.

TON_DELAY (60h)

The TON_DELAY command sets the time, (in ms), from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise.

Command	TON_DELAY															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x					4ms/LSB										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The value is unsigned and 1LSB=4ms. The maximum value is 60h=0x0100 (1024ms). The default value is 0x0000 (0ms).

TON_RISE (61h)

The TON_RISE command sets the soft-start time, (in ms), from when the output starts to rise until the voltage has reached the regulation point.

Command	TON_RISE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

The only supported values are as follows:
3'b001: 2ms
3'b010: 4ms
3'b011: 8ms
3'b100 and up: 16ms.
The default value is 0x0001, i.e. 2ms for soft-start time.

STATUS BYTE (78h)

The STATUS_BYTE command returns the value of a number of flags indicating the state of this product. Accesses to this command should use the read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

Bits	Name	Behavior	Default	Description
[7]	Reserved		0	Always read as 0.
[6]	OFF	Live	0	0:product enabled 1:product disabled, this can be from: the OC fault, the OT fault, the bad MOSFET fault, the UV/OV fault, or the OPERATION command turning off
[5]	VOUT_OV		0	An output overvoltage fault has occurred.
[4]	Iout_OC_FAULT	Latched	0	0:no over current fault detected 1:over current fault detected
[3]	VIN_UV		0	Not supported, always read as 0
[2]	OT_FAULT_WARN	Live	0	0:no over temperature warning or fault detected 1:over temperature warning or fault detected
[1]	CUMM_ERROR	Latched	0	0:no communication error detected 1:communication error detected
[0]	NONE_OF_THE_ABOVE	Live	0	0:no other fault or warning 1:fault or warning not listed in bits [7:1] has occurred.

STATUS WORD (79h)

The STATUS_WORD returns the value of a number of flags indicating the state of this product. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

Bits	Name	Behavior	Default	Description
[15]	VOUT_STATUS	Live	0	0:no output fault or warning 1:output fault or warning
[14]	IOUT_STATUS	Live	0	0:no Iout fault 1:Iout falut
[13]	VIN_STATUS	Live	0	0:no Vin Fault 1:Vin Fault, at the period when Vin starts up, the initial flag is 1 before Vin pass UVLO threshold. The flag cleared once Vin passes UVLO.
[12]	MFR_STATUS		0	Always read as 0
[11]	POWETR_GOOD#	Live	0	0:power good signal is asserted 1:power good signal is not asserted
[10]	Reserved		0	Always read as 0
[9]	Reserved		0	Always read as 0
[8]	UNKNOWN	Latched	0	0:no any other fault has occurred 1:a fault type not specified in bits [15:1] of the STATUS_WORD has been detected.
Low Byte	STATUS_BYTE			STATUS BYTE is the low byte of the STATUS_WORD.

STATUS_ VOUT (7Ah)

The STATUS_VOUT command returns one data byte with contents as follows:

Bits	Name	Behavior	Default	Description
[7]	VOUT_OV_FAULT	Live	0	0:no output OV fault 1:output OV fault
[6]	Reserved	Latched	0	Always read as 0
[5]	Reserved	Latched	0	Always read as 0
[4]	VOUT_UV_FAULT	Live	0	0:no output UV fault 1:output UV fault
[3]	VOUT_MAX_MIN	Live	0	0:no VOUT_MAX, VOUT_MIN warning 1:an attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX command or lower than the limit allowed by the VOUT_MIN command.
[2]	Reserved		0	Always read as 0
[1]	Reserved		0	Always read as 0
[0]	UNKNOWN	Latched	0	0:no any other fault has occurred 1:a fault type not specified in bits [15:1] of the STATUS_WORD has been detected.

STATUS_ IOUT (7Bh)

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	IOUT_OC	IOUT_OC & VOUT_UV	IOUT_OC_WARNING	x	x	x	x	x
Default Value	0	0	0	0	0	0	0	0

STATUS_ INPUT (7Ch)

The STATUS_INPUT returns the value of flags indicating input voltage status of this product. To clear bits in this register, the underlying fault or warning should be removed and a CLEAR_FAULTS command issued.

Bits	Name	Behavior	Default	Description
[7]	VIN_OV_FAULT	R, Latched	0	0:no Over voltage detected on the OV pin 1:over voltage detected on the OV pin
[6]	VIN_OV_WARN	R, Latched	0	0:over voltage condition on VIN has not occurred 1:over voltage condition on VIN has occurred
[5]	VIN_UV_WARN	R, Latched	0	0:under voltage condition on VIN has not occurred 1:under voltage condition on VIN has occurred
[4:0]	Reserved		0	Always read as 00000

STATUS_ TEMPERATURE (7Dh)

The STATUS_TEMPERATURE returns the value of flags indicating the VIN overvoltage or under-voltage of this product. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

Bits	Name	Behavior	Default	Description
[7]	OT_FAULT	R, Latched	0	1:over-temperature Warning has occurred
[6]	OT_WARNING	R, Latched	0	1:over-temperature Warning has occurred
[5:0]	Reserved	R	0	Always read as 0

STATUS_ CML (7Eh)

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	Invalid unsupported command	Invalid / unsupported data	x	Memory fault detected	x	x	Other fault	Memory busy
Default Value	0	0	0	0	0	0	0	0

READ_VIN (88h)

The READ_VIN command returns the 10-bit measured value of the input voltage.

Command	READ_VIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x						25mV/LSB									
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_VOUT (8Bh)

The READ_VOUT command returns the 10-bit measured value of the output voltage.

Command	READ_VOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x						1.25mV/LSB									
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_IOUT (8Ch)

The READ_IOUT command returns the 10-bit measured value of the total output current. This value is also used to compare with the IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT, and then affects the STATUS_IOUT.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x						62.5mA/LSB									
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_TEMPERATURE_1 (8Dh)

The READ_TEMPERATURE_1 command returns the internal sensed temperature. This value is also used internally for the Over Temperature Fault and Warning detection. This data has a range of -255degC to +255degC.

Command	READ_TEMPERATURE_1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x						Sign	1degC/LSB								
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_TEMPERATURE_1 is a 2-byte, twos complement integer. The bit9 is the sign bit. Below table shows the relationship between direct value and real word value.

Sing	Direct Value	Real Value degC
0	0 0000 0000	0
0	0 0000 0001	1
0	1 1111 1111	+511
1	0 0000 0000	-511
1	1 1111 1111	-1

PMBUS_REVISION (98h)

The PMBUS_REVISION command returns the protocol revision we used. Accesses to this command should use the read byte protocol. Bits [7:4] indicate the PMBus™ revision of specification Part I to which the device is compliant. Bits [3:0] indicate the revision of specification Part II to which the device is compliant.

Command	PMBus™ REVISION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Default Value	0	0	1	1	0	0	1	1

Bits [7:4] always reads as 4'b0011, specification PMBus™ Part I Revision 1.3.
Bits [3:0] always reads as 4'b0011, specification PMBus™ Part II Revision 1.3.

MFR_CTRL_VOUT (D1h)

The MFR_CTRL_VOUT command is used to adjust the output voltage behaviors of this product.

Bits	Name	Behavior	Default	Description
[7]	Reserved	Live	0	N/A
[6]	Vo Discharge	Live	0	1:output voltage discharge at CTRL low. 0:no active output voltage discharge.
[5:0]	Reserved	Live	0	N/A

Bit[6] (Vo discharge): Enable or disable active output voltage discharge when this product is commanded off through CTRL or the OPERATION command.

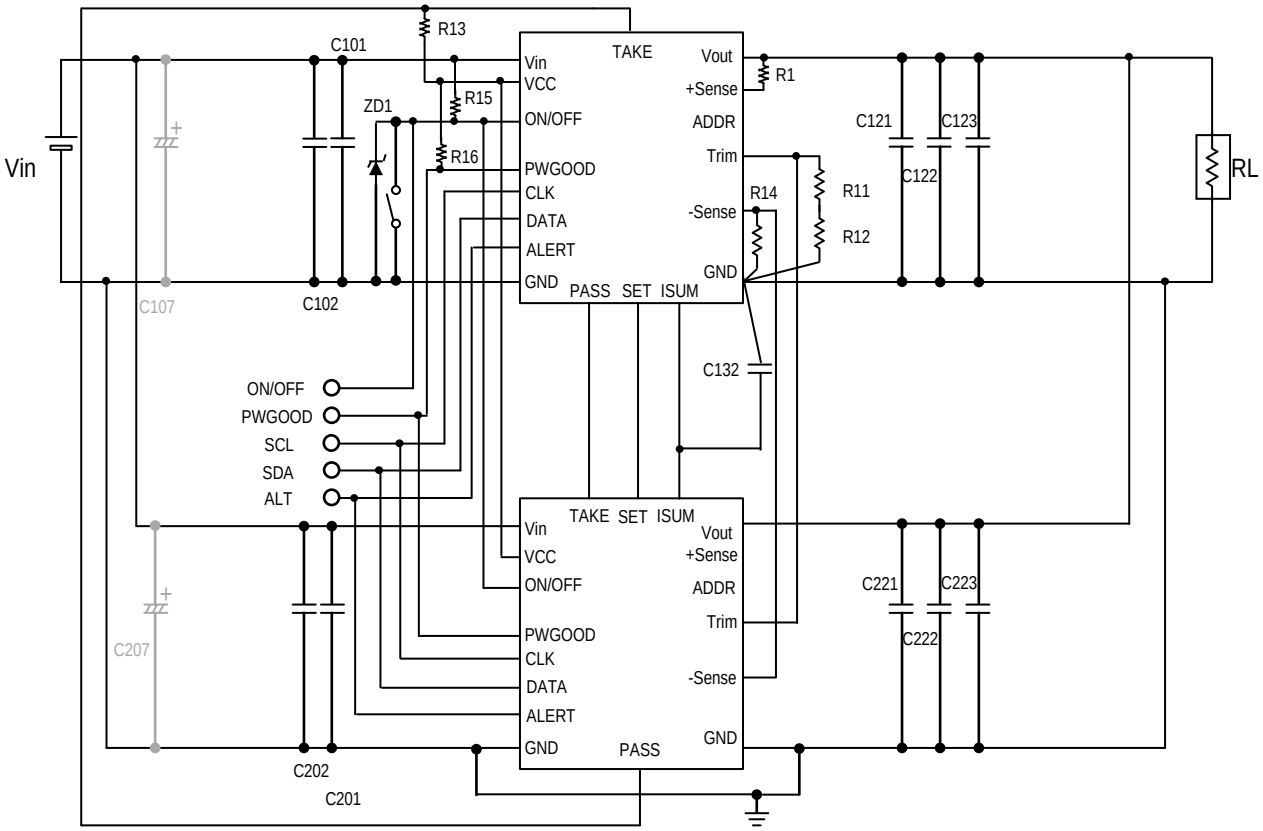
MFR_ADDR_PMBUS (D3h)

Command	MFR_ADDR_PMBus							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Enable	ADDR						
Default Value	0	0	0	0	0	0	0	0

Bit[7] (enable bit):
1: the address is decided by MFR_ADDR_PMBUS [6:0].
0: the address is decided by ADDR pin.
The default value of D3h is 0x00.

APPENDIX

Test Circuit



*1: If there is a non-negligible parasitic impedance between the power supply and the converter, such as during evaluation, the optional input capacitor “C107 and C207” may be required to reduce the impedance. The recommended optional capacitor is an example. Please consider the optimum value for the case. This capacitor is usually an aluminum electrolytic type. It isn't necessary to place the capacitor near the input terminal of the converter.
This would typically be aluminum electrolytic type and does not need to be close to the input terminals of converter.
*2: Do not connect any additional components between the Trim pin and Vout or between the Trim and Sense pins. Use only the specified connections.

APPENDIX

Test Circuit

Reference No.	Part Name
C101,C102 C201,C202	22uF/25V GRM32ER71E226KE15 (Murata)
C121, C122, C123,C221, C222,C223	220uF/4V GRM32EC80G227ME05 (Murata)
C132	1000pF/50V GRM1552C1H102JA01 (Murata)
R1,R14	1005, Chip resister, 0 ohm
R11, R12	1005, Chip resister
R13,R14,R15	1005, Chip resister, 10 kohm
ZD1	EDZV3.3B (Rohm)
C107,C207	No mount or Electrolytic Capacitor (if necessary)

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Refer to: https://power.murata.com/en/requirements

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