DSA1101/21/05/25

Low-Jitter Precision CMOS Oscillator for Automotive

Features

- Automotive AEC-Q100 Qualified
- Two Rise/Fall Time Options for EMI Reduction
- Low RMS Phase Jitter: <1 ps (typ.)
- High Stability: ±20 ppm, ±25 ppm, ±50 ppm
- Wide Temperature Range:
  - Automotive Grade 1: –40°C to +125°C
  - Automotive Grade 2: –40°C to +105°C
  - Automotive Grade 3: –40°C to +85°C
- High Supply Noise Rejection: –50 dBc
- Wide Freq. Range: 2.3 MHz to 170 MHz
- Small Industry Standard Footprints
  - 2.5 mm x 2.0 mm VDFN
  - 3.2 mm x 2.5 mm VDFN and Wettable Flank
  - 5.0 mm x 3.2 mm CDFN
- Excellent Shock and Vibration Immunity
  - Qualified to MIL-STD-883
- High Reliability
  - 20x Better MTF than Quartz Oscillators
- Low Current Consumption
- Supply Range of 2.25V to 3.63V
- Standby and Output Enable Function
- Lead-Free and RoHS Compliant

Applications

- Automotive Infotainment
- Automotive ADAS
- Automotive Camera Module
- Automotive LIDAR and RADAR

Benefits

- Replace High Temperature Crystals and Quartz Oscillators

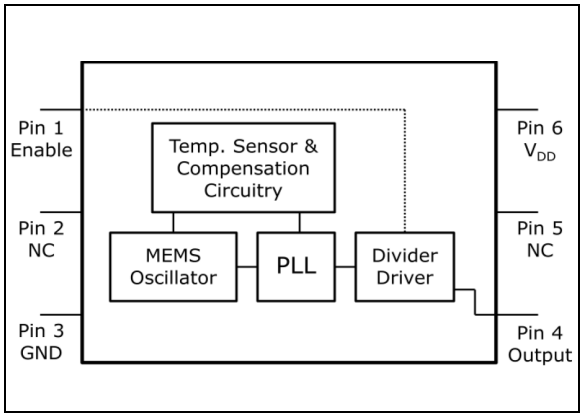
General Description

The DSA1101 and DSA1121 series of high performance oscillators utilize a proven silicon MEMS technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the need for quartz or SAW technology, MEMS oscillators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

DSA1101 has a standby feature that allows it to completely power-down when EN pin is pulled low. For DSA1121, only the outputs are disabled when EN is low. Both oscillators are available in industry standard packages, including the small 2.5 mm x 2.0 mm, and are “drop-in” replacements for standard 4-pin and 6-pin CMOS quartz crystal oscillators.

The DSA1105/25 is functionally equivalent to the DSA1101/21, but it has lower drive strength for EMI reduction.

Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage, V_{IN} .....–0.3V to V_{DD} +0.3V
Supply Voltage .....–0.3V to + 4.0V
ESD Protection On All Pins .....4000V HBM, 1500V CDM (max.)

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

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ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	V_{DD}	2.25	—	3.63	V	—
Supply Current	I_{DD}	—	—	0.095	mA	DSA1101/05, EN pin low. Output is disabled and device is in standby
		—	20	22		DSA1121/25, EN pin low, output is disabled
		—	21	35		EN pin high, output is enabled C_L = 15 pF, F_O = 100 MHz
Frequency Stability (Including frequency variations due to initial tolerance, temp. and power supply voltage)	Δf	—	—	±20	ppm	All temp ranges
		—	—	±25		
		—	—	±50		
Aging	Δf	—	—	±5	ppm	1 year @ 25°C
Startup Time (Note 2)	t_{SU}	—	—	5	ms	T = 25°C
Input Logic Levels						
Input Logic High	V_{IH}	0.75 x V_{DD}	—	—	V	—
Input Logic Low	V_{IL}	—	—	0.1 x V_{DD}	V	—
Output Disable Time (Note 3)	t_{DS}	—	—	5	ns	—
Output Enable Time	t_{EN}	—	—	5	ms	DSA1101/05
				20	ns	DSA1121/25
Enable Pull-Up Resistor (Note 4)	—	—	40	—	kΩ	Internally pulled-up
CMOS Output						
Output Logic Level High	V_{OH}	0.9 x V_{DD}	—	—	V	I = ±6 mA (DSA1101/21), I = ±1.6 mA (DSA1105/25)
Output Logic Level Low	V_{OL}	—	—	0.1 x V_{DD}	V	
Output Transition Rise Time	t_R	—	1.1	2	ns	DSA1101/21, 20% to 80%, C_L = 15 pF
		—	4	5		DSA1105/25, 20% to 80%, C_L = 15 pF
Output Transition Fall Time	t_F	—	1.3	2	ns	DSA1101/21, 20% to 80%, C_L = 15 pF
		—	4.7	6		DSA1105/25, 20% to 80%, C_L = 15 pF
Frequency	f_O	2.3	—	170	MHz	C_L = 15 pF and –40°C to +85°C
		3.3	—	170		C_L = 15 pF, –40°C to +105°C and –40°C to +125°C
Output Duty Cycle	SYM	45	—	55	%	—
Period Jitter	J_{PER}	—	3	—	ps_{RMS}	F_{OUT} = 125 MHz
Integrated Phase Noise	J_{PH}	—	0.3	—	ps_{RMS}	200 kHz to 20 MHz @ 125 MHz
		—	0.38	—		100 kHz to 20 MHz @ 125 MHz
		—	1.7	2		12 kHz to 20 MHz @ 125 MHz

Note 1: Pin 6 V_{DD} should be filtered with 0.1 µF capacitor.

2: t_{SU} is time to 100 ppm of output frequency after V_{DD} is applied and outputs are enabled.

3: Output Waveform and Test Circuit figures define the parameters.

4: Output is enabled if pad is floated or not connected.

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TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range (T)	T_A	–40	—	+85	°C	Ordering Option I
	T_A	–40	—	+105	°C	Ordering Option L
	T_A	–40	—	+125	°C	Ordering Option A
Junction Operating Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_A	–40	—	+150	°C	—
Soldering Temperature Range	T_S	—	—	+260	°C	Soldering, 40s

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: DSA1101/21/05/25 PIN FUNCTION TABLE

Pin Number 5x3.2	Pin Number 3.2x2.5	Pin Number 2x2.5	Pin Name	Description
1	1	1	EN	Enable.
2	2	2	NC	Do not connect.
3	3	3	GND	Ground.
4	4	4	OUT	Output.
5	5	5	NC	Do not connect.
6	6	6	VDD	Supply voltage.

TABLE 2-2: OUTPUT ENABLE MODES

EN Pin	DSA1101/05	DSA1121/25
High	Output Active	Output Active
NC	Output Active	Output Active
Low	Standby	Output Disabled

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3.0 NOMINAL PERFORMANCE CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

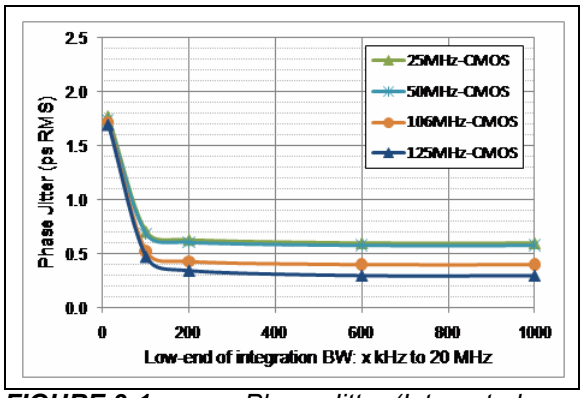

FIGURE 3-1: *Phase Jitter (Integrated Phase Noise).*

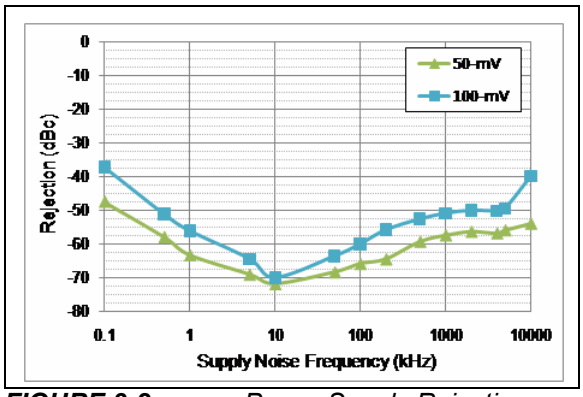

FIGURE 3-2: *Power Supply Rejection Ratio.*

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4.0 OUTPUT WAVEFORM

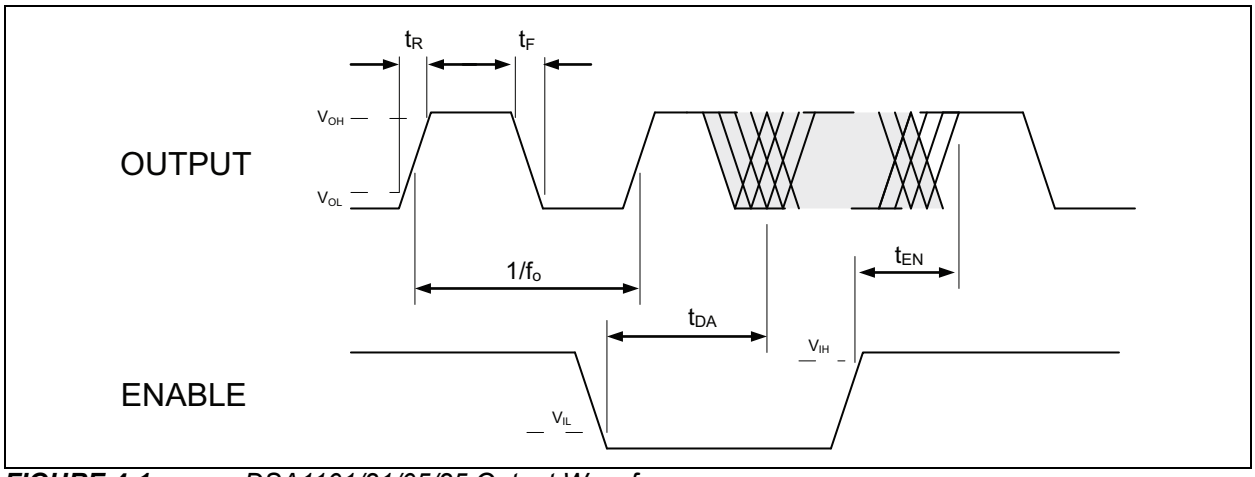

FIGURE 4-1: *DSA1101/21/05/25 Output Waveform.*

5.0 TYPICAL TERMINATION SCHEME

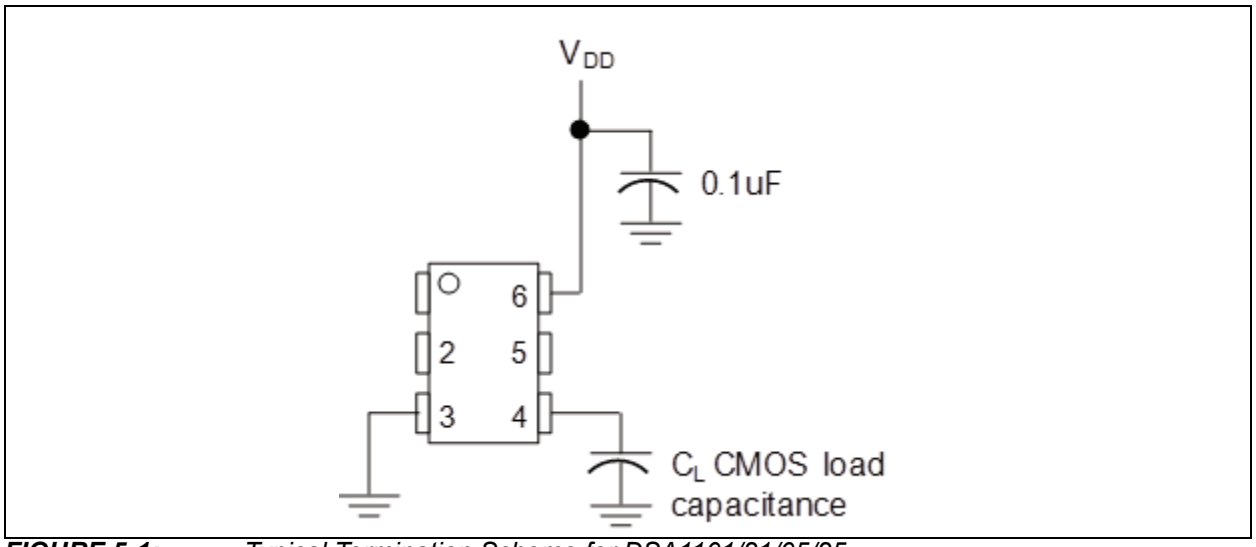

FIGURE 5-1: *Typical Termination Scheme for DSA1101/21/05/25.*

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6.0 BOARD LAYOUT (RECOMMENDED)

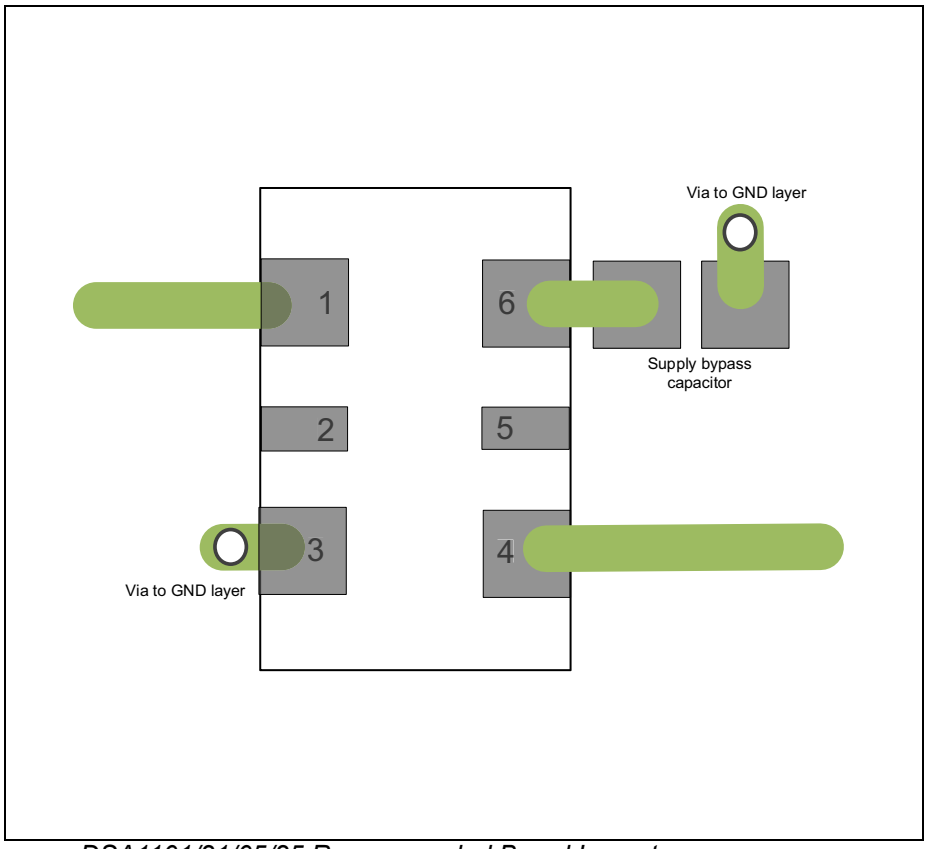

FIGURE 6-1: *DSA1101/21/05/25 Recommended Board Layout.*

7.0 SOLDER REFLOW PROFILE

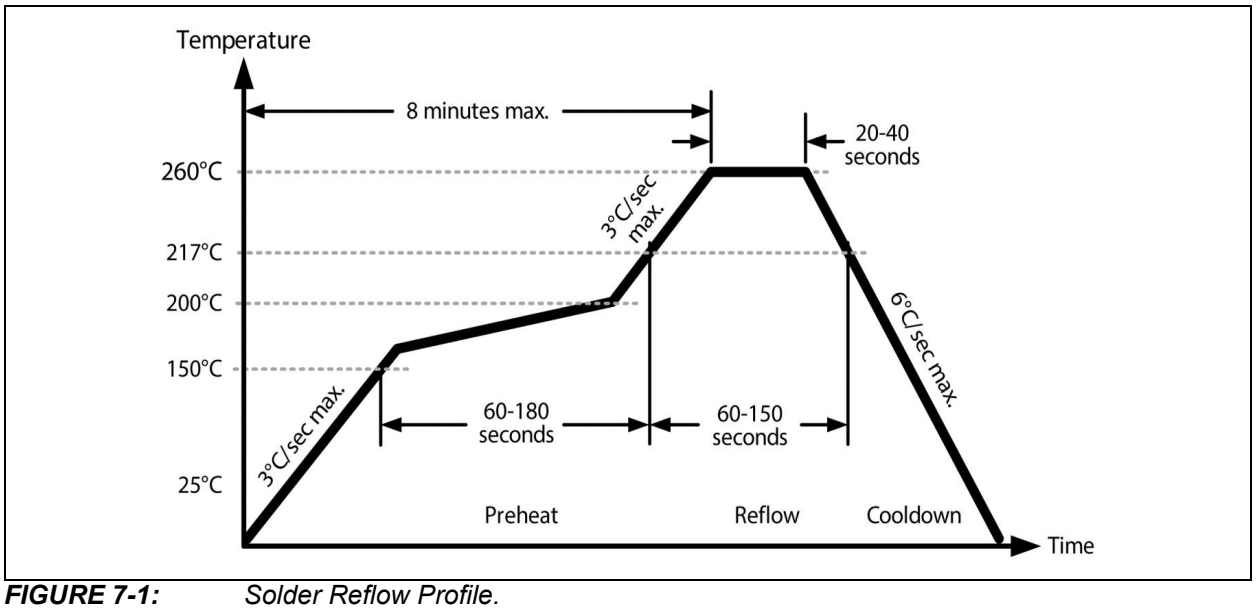

FIGURE 7-1: *Solder Reflow Profile.*

TABLE 7-1: SOLDER REFLOW

MSL 1 @ 260°C Refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp.)	3°C/sec. max.
Preheat Time 150°C to 200°C	60 to 180 sec.
Time Maintained above 217°C	60 to 150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20 to 40 sec.
Ramp-Down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

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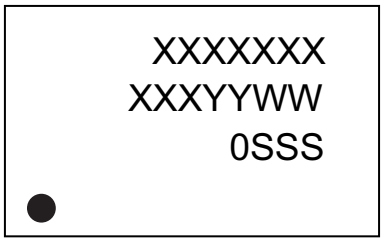
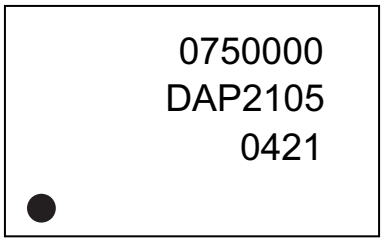
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

6-Pin CDFN/VDFN*



Example

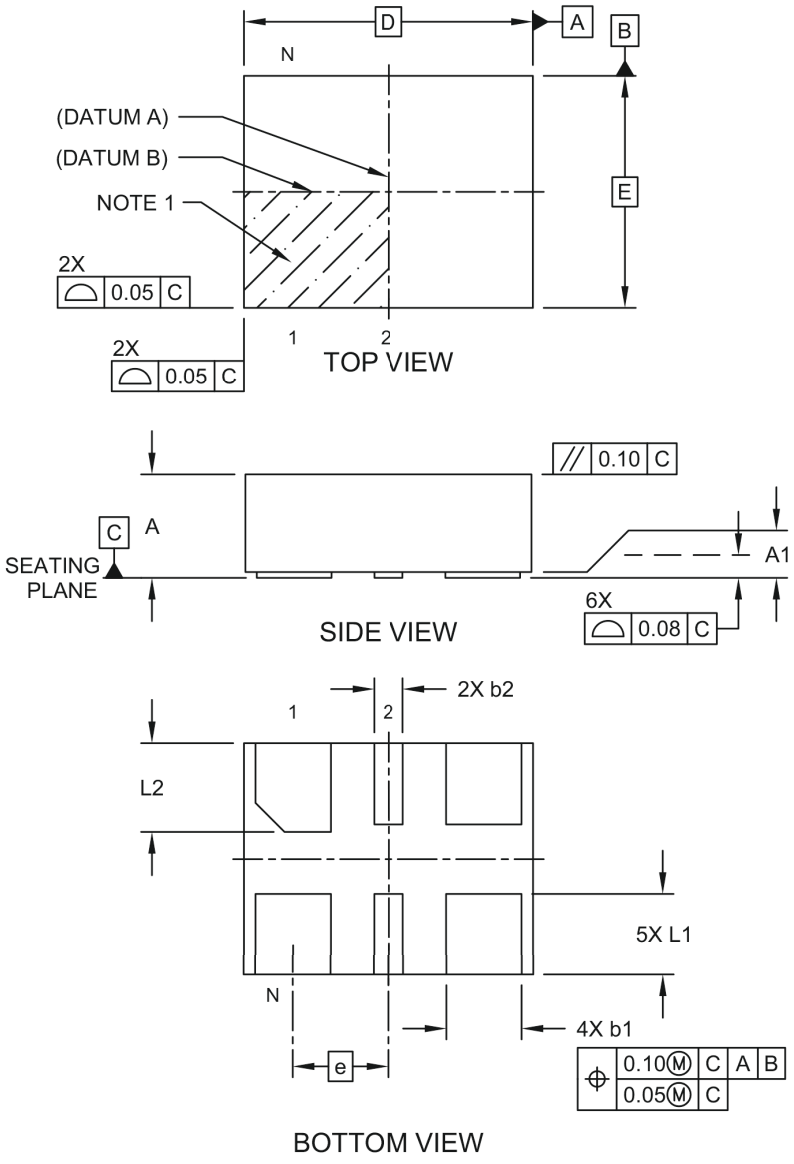


Legend:	XX...X	Product code, customer-specific information, or frequency in MHz without printed decimal point
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	SSS	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.
		Underbar (_) and/or Overbar (¯) symbol may not be to scale.

6-Lead VDFN 2.5 mm x 2.0 mm Package Outline and Recommended Land Pattern

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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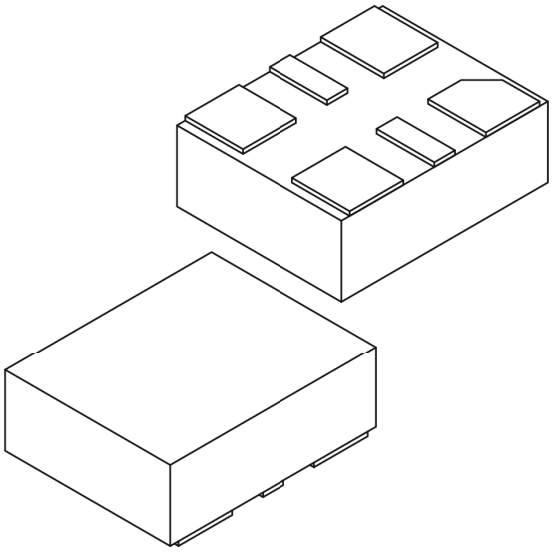
6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		0.825 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D		2.50 BSC	
Overall Width	E		2.00 BSC	
Terminal Width	b1	0.60	0.65	0.70
Terminal Width	b2	0.20	0.25	0.30
Terminal Length	L1	0.60	0.70	0.80
Terminal Length	L2	0.665	0.765	0.865

Notes:

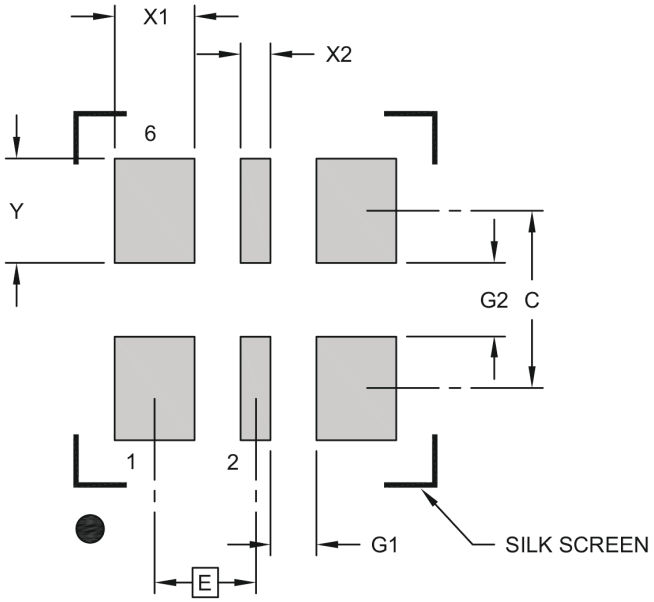
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1005 Rev C Sheet 2 of 2

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.825 BSC	
Contact Pad Width (X4)	X1			0.65
Contact Pad Width (X2)	X2			0.25
Contact Pad Length (X6)	Y			0.85
Contact Pad Spacing	C		1.45	
Space Between Contacts (X4)	G1	0.38		
Space Between Contacts (X3)	G2	0.60		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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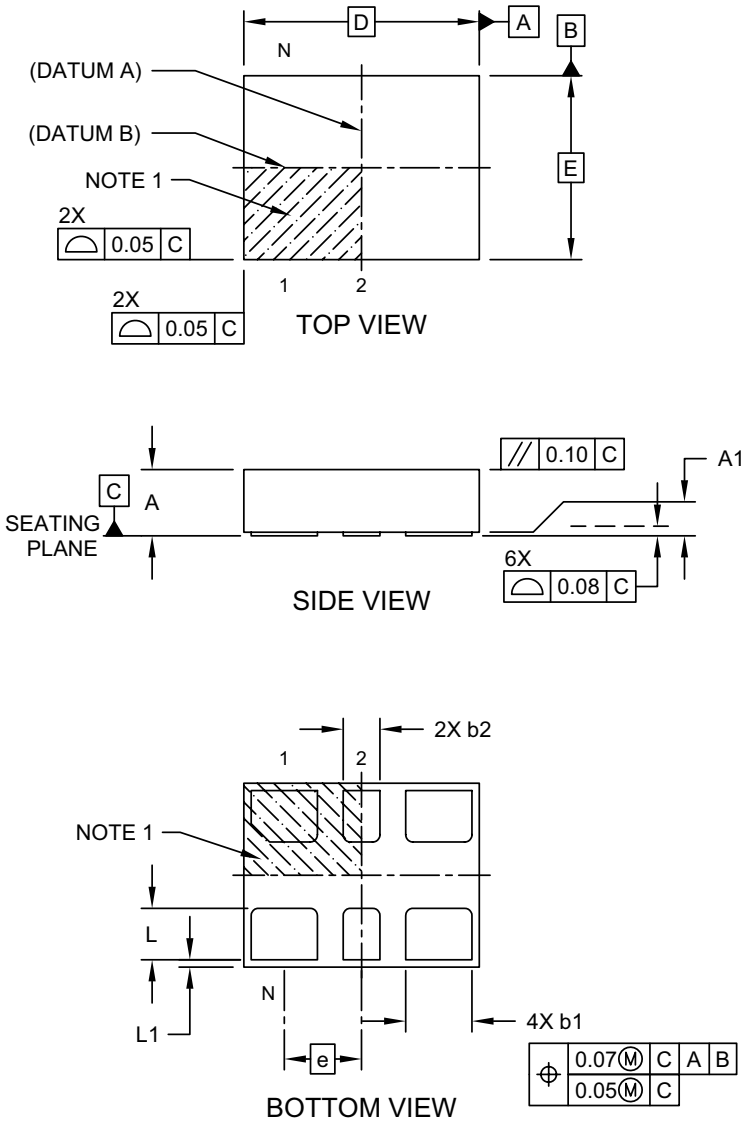
6-Lead VDFN 3.2 mm x 2.5 mm Package Outline and Recommended Land Pattern

6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

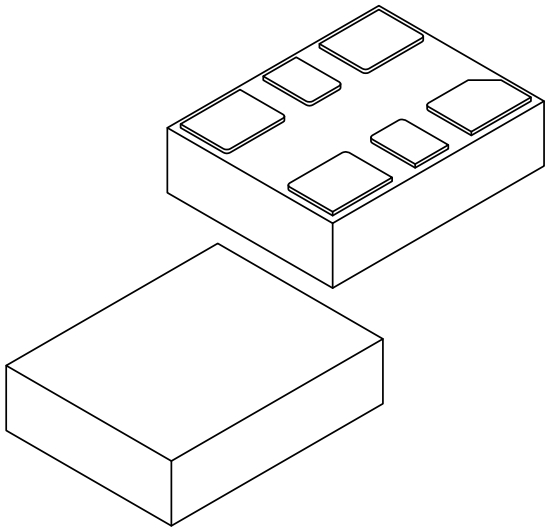
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1007A Sheet 1 of 2

6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		1.05 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D		3.20 BSC	
Overall Width	E		2.50 BSC	
Terminal Width	b1	0.85	0.90	0.95
Terminal Width	b2	0.45	0.50	0.55
Terminal Length	L	0.65	0.70	0.75
Terminal Pullback	L1		0.10 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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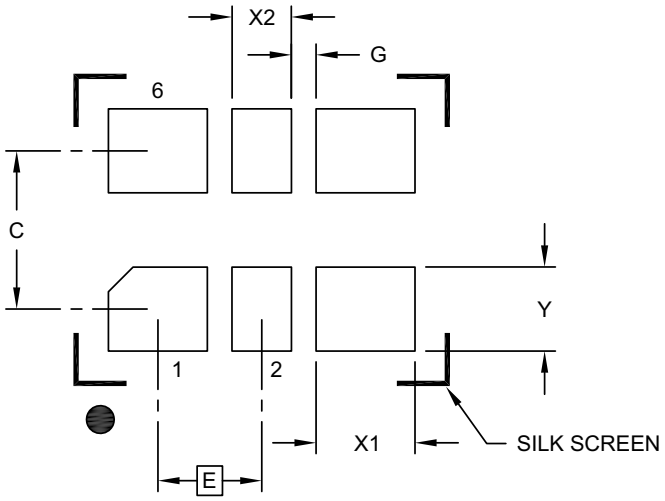
6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.05 BSC	
Contact Pad Spacing	C		1.60	
Contact Pad Width (X4)	X1			1.00
Contact Pad Width (X2)	X2			0.60
Contact Pad Length (X6)	Y			0.85
Space Between Contacts (X4)	G1	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

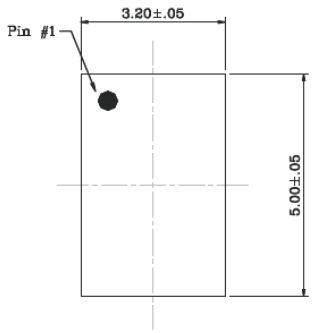
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3007A

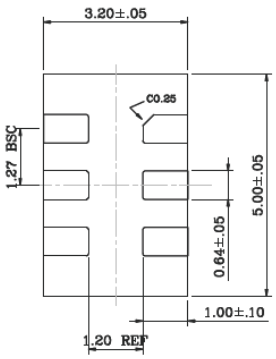
6-Lead CDFN 5.0 mm x 3.2 mm Package Outline and Recommended Land Pattern

TITLE
6 LEAD CDFN 5.0x3.2mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

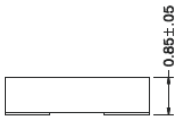
DRAWING #	CDFN5032-6LD-PL-1	UNIT	MM



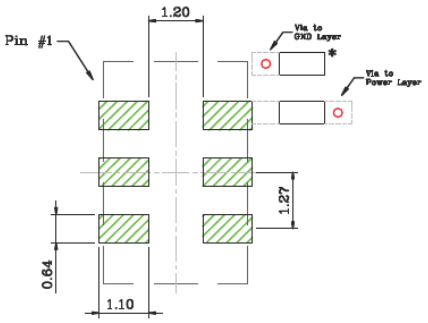
Top View



Bottom View



Side View



Recommended Land Pattern

NOTE:

1. * Power Supply Decoupling Capacitor is required in Recommended Land Pattern.
2. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
3. Red circles in Recommended Land Pattern are thermal VIA.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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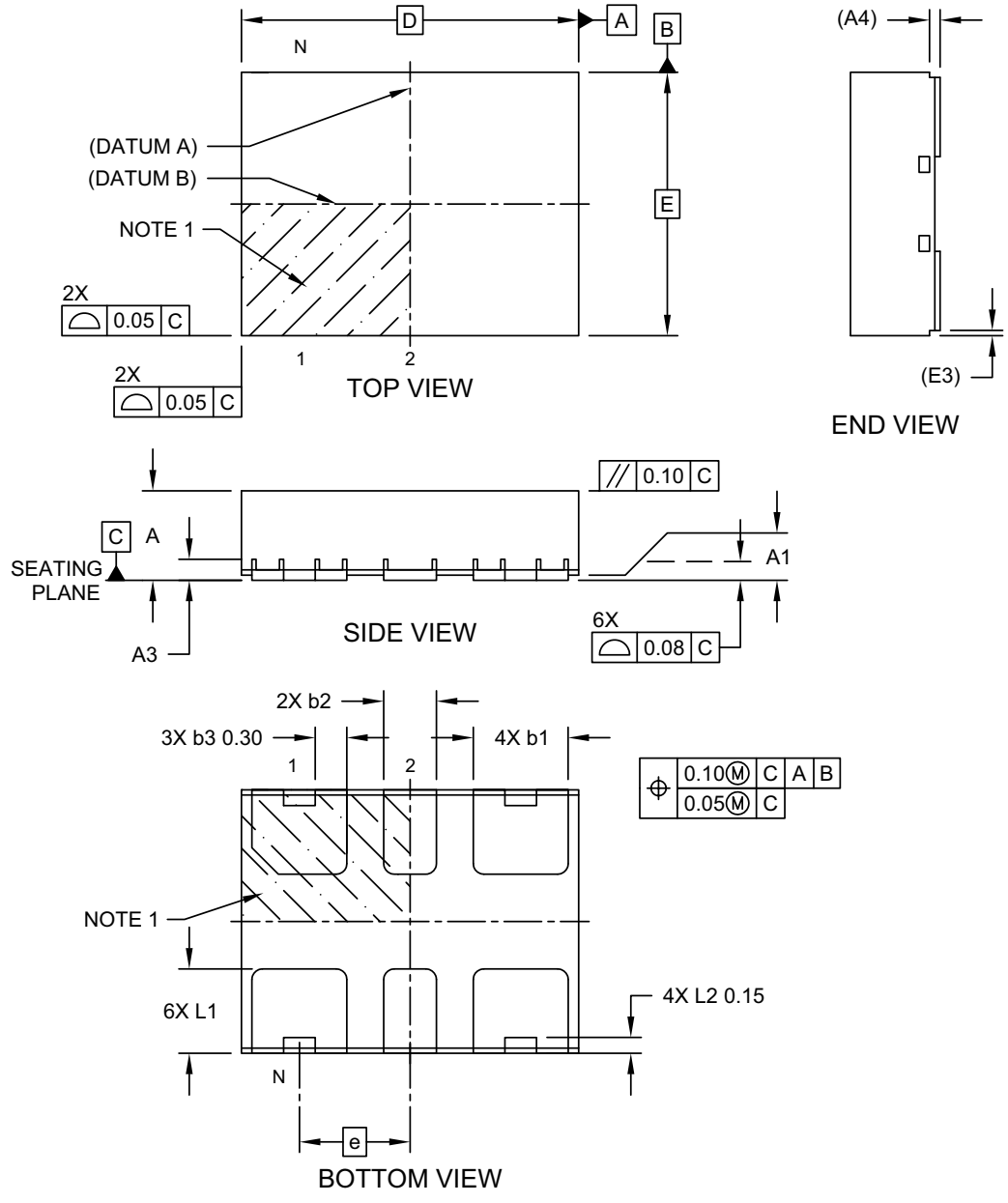
6-Lead 3.2 mm x 2.5 mm VDFN with Stepped Wettable Flanks

6-Lead Very Thin Plastic Dual Flat, No Lead Package (2YX) - 3.2x2.5x0.9 mm Body [VDFN] With Stepped Wettable Flanks

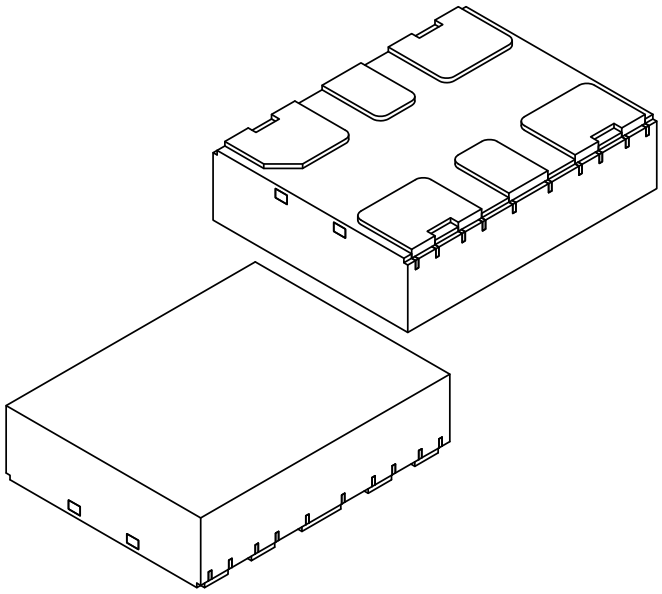
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-484 Rev A Sheet 1 of 2

6-Lead Very Thin Plastic Dual Flat, No Lead Package (2YX) - 3.2x2.5x0.9 mm Body [VDFN] With Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		1.05 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.15	0.20	0.25
Overall Length	D		3.20 BSC	
Overall Width	E		2.50 BSC	
Terminal Width	b1	0.85	0.90	0.95
Terminal Width	b2	0.45	0.50	0.55
Terminal Width	b3	0.25	0.30	0.35
Terminal Length	L1	0.70	0.80	0.90
Terminal Notch Length	L2		0.15 REF	
Step Width	E3		0.05 REF	
Step Height	A4		0.10 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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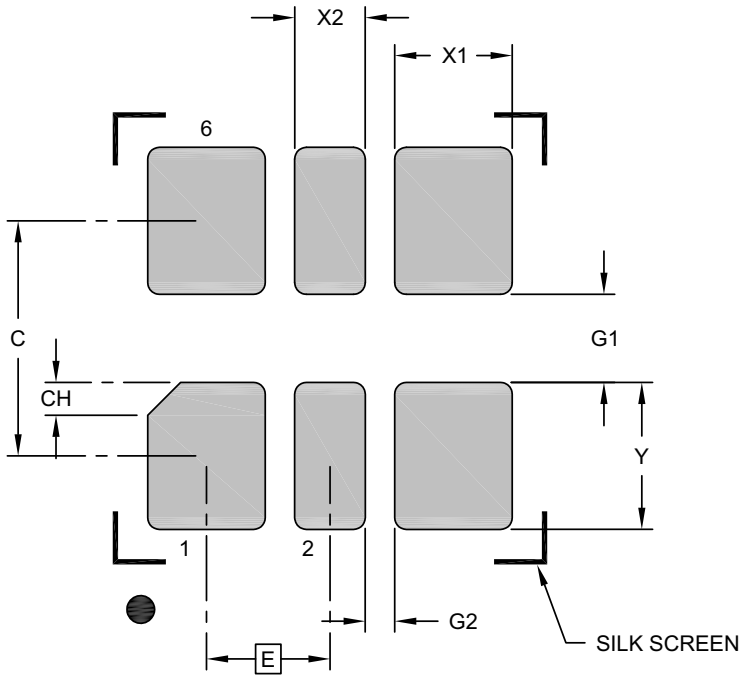
6-Lead Very Thin Plastic Dual Flat, No Lead Package (2YX) - 3.2x2.5x0.9 mm Body [VDFN] With Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.05 BSC		
Contact Pad Spacing	C		2.00	
Contact Pad Width (X20)	X1			1.00
Optional Center Pad Width	X2			0.60
Contact Pad Length (X20)	Y			0.80
Contact Pad to Contact Pad (X3)	G1	0.75		
Contact Pad to Contact Pad (X4)	G2	0.25		
Terminal 1 Corner Chamfer	CH	0.28x45°		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2484 Rev A

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (March 2018)

- Initial release of DSA1101/21/05/25 as Microchip data sheet DS20005890A.

Revision B (May 2018)

- Typographical errors were changed in the last paragraph of the General Description and in the CMOS Output section of the Electrical Characteristics Table under the Conditions column that corrects the part numbers from DSC1105/25 and DSC1101/21 to DSA1105/25 and DSA1101/21.
- Added the Automotive Suffix to the Product Identification System.

Revision C (February 2021)

- Added 6-Lead 3.2 mm x 2.5 mm VDFN with Stepped Wettable Flanks package option throughout document.
- Updated 6-Lead VDFN 2.5 mm x 2.0 mm Package Outline and Recommended Land Pattern drawing.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XXX.XXXX	X	VXX
Device	Package	Temp. Range	Stability	Frequency	Packing Option	Automotive Suffix

Device:	DSA1101/21:	Low-Power Precision CMOS Oscillator for Automotive with Standby
	DSA1105/25:	Low-Power Precision CMOS Oscillator for Automotive
Package:	B =	6-Lead 5.0 mm x 3.2 mm CDFN
	C =	6-Lead 3.2 mm x 2.5 mm VDFN
	D =	6-Lead 2.5 mm x 2.0 mm VDFN
	W =	6-Lead 3.2 mm x 2.5 mm VDFN with Wettable Flanks
Temperature Range:	I =	–40°C to +85°C (Grade 3)
	L =	–40°C to +105°C (Grade 2)
	A =	–40°C to +125°C (Grade 1)
Stability:	1 =	±50 ppm
	2 =	±25 ppm
	3 =	±20 ppm
Frequency:	xxx.xxxx =	2.3 MHz to 170 MHz (user-defined)
Packing Option:	<blank> =	110/Tube
	T =	1,000/Reel
Automotive Suffix:	Vxx =	Automotive Suffix in which “xx” is assigned by Microchip

Please use the Microchip Clockworks to check AEC-Q100 compliance status and build the exact part number.

Examples:

a) DSA1101CL3-030.0000VAO:	Low-Power Precision CMOS Oscillator for Automotive with Standby, 6-LD 3.2X2.5 VDFN, Grade 2 Temperature Range, ±20 ppm, 30 MHz Output Frequency, 110/ Tube, Automotive Suffix
b) DSA1121DI1-075.0000TVAO:	Low-Power Precision CMOS Oscillator for Automotive with Standby, 6-LD 2.5x2.0 VDFN, Grade 3 Temperature Range, ±50 ppm, 75 MHz Output Frequency, 1,000/Reel, Automotive Suffix
c) DSA1105BL2-027.0000VAO:	Low-Power Precision CMOS Oscillator for Automotive, 6-LD 5.0x3.2 CDFN, Grade 2 Temperature Range, ±25 ppm, 27 MHz Output Frequency, 110/ Tube, Automotive Suffix
d) DSA1125CA3-033.0000TVAO:	Low-Power Precision CMOS Oscillator for Automotive, 6-LD 3.2x2.5 VDFN, Grade 1 Temperature Range, ±20 ppm, 33 MHz Output Frequency, 1000/Reel, Automotive Suffix

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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