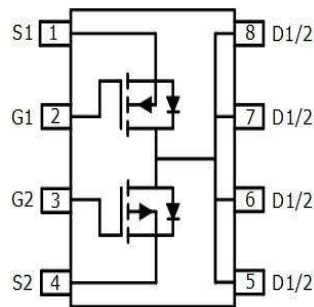


**OptiMOS™2 + OptiMOS™-P 2 Small Signal Transistor**
**Features**

- Complementary P + N channel
- Enhancement mode
- Super Logic level (2.5V rated)
- Common drain
- Avalanche rated
- 175 °C operating temperature
- Qualified according to AEC Q101
- 100% lead-free; RoHS compliant
- Halogen-free according to IEC61246-21

**Product Summary**

		P	N	
$V_{DS}$		-20	20	V
$R_{DS(on),max}$	$V_{GS}=\pm 4.5\text{ V}$	150	55	mΩ
	$V_{GS}=\pm 2.5\text{ V}$	310	95	
$I_D$		-3.2	5.1	A



Type	Package	Marking	Lead Free	Halogen Free	Packing
BSZ215C H	PG-TSDSON-8 LTI	215C	Yes	Yes	Non dry

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified <sup>1)</sup>**

Parameter	Symbol	Conditions	Value		Unit
			P	N	
Continuous drain current	$I_D$	$T_A=25\text{ °C}$	-3.2	5.1	A
		$T_A=100\text{ °C}$	-2.2	3.6	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}$	-13	20	
Avalanche energy, single pulse	$E_{AS}$	P: $I_D=-3.2\text{ A}$ , N: $I_D=5.1\text{ A}$ , $R_{GS}=25\text{ }\Omega$	11	11	mJ
Gate source voltage	$V_{GS}$		$\pm 12$		V
Power dissipation	$P_{tot}$ <sup>2)</sup>	$T_A=25\text{ °C}$	2.5		W
Operating and storage temperature	$T_j, T_{stg}$		-55 ... 175		°C
ESD class		JESD22-A114-HBM	0 (<250V)		
Soldering temperature	$T_{solder}$		260		°C
IEC climatic category; DIN IEC 68-1			55/175/56		

<sup>1)</sup> Remark: only one of both transistors active

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	P	$R_{thJC}$		-	-	8	K/W
	N						
Device on PCB		$R_{thJA}$	6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	-	60	K/W

**Electrical characteristics, at  $T_j=25\text{ }^\circ\text{C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	P	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=-250\text{ }\mu\text{A}$	-	-	-20	V
	N		$V_{GS}=0\text{ V}, I_D=250\text{ }\mu\text{A}$	20	-	-	
Gate threshold voltage	P	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-110\text{ }\mu\text{A}$	-1.4	-1.0	-0.7	
	N		$V_{DS}=V_{GS}, I_D=110\text{ }\mu\text{A}$	0.8	1.1	1.4	
Zero gate voltage drain current	P	$I_{DSS}$	$V_{DS}=-20\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	-	-0.1	$\mu\text{A}$
	N		$V_{DS}=20\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	-	0.1	
	P		$V_{DS}=-20\text{ V}, V_{GS}=0\text{ V}, T_j=175\text{ }^\circ\text{C}$	-	-	-50	
	N		$V_{DS}=20\text{ V}, V_{GS}=0\text{ V}, T_j=175\text{ }^\circ\text{C}$	-	-	50	
Gate-source leakage current	P	$I_{GSS}$	$V_{GS}=\pm 12\text{ V}, V_{DS}=0\text{ V}$	-	-	$\pm 100$	nA
	N						
Drain-source on-state resistance	P	$R_{DS(on)}$	$V_{GS}=-2.5\text{ V}, I_D=2.1\text{ A}$	-	144	310	m $\Omega$
	N		$V_{GS}=2.5\text{ V}, I_D=1.9\text{ A}$	-	63	95	
	P		$V_{GS}=-4.5\text{ V}, I_D=-3.2\text{ A}$	-	95	150	
	N		$V_{GS}=4.5\text{ V}, I_D=5.1\text{ A}$	-	41	55	
Transconductance	P	$g_{fs}$	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=-2.2\text{ A}$	4	7.9	-	S
	N		$ V_{DS} >2 I_D R_{DS(on)max}, I_D=3.6\text{ A}$	5.5	11	-	

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	P	$C_{iss}$	$V_{GS}=0\text{ V}$ , P: $V_{DS}=-10\text{ V}$ , N: $V_{DS}=10\text{ V}$ , $f=1\text{ MHz}$	-	300	400	pF			
	N			-	315	419				
Output capacitance	P	$C_{oss}$		P: $V_{DD}=-10\text{ V}$ , $V_{GS}=-4.5\text{ V}$ , $R_G=6\ \Omega$ , $I_D=-3.2\text{ A}$	-	92	120			
	N				-	114	152			
Reverse transfer capacitance	P	$C_{rss}$			N: $V_{DD}=10\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $R_G=6\ \Omega$ , $I_D=5.1\text{ A}$	-	92	140		
	N					-	16	24		
Turn-on delay time	P	$t_{d(on)}$				P: $V_{DD}=-10\text{ V}$ , $V_{GS}=-4.5\text{ V}$ , $R_G=6\ \Omega$ , $I_D=-3.2\text{ A}$	-	7.4	-	ns
	N						-	4.9	-	
Rise time	P	$t_r$	N: $V_{DD}=10\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $R_G=6\ \Omega$ , $I_D=5.1\text{ A}$				-	3.7	-	
	N						-	2.0	-	
Turn-off delay time	P	$t_{d(off)}$		N: $V_{DD}=10\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $R_G=6\ \Omega$ , $I_D=5.1\text{ A}$			-	11.3	-	
	N						-	12.2	-	
Fall time	P	$t_f$			N: $V_{DD}=10\text{ V}$ , $V_{GS}=4.5\text{ V}$ , $R_G=6\ \Omega$ , $I_D=5.1\text{ A}$		-	4.7	-	
	N						-	1.4	-	

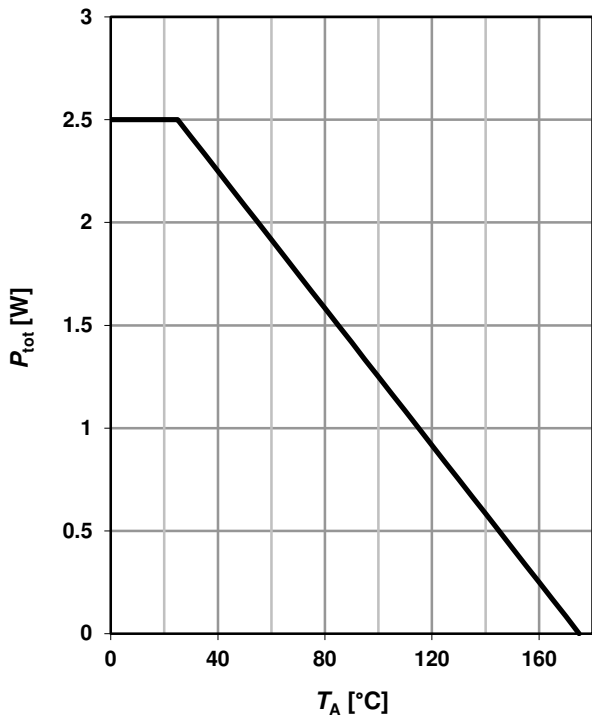
**Gate Charge Characteristics**

Gate to source charge	P	$Q_{gs}$	$V_{DD}=-10\text{ V}$ , $I_D=-3.2\text{ A}$ , $V_{GS}=0\text{ to }-4.5\text{ V}$	-	-0.58	-0.8	nC
Gate to drain charge		$Q_{gd}$		-	-1.3	-1.7	
Switching charge		$Q_g$		-	-3.0	-4.6	
Gate plateau voltage		$V_{plateau}$		-	-1.9	-	
Gate to source charge	N	$Q_{gs}$	$V_{DD}=10\text{ V}$ , $I_D=5.1\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$	-	0.7	1.0	
Gate to drain charge		$Q_{gd}$		-	0.4	-	
Switching charge		$Q_g$		-	2.1	2.8	
Gate plateau voltage		$V_{plateau}$		-	2.3	-	

Parameter	Symbol	Conditions	Values			Unit		
			min.	typ.	max.			
<b>Reverse Diode</b>								
Diode continuous forward current	P	$I_S$	$T_C=25\text{ °C}$	-	-	-2.1	A	
	N					2.3		
Diode pulse current	P	$I_{S,pulse}$		-	-	-13		
	N					20		
Diode forward voltage	P	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=3.2\text{ A},$ $T_j=25\text{ °C}$	-	-0.98	-1.2	V	
	N		$V_{GS}=0\text{ V}, I_F=5.1\text{ A},$ $T_j=25\text{ °C}$	-	0.9	1.2		
Reverse recovery time	P	$t_{rr}$	$V_R=\pm 10\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$		12.2		ns	
	N			-	10.9	-		
Reverse recovery charge	P	$Q_{rr}$				4.6		nC
	N			-	3.4	-		

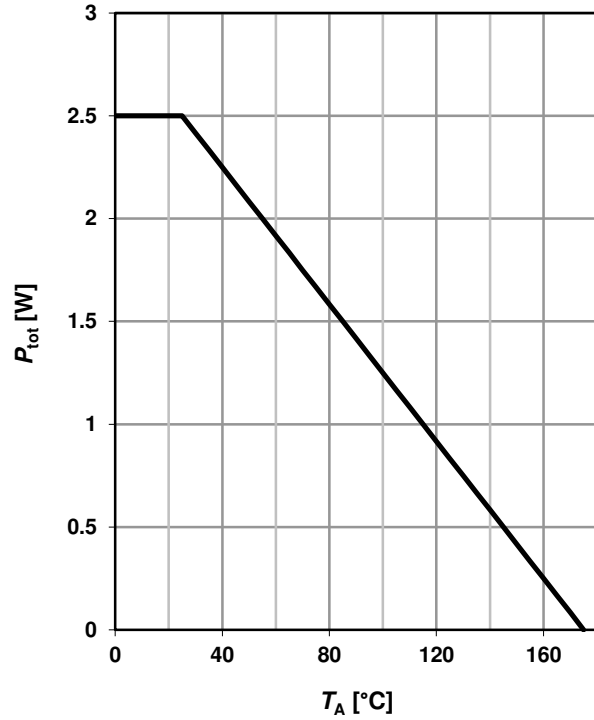
**1 Power dissipation (P)**

$$P_{tot}=f(T_A)$$



**2 Power dissipation (N)**

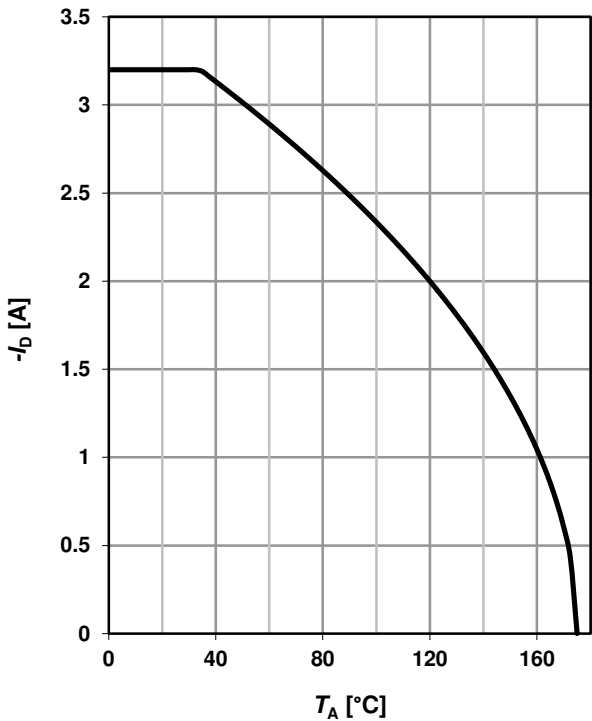
$$P_{tot}=f(T_A)$$



**3 Drain current (P)**

$$I_D=f(T_A)$$

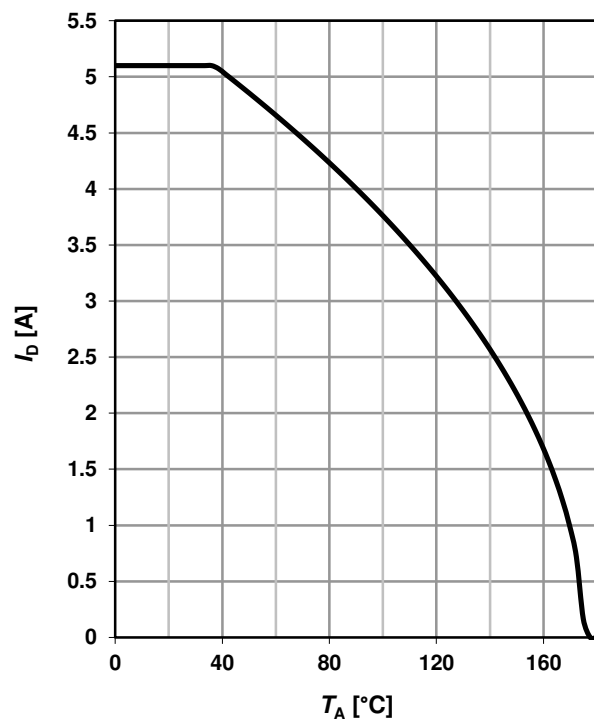
parameter:  $V_{GS} \leq 4.5$  V



**4 Drain current (N)**

$$I_D=f(T_A)$$

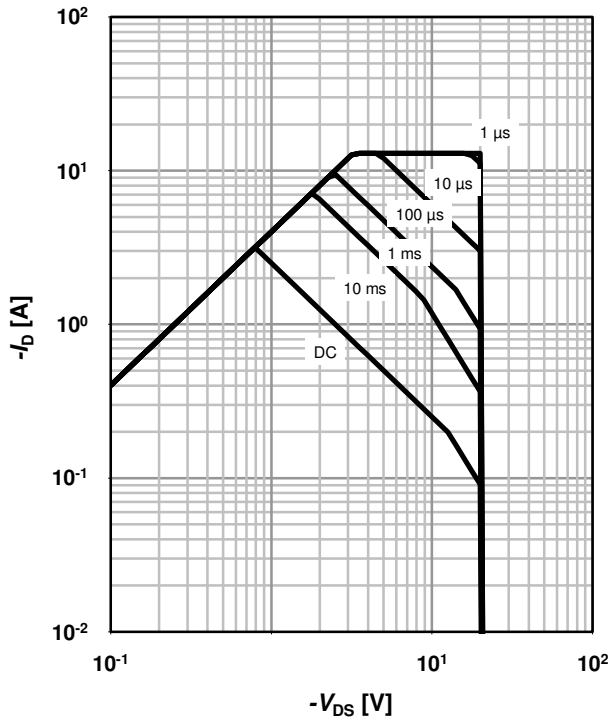
parameter:  $V_{GS} \geq 4.5$  V



**5 Safe operating area (P)**

$I_D=f(V_{DS}); T_A=25\text{ }^\circ\text{C}; D=0$

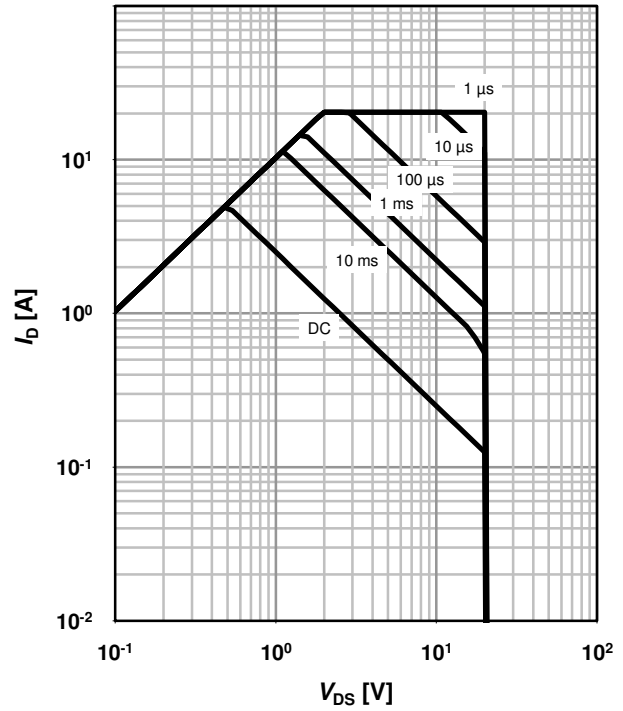
parameter:  $t_p$



**6 Safe operating area (N)**

$I_D=f(V_{DS}); T_A=25\text{ }^\circ\text{C}; D=0$

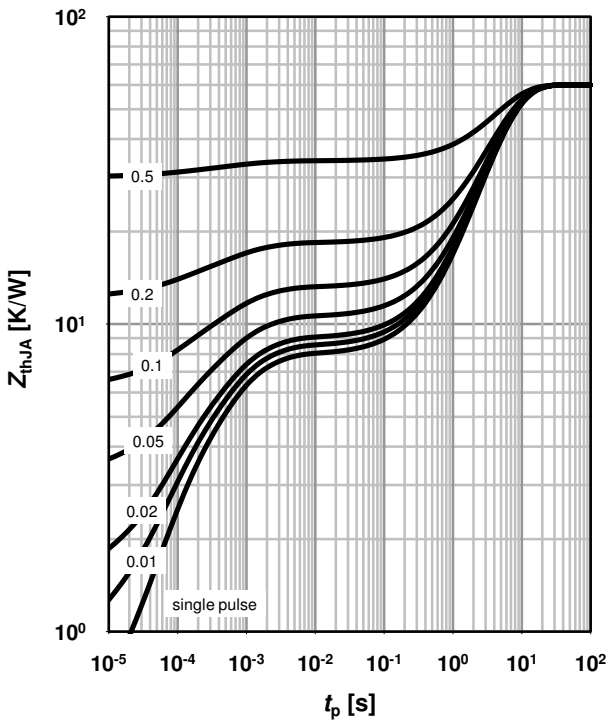
parameter:  $t_p$



**7 Max. transient thermal impedance (P)**

$Z_{thJA}=f(t_p)$

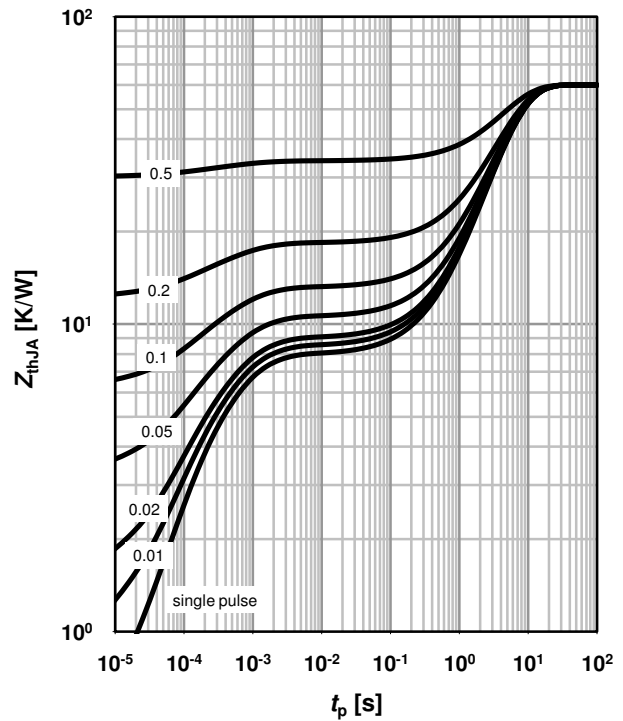
parameter:  $D=t_p/T$



**8 Max. transient thermal impedance (N)**

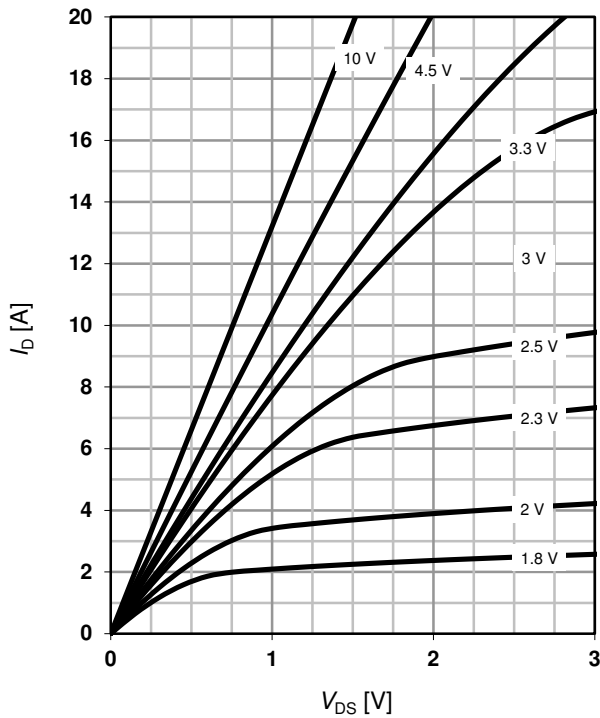
$Z_{thJA}=f(t_p)$

parameter:  $D=t_p/T$

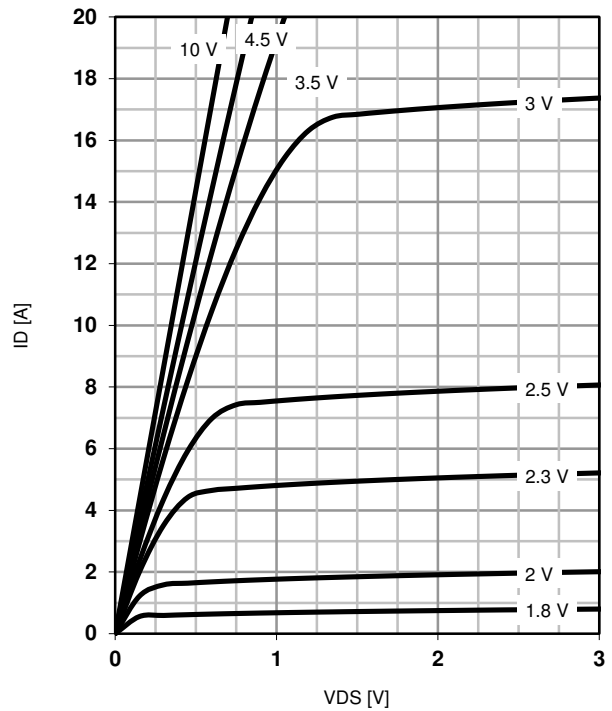


**9 Typ. output characteristics (P)**

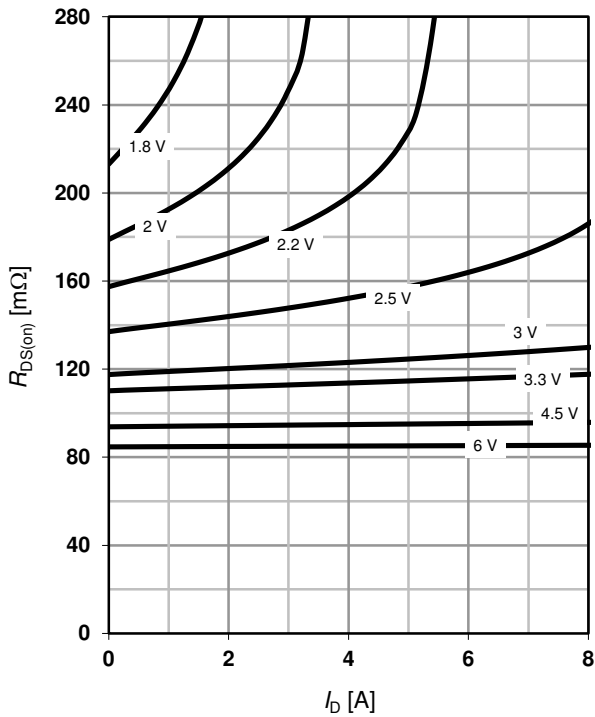
$$I_D = f(V_{DS}); T_j = 25\text{ °C}$$

 parameter:  $V_{GS}$ 

**10 Typ. output characteristics (N)**

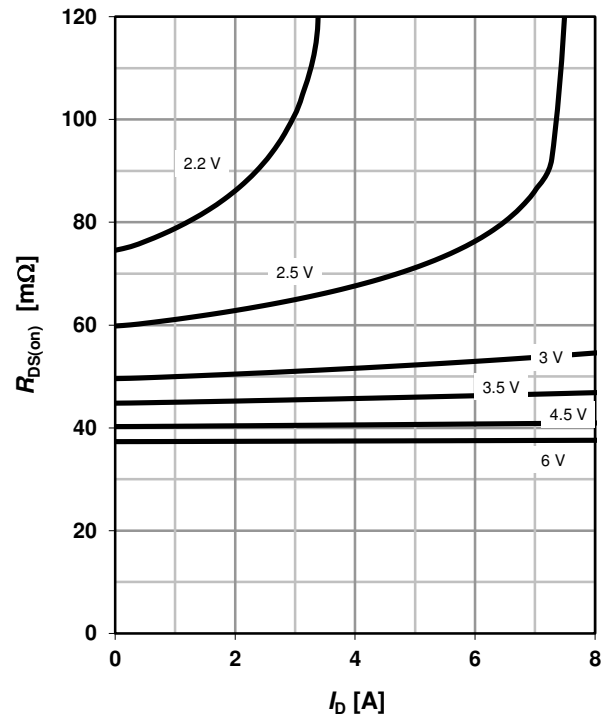
$$I_D = f(V_{DS}); T_j = 25\text{ °C}$$

 parameter:  $V_{GS}$ 

**11 Typ. drain-source on resistance (P)**

$$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$$

 parameter:  $V_{GS}$ 

**12 Typ. drain-source on resistance (N)**

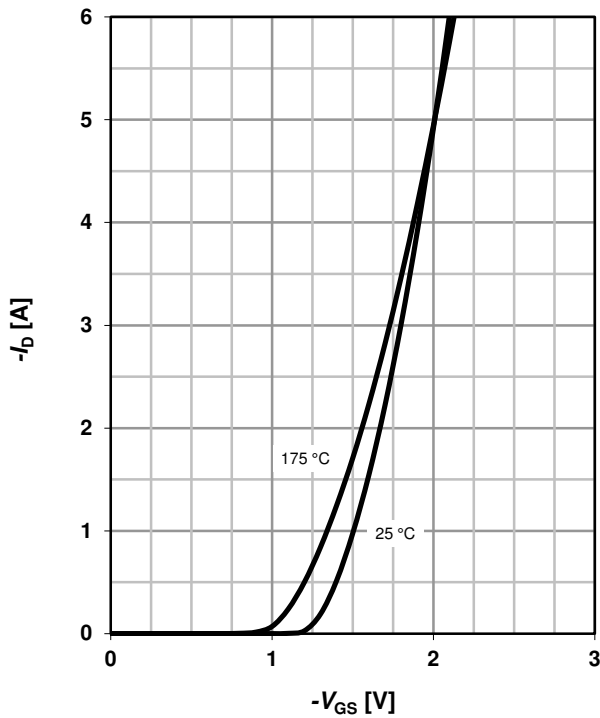
$$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$$

 parameter:  $V_{GS}$ 


**13 Typ. transfer characteristics (P)**

$$I_D = f(V_{GS}); |V_{DS}| > 2 |I_D| R_{DS(on)max}$$

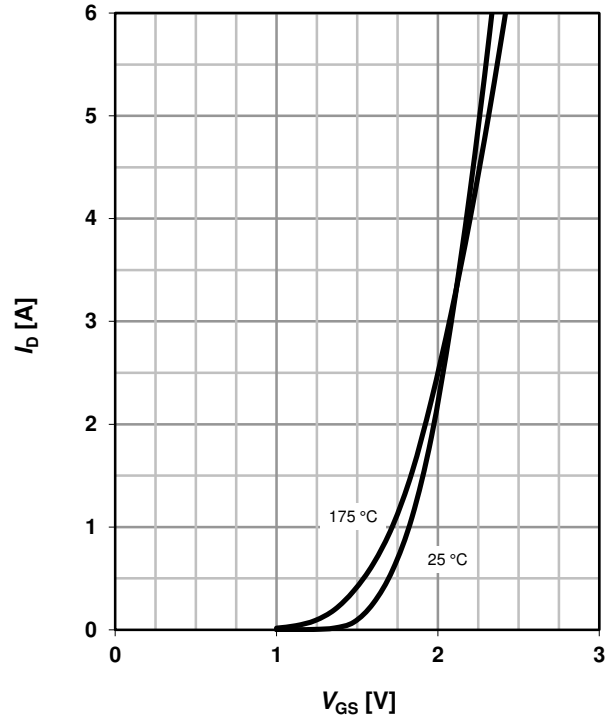
parameter:  $T_j$



**14 Typ. transfer characteristics (N)**

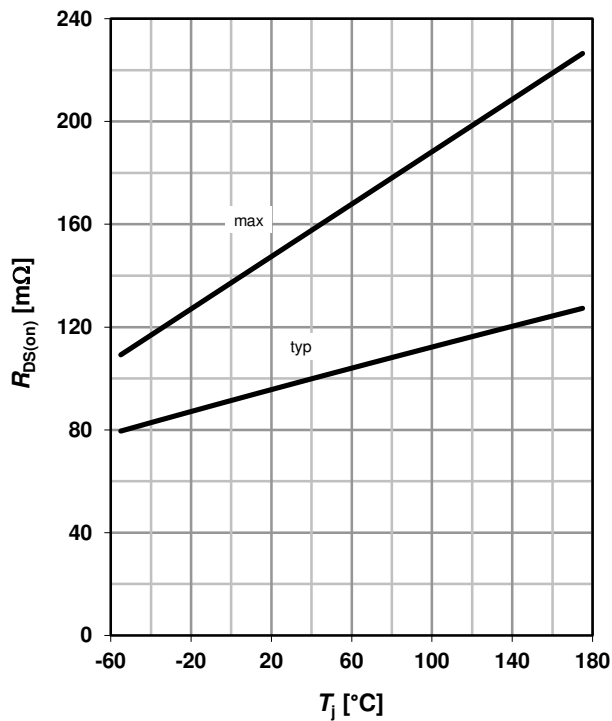
$$I_D = f(V_{GS}); |V_{DS}| > 2 |I_D| R_{DS(on)max}$$

parameter:  $T_j$



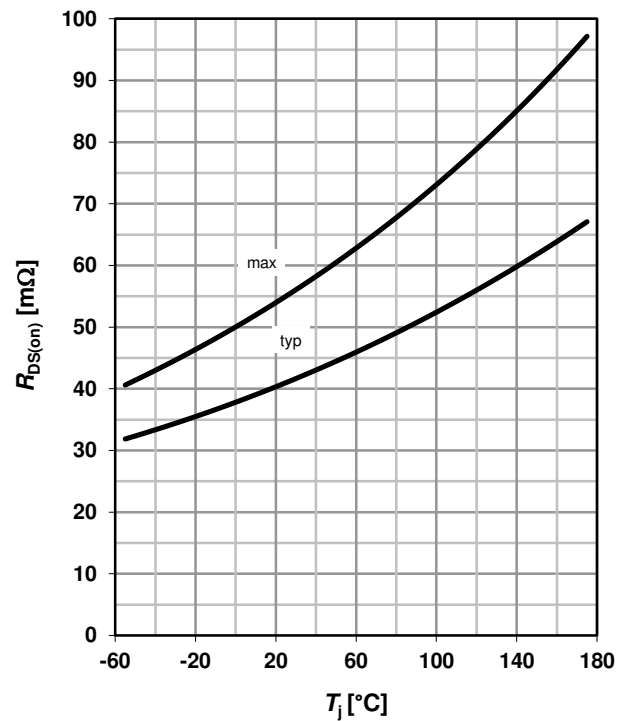
**15 Drain-source on-state resistance (P)**

$$R_{DS(on)} = f(T_j); I_D = -3.2 A; V_{GS} = -4.5 V$$



**16 Drain-source on-state resistance (N)**

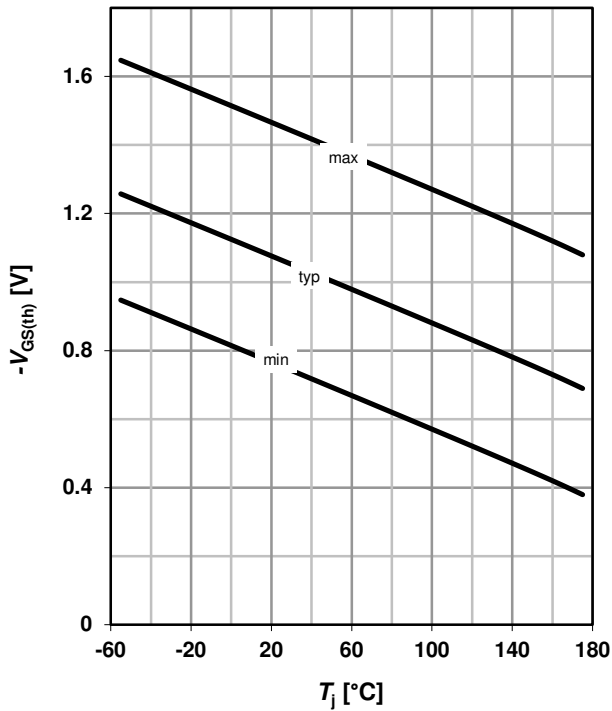
$$R_{DS(on)} = f(T_j); I_D = 5.1 A; V_{GS} = 4.5 V$$



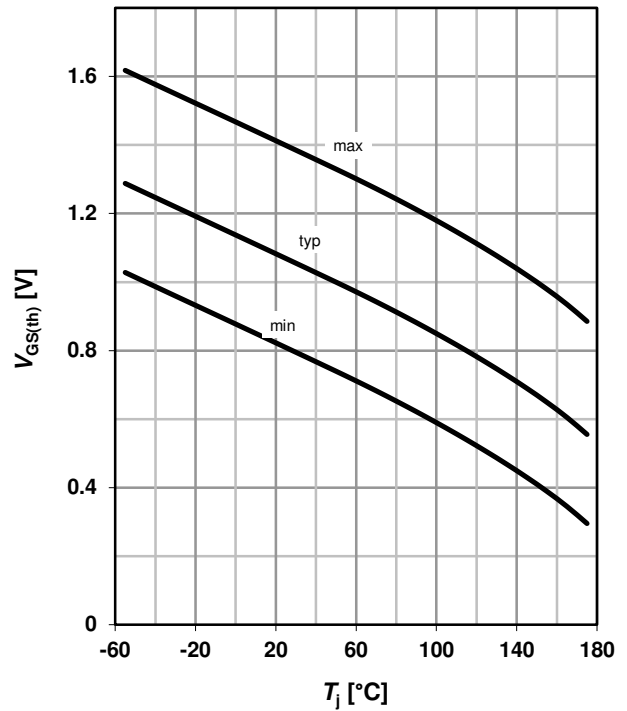


**17 Typ. gate threshold voltage (P)**

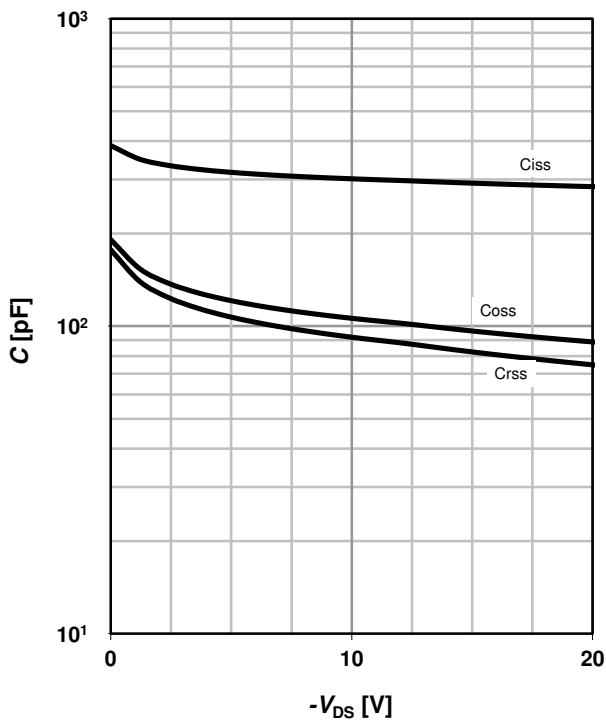
$$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}; I_D=-110 \mu A$$


**18 Typ. gate threshold voltage (N)**

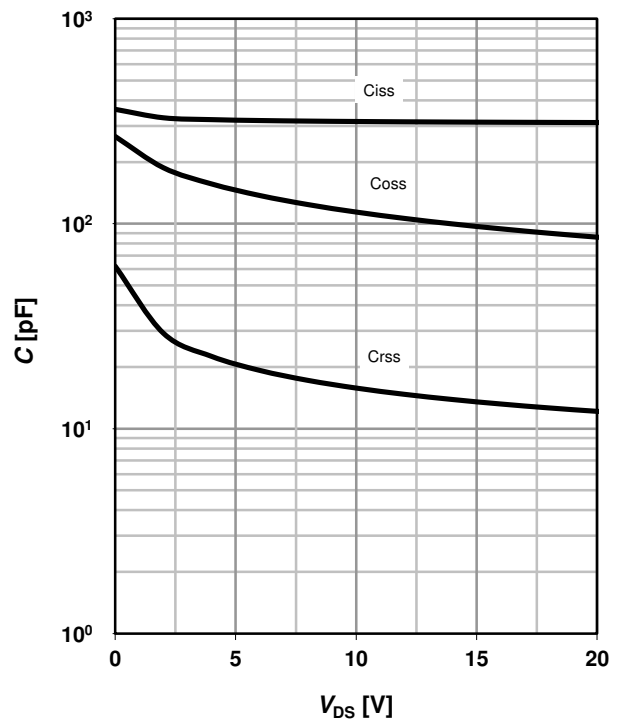
$$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}; I_D=110 \mu A$$


**19 Typ. capacitances (P)**

$$C=f(V_{DS}); V_{GS}=0 V; f=1 MHz$$

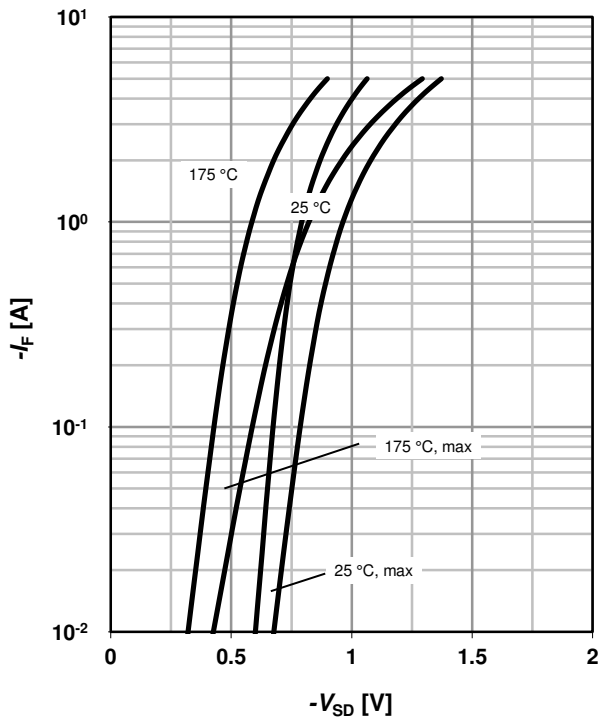

**20 Typ. capacitances (N)**

$$C=f(V_{DS}); V_{GS}=0 V; f=1 MHz$$

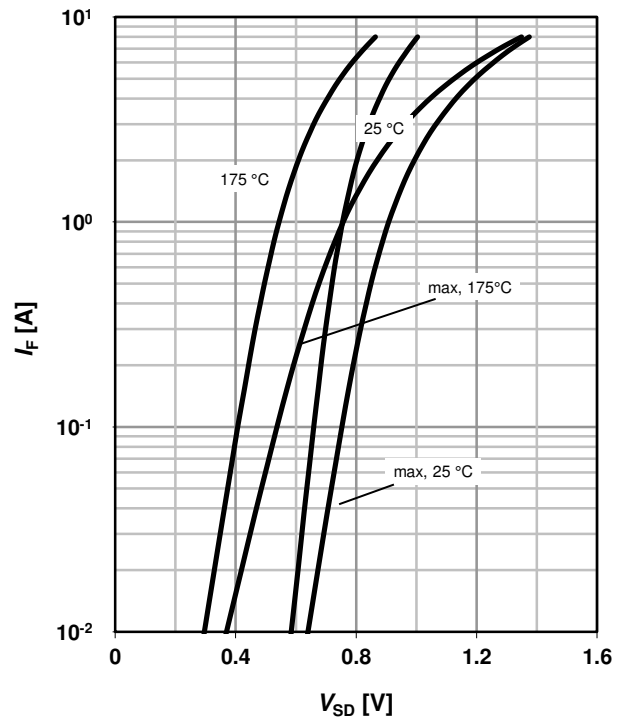


**21 Forward characteristics of reverse diode (P)**

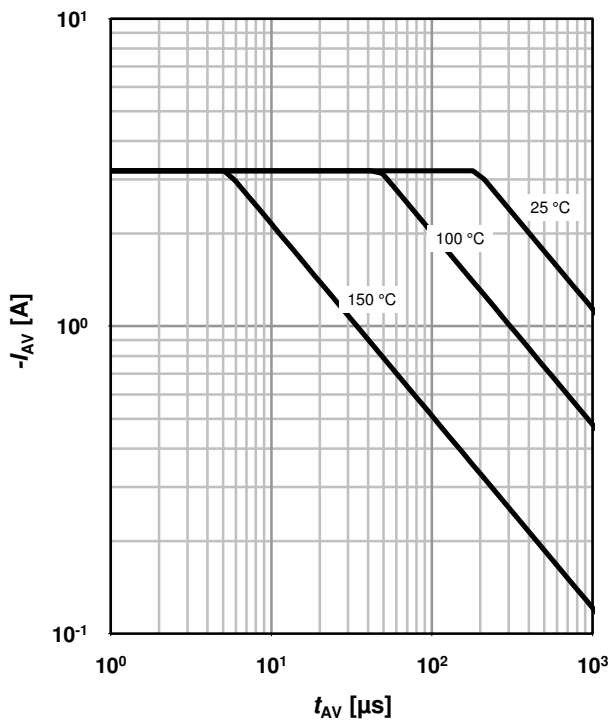
$$I_F = f(V_{SD})$$

 parameter:  $T_j$ 

**22 Forward characteristics of reverse diode (N)**

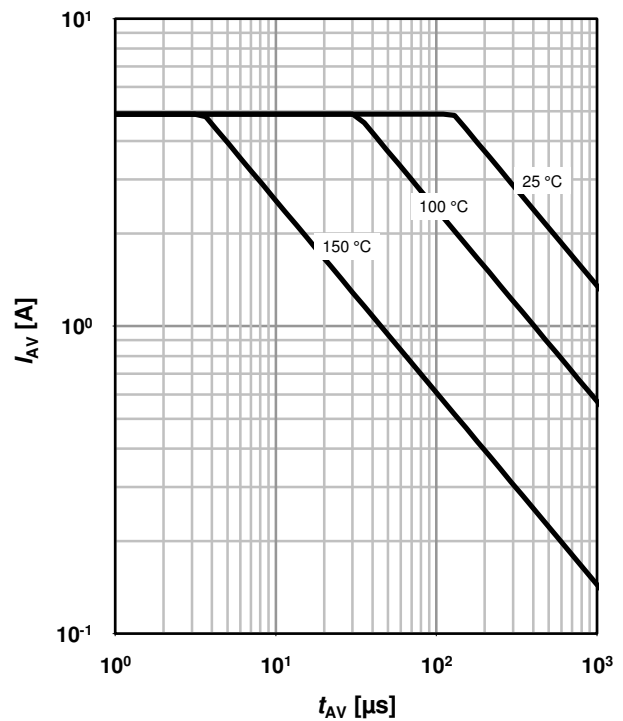
$$I_F = f(V_{SD})$$

 parameter:  $T_j$ 

**23 Avalanche characteristics (P)**

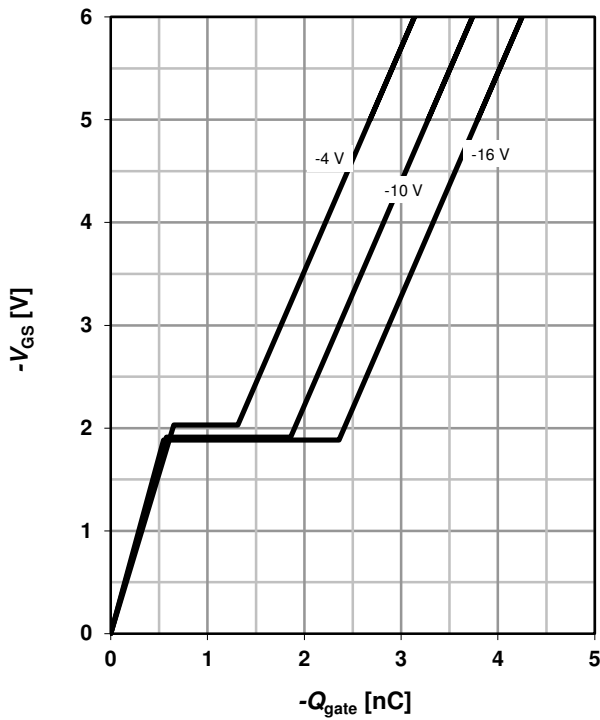
$$I_{AS} = f(t_{AV}); R_{GS} = 25 \Omega$$

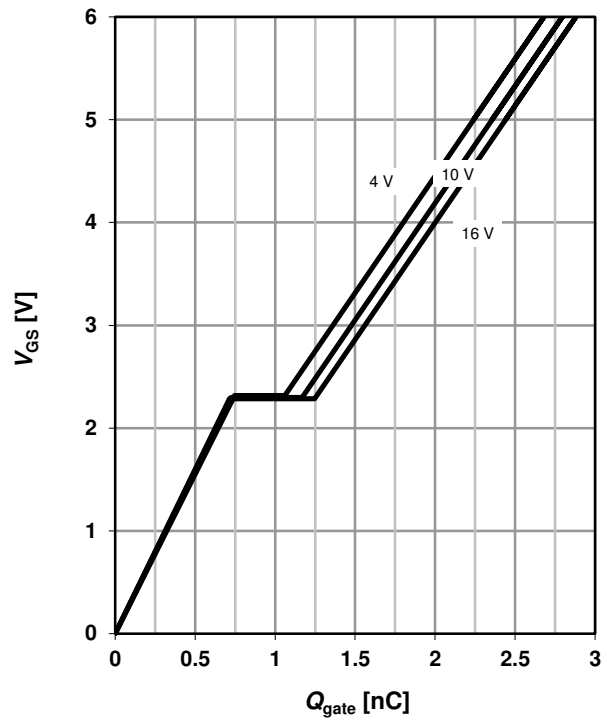
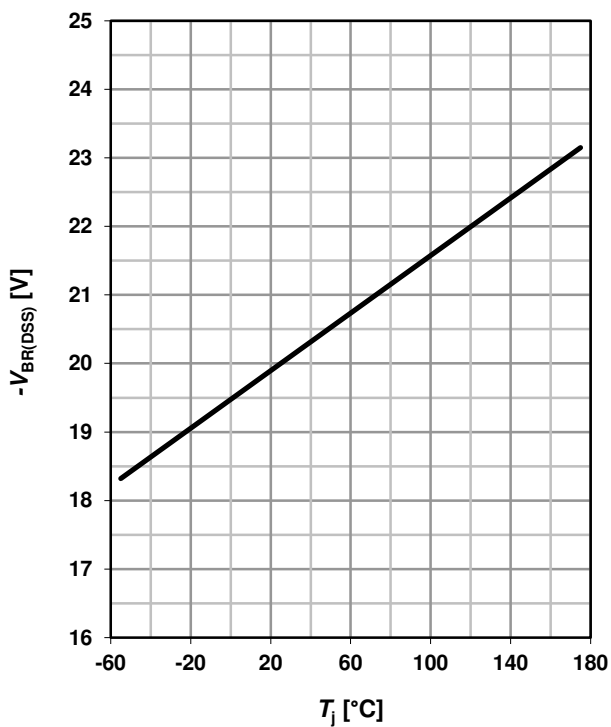
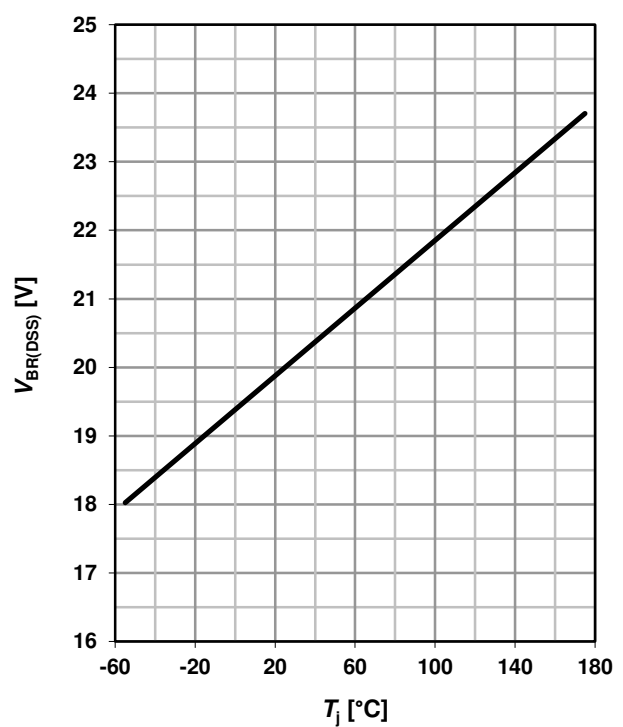
 parameter:  $T_{j(\text{start})}$ 

**24 Avalanche characteristics (N)**

$$I_{AS} = f(t_{AV}); R_{GS} = 25 \Omega$$

 parameter:  $T_{j(\text{start})}$ 


**25 Typ. gate charge (P)**
 $V_{GS}=f(Q_{gate}); I_D=-3.2A$  pulsed

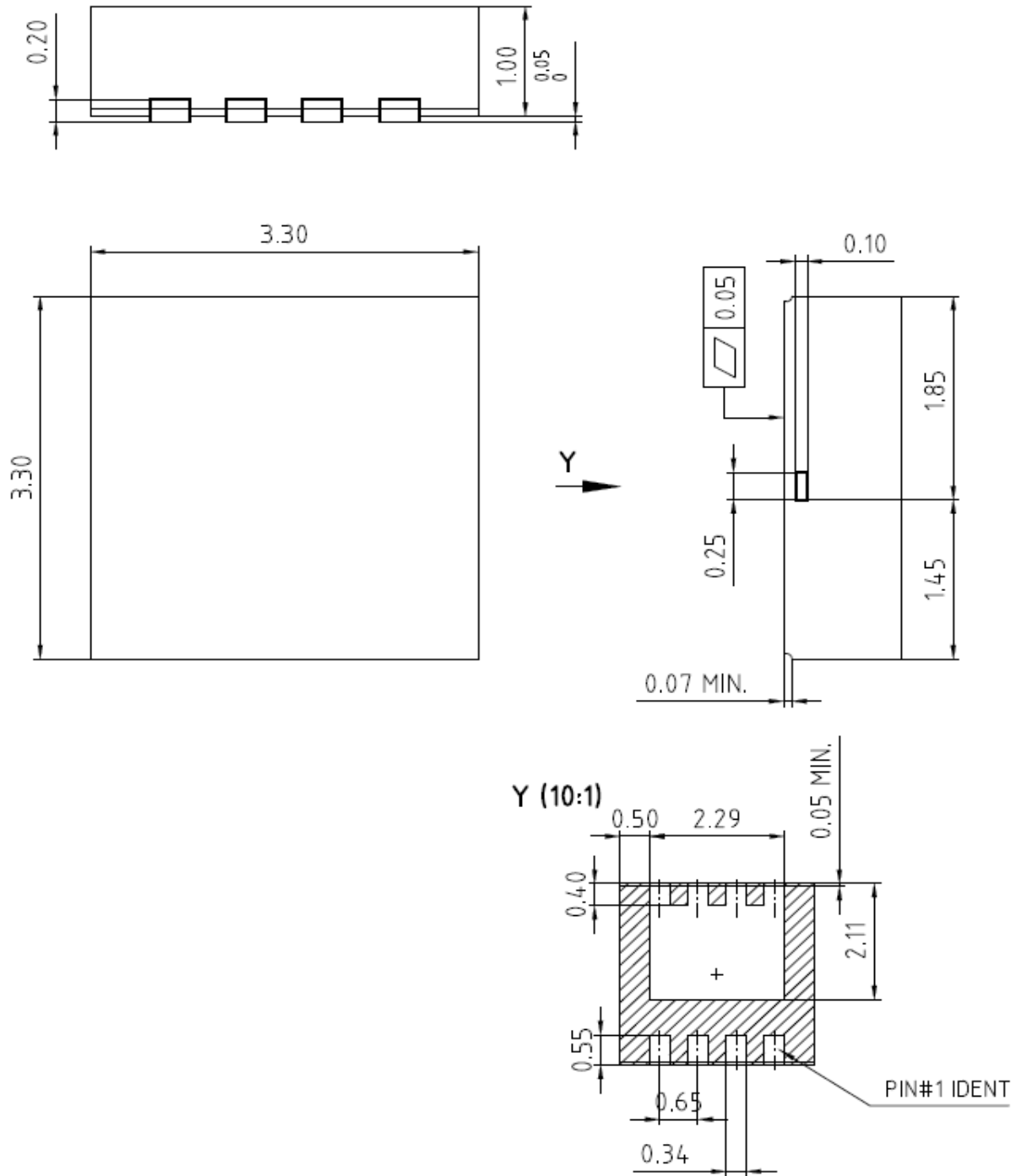
 parameter:  $V_{DD}$ 

**26 Typ. gate charge (N)**
 $V_{GS}=f(Q_{gate}); I_D=5.1A$  pulsed

 parameter:  $V_{DD}$ 

**27 Drain-source breakdown voltage (P)**
 $V_{BR(DSS)}=f(T_j); I_D=-250 \mu A$ 

**28 Drain-source breakdown voltage (N)**
 $V_{BR(DSS)}=f(T_j); I_D=250 \mu A$ 


Package Outline

PG-TSDSON-8LTI

PG-TSDSON-8LTI : Outline



Dimensions in mm

# 20V OptiMOS™ 2 Small Signal Transistor

## BSZ215C H

### Revision History

BSZ215C H

**Revision: 2016-10-06, Rev. 2.3**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.3	2016-10-06	Update package drawing

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