ISL6442

Dual (180° Out-of-Phase) PWM and Linear Controller

FN9204
Rev 2.00
Oct 31, 2008

The ISL6442 is a high-performance, triple output controller that provides a single high-frequency power solution primarily for Broadband, DSL and Networking applications. This device integrates complete control, monitoring and protection functions for two synchronous buck PWM controllers and one linear controller. Input voltage ripple and total RMS input current is substantially reduced by synchronized 180° out-of-phase operation of the two PWMs.

The two PWM buck converters provide simple voltage mode control. The output voltage of the converters can be precisely regulated to as low as 0.6V, with a maximum tolerance of ±1.5% over temperature and line variations. Programmable switching frequency up to 2.5MHz provides fast transient response and small external components. The linear controller provides a low-current output.

The ISL6442 has voltage-tracking capability. Each controller has soft-start and independent enable functions combined on a single pin. A capacitor from SS/EN to ground sets the soft-start time; pulling SS/EN pin below 1V disables the controller. Both outputs can soft-start into a pre-biased load.

The ISL6442 incorporates robust protection features. An adjustable overcurrent protection circuit monitors the output current by sensing the voltage drop across the upper MOSFET $r_{DS(ON)}$. Hiccup mode overcurrent operation protects the DC/DC converters from damage under over load and short circuit conditions. A PGOOD signal is issued when soft-start is complete and PWM outputs are within 10% of their regulated values and the linear regulator output is higher than 75% of its nominal value. Thermal shut-down circuitry turns the device off if the IC temperature exceeds +150°C.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6442IAZ*	ISL 6442IAZ	-40 to +85	24 Ld QSOP	M24.15

*Add “-TK” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

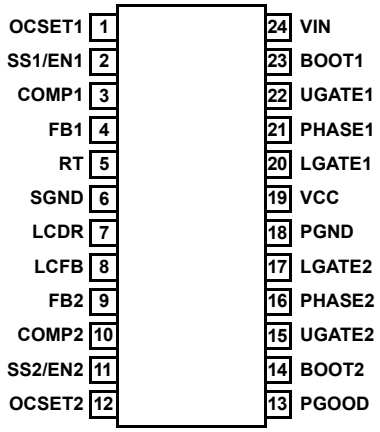
- 4.5V to 5.5V or 5.5V to 24V Input Voltage Range
- ±1.5% PWM Switcher Reference Accuracy Over Line and Temperature
- Three Programmable Power Output Voltages
  - Two PWM Controllers with Out-of-Phase Operation
  - Voltage-Mode PWM Control
  - One Linear Controller
- Programmable Switching Frequency from 300kHz to 2.5MHz
- Fast Transient Response
  - High-Bandwidth Error Amplifier
- Extensive Circuit Protection Functions
  - Overvoltage, Undervoltage, and Overtemperature
  - Programmable Overcurrent Limit with Hiccup Mode Operation
  - Lossless Current Sensing (No Sense Resistor Needed)
- Externally Adjustable Soft-Start Time
  - Independent Enable Control
  - Voltage Tracking Capability
  - Able to Soft-Start into a Pre-Biased Load
- PGOOD Output with Delay
- 24 Ld QSOP
- Pb-Free (RoHS Compliant)

Applications

- Complete 1 Chip Solution for DSL Modems/Routers
- DSP, ASIC, and FPGA Point of Load Regulation
- ADSL, Broadband and Networking Applications

Pinout

ISL6442
(24 LD QSOP)
TOP VIEW



Block Diagram

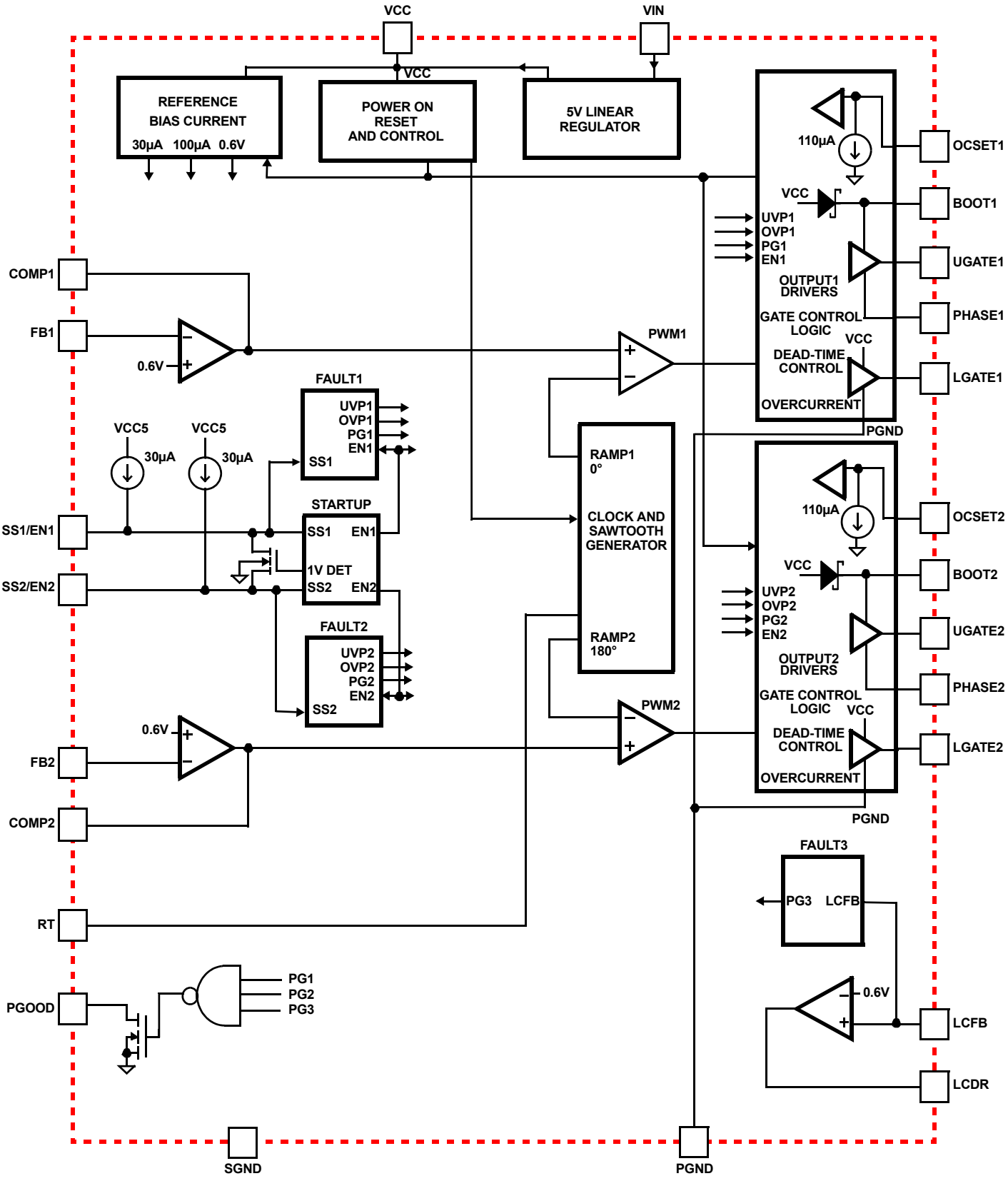


FIGURE 1. BLOCK DIAGRAM

Typical Application Schematics

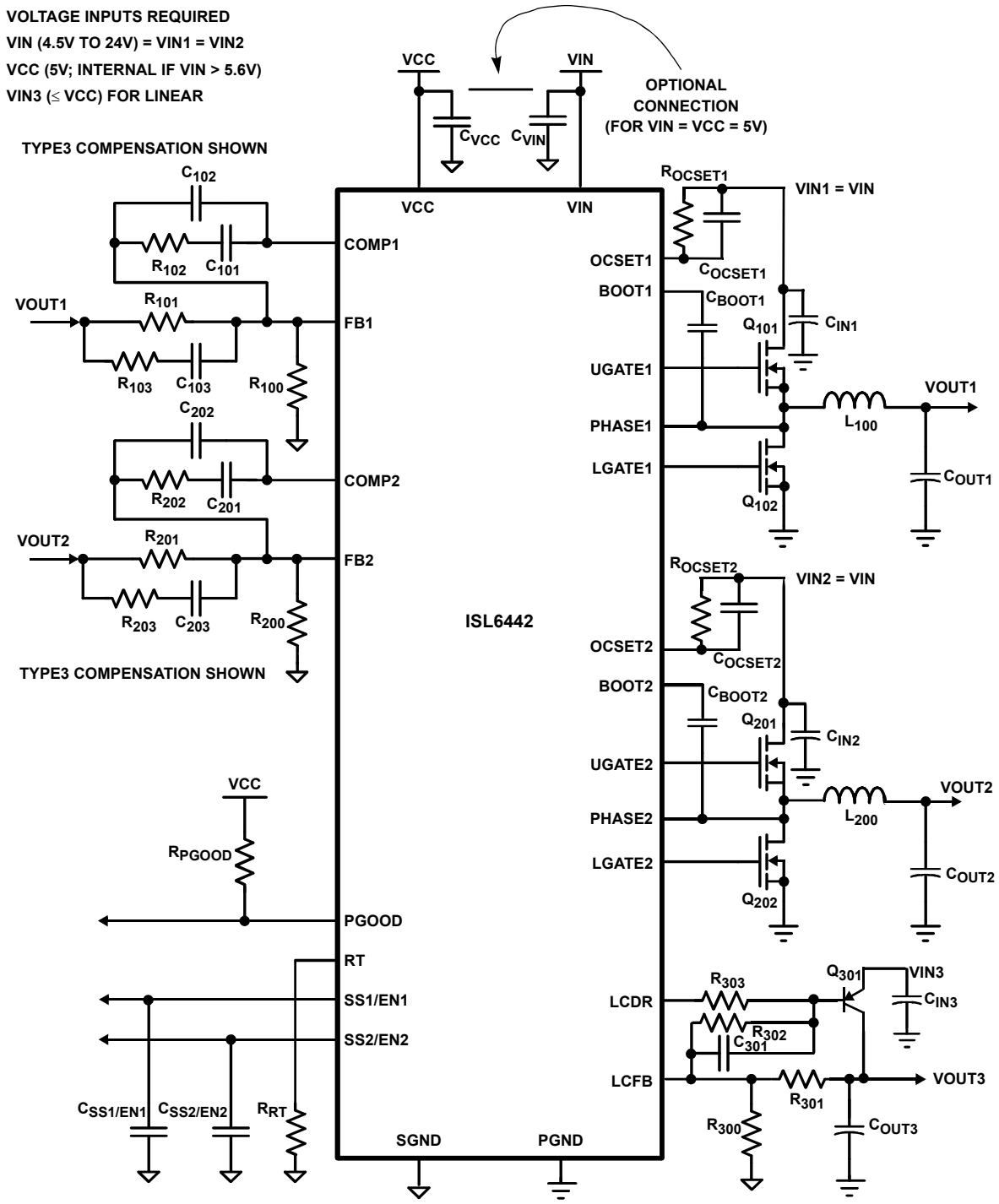


FIGURE 2. ISL6442 TYPICAL APPLICATION

Absolute Maximum Ratings (Note 1)

SS1/EN1, SS2/EN2, COMP1, COMP2 to SGND . . . -0.3V to +6.0V
VCC, FB1, FB2, RT, PGOOD to SGND . . . . . -0.3V to +6.0V
LCDR, LCFB to SGND. . . . . -0.3V to +6.0V
VIN, OCSET1, and OCSET2 to PGND . . . . . -0.3V to +28V
BOOT1 and BOOT2 to PGND . . . . . -0.3V to +33V
BOOT1 to PHASE1, and BOOT2 to PHASE2 . . . . . -0.3V to +6.0V
UGATE1 to PHASE1 . . . . . -0.3V to (BOOT1 +0.3V)
UGATE2 to PHASE2 . . . . . -0.3V to (BOOT2 +0.3V)
LGATE1, LGATE2 to PGND . . . . . -0.3V to (VCC+0.3V)
PHASE1, PHASE2 to PGND . . . . . -1V to 28V
SGND to PGND . . . . . -0.3V to 0.3V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
QSOP Package 85
Maximum Junction Temperature (Plastic Package). -55°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Temperature Range . . . . . -40°C to +85°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

VCC Supply Voltage . . . . . .5V ±10%
VIN Supply Voltage . . . . . 5.5V to 24V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. All voltages are measured with respect to GND.
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Operating Conditions Unless Otherwise Noted: VIN = 12V, or V_{CC} = 5V ±10%, T_A = -40°C to +85°C. Typical values are at +25°C. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIN SUPPLY						
Input Operating Supply Current	I_{CC_op}	VIN = 5.5V or 12V; $LGATE_x$, $UGATE_x$ Open, FB forced above regulation point (no switching)		4.5	7.5	mA
		VIN = 24V		50	70	mA
Input Standby Supply Current	I_{CC_sb}	VIN = 5.5V, 12V, 24V; SS1/EN1 = SS2/EN2 = 0V		1.25	2	mA
VCC INTERNAL REGULATOR						
Output Voltage	V_{VCC}	VIN > 5.5V	4.5	5.2	5.5	V
Maximum Output Current	I_{ICC_max}	VIN = 12V	80			mA
VCC Current Limit (Note 3)	I_{ICC_CL}	VCC is pulled to PGND; (Note 4)		300		mA
REFERENCE AND SOFT-START						
Reference Voltage at FB1, FB2	V_{REF1}, V_{REF2}	VIN = 5V or 12V; T_A = +25°C		0.6000		V
		VIN = 5V or 12V; T_A = 0°C to +85°C	0.5925		0.6085	V
		VIN = 5V or 12V; T_A = -40°C to +85°C	0.5900		0.6085	V
Reference Voltage at FB1, FB2	V_{REF1}, V_{REF2}	VIN = 24V; T_A = +25°C		0.6015		V
		VIN = 24V; T_A = 0°C to +85°C	0.5940		0.6100	V
		VIN = 24V; T_A = -40°C to +85°C	0.5915		0.6100	V
EN_x/SS_x Soft-Start Current	I_{SSx}		20	30	40	µA
EN_x/SS_x Enable Threshold	V_{ENx}		0.8	1.0	1.2	V
EN_x/SS_xEnable Threshold Hysteresis	V_{ENx_hys}	(Note 3)		50		mV
EN_x/SS_x Soft-Start Top of Ramp Voltage	V_{SSx_top}	(Note 3)		3.2		V
POWER-ON RESET ON VCC						
Rising Threshold	V_{POR_r}		4.2	4.4	4.475	V
Falling Threshold	V_{POR_f}		3.85	4.0	4.1	V

Electrical Specifications Operating Conditions Unless Otherwise Noted: VIN = 12V, or V_{CC} = 5V ±10%, T_A = -40°C to +85°C. Typical values are at +25°C. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM CONVERTERS						
Minimum UGATE on Time	t_{UGATE_min}	(Note 3)		100		ns
Maximum Duty Cycle	DC_{max}	VIN = 4.5 or 12V; F_{SW} = 300kHz	95			%
Maximum Duty Cycle	DC_{max}	VIN = 4.5V; F_{SW} = 2.5MHz	80			%
FB_x Pin Bias Current	I_{FBx}	(Note 3)		80		nA
OSCILLATOR						
Low End Frequency	F_{SW}	VIN = 5V or 12V; RT = 52.3kΩ	270	300	330	kHz
		VIN = 24V; RT = 52.3kΩ	270	305	340	kHz
High End Frequency	F_{SW}	VIN = 5V; RT = 5.23kΩ	2.25	2.5	2.75	MHz
		VIN = 12V; RT = 5.23kΩ	2.25	2.55	2.85	MHz
Frequency Adjustment Range	F_{SW}	RT = 52.3kΩ; (Note 3)		0.3		MHz
		RT = 5.23kΩ; (Note 3)		2.5		MHz
PWM Sawtooth Ramp Amplitude (Peak-to-Peak)	V_{P-P}	(Note 4)		1.25		V
PWM CONTROLLER GATE DRIVERS						
Gate Drive Peak Current		(Note 3)		0.7		A
Rise Time		(Note 3); C_L = 1000pF		20		ns
Fall Time		(Note 3); C_L = 1000pF		20		ns
Dead Time Between Drivers		(Note 3)		30		ns
ERROR AMPLIFIERS						
DC Gain	Gain	(Note 4)		88		dB
Gain-Bandwidth Product	GBWP	(Note 4)		15		MHz
Slew Rate	SR	(Note 4); COMP = 10pF		5		V/µs
Maximum Output Voltage	V_{EA_max}	VCC = 5V; RL = 10kΩ to ground	3.9	4.4		
PROTECTION and OUTPUT MONITOR						
Overvoltage Threshold	OV		113	116	121	%
Undervoltage Threshold	UV		78	82	88	%
OCSET Current Source	I_{OCSET}	V_{OCSET} = 4.5V	80	110	140	µA
LINEAR CONTROLLER						
Drive Sink Current	I_{LCDR}	LCDR	50			mA
LCFB Feedback Threshold	V_{LCFB}	T_A = +25°C		0.595		V
		T_A = -40°C to +85°C	0.570		0.620	V
		T_A = 0°C to +70°C	0.580		0.610	V
LCFB Input Leakage Current	I_{LCFB}	(Note 3)		80		nA
PGOOD						
Power-Good Lower Threshold	PG_low_x	LCFB = VCC, LDO disabled PGOOD for Ch1 and Ch2 only	88	91	94	%
Power-Good Higher Threshold	PG_hi_x	LCFB = VCC, LDO disabled PGOOD for Ch1 and Ch2 only	107	110	113	%

Electrical Specifications Operating Conditions Unless Otherwise Noted: VIN = 12V, or V_{CC} = 5V ±10%, T_A = -40°C to +85°C. Typical values are at +25°C. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power-Good Lower Threshold	PG_low_3	LDO enabled, PGOOD for LDO; Ch1 and Ch2 disabled; (Note 3)		75		%
PGOOD Delay	t_{PGOOD}	(Note 3); F_{SW} = 1.4MHz		370		ms
PGOOD Leakage Current	I_{PGOOD}	V_{PULLUP} = 5.5V			5	µA
PGOOD Voltage Low	V_{PG_low}	I_{PGOOD} = -4mA			0.5	V
THERMAL						
Shutdown Temperature		(Note 4)		150		°C
Shutdown Hysteresis		(Note 4)		20		°C

NOTES:

3. Limits established by characterization and are not production tested.
4. Design guideline only; not production tested.

Typical Performance Curves

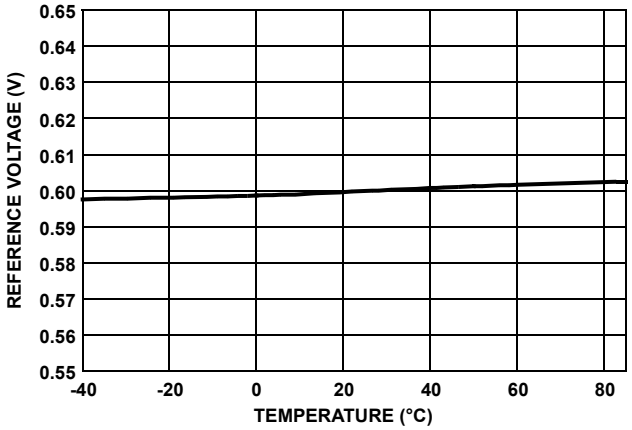


FIGURE 3. REFERENCE VOLTAGE VARIATION OVER TEMPERATURE

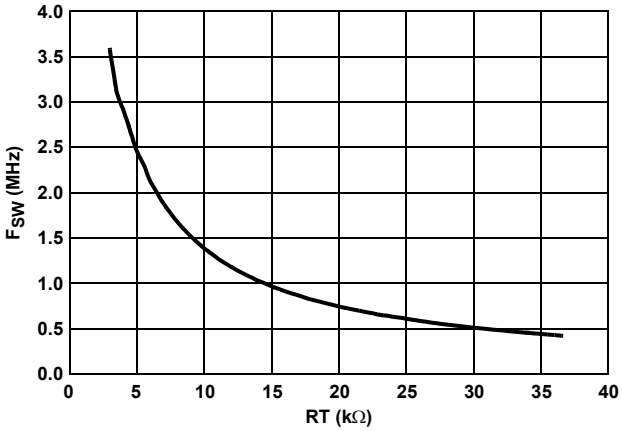


FIGURE 4. FREQUENCY vs RT RESISTOR

Pin Descriptions

BOOT1, 2 (Pins 23, 14) - These pins power the upper MOSFET drivers of each PWM converter. The anode of the each internal bootstrap diode is connected to the VCC pin. The cathode of the bootstrap diode is connected to this pin, which should also connect to the bootstrap capacitor.

UGATE1, 2 (Pins 22, 15) - These pins provide the gate drive for upper MOSFETs, bootstrapped from the VCC pin.

PHASE1, 2 (Pins 21, 16) - These are the junction points of the upper MOSFET sources, output filter inductor and lower MOSFET drains. Connect these pins accordingly to the respective converter.

LGATE1, 2 (Pins 20, 17) - These are the outputs of the lower N-Channel MOSFET drivers, sourced from the VCC pin.

PGND (Pin 18) - This pin provides the power ground connection for the lower gate drivers. This pin should be connected to the source of the lower MOSFET for PWM1 and PWM2 and the negative terminals of the external input capacitors.

FB1, 2 (Pins 4, 9) - These pins are connected to the feedback resistor divider and provide the voltage feedback signals for the respective controller. They set the output voltage of the converter. In addition, the PGOOD circuit and OVP circuit use these inputs to monitor the output voltage status.

COMP1, 2 (Pins 3, 10) - These pins are the error amplifier outputs for the respective PWM. They are used, along with the FB pins, as the compensation point for the PWM error amplifier.

PGOOD (Pin 13) - This is an open drain logic output used to indicate the status of the output voltages. This pin is pulled low when either of the two PWM outputs is not within 10% of the respective nominal voltage or when the linear output drops below 75% of its nominal voltage. To maintain the PGOOD function if the linear output is not used, connect LCFB to VCC.

SGND (Pin 6) - This is the signal ground, common to both controllers, and must be routed separately from the high current grounds (PGND). All voltage levels are measured with respect to this pin.

VIN (Pin 24) - This pin powers the controllers with an internal linear regulator (if VIN > 5.5V) and must be closely decoupled to ground using a ceramic capacitor as close to the VIN pin as possible. VIN is also the input voltage applied to the upper FET of both converters.

TABLE 1. INPUT SUPPLY CONFIGURATION

INPUT	PIN CONFIGURATION
5.5V to 24V	Connect the input supply to the VIN pin. The VCC pin will provide a 5V output from the internal voltage regulator.
5V ±10%	Connect the input supply to the VCC pin.

VCC (Pin 19) - This pin supplies the bias for the regulators, powers the low side gate drivers and external boot circuitry for high side gate drivers. The IC may be powered directly from a single 5V (±10%) supply at this pin; when used as a 5V supply input, this pin must be externally connected to VIN. When VIN > 5.5, VCC is the output of the internal 5V linear regulator output. The VCC pin must always be decoupled to power ground with a minimum of 1µF ceramic capacitor, placed very close to the pin.

RT (Pin 5) - This is the operating frequency adjustment pin. By placing a resistor from this pin to SGND, the oscillator frequency can be programmed from 300kHz to 2.5MHz.

SS1/EN1, 2 (Pins 2, 11) - These pins provide enable/disable and soft-start function for their respective controllers. The output is held off when the pin is pulled to the ground. When the chip is enabled, the regulated 30µA pull-up current source charges the capacitor connected from the pin to ground. The output voltage of the converter follows the ramping voltage on the SS/EN pin. Note that if either input is held low during power-up, neither channel will start a soft-start ramp until both are released. Once both outputs are running, then either one can be separately disabled and then enabled. But if both are disabled, that requires that both are released before either starts up. See ***Soft-Start and Voltage Tracking*** section for more details.

LCFB (Pin 8) - This pin is the feedback pin for the linear controller. An external voltage divider network connected to this pin sets the output voltage of the linear controller. If the linear controller is not used, tie this pin to VCC.

LCDR (Pin 7) - Open drain output PNP Transistor Driver. LCDR connects to the base of an external PNP pass transistor to form a positive linear regulator.

OCSET1, 2 (Pins 1, 12) - These pins are the overcurrent set points for the respective PWM controllers. Connect a resistor (R_{OCSET}) from this pin to the drain of the upper MOSFET. R_{OCSET}, an internal 100µA current source, and the upper MOSFET ON resistance $r_{DS(ON)}$ set the converter overcurrent (OC) trip point according to Equation 1:

$$I_{OC} = \frac{I_{OCSET} \bullet R_{OCSET}}{r_{DS(ON))}} \quad \text{(EQ. 1)}$$

I_{OC} includes the DC load current, as well as the ripple current. An overcurrent trip initiates hiccup mode.

Functional Description

Soft-Start and Voltage Tracking

After the VCC pin exceeds its rising POR trip point (nominal 4.4V), the chip operation begins. While the voltage on both SS1/EN1 and SS2/EN2 is below 1.0V, the internal switch between SS1/EN1 and SS2/EN2 is turned on so that the voltage across these two pins is the same. If either pin is held low externally, nothing happens until both pins are released.

Then both 30µA current sources will start charging up both capacitors in parallel. Once the voltage on both of these pins is above 1.0V, this internal switch is turned off and each 30µA internal current source charges its corresponding soft-start capacitor connected to its soft-start pin. The charging continues until the voltage across the soft-start capacitor reaches 3.2V. However, the output voltage reaches its regulation value when the soft-start capacitor voltage reaches 1.6V. Figure 5 shows the typical waveforms for SS2/EN2 and VOUT2; SS1/EN1 and VOUT1 are similar.

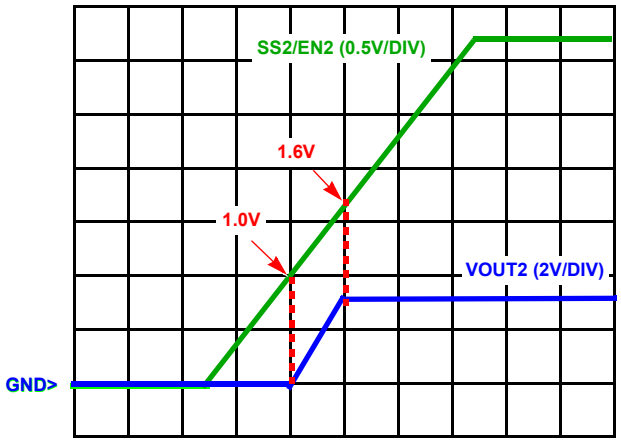


FIGURE 5. SOFT-START

The soft-start ramps for each output can be selected independently, but the ISL6442 also has voltage tracking capability. By selecting the soft-start capacitance to be proportional to the output voltage, the output voltage can be tracked. For example, in Figure 6, SS1 capacitor = 0.18µF and SS2 capacitor = 0.33µF, which match the output voltage ratio (1.8V and 3.3V). Therefore, the lower VOUT1 ramp will track with the VOUT2 ramp until they both reach 1.8V; VOUT1 then levels off, while VOUT2 continues rising towards 3.3V.

The basic timing equation is shown in Equation 2:

$$t = C \bullet \frac{dV}{I} \qquad \text{(EQ. 2)}$$

where:

t is the charge time

C is the external capacitance

dV is the voltage charged

I is the charging current (nominal 30µA)

From 0.0V to 1.0V, C = (C1 + C2 µF); dV = 1V; I = (30 + 30µA); for a 0.1µF capacitor on each pin, t = 3.3ms. This time represents the delay from when the soft-start ramp begins, until the output voltage ramp begins.

Then, from 1.0V to 1.6V, the outputs will ramp individually from zero to full-scale. Use the same equation to calculate the time for each ramp; now if V = 0.6V, C = 0.1µF, and I = 30µA, then t = 2ms.

Finally, there is a delay after 1.6V, until the ramp gets to ~3.2V, which signals that the ramp is done; when both ramps are done, the PGOOD delay begins.

Figure 7 shows a typical power-up sequence. VIN turns on and begins to ramp up; once VCC passes the rising POR trip point, the linear output is enabled (with no soft-start ramp). The SS1/EN1 pins also start charging (if not held low externally); after a delay for them to reach 1V, VOUT1 and VOUT2 begin to ramp; they are shown in tracking mode.

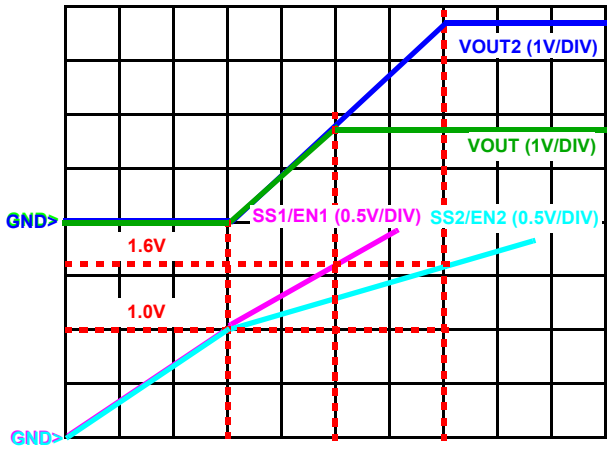


FIGURE 6. VOLTAGE TRACKING

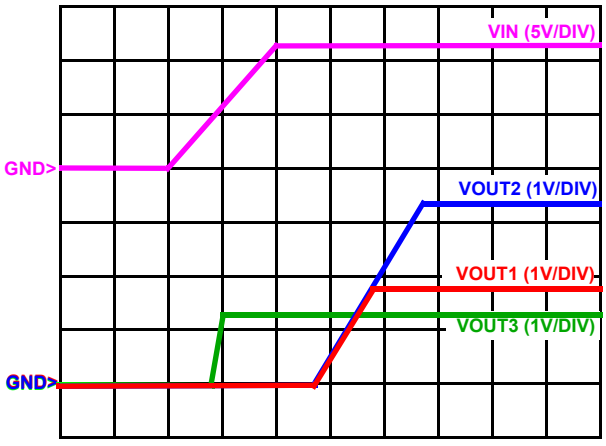


FIGURE 7. OUTPUT VOLTAGES

Figure 8 shows pre-biased outputs before soft-start. The solid blue curve shows no pre-bias; the output starts ramping from GND. The magenta dotted line shows the output pre-biased to a voltage less than the final output. The FETs don't turn on until the soft-start ramp voltage exceeds the output voltage; then the output starts ramping seamlessly from there. The cyan dotted line shows the output pre-biased above the final output (but below the OVP (Overvoltage Protection)). The FETs will not turn on until the end of the soft-start ramp; then the output will be quickly pulled down to the final value.

If the output is pre-biased above the OVP level, the ISL6442 will go into OVP at the end of soft-start, which will keep the FETs off. The output can recover if the voltage goes below the UV (Undervoltage) trip point, at which time a retry will occur. If successful, the output will ramp back up to the normal level.

VOUT1 has the same functionality as previously described for VOUT2. Each output should react independently of the other, unless they are related by the circuit configuration.

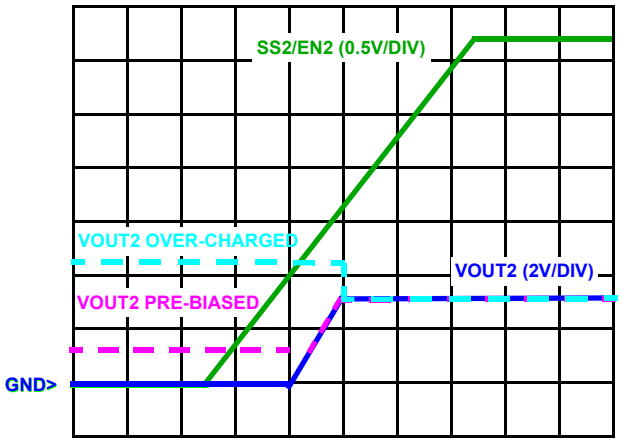


FIGURE 8. SOFT-START WITH PRE-BIAS

NOTE: Neither output cannot be independently disabled during power-up; both SS/EN pins are pulled low internally during POR, and due to the internal switch, neither will start charging if either pin is still held low. Once the outputs are running, either output can be disabled and then enabled again, without affecting the other one that's running. But if both SS/EN pins are held low at the same time, then the internal switch will turn on, and both SS/EN pins must be released before they both start to ramp.

The linear output does not have a soft-start ramp; however, it may follow the ramp of its input supply, if timed to coincide with its rise, after the VCC rising POR trip. If the input to the linear is from one of the two switcher outputs, then it will share the same ramp rate as the switcher.

PGOOD

A group of comparators (separate from the protection comparators) monitor the output voltages (via the FB pins) for PGOOD. Each switcher has an lower and upper boundary (nominally around 90% and 110% of the target value) and the linear has a lower boundary (around 75% of the target). Once both switcher output ramps are done, and all 3 outputs are within their expected ranges, the PGOOD will start an internal timer, with Equation 3:

$$t_{PGOOD} = \frac{0.5236}{F_{SW}} \quad \text{(EQ. 3)}$$

where:

t_{PGOOD} is the delay time (in sec)

F_{SW} is the switching frequency (in MHz)

Once the time-out is complete, the internal pull-down device will shut off, allowing the open-drain PGOOD output to rise through an external pull-up resistor, to a 5V (or lower) supply, which signals that the "Power is GOOD". Figure 9 shows the three outputs turning on, and the delay for PGOOD. If any of the conditions is subsequently violated, then PGOOD goes low. Once the voltage returns to the normal region, a new delay will start, after which the PGOOD will go high again.

The PGOOD delay is inversely proportional to the clock frequency. If the clock is running as slow as 524kHz, the delay will be one second long. There is no way to adjust the PGOOD delay independently of the clock.

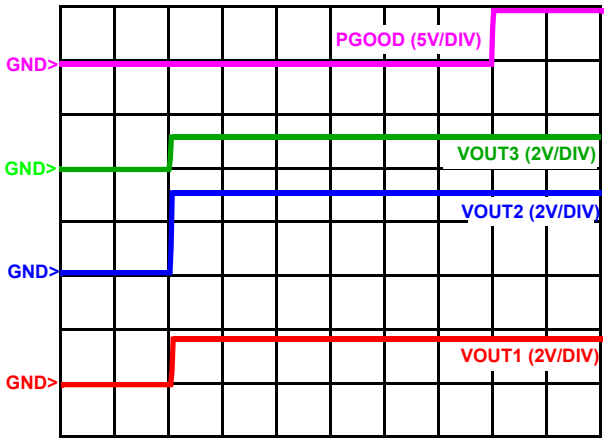


FIGURE 9. PGOOD DELAY

Monotonic Output

During soft-start period, the low side MOSFET is disabled to achieve monotonic output voltage when the inductor current is negative. This also allows ramping up into a pre-charged output voltage.

Switching Frequency

The switching frequency of the ISL6442 is determined by the external resistor placed from the RT pin to SGND. See Figure 10 for a graph of Frequency versus RT Resistance. The "Electrical Specifications" Table on page 5 lists a low end value of 52.3kΩ for 300kHz operation (not shown on graph). Running at both high frequency and high VIN voltages is not recommended, due to the increased power dissipation on-chip (mostly from the internal VCC regulator, which supplies gate drivers). The user should check the maximum acceptable IC temperature, based on their particular conditions.

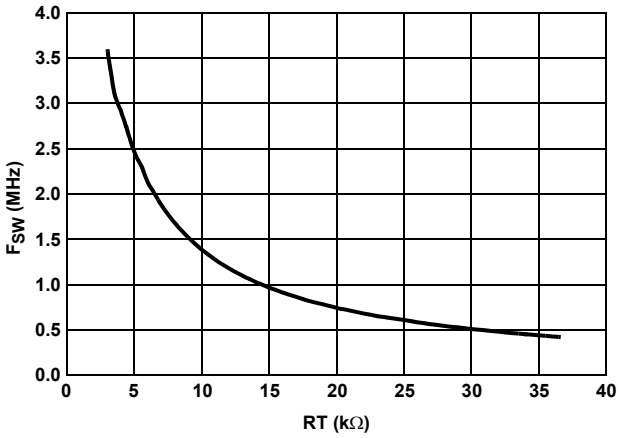


FIGURE 10. FREQUENCY vs RT RESISTOR

Output Regulation

Figure 11 shows the generic feedback resistor circuit for any of the three V_{OUT}'s; the V_{OUT} is divided down to equal the reference. All three use a 0.6V internal reference (check the "Electrical Specifications" Table on page 4 for the exact reference value at 24V). The R_{UP} is connected to the V_{OUT}; the R_{LOW} to GND; the common point goes to the FB pin.

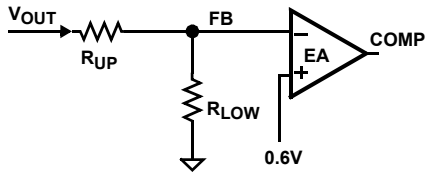


FIGURE 11. OUTPUT REGULATION

V_{OUT} must be greater than 0.6V and 2 resistors are needed, and their accuracy directly affect the regulator tolerance.

$$FB = V_{OUT} \cdot \frac{R_{LOW}}{R_{UP} + R_{LOW}} \quad \text{(EQ. 4)}$$

Use Equation 5 to choose the resistor values. R_{UP} is part of the compensation network for the switchers, and should be selected to be compatible; 1kΩ to 5kΩ is a good starting value. Find FB from the "Electrical Specifications" Table on page 5 (for the right condition), plug in the desired value for V_{OUT}, and solve for R_{LOW}.

$$R_{LOW} = \frac{FB \cdot R_{UP}}{V_{OUT} - FB} \quad \text{(EQ. 5)}$$

The maximum duty cycle of the ISL6442 approaches 100% at low frequency, but falls off at higher frequency; see the "Electrical Specifications" Table on page 5. In addition, there is a minimum UGATE pulse width, in order to properly sense overcurrent. The two switchers are 180° out of phase.

The linear output voltage is restricted to approximately a 1V to 4V range. VIN3 should be equal or less than VCC (in order to be sure that LCDR can turn off the PNP). Note that the linear output is off until the rising POR trips; it does not have a soft-start ramp, and it does NOT shut off, unless VCC goes back below the falling POR trip point. It is suggested that using one of the switcher outputs as the input to the linear allows it to be ramped and enabled/disabled with that switcher.

Protection Mechanisms

OCP - (Function independent for both PWM). The overcurrent function protects the PWM Converter from a shorted output by using the upper MOSFET's ON-resistance, $r_{DS(ON)}$ to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor. The overcurrent function cycles the soft-start function in a hiccup mode to provide fault protection. A resistor connected to the drain of the upper MOSFET and OCSET pin programs the overcurrent trip level. The PHASE node voltage will be compared against the voltage on the OCSET pin, while the upper MOSFET is on. A current (typically 110µA) is pulled from the OCSET pin to establish the OCSET voltage. If PHASE is lower than OCSET while the upper MOSFET is on then an overcurrent condition is detected for that clock cycle. The upper gate pulse is immediately terminated, and a counter is incremented. If an overcurrent condition is detected for 32 consecutive clock cycles, and the circuit is not in soft-start, the ISL6442 enters into the soft-start hiccup mode. During hiccup, the external capacitor on the SS/EN pin is discharged, then released and a soft-start cycle is initiated. During soft-start, pulse termination current limiting is enabled, but the 32-cycle hiccup counter is held in reset until soft-start is completed.

Figure 12 shows an example of the hiccup mode. As the SS2/EN2 is pulled below the enable trip point, VOUT2 shuts off, and the voltage goes to GND, at which time the output current goes to zero. As SS2/EN2 rises above the enable trip point, the output tries to turn on, the current spikes up, and then is held constant (by the pulse-termination current limiting); the output voltage rises, but not up to the desired value. When the SS2/EN2 ramp reaches ~3V, the cycle repeats, and can continue indefinitely. If the short-circuit is removed, the output will ramp up with the next soft-start, and normal operation will resume. VOUT1 and SS1/EN1 will independently function the same way.

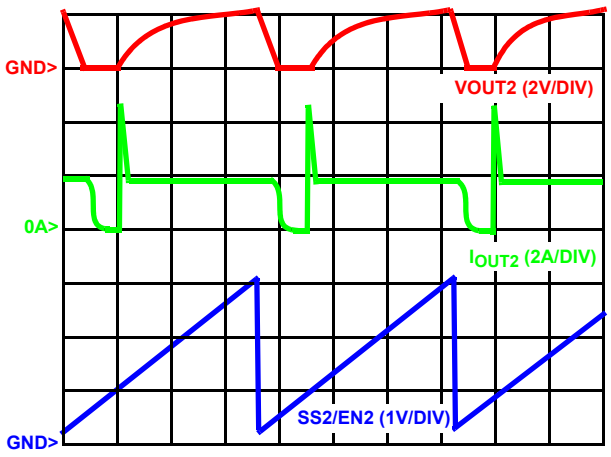


FIGURE 12. OVERCURRENT PROTECTION

UVP - (Function independent for both PWM). If the voltage on the FB pin falls to 82% (typical) of the reference voltage for 8 consecutive PWM cycles, then the circuit enters into soft-start hiccup mode. This mode is identical to the overcurrent hiccup mode. The UVP comparator is separate from the one sensing for PGOOD, which should have already detected a problem, before the UVP trips.

OVP - (Function independent for both PWM). If voltage on FB pin rises to 116% (typical) of the reference voltage, the lower gate driver is turned on continuously (with diode emulation enabled). If SS_DN (internal soft-start done signal) is true (not in soft-start) and the overvoltage condition continues for 32 consecutive PWM cycles, then that output is latched off with the gate drivers three-stated. The capacitor on the SS/EN pin will not be discharged. The switcher will restart when the SS/EN pin is externally driven below 1V, or if power is recycled to the chip, or when the voltage on the FB pin falls to the 82% (typical) undervoltage threshold - after 8 clock cycles the chip will enter soft-start hiccup mode. The hiccup mode is identical to the overcurrent hiccup mode. The OVP comparator is separate from the one sensing for PGOOD, which should have already detected a problem, before the OVP trips.

Application Guidelines

PWM Controller

DISCUSSION

The PWM must be compensated such that it achieves the desired transient performance goals, stability, and DC regulation requirements.

The first parameter that needs to be chosen is the switching frequency, F_{SW}. This decision is based on the overall size constraints and the frequency plan of the end equipment. Smaller space requires higher frequency. This allows the output inductor, input capacitor bank, and output capacitor bank to be reduced in size and/or value. The power supply must be designed such that the frequency and its distribution over component tolerance, time and temperature causes minimal interference in RF stages, IF stages, PLL loops, mixers, etc.

INDUCTOR SELECTION

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current, and the ripple voltage is a function of the ripple current. The ripple current and voltage are approximated by the following equations, where ESR is the output capacitance ESR value.

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_{SW} \bullet L} \bullet \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 6)}$$

$$\Delta V_{OUT} = \Delta I \times ESR \quad \text{(EQ. 7)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance value reduces the converter's response time to a load transient (and usually increases the DCR of the inductor, which decreases the efficiency). Increasing the switching frequency (F_{SW}) for a given inductor also reduces the ripple current and voltage.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6442 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_{OUT} \times I_{TRAN}}{V_{IN} - V_{OUT}} \quad \text{(EQ. 8)}$$

$$t_{FALL} = \frac{L_{OUT} \times I_{TRAN}}{V_{OUT}} \quad \text{(EQ. 9)}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. With a +5V input source, the worst case response time can be either at the application or removal of load and dependent upon the output voltage setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Finally, check that the inductor I_{sat} rating is sufficiently above the maximum output current (DC load plus ripple current).

OUTPUT CAPACITOR SELECTION

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not

to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements. Keep in mind that not all applications have the same requirements; some may need many ceramic capacitors in parallel; others may need only one.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

INPUT CAPACITOR SELECTION

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q1 (upper FET) turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q1 and the source of Q2 (lower FET).

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

SWITCHER MOSFET SELECTION

V_{IN} for the ISL6442 has a wide operating voltage range allowed, so both FETs should have a source-drain breakdown voltage (V_{DS}) above the maximum supply voltage expected; 20V or 30V are typical values available.

The ISL6442 gate drivers ($UGATE_x$ and $LGATE_x$) were designed to drive single FETs (for up to ~10A of load current) or smaller dual FETs (up to 4A). Both sets of drivers are sourced by the internal VCC regulator (unless $V_{IN} = V_{CC} = 5V$, in which case the gate driver current comes from the external 5V supply). The maximum current of the regulator (I_{CC_max}) is listed in the "Electrical Specifications" Table on page 4; this may limit how big the FETs can be. In addition, the power dissipation of the regulator is a major contributor to the overall IC power dissipation (especially as C_{in} of the FET or V_{IN} or F_{SW} increases).

Since V_{CC} is around 5V, that affects the FET selection in two ways. First, the FET gate-source voltage rating (V_{GS}) can be as low as 12V (this rating is usually consistent with the 20V or 30V breakdown chosen above). Second, the FETs must have a low threshold voltage (around 1V), in order to have its $r_{DS(ON)}$ rating at $V_{GS} = 4.5V$ in the 10mΩ to 40mΩ range that is typically used for these applications. While some FETs are also rated with gate voltages as low as 2.7V, with typical thresholds under 1V, these can cause application problems. As LGATE shuts off the lower FET, it does not take much ringing in the LGATE signal to turn the lower FET back on, while the Upper FET is starting to turn on, causing some shoot-through current. Therefore, avoid FETs with thresholds below 1V.

If the power efficiency of the system is important, then other FET parameters are also considered. Efficiency is a measure of power losses from input to output, and it contains two major components: losses in the IC (mostly in the gate drivers) and losses in the FETs. For low duty cycle applications (such as 12V in to 1.5V out), the upper FET is usually chosen for low gate charge, since switching losses are key, while the lower FET is chosen for low $r_{DS(ON)}$, since it is on most of the time. For high duty cycles (such as 5.0V in to 3.3V out), the opposite may be true.

Feedback Compensation Equations

This section highlights the design consideration for a voltage mode controller requiring external compensation. To address a broad range of applications, a type-3 feedback network is recommended (see Figure 13).

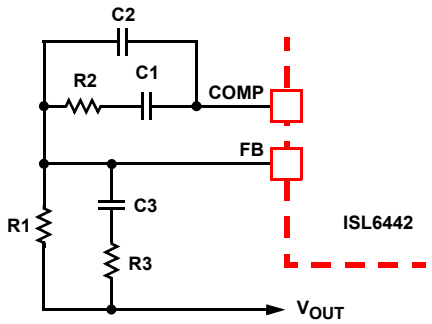


FIGURE 13. COMPENSATION CONFIGURATION FOR ISL6442 CIRCUIT

Figure 14 highlights the voltage-mode control loop for a synchronous-rectified buck converter, applicable to the ISL6442 circuit. The output voltage (V_{OUT}) is regulated to the reference voltage, V_{REF}. The error amplifier output (COMP pin voltage) is compared with the oscillator (OSC) modified sawtooth wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L and C). The output filter capacitor bank's equivalent series resistance is represented by the series resistor E.

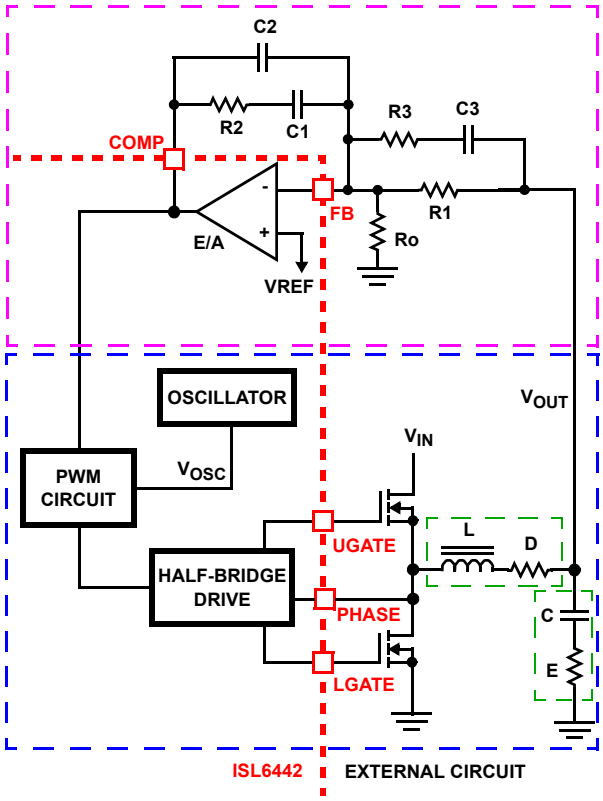


FIGURE 14. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC gain, given by $d_{MAX}V_{IN}/V_{OSC}$, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{CE}. For the purpose of this analysis, L and D represent the channel inductance and its DCR, while C and E represent the total output capacitance and its equivalent series resistance.

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \quad \text{(EQ. 10)}$$

$$F_{CE} = \frac{1}{2\pi \cdot C \cdot E} \quad \text{(EQ. 11)}$$

The compensation network consists of the error amplifier (internal to the ISL6442) and the external R1-R3, C1-C3 components. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (F_0; typically 0.1 to 0.3 of F_{SW}) and adequate phase margin (better than 45°). Phase margin is the difference between the closed loop phase at F_{0dB} and 180°. The equations that follow relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 14. Use the following guidelines for locating the poles and zeros of the compensation network:

1. Select a value for R1 (1kΩ to 5kΩ, typically). Calculate value for R2 for desired converter bandwidth (F_0). If setting the output voltage via an offset resistor connected to the FB pin, Ro in Figure 14, the design procedure can be followed as presented in Equation 12.

$$R2 = \frac{V_{OSC} \cdot R1 \cdot F_0}{d_{MAX} \cdot V_{IN} \cdot F_{LC}} \quad \text{(EQ. 12)}$$

2. Calculate C1 such that F_{Z1} is placed at a fraction of the F_{LC}, at 0.1 to 0.75 of F_{LC} (to adjust, change the 0.5 factor to desired number). The higher the quality factor of the output filter and/or the higher the ratio F_{CE}/F_{LC}, the lower the F_{Z1} frequency (to maximize phase boost at F_{LC}).

$$C1 = \frac{1}{2\pi \cdot R2 \cdot 0.5 \cdot F_{LC}} \quad \text{(EQ. 13)}$$

3. Calculate C2 such that F_{P1} is placed at F_{CE}.

$$C2 = \frac{C1}{2\pi \cdot R2 \cdot C1 \cdot F_{CE} - 1} \quad \text{(EQ. 14)}$$

4. Calculate R3 such that F_{Z2} is placed at F_{LC}. Calculate C3 such that F_{P2} is placed below F_{SW} (typically, 0.5 to 1.0 times F_{SW}). F_{SW} represents the switching frequency. Change the numerical factor to reflect desired placement of this pole. Placement of F_{P2} lower in frequency helps reduce the gain of the compensation network at high frequency, in turn reducing the HF ripple component at the COMP pin and minimizing resultant duty cycle jitter.

$$R3 = \frac{R1}{\frac{F_{SW}}{F_{LC}} - 1} \qquad C3 = \frac{1}{2\pi \cdot R3 \cdot 0.7 \cdot F_{SW}} \quad \text{(EQ. 15)}$$

It is recommended a mathematical model is used to plot the loop response. Check the loop gain against the error amplifier's open-loop gain. Verify phase margin results and adjust as necessary. The following equations describe the frequency response of the modulator (G_{MOD}), feedback compensation (G_{FB}) and closed-loop response (G_{CL}):

$$G_{MOD}(f) = \frac{d_{MAX} \cdot V_{IN}}{V_{OSC}} \cdot \frac{1 + s(f) \cdot E \cdot C}{1 + s(f) \cdot (E + D) \cdot C + s^2(f) \cdot L \cdot C} \quad \text{(EQ. 16)}$$

$$G_{FB}(f) = \frac{1 + s(f) \cdot R2 \cdot C1}{s(f) \cdot R1 \cdot (C1 + C2)} \cdot \frac{1 + s(f) \cdot (R1 + R3) \cdot C3}{(1 + s(f) \cdot R3 \cdot C3) \cdot \left(1 + s(f) \cdot R2 \cdot \left(\frac{C1 \cdot C2}{C1 + C2}\right)\right)} \quad \text{(EQ. 17)}$$

$$G_{CL}(f) = G_{MOD}(f) \cdot G_{FB}(f) \quad \text{(EQ. 18)}$$

where:

$$s(f) = 2\pi \cdot f \cdot j$$

COMPENSATION BREAK FREQUENCY EQUATIONS

$$F_{Z1} = \frac{1}{2\pi \cdot R2 \cdot C1} \quad \text{(EQ. 19)}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R1 + R3) \cdot C3} \quad \text{(EQ. 20)}$$

$$F_{P1} = \frac{1}{2\pi \cdot R2 \cdot \frac{C1 \cdot C2}{C1 + C2}} \quad \text{(EQ. 21)}$$

$$F_{P2} = \frac{1}{2\pi \cdot R3 \cdot C3} \quad \text{(EQ. 22)}$$

Figure 15 shows an asymptotic plot of the DC/DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown. Using the previously mentioned guidelines should yield a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} against the capabilities of the error amplifier. The closed loop gain, G_{CL}, is constructed on the log-log graph of Figure 15 by adding the modulator gain, G_{MOD} (in dB), to the feedback compensation gain, G_{FB} (in dB). This is equivalent to multiplying the modulator transfer function and the compensation transfer function and then plotting the resulting gain.

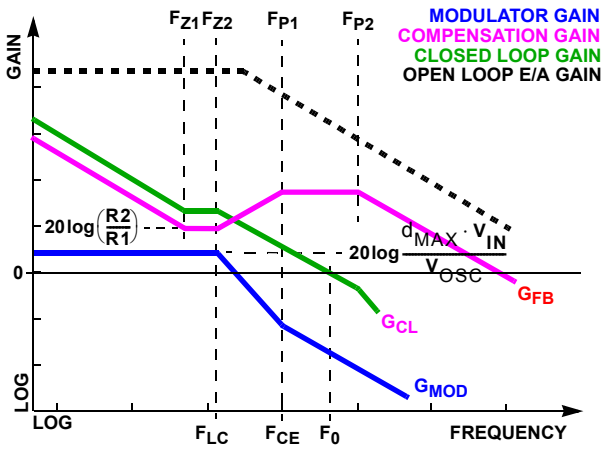


FIGURE 15. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

A stable control loop has a gain crossing with close to a -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin. The mathematical model presented makes a number of approximations and is generally not accurate at frequencies approaching or exceeding half the switching frequency. When designing compensation networks, select target crossover frequencies in the range of 10% to 30% of the switching frequency, F_{SW}.

Linear Regulator Compensation

DISCUSSION

The linear regulator controller controls an external pass element, typically a PNP bipolar junction transistor; see Figure 16 for reference. The error amplifier in the ISL6442 has approximately 72dB (V) of gain. The linear regulator circuit must be compensated such that the gain of the internal error amplifier crosses through 0dB with a slope of 20dB/decade. This allows easily predictable phase response through the 0dB point. The output circuit has a dominant pole determined by the output capacitance and the combination of the sense resistor and the output resistance of the BJT.

$$F_{P1} = \frac{1}{2\pi \bullet R_{OUT} \bullet C_{OUT}} \quad \text{(EQ. 23)}$$

where:

$$R_{OUT} = \frac{1}{\frac{1}{R301 + R302} + \frac{1}{r_o}} \quad \text{(EQ. 24)}$$

For most pass elements, r_o is approximately 100kΩ.

It also has a zero determined by the ESR value of the output capacitor and the Capacitance value of the output capacitor:

$$F_{Z1} = \frac{1}{2\pi \bullet R_{ESR} \bullet C_{OUT}} \quad \text{(EQ. 25)}$$

The compensation network is composed of R300, C300, the internal circuitry of the ISL6442, β (also know as h_{FE} in data sheets) of the pass element, and the Miller capacitance of the pass element. The pole is located at:

$$F_{P2} = \frac{1}{2\pi \bullet R_X \bullet C_X} \quad \text{(EQ. 26)}$$

where:

$$R_X = \frac{1}{\frac{1}{R300} + \frac{1}{1.20k\Omega} + \frac{1}{320\Omega \bullet \beta}} \quad \text{(EQ. 27)}$$

and:

$$C_X = C300 + 180pF + C_{Miller} \quad \text{(EQ. 28)}$$

If C_{Miller} is unspecified, use 1000pF.

The Zero is located at:

$$F_{Z2} = \frac{1}{2\pi \bullet ESR_{C300} \bullet C300} \quad \text{(EQ. 29)}$$

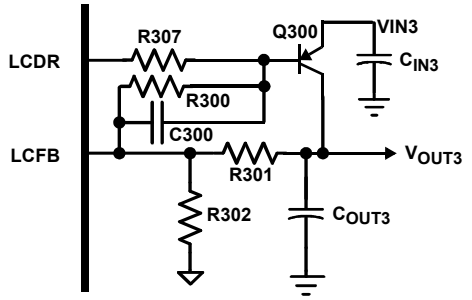


FIGURE 16. LINEAR COMPENSATION COMPONENTS

Strategy

1. The output capacitor of the linear regulator circuit must be chosen such that the ESR Zero is less than 200kHz:

$$F_{Z1} < 200kHz \quad \text{(EQ. 30)}$$

2. The voltage divider can be chosen to sink 250µA to 1.5mA of sense current, but this is simply a guideline, not a rule. The values should be chosen such that

$$R301 = \frac{V_{OUT3} - 0.6V}{I_{sen}} \quad \text{(EQ. 31)}$$

$$R302 = \frac{0.6V}{I_{sen}} \quad \text{(EQ. 32)}$$

where I_{sen} = is the current through the resistor divider, and 0.6V is the internal voltage reference that LCFB will equal.

3. Compute the pole and zero for the linear regulator circuit from Equations 31 and 32.
4. Make:

$$F_{P2} = \frac{F_{Z1}}{10} \quad \text{(EQ. 33)}$$

5. Fix R300 at 100Ω. Solve for C300. Use an MLCC, COG or NPO type capacitor for this value.

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding.

Figure 17 shows the critical power components of the converter. To minimize the voltage overshoot, the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in Figure 17 should be located as close together as possible. Please note that the capacitors C_{IN} and C_{OUT} each represent numerous physical capacitors. Locate the ISL6442 within 1 inch of the MOSFETs, Q1 and Q2. The circuit traces for the MOSFETs' gate and source connections from the ISL6442 must be sized to handle up to 2A peak current.

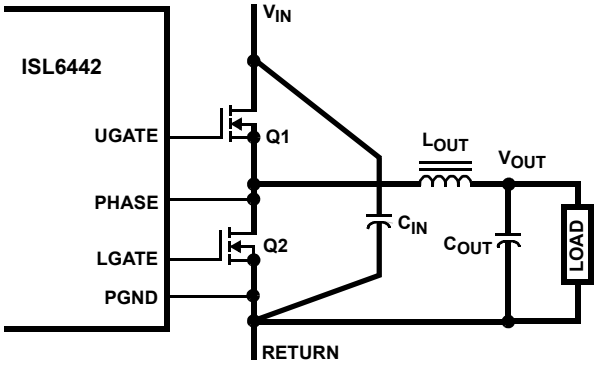


FIGURE 17. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

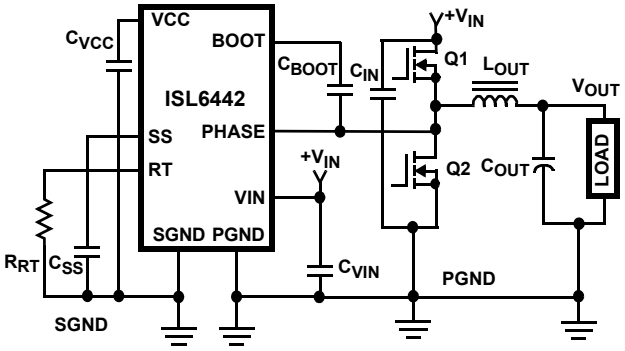


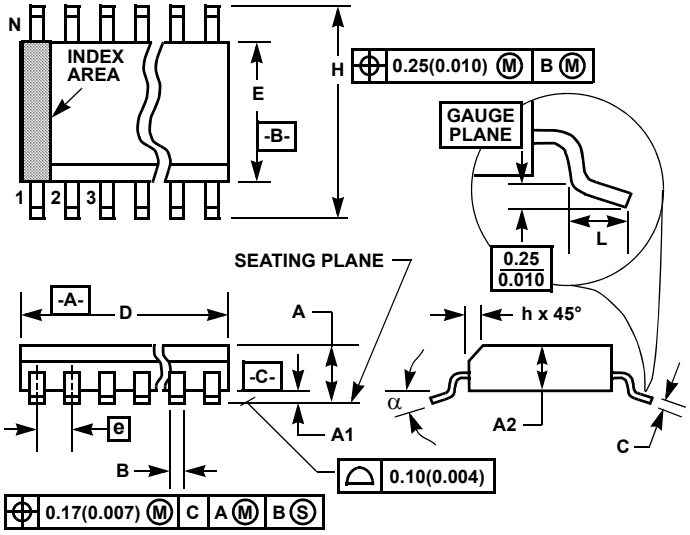
FIGURE 18. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

Figure 18 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Locate the RT resistor as close as possible to the RT pin and the SGND pin. Provide local decoupling between VCC and GND pins.

For each switcher, minimize any leakage current paths on the SS/EN pin and locate the capacitor, C_{SS} close to the SS/EN pin because the internal current source is only 30µA. All of the compensation network components for each switcher should be located near the associated COMP and FB pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins (but keep the noisy PHASE plane away from the IC (except for the PHASE pin connection).

The OCSET circuits (see Figure 2) should have a separate trace from the upper FET to the OCSET R and C; that will more accurately sense the VIN at the FET than just tying them to the VIN plane. The OCSET R and C should be placed near the IC pins.

Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M24.15

24 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150” WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.337	0.344	8.55	8.74	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

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