ISLA222S

Dual 12-bit, 250/200/125 MSPS JESD204B High Speed Serial Output ADC

FN8302
Rev 1.00
July 6, 2015

The ISLA222S is a series of low-power, high-performance, dual-channel 12-bit, analog-to-digital converters. Designed with FemtoCharge™ technology on a standard CMOS process, the series supports sampling rates of up to 250MSPS. The ISLA222S is part of a pin-compatible family of 12- and 14-bit dual-channel A/Ds with maximum sample rates ranging from 125MSPS to 250MSPS and shares the same analog core as Intersil's proven ISLA222P series of ADCs. The family minimizes power consumption while providing state of the art dynamic performance, offering an optimal performance vs power trade-off.

Differentiating the ISLA222S from the ISLA222P is its highly configurable, JESD204B-compliant, high-speed serial output link. The link offers data rates up to 4.375Gbps per lane and multiple packing modes. It can be configured to use one, two, or three lanes to transmit the conversion data, allowing for flexibility in the receiver design. The SERDES transmitter also provides deterministic latency and multi-chip time alignment support to satisfy an application's complex synchronization requirements.

A Serial Peripheral Interface (SPI) port allows for extensive configurability of the JESD204B transmitter including access to its built-in link and transport layer test patterns. The SPI port also provides control for numerous additional features including the fine gain and offset adjustments of the two ADC cores as well as the programmable clock divider, enabling 2x and 4x harmonic clocking.

The ISLA222S is available in a space saving 7mmx7mm 48 Ld QFN package. The package features a thermal pad for improved thermal performance and is specified over the full industrial temperature range (-40°C to +85°C).

Features

- JESD204A/B high-speed data interface
  - JESD204A compliant
  - JESD204B device subclass 0 compliant
  - JESD204B device subclass 2 compatible
  - Up to 3 JESD204 output lanes running up to 4.375Gbps
  - Highly configurable JESD204 transmitter
- Multiple chip time alignment and deterministic latency support (JESD204B device subclass 2)
- SPI programmable debugging features and test patterns
- 48-pin QFN 7mmx7mm package

Key Specifications

- SNR at 250/200/125MSPS

  70.6/71.2/71.7 dBFS f_{IN} = 30MHz

  70.3/70.7/70.9 dBFS f_{IN} = 190MHz
- SFDR at 250/200/125MSPS

  87/93/95 dBc f_{IN} = 30MHz

  84/93/86 dBc f_{IN} = 190MHz
- Total Power Consumption: 989mW at 250MSPS

Applications

- Radar and satellite antenna array processing
- Broadband communications and microwave receivers
- High-performance data acquisition
- Communications test equipment
- High-speed medical imaging

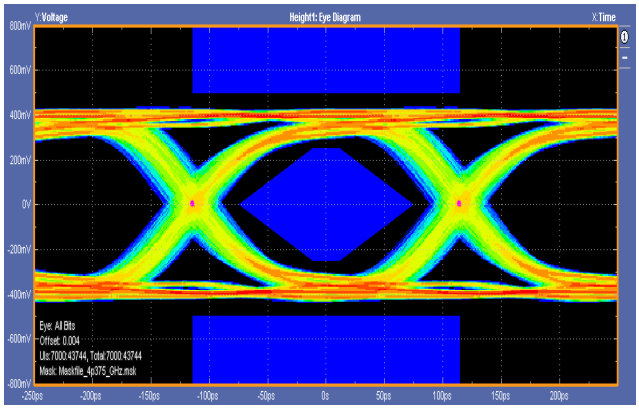


FIGURE 1. SERDES DATA EYE AT 4.375Gbps

Pin-compatible Family

MODEL	RESOLUTION	SPEED (MSPS)
ISLA224S25	14	250
ISLA224S20	14	200
ISLA224S12	14	125
ISLA222S25	12	250
ISLA222S20	12	200
ISLA222S12	12	125

Table of Contents

Block Diagram 3
Pin Configuration 3
Pin Descriptions 4
Absolute Maximum Ratings 5
Thermal Information 5
Recommended Operating Conditions 5
Electrical Specifications 5
Digital Specifications 8
Switching Specifications 8
Typical Performance Curves 10
Theory of Operation 15
Functional Description 15
Power-on Calibration 15
User Initiated Reset 16
Temperature Calibration 17
Analog Input 18
Clock Input 18
Jitter 19
Voltage Reference 19
Digital Outputs 19
Power Dissipation 19
Nap/Sleep 19
Data Format 20
Clock Divider Synchronous Reset 20
Soft Reset 20
JESD204 Transmitter 20
Overview 20
Initial Lane Alignment 21
Test Patterns 22
Serial Peripheral Interface 26
SPI Physical Interface 26
SPI Configuration 27
Device Information 27
Device Configuration/Control 27
Global Device Configuration/Control 28
ADDRESS 0xDF - 0xF3: JESD204 Registers 29
Address 0xDF-0xEE: JESD204 Parameter Interface 29
SPI Memory Map 31
Equivalent Circuits 35
ADC Evaluation Platform 36
Layout Considerations 36
Split Ground and Power Planes 36
Clock Input Considerations 36
Exposed Paddle 36
Bypass and Filtering 36
CML Outputs 36
Unused Inputs 36
Definitions 36
Revision History 37
About Intersil 37
Package Outline Drawing 38

Block Diagram

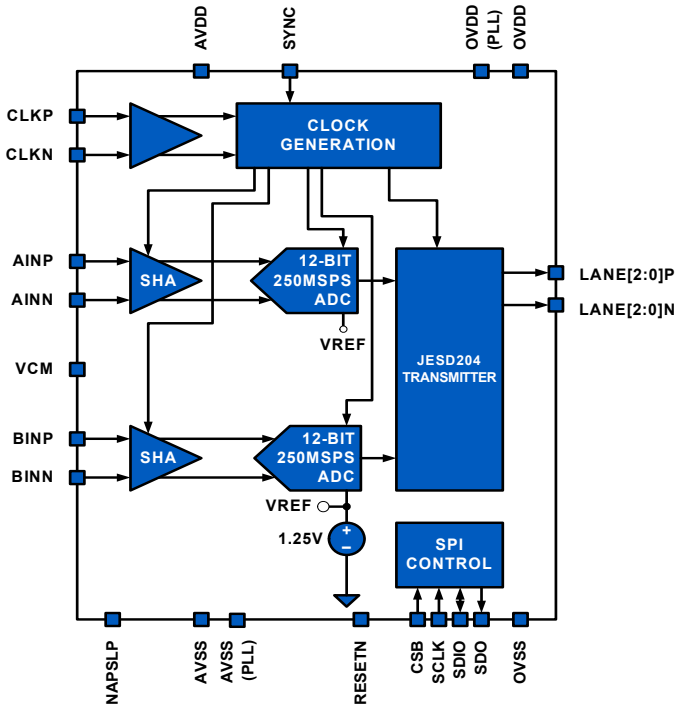
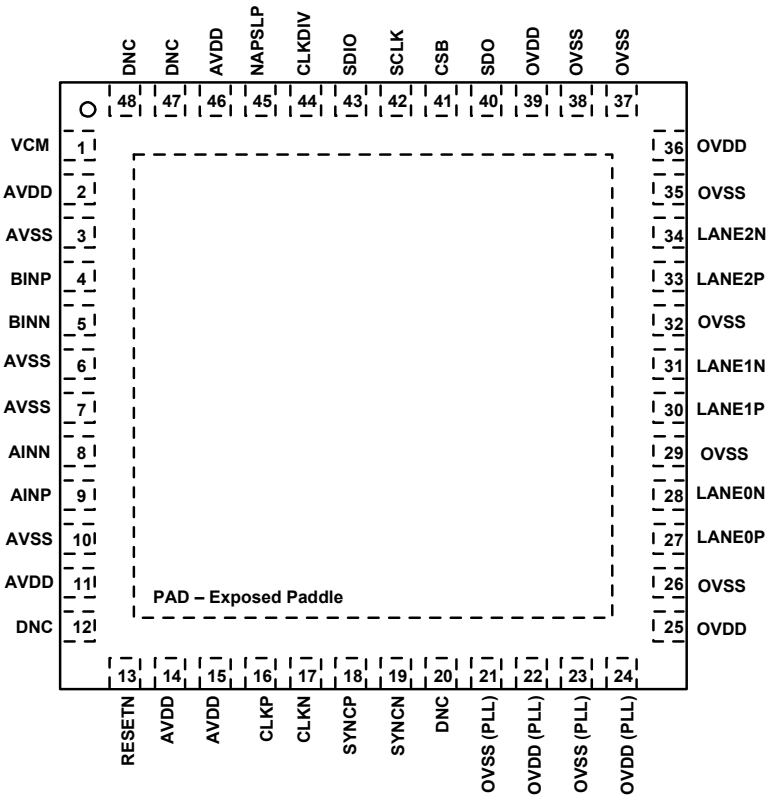


FIGURE 2. BLOCK DIAGRAM

Pin Configuration

ISLA222S
(48 LD QFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	NAME	FUNCTION
2, 11, 14, 15, 46	AVDD	1.8V Analog Supply
12, 20, 47, 48	DNC	Do Not Connect
3, 6, 7, 10	AVSS	Analog Ground
4, 5	BINP, BINN	B-Channel Analog Input Positive, Negative
8, 9	AINN, AINP	A-Channel Analog Input Negative, Positive
1	VCM	Common Mode Output
44	CLKDIV	Clock Divider Control
16, 17	CLKP, CLKN	Clock Input True, Complement
45	NAPSLP	Power Control (Nap, Sleep modes)
13	RESETN	Power On Reset (Active Low)
26, 29, 32, 35, 37, 38	OVSS	Output Ground
25, 36, 39	OVDD	1.8V Digital Supply
22, 24	OVDD (PLL)	1.8V Analog Supply for SERDES PLL
21, 23	OVSS (PLL)	Analog Ground Supply for SERDES PLL
18, 19	SYNCP, SYNCN	JESD204 SYNC Input
27, 28	LANE0P, LANE0N	SERDES Lane 0
30, 31	LANE1P, LANE1N	SERDES Lane 1
33, 34	LANE2P, LANE2N	SERDES Lane 2
40	SDO	SPI Serial Data Output
41	CSB	SPI Chip Select (active low)
42	SCLK	SPI Clock
43	SDIO	SPI Serial Data Input/Output
PAD	-	Exposed Paddle. Analog Ground (connect to AVSS)

Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISLA222S25IR1Z	ISLA222S25 IR1Z	-40 to +85	48 Ld QFN	L48.7x7G
ISLA222S20IR1Z	ISLA222S20 IR1Z	-40 to +85	48 Ld QFN	L48.7x7G
ISLA222S12IR1Z	ISLA222S12 IR1Z	-40 to +85	48 Ld QFN	L48.7x7G
ISLA224S25IR48EV1Z	FMC Based Evaluation Board (Supports 125/200/250 speed grades), Dual 14-bit Evaluation Board, which can be configured for 12-bit operation; Interfaces with ADCMB-HSFMCEV1Z Motherboard and Other FPGA Vendor FMC Based Evaluation Platforms.			
ADCMB-HSFMCEV1Z	FMC Based Motherboard			

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see device information page for ISLA222S12, ISLA222S20, ISLA222S25. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

AVDD to AVSS . . . . . -0.4V to 2.1V
OVDD to OVSS . . . . . -0.4V to 2.1V
AVSS to OVSS . . . . . -0.3V to 0.3V
Analog Inputs to AVSS . . . . . -0.4V to AVDD + 0.3V
Clock Inputs to AVSS . . . . . -0.4V to AVDD + 0.3V
Logic Input to AVSS . . . . . -0.4V to OVDD + 0.3V
Logic Inputs to OVSS . . . . . -0.4V to OVDD + 0.3V
Latch-up (Tested per JESD-78C; Class 2, Level A). 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld QFN (Notes 3, 4, 5)	24	0.4

Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Pb-free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Operating Temperature . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
5. For solder stencil layout and reflow guidelines, please see Tech Brief. TB389

Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -2dBFS, f_{SAMPLE} = Maximum Conversion Rate (per speed grade). **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	ISLA222S25			ISLA222S20			ISLA222S12			UNIT
			MIN (Note 6)	TYP	MAX (Note 6)	MIN (Note 6)	TYP	MAX (Note 6)	MIN (Note 6)	TYP	MAX (Note 6)	
DC SPECIFICATIONS												
Analog Input												
Full Scale Analog Input Range	V_{FS}	Differential	**1.9**	2.00	**2.1**	**1.9**	2.0	**2.1**	**1.9**	2.0	**2.1**	V_{P-P}
Input Resistance	R_{IN}	Differential		600			600			600		Ω
Input Capacitance	C_{IN}	Differential		7.4			7.4			7.4		pF
Full Scale Range Temp. Drift	A_{VTC}	Full Temp		115			58			58		ppm/°C
Input Offset Voltage	V_{OS}			±1			±1			±1		mV
Gain Error	E_G			1			1			1		%
Common-mode Output Voltage	V_{CM}			0.94			0.94			0.94		V
Common Mode Input Current (per pin)	I_{CM}			6.0			6.0			6.0		µA/MSPS
Clock Inputs												
Inputs Common Mode Voltage				0.9			0.9			0.9		V
CLKP, CLKN Swing				1.8			1.8			1.8		V
Power Requirements												
1.8V Analog Supply Voltage	AVDD			1.8			1.8			1.8		V
1.8V Digital Supply Voltage	OVDD			1.8			1.8			1.8		V
1.8V Analog Supply Current	I_{AVDD}			353	**397**		324	**365**		282	**316**	mA
1.8V Digital Supply Current	I_{OVDD}	Minimum number of lanes active		195	**218**		179	**200**		123	**173**	mA

Electrical Specifications All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -2dBFS, f_{SAMPLE} = Maximum Conversion Rate (per speed grade). **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	ISLA222S25			ISLA222S20			ISLA222S12			UNIT
			MIN (Note 6)	TYP	MAX (Note 6)	MIN (Note 6)	TYP	MAX (Note 6)	MIN (Note 6)	TYP	MAX (Note 6)	
Power Supply Rejection Ratio (Note 7)	PSRR	30MHz 200mV$_{P-P}$		40			40			40		dB
		1MHz 200mV$_{P-P}$		47			47			47		dB
Total Power Dissipation												
Normal Mode	P_D			989	**1107**		910	**1017**		731	**843**	mW
Nap Mode	P_D			422	**484**		391	**450**		290	**398**	mW
Sleep Mode	P_D	CSB at logic high		6	**12**		6	**12**		6	**12**	mW
Nap Mode Wakeup Time		Sample Clock Running		5			5			5		µs
Sleep Mode Wakeup Time		Sample Clock Running		1			1			1		ms
AC SPECIFICATIONS (Note 8)												
Differential Nonlinearity	DNL	f_{IN} = 105MHz No Missing Codes	**-1.0**	±0.15		**-1.0**	±0.1		**-1.0**	±0.1		LSB
Integral Nonlinearity	INL		**-1.5**	0.8	**1.5**	**-1.0**	0.4	**1.0**	**-1.0**	0.5	**1.0**	LSB
Minimum Conversion Rate (Note 9)	f_S MIN	ISLA222S25, ISLA222S20 (3 Lanes, Efficient Packing) ISLA222S12 (2 Lanes, Simple Packing)		100			100			50		MSPS
Maximum Conversion Rate	f_S MAX	Efficient Packing	**250**			**200**			**125**			MSPS
		Simple Packing										MSPS
Minimum Serdes Lane Data Rate		Independent of Packing Mode		1.0			1.0			1.0		GBPS
Maximum Serdes Lane Data Rate (See "Lane data rate" on page 22.)		Independent of Packing Mode	**3.75**	4.375		**3.0**	4.375		**3.75**	4.375		GBPS
Signal-to-noise Ratio (Note 10)	SNR	f_{IN} = 30MHz		70.6			71.2			71.7		dBFS
		f_{IN} = 105MHz	**69.4**	70.6		**70.3**	71.1		**70.7**	71.5		dBFS
		f_{IN} = 190MHz		70.3			70.7			70.9		dBFS
		f_{IN} = 363MHz		69.4			69.5			69.3		dBFS
		f_{IN} = 495MHz		68.6			68.5			68.0		dBFS
		f_{IN} = 605MHz		67.9			67.6			66.9		dBFS

Electrical Specifications All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), A_{IN} = -2dBFS, f_{SAMPLE} = Maximum Conversion Rate (per speed grade). **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	ISLA222S25			ISLA222S20			ISLA222S12			UNIT
			MIN (Note 6)	TYP	MAX (Note 6)	MIN (Note 6)	TYP	MAX (Note 6)	MIN (Note 6)	TYP	MAX (Note 6)	
Signal-to-noise and Distortion (Note 10)	SINAD	f_{IN} = 30MHz		70.5			71.1			71.7		dBFS
		f_{IN} = 105MHz	**69.0**	70.4		**70.2**	71.0		**70.4**	71.3		dBFS
		f_{IN} = 190MHz		70.0			70.5			70.7		dBFS
		f_{IN} = 363MHz		69.0			68.9			67.8		dBFS
		f_{IN} = 495MHz		65.4			64.0			61.4		dBFS
		f_{IN} = 605MHz		59.3			58.0			54.1		dBFS
Effective Number of Bits (Note 10)	ENOB	f_{IN} = 30MHz		11.42			11.52			11.61		Bits
		f_{IN} = 105MHz	**11.17**	11.40		**11.37**	11.50		**11.40**	11.55		Bits
		f_{IN} = 190MHz		11.34			11.42			11.46		Bits
		f_{IN} = 363MHz		11.16			11.16			10.97		Bits
		f_{IN} = 495MHz		10.57			10.34			9.91		Bits
		f_{IN} = 605MHz		9.56			9.35			8.69		Bits
Spurious-free Dynamic Range (Note 10)	SFDR	f_{IN} = 30MHz		87			93			95		dBc
		f_{IN} = 105MHz	**74**	83		**76**	89		**76**	87		dBc
		f_{IN} = 190MHz		84			93			86		dBc
		f_{IN} = 363MHz		79			88			71		dBc
		f_{IN} = 495MHz		66			85			61		dBc
		f_{IN} = 605MHz		58			83			52		dBc
Spurious-Free Dynamic Range Excluding H2, H3 (Note 10)	SFDRX23	f_{IN} = 30MHz		87			93			98		dBc
		f_{IN} = 105MHz		89			95			96		dBc
		f_{IN} = 190MHz		88			93			90		dBc
		f_{IN} = 363MHz		84			88			85		dBc
		f_{IN} = 495MHz		85			85			82		dBc
		f_{IN} = 605MHz		88			83			81		dBc
Intermodulation Distortion	IMD	f_{IN} = 70MHz		-84			-82			-81		dBFS
		f_{IN} = 170MHz		-92			-99			-100		dBFS
Channel-to-channel Isolation		f_{IN} = 10MHz		88			90			100		dB
		f_{IN} = 124MHz		82			87			86		dB
Word Error Rate	WER			10^{-13}			10^{-13}			10^{-13}		
Full Power Bandwidth	FPBW			675			675			675		MHz

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. PSRR is calculated by the equation 20*log10(A/B), where B is the amplitude of a disturber sinusoid on AVDD at the device pins, and A is the amplitude of the spur in the captured data at the frequency of the disturber sinusoid.
8. AC Specifications apply after internal calibration of the ADC is invoked at the given sample rate and temperature. Refer to "Power-on Calibration" on page 15 and "User Initiated Reset" on page 16 for more detail.
9. The DLL Range setting must be changed via SPI for ADC core sample rates below 80MSPS. The JESD204 transmitter can support ADC sample rates below 100MSPS, as long as the SERDES lane data rate is greater than or equal to 1Gbps.
10. Minimum specification guaranteed when calibrated at +85°C.

Digital Specifications **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
CMOS INPUTS						
Input Current High (RESETN)	I_{IH}	V_{IN} = 1.8V		1	**10**	µA
Input Current Low (RESETN)	I_{IL}	V_{IN} = 0V	**-25**	-12	**-7**	µA
Input Current High (SDIO, SCL, SDA SCLK)	I_{IH}	V_{IN} = 1.8V		4	**12**	µA
Input Current Low (SDIO, SCL, SDA SCLK)	I_{IL}	V_{IN} = 0V	**-600**	-400	**-300**	µA
Input Current High (CSB)	I_{IH}	V_{IN} = 1.8V	**40**	52	**70**	µA
Input Current Low (CSB)	I_{IL}	V_{IN} = 0V		1	**10**	µA
Input Voltage High (SDIO, RESETN)	V_{IH}		**1.17**			V
Input Voltage Low (SDIO, RESETN)	V_{IL}				**0.63**	V
Input Current High (NAPSLP, CLKDIV) (Note 11)	I_{IH}		**19**	25	**30**	µA
Input Current Low (NAPSLP, CLKDIV)	I_{IL}		**--30**	-25	**-19**	µA
Input Capacitance	C_{DI}			4		pF
LVDS INPUTS (SYNCP, SYNCN)						
Input Common Mode Range	V_{ICM}		**825**		**1575**	mV
Input Differential Swing (peak-to-peak, single-ended)	V_{ID}		**250**		**450**	mV
Input Pull-up and Pull-down Resistance	R_{Ipu}			100		kΩ
CML OUTPUTS						
Output Common Mode Voltage				1.14		V

Switching Specifications **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
ADC OUTPUT						
Aperture Delay	t_A			190		ps
RMS Aperture Jitter	j_A			100		fs
Synchronous Clock Divider Reset Recovery Time (Note 12)	t_{RSTRT}	DLL recovery time after Synchronous Reset		250		µs
Latency (ADC Pipeline Delay)	L			10		cycles
Overvoltage Recovery	t_{OVR}			1		cycles
SERDES						
PLL Lock Time				250		µs
PLL Bandwidth				2.2		MHz
Added Random Jitter				5		ps RMS
Added Deterministic Jitter				7		ps P-P
Maximum Input Sample Clock Total Jitter to Maintain SERDES BER <1E-12		Integrated from 1kHz to 10MHz offset from carrier		5		ps rms

Switching Specifications Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
LVDS Inputs						
SYNCP, SYNCN Setup Time (with Respect to the Positive Edge of CLKP)	t_{RSTS}	AVDD, OVDD = 1.7V to 1.9V, T_A = -40°C to +85°C	400	75		ps
SYNCP, SYNCN Hold Time (with respect to the positive edge of CLKP)	t_{RSTH}	AVDD, OVDD = 1.7V to 1.9V, T_A = -40°C to +85°C		150	350	ps
CML Outputs						
Output Rise Time	t_R			165		ps
Output Fall Time	t_F			145		ps
Data Output Duty Cycle				50		%
Differential Output Resistance				100		Ω
Differential Output Voltage (Note 13)				760		mV_{P-P}
SPI INTERFACE (Notes 14, 15)						
SCLK Period	t_{CLK}	Write Operation	**7**			cycles
	t_{CLK}	Read Operation	**16**			cycles
CSB↓ to SCLK↑ Setup Time	t_S	Read or Write	**2**			cycles
CSB↑ after SCLK↑ Hold Time	t_H	Read or Write	**5**			cycles
Data Valid to SCLK↑ Setup Time	t_{DS}	Read or Write	**6**			cycles
Data Valid after SCLK↑ Hold Time	t_{DH}	Read or Write	**4**			cycles
Data Valid after SCLK↓ Time	t_{DVR}	Read			**4**	cycles

NOTES:

11. The Tri-Level Inputs internal switching thresholds are approximately. 0.43V and 1.34V. It is advised to float the inputs, tie to ground or AVDD depending on desired function.
12. The synchronous clock divider reset function is available as a (SPI-programmable) overload on the SYNC input.
13. The voltage is expressed in peak-to-peak differential swing. The peak-to-peak single-ended swing is 1/2 of the differential swing.
14. The SPI interface timing is directly proportional to the ADC sample period (t_S). Values above reflect multiples of a 4ns sample period, and must be scaled proportionally for lower sample rates. ADC sample clock must be running for SPI communication.
15. The SPI may operate asynchronously with respect to the ADC sample clock.

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -2dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 250MSPS.

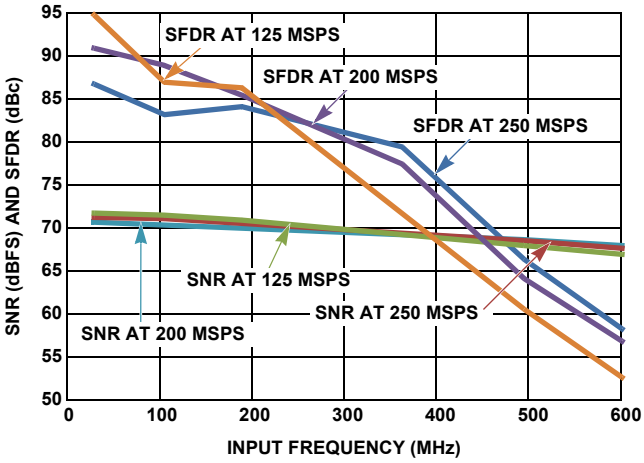


FIGURE 3. SNR AND SFDR vs f_{IN}

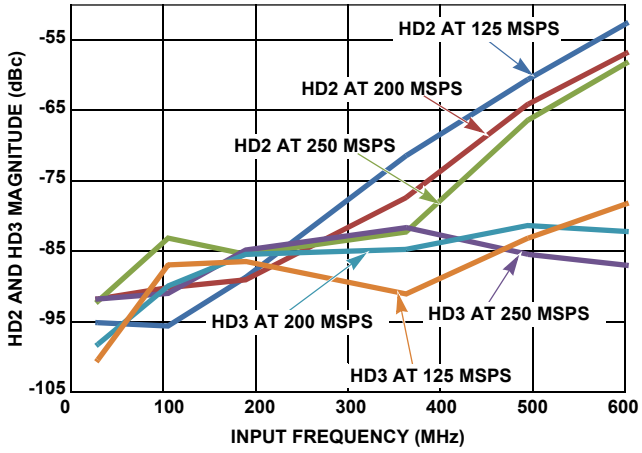


FIGURE 4. HD2 AND HD3 vs f_{IN}

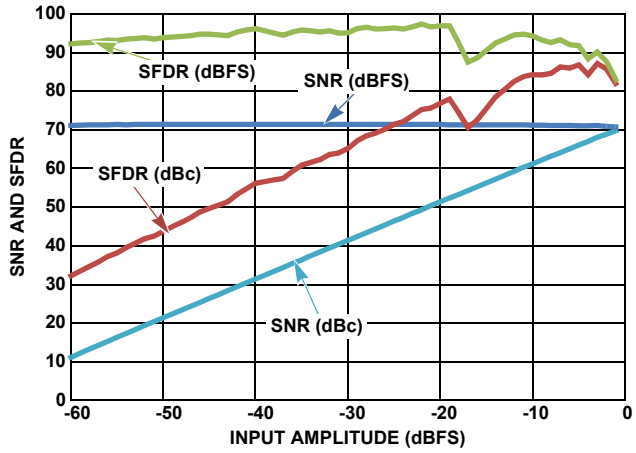


FIGURE 5. SNR AND SFDR vs A_{IN} (250MSPS)

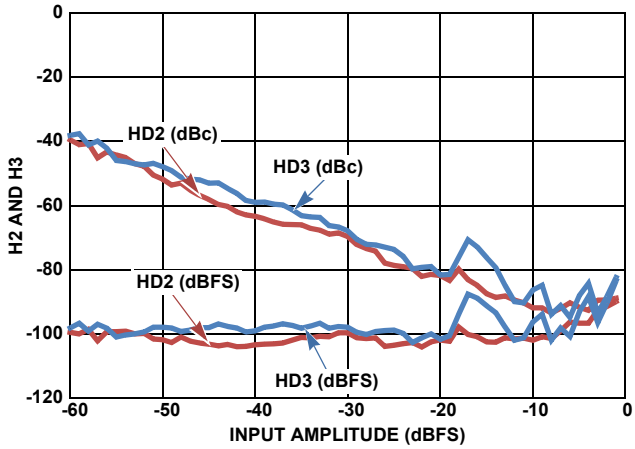


FIGURE 6. HD2 AND HD3 vs A_{IN} (250MSPS)

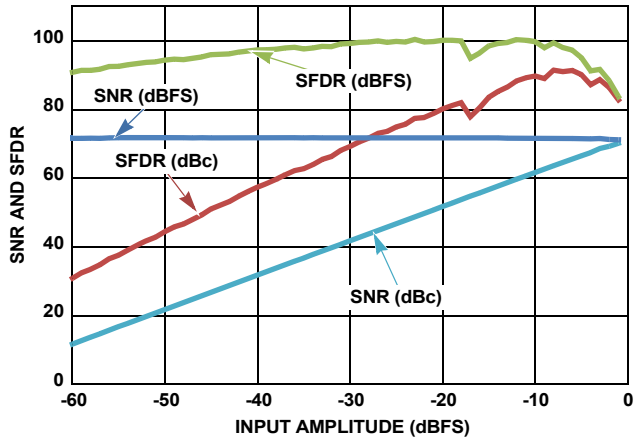


FIGURE 7. SNR AND SFDR vs A_{IN} (125MSPS)

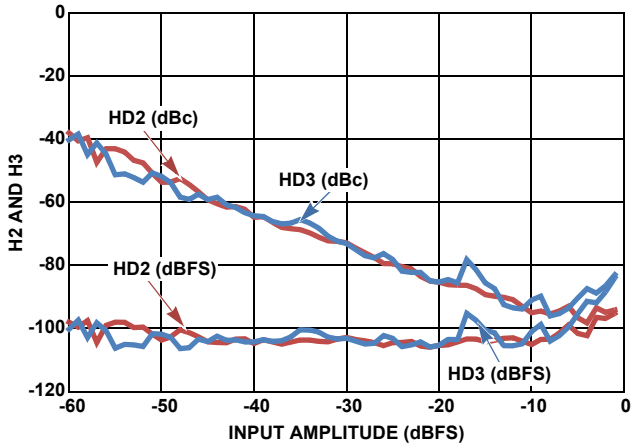


FIGURE 8. H2 AND H3 vs A_{IN} (125MSPS)

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -2dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 250MSPS. **(Continued)**

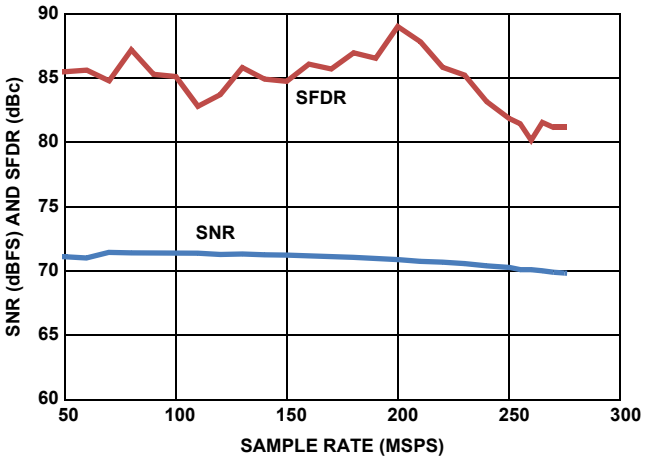


FIGURE 9. SNR AND SFDR vs f_{SAMPLE}

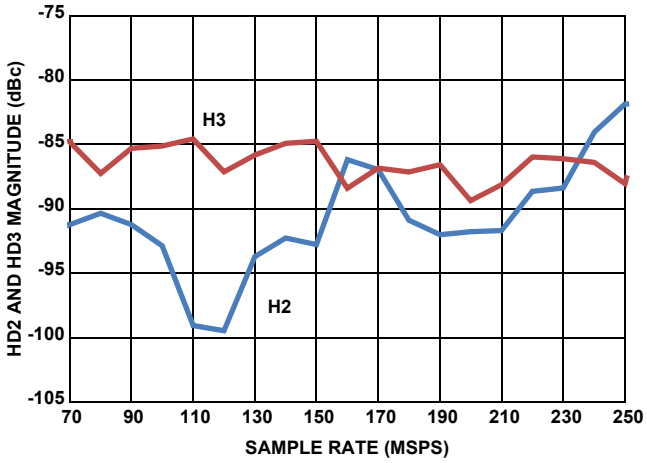


FIGURE 10. HD2 AND HD3 vs f_{SAMPLE}

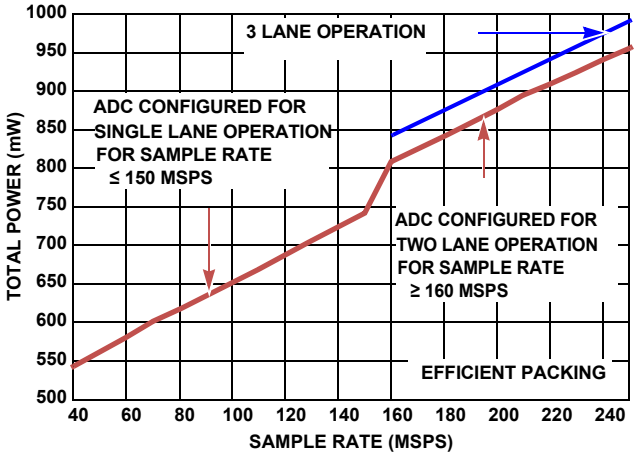


FIGURE 11. POWER vs f_{SAMPLE}

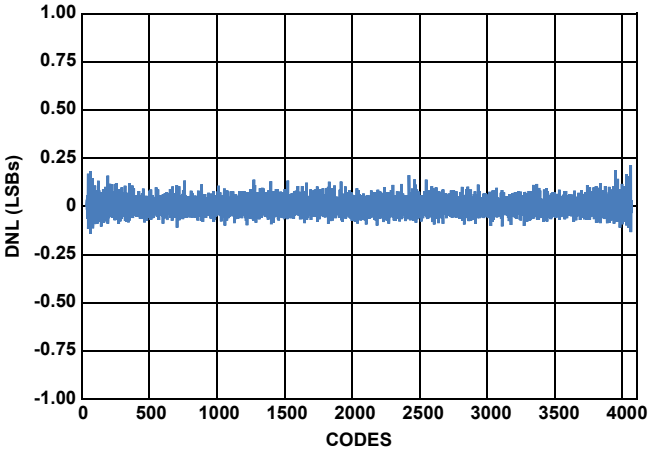


FIGURE 12. DIFFERENTIAL NONLINEARITY (250MSPS)

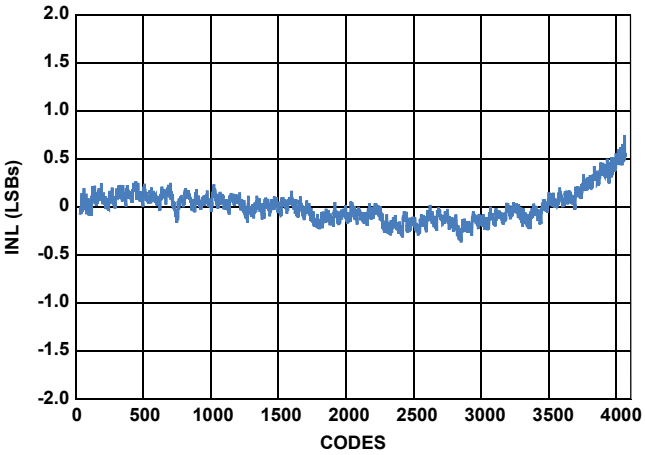


FIGURE 13. INTEGRAL NONLINEARITY (250MSPS)

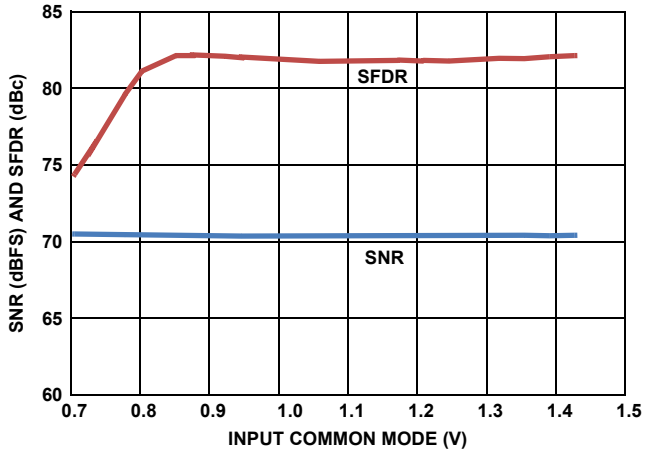


FIGURE 14. SNR AND SFDR vs VCM (250MSPS)

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -2dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 250MSPS. **(Continued)**

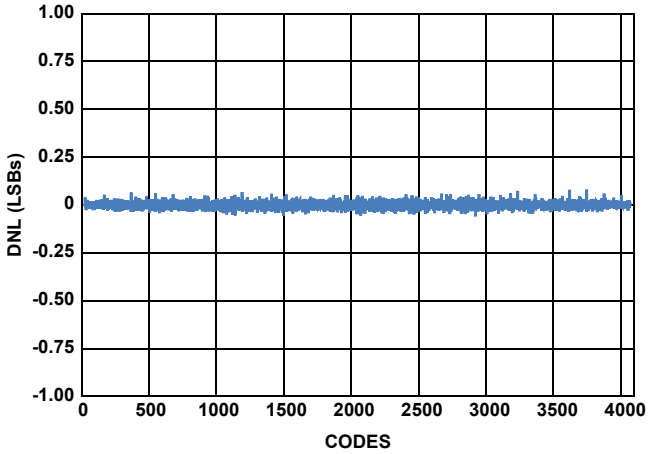


FIGURE 15. DIFFERENTIAL NONLINEARITY (125MSPS)

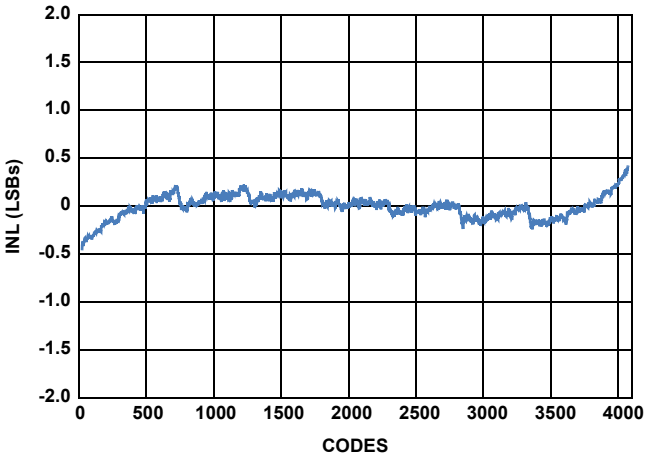


FIGURE 16. INTEGRAL NONLINEARITY (125MSPS)

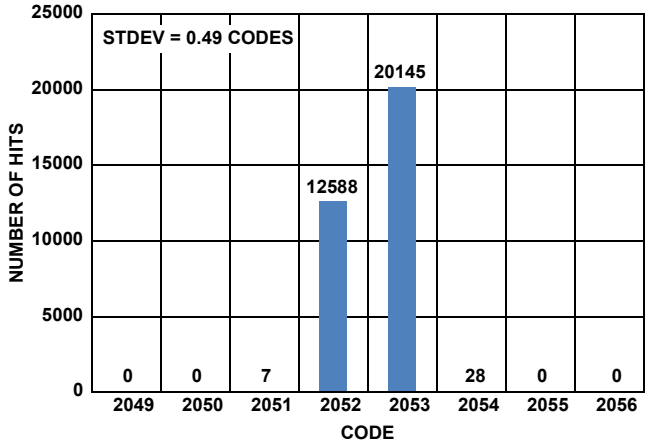


FIGURE 17. NOISE HISTOGRAM (250MSPS)

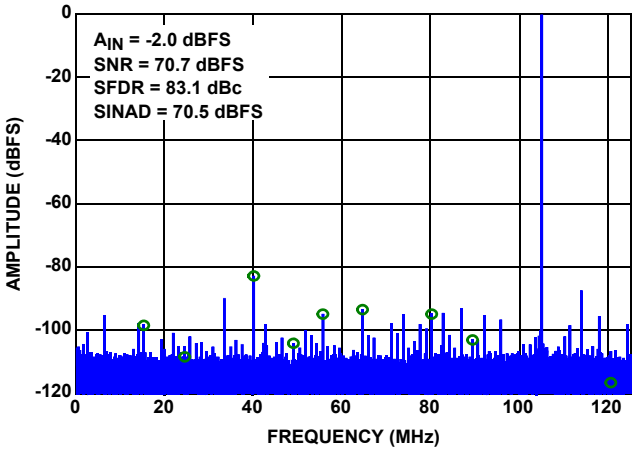


FIGURE 18. SINGLE-TONE SPECTRUM AT 105MHz (250MSPS)

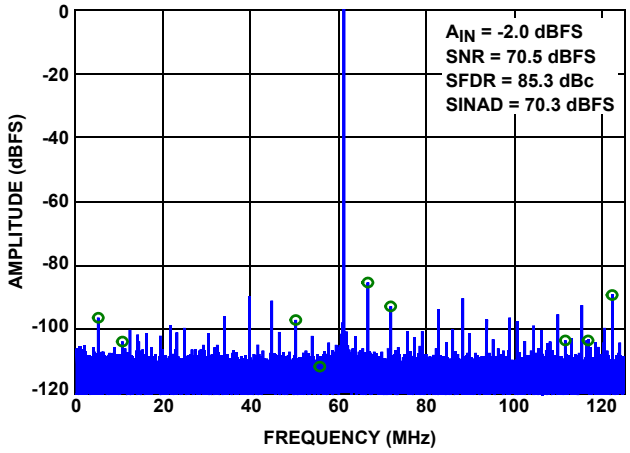


FIGURE 19. SINGLE-TONE SPECTRUM AT 190MHz (250MSPS)

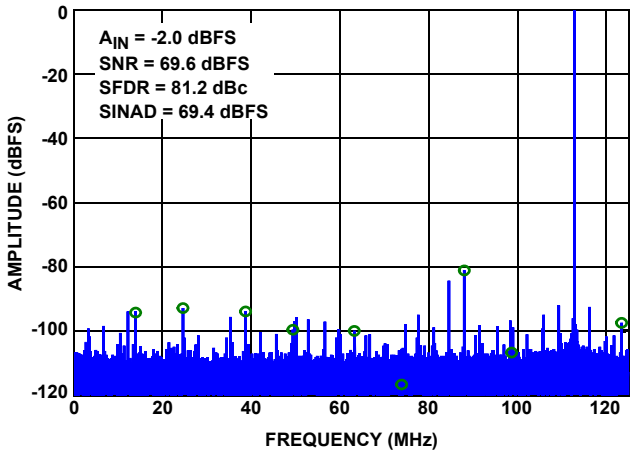


FIGURE 20. SINGLE-TONE SPECTRUM AT 363MHz (250MSPS)

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -2dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 250MSPS. **(Continued)**

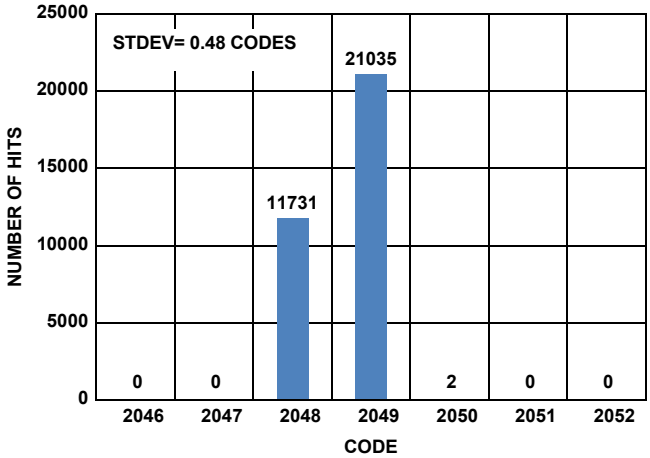


FIGURE 21. NOISE SPECTRUM (125MSPS)

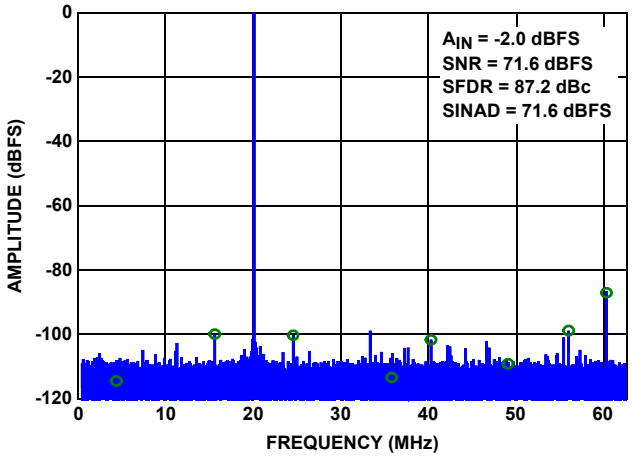


FIGURE 22. SINGLE-TONE SPECTRUM AT 105MHz (125MSPS)

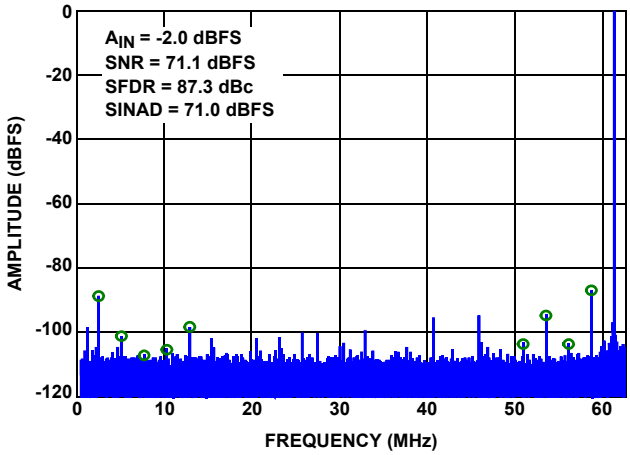


FIGURE 23. SINGLE-TONE SPECTRUM AT 190MHz (125MSPS)

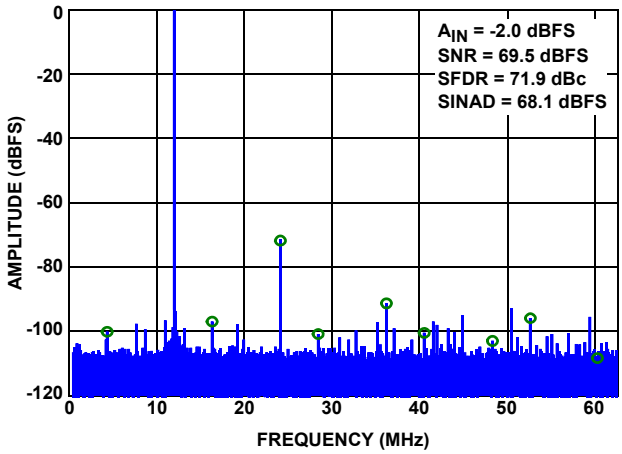


FIGURE 24. SINGLE-TONE SPECTRUM AT 363MHz (125MSPS)

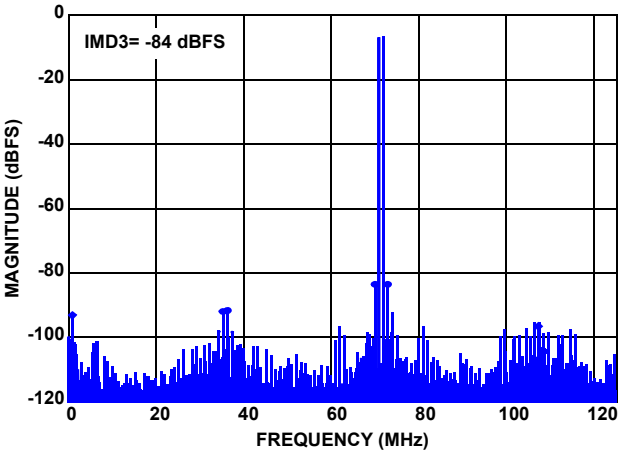


FIGURE 25. TWO-TONE SPECTRUM (F1 = 70MHz, F2 = 71MHz AT -7dBFS) (250MSPS)

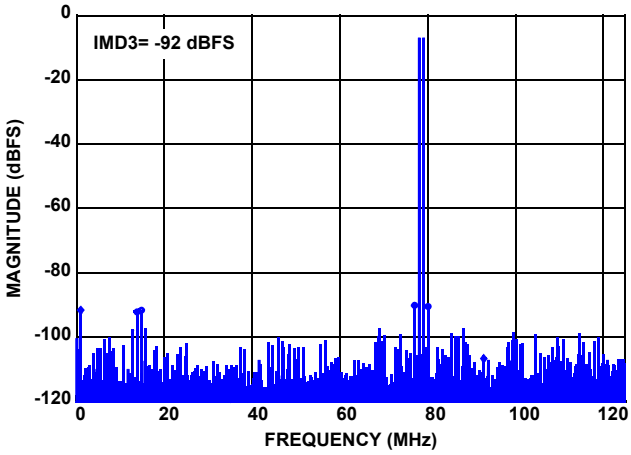


FIGURE 26. TWO-TONE SPECTRUM (F1 = 170MHz, F2 = 171MHz AT -7dBFS) (250MSPS)

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -2dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 250MSPS. **(Continued)**

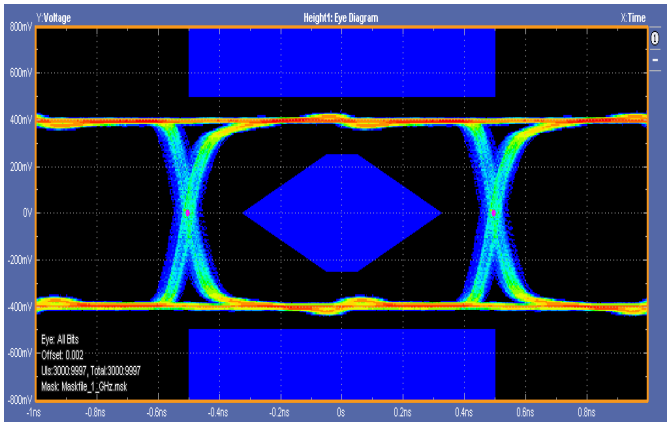


FIGURE 27. SERDES DATA EYE at 1.0Gbps

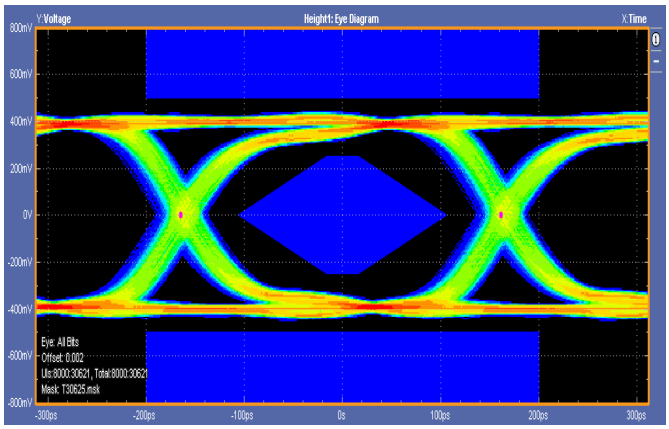


FIGURE 28. SERDES DATA EYE at 3.0Gbps

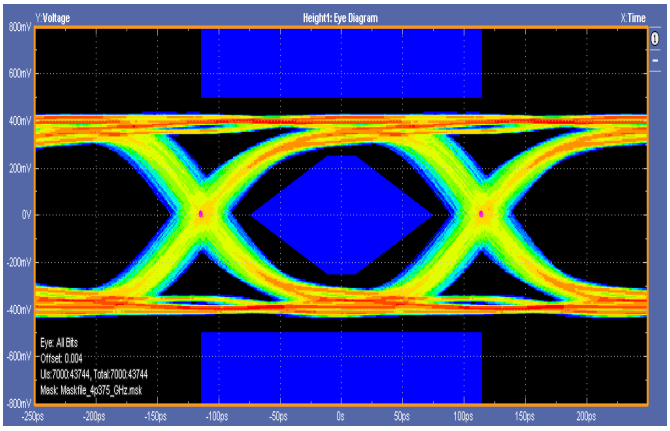


FIGURE 29. SERDES DATA EYE at 4.375Gbps

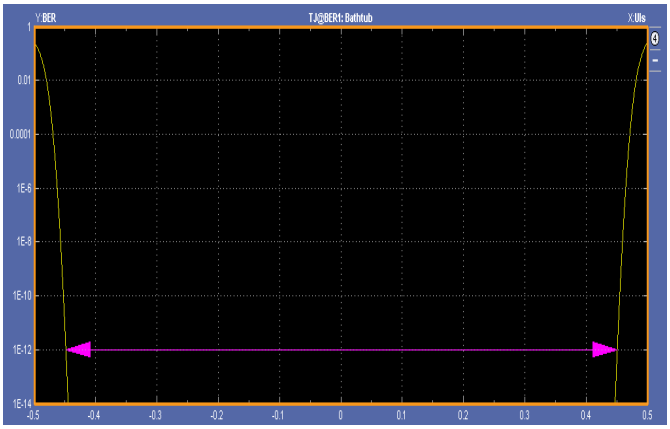


FIGURE 30. SERDES BATHTUB at 1.0Gbps

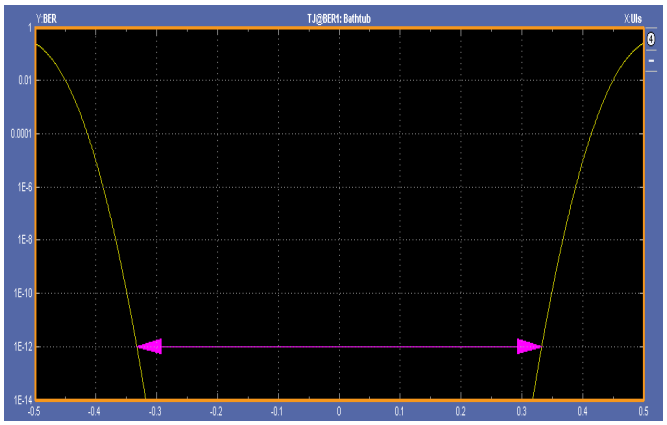


FIGURE 31. SERDES BATHTUB at 3.0Gbps

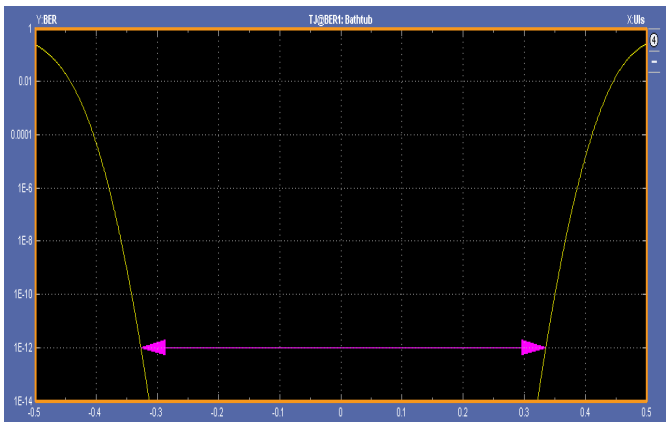


FIGURE 32. SERDES BATHTUB at 4.375Gbps

Typical Performance Curves

All Typical Performance Characteristics apply under the following conditions unless otherwise noted: AVDD = OVDD = 1.8V, T_A = +25°C, A_{IN} = -2dBFS, f_{IN} = 105MHz, f_{SAMPLE} = 250MSPS. **(Continued)**

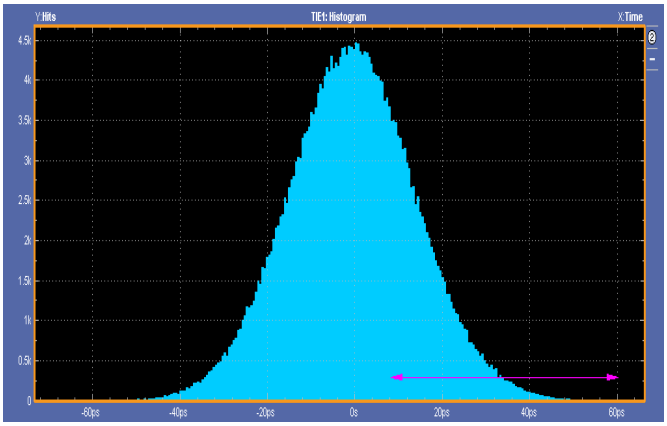


FIGURE 33. SERDES HISTOGRAM at 1.0Gbps

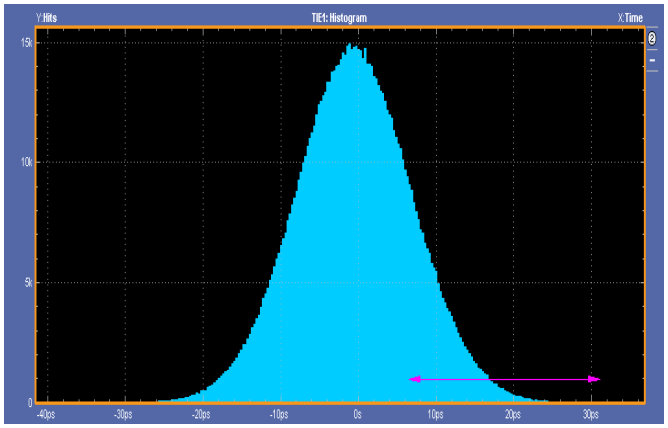


FIGURE 34. SERDES HISTOGRAM at 3.0Gbps

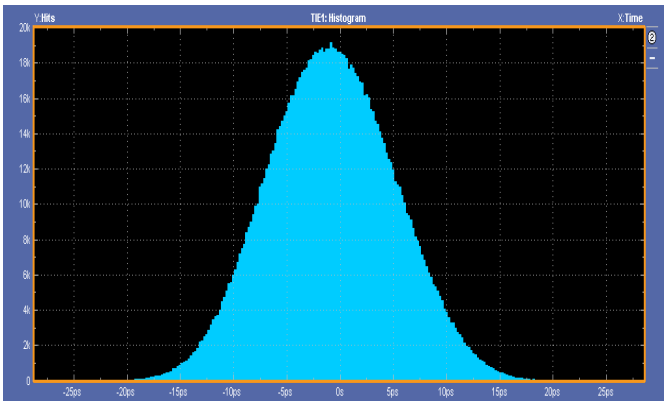


FIGURE 35. SERDES HISTOGRAM at 4.375Gbps

Theory of Operation

Functional Description

The ISLA222S is based upon a 12-bit, 250MSPS ADC converter core that utilizes a pipelined successive approximation architecture (see Figure 36). The input voltage is captured by a Sample-hold Amplifier (SHA) and converted to a unit of charge. Proprietary charge-domain techniques are used to successively compare the input to a series of reference charges. Decisions made during the successive approximation operations determine the digital code for each input value. Digital error correction is also applied.

Power-on Calibration

The ADC core(s) perform a self-calibration at start-up. An internal Power-on-reset (POR) circuit detects the supply voltage ramps and initiates the calibration when the analog and digital supply voltages are above a threshold. The following conditions must be adhered to for the power-on calibration to execute successfully:

- A frequency-stable conversion clock must be applied to the CLKP/CLKN pins
- DNC pins must not be connected
- SDO has an internal pull-up and should not be driven externally
- RESETN is pulled low by the ADC internally during POR. External driving of RESETN is optional.
- SPI communications must not be attempted during calibration, with the only exception of performing read operations on the cal_done register at address 0xB6.

A user-initiated reset can subsequently be invoked in the event that the above conditions cannot be met at power-up.

After the power supply has stabilized, the internal POR releases RESETN and an internal pull-up pulls it high, which starts the calibration sequence. If a subsequent user-initiated reset is desired, the RESETN pin should be connected to an open-drain driver with an off-state/high impedance state leakage of less

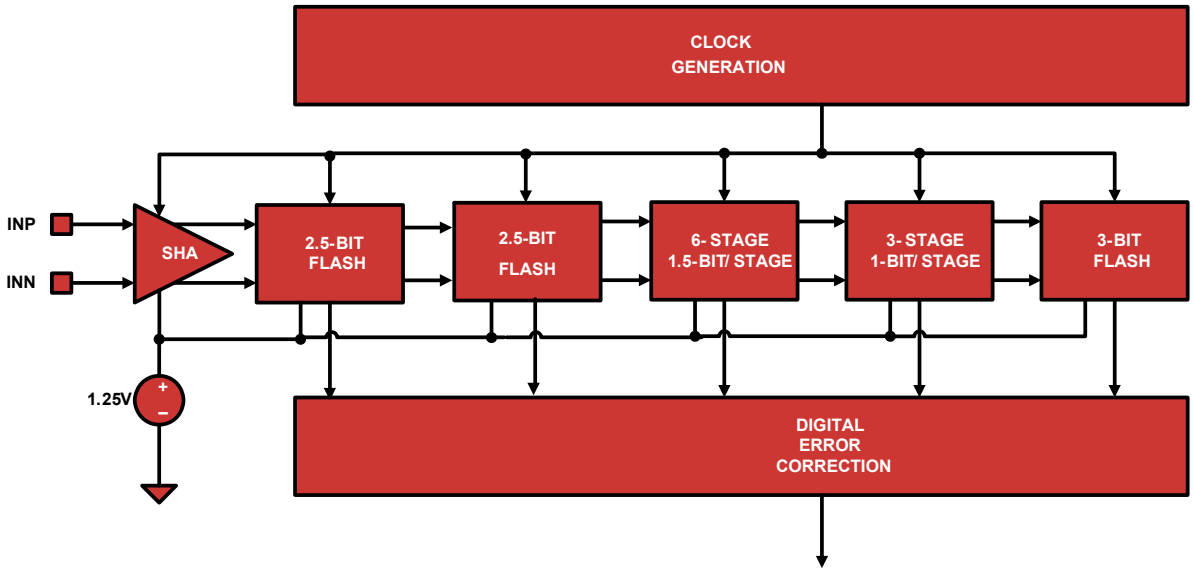


FIGURE 36. ADC CORE BLOCK DIAGRAM

than 0.5mA to assure exit from the reset state so calibration can start.

The calibration sequence is initiated on the rising edge of RESETN, as shown in Figure 37. Calibration status can be determined by reading the cal_status bit (LSB) at 0xB6. This bit is ‘0’ during calibration and goes to a logic ‘1’ when calibration is complete. During calibration the JESD204 transmitter PLL is not locked to the ADC sample clock, so the CML outputs will toggle at an undetermined rate. Normal operation is resumed once calibration is complete.

At 250MSPS the nominal calibration time is 280ms, while the maximum calibration time is 550ms.

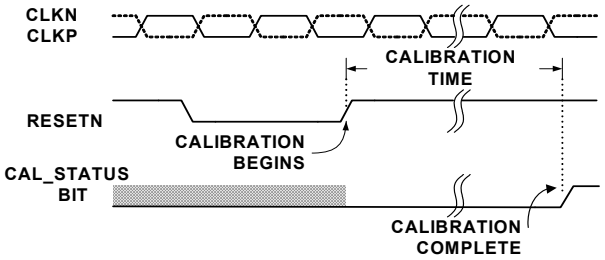


FIGURE 37. CALIBRATION TIMING

User Initiated Reset

Recalibration of the ADC can be initiated at any time by driving the RESETN pin low for a minimum of one clock cycle. An open-drain driver with a drive strength in its high impedance state of less than 0.5mA is recommended, as RESETN has an internal high impedance pull-up to OVDD. As is the case during power-on reset, RESETN and DNC pins must be in the proper state for the calibration to successfully execute.

The performance of the ISLA222S changes with variations in temperature, supply voltage or sample rate. The extent of these changes may necessitate recalibration, depending on system performance requirements. Best performance will be achieved by recalibrating the ADC under the environmental conditions at which it will operate.

A supply voltage variation of <100mV will generally result in an SNR change of <0.5dBFS and SFDR change of <3dBc. In situations where the sample rate is not constant, best results will be obtained if the device is calibrated at the highest sample rate. Reducing the sample rate by less than 80MSPS will typically result in an SNR change of <0.5dBFS and an SFDR change of <3dBc.

Figures 38 through 43 show the affect of temperature on SNR and SFDR performance with power on calibration performed at -40°C, +25°C, and +85°C. Each plot shows the variation of SNR/SFDR across temperature after a single power on calibration at -40°C, +25°C and +85°C. Best performance is typically achieved by a user-initiated power on calibration at the operating conditions, as stated earlier. However, it can be seen that performance drift with temperature is not a very strong function of the temperature at which the power on calibration is performed.

Temperature Calibration

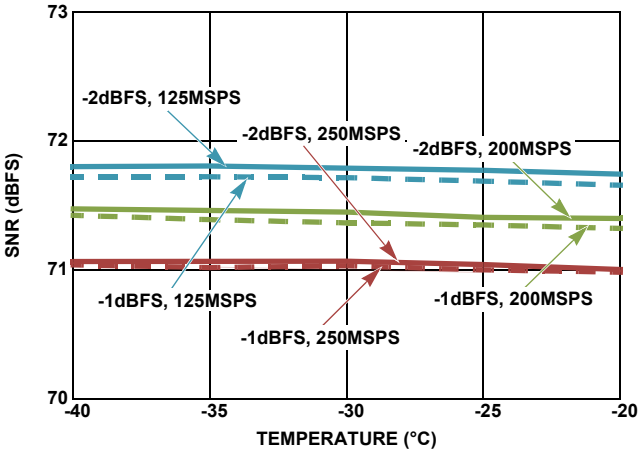


FIGURE 38. TYPICAL SNR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT -40°C, f_{IN} = 105MHz

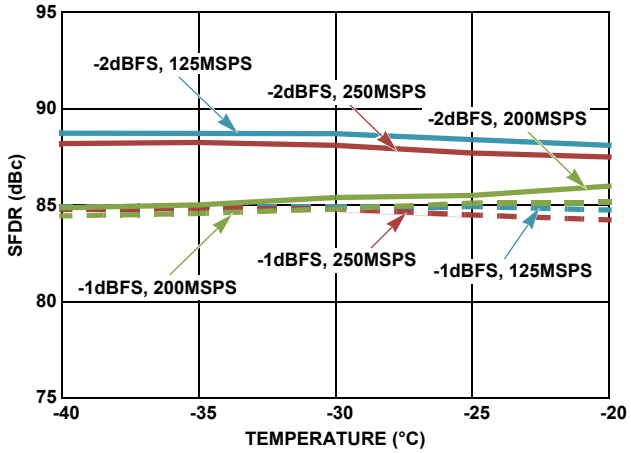


FIGURE 39. TYPICAL SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT -40°C, f_{IN} = 105MHz

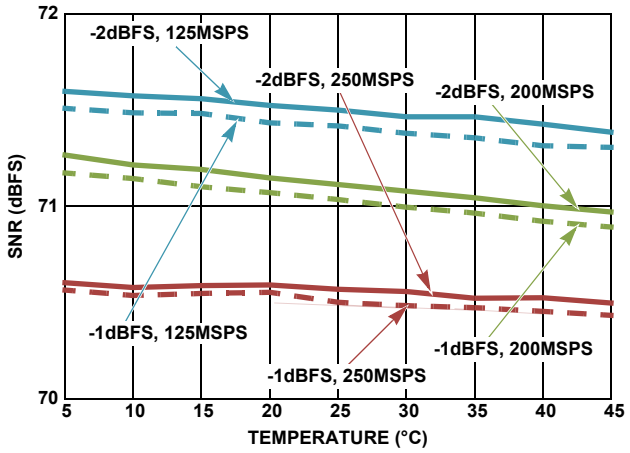


FIGURE 40. TYPICAL SNR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +25°C, f_{IN} = 105MHz

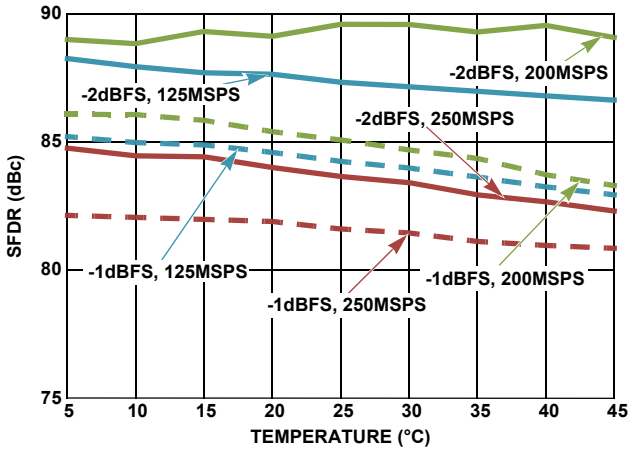


FIGURE 41. TYPICAL SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +25°C, f_{IN} = 105MHz

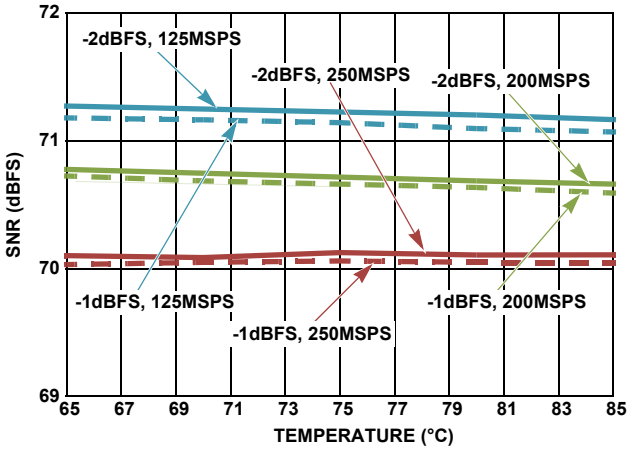


FIGURE 42. TYPICAL SNR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +85°C, f_{IN} = 105MHz

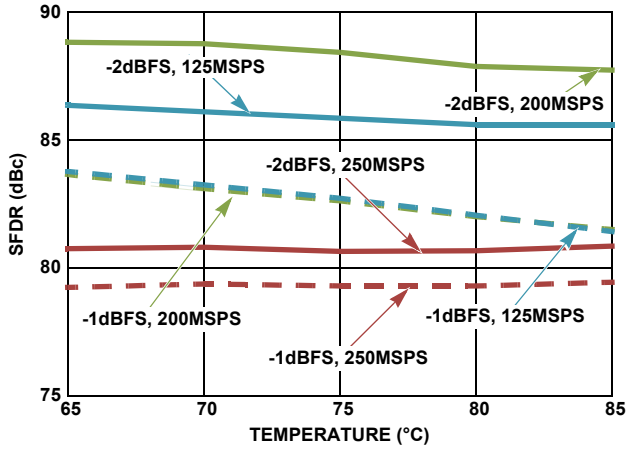


FIGURE 43. TYPICAL SFDR PERFORMANCE vs TEMPERATURE, DEVICE CALIBRATED AT +85°C, f_{IN} = 105MHz

Analog Input

A single fully differential input (VINP/VINN) connects to the Sample and Hold Amplifier (SHA) of each unit ADC. The ideal full-scale input voltage is 2.0V, centered at the VCM voltage as shown in Figure 44.

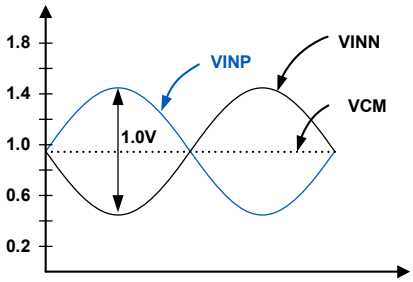


FIGURE 44. ANALOG INPUT RANGE

Best performance is obtained when the analog inputs are driven differentially. The common mode output voltage, VCM, should be used to properly bias the inputs as shown in Figures 45 through 47. An RF transformer will give the best noise and distortion performance for wideband and/or high intermediate frequency (IF) inputs. Two different transformer input schemes are shown in Figures 45 and 46.

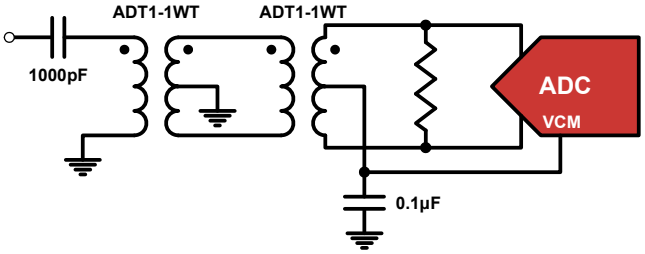


FIGURE 45. TRANSFORMER INPUT FOR GENERAL PURPOSE APPLICATIONS

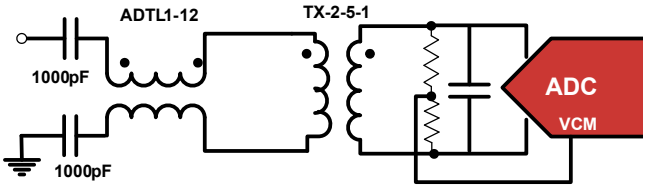


FIGURE 46. TRANSMISSION-LINE TRANSFORMER INPUT FOR HIGH IF APPLICATIONS

This dual transformer scheme is used to improve common mode rejection, which keeps the common mode level of the input matched to VCM. The value of the shunt resistor should be determined based on the desired load impedance. The differential input resistance of the ISLA222S is 600Ω.

The SHA design uses a switched capacitor input stage (see Figure 60 on page 35), which creates current spikes when the sampling capacitance is reconnected to the input voltage. This causes a disturbance at the input, which must settle before the next sampling point. Lower source impedance will result in faster settling and improved performance. Therefore a 2:1 or 1:1 transformer and low shunt resistance are recommended for optimal performance.

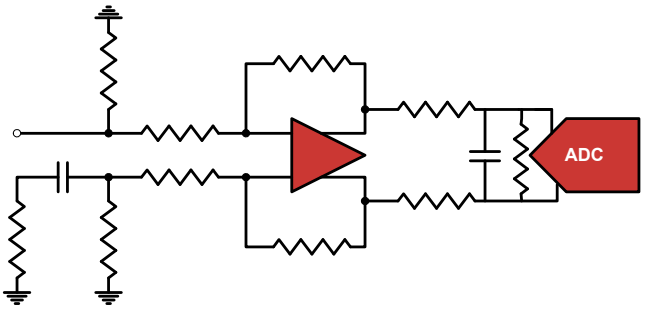


FIGURE 47. DIFFERENTIAL AMPLIFIER INPUT

A differential amplifier, as shown in the simplified block diagram in Figure 47, can be used in applications that require DC-coupling. In this configuration, the amplifier will typically dominate the achievable SNR and distortion performance. Intersil's new ISL552xx differential amplifier family can also be used in certain AC applications with minimal performance degradation. Contact Intersil sales support with your needs.

When an over range occurs, the data sample output bits are held at full scale (all 0's or all 1's), thus allowing the detection of this condition in the receiver device.

Clock Input

The clock input circuit is a differential pair (see Figure 61 on page 35). Driving these inputs with a high level (up to $1.8V_{P-P}$ on each input) sine or square wave will provide the lowest jitter performance. A transformer with 4:1 impedance ratio will provide increased drive levels. The clock input is functional with AC-coupled LVDS, LVPECL, and CML drive levels. To maintain the lowest possible aperture jitter, it is recommended to have high slew rate at the zero crossing of the differential clock input signal.

The recommended drive circuit is shown in Figure 48. A duty range of 40% to 60% is acceptable. The clock can be driven single-ended, but this will reduce the edge rate and may impact SNR performance. The clock inputs are internally self-biased to $AV_{DD}/2$ through a Thevenin equivalent of 10kΩ to facilitate AC coupling.

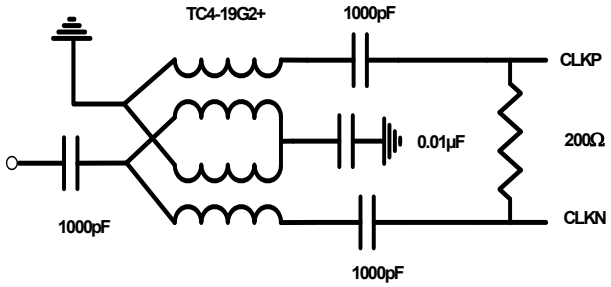


FIGURE 48. RECOMMENDED CLOCK DRIVE

A selectable 2x or 4x frequency divider is provided in series with the clock input. The divider can be used in the 2x mode with a sample clock equal to twice the desired sample rate or in 4x mode with a sample clock equal to four times the desired sample rate. Use of the 2x or 4x frequency divider enables the use of the phase slip feature, which enables the system to be able to select the phase of the divide by 2 or divide by 4 that causes the ADC to sample the analog input.

TABLE 1. CLKDIV PIN SETTINGS

CLKDIV PIN	DIVIDE RATIO
AVSS	2
Float	1
AVDD	4

The clock divider can also be controlled through the SPI port, which overrides the CLKDIV pin setting. See "SPI Physical Interface" on page 26. A Delay-locked Loop (DLL) generates internal clock signals for various stages within the charge pipeline. If the frequency of the input clock changes, the DLL may take up to 52µs to regain lock at 250MSPS. The lock time is inversely proportional to the sample rate.

The DLL has two ranges of operation, slow and fast. The slow range can be used for ADC core sample rates between 40MSPS and 100MSPS, while the default fast range can be used from 80MSPS to the maximum specified sample rate. The lane data rate is related to the ADC core sample rate by a relationship that is defined by the JESD204 transmitter configuration and has additional frequency constraints; see"JESD204 Transmitter" on page 20 for additional details.

Jitter

In a sampled data system, clock jitter directly impacts the achievable SNR performance. The theoretical relationship between clock jitter (t_J) and SNR is shown in Equation 1 and is illustrated in Figure 49.

$$SNR = 20 \log_{10}\left(\frac{1}{2\pi f_{IN} t_J}\right) \quad \text{(EQ. 1)}$$

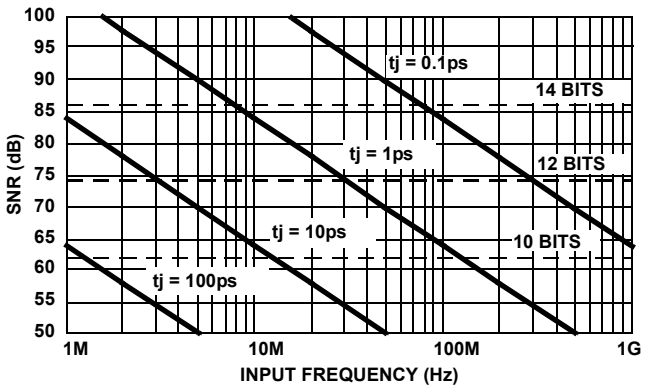


FIGURE 49. SNR vs CLOCK JITTER

This relationship shows the SNR that would be achieved if clock jitter were the only non-ideal factor. In reality, achievable SNR is limited by internal factors such as linearity, aperture jitter and thermal noise as well. Internal aperture jitter is the uncertainty in the sampling instant. The internal aperture jitter combines with the input clock jitter in a root-sum-square fashion, since they are not statistically correlated, and this determines the total jitter in the system. The total jitter, combined with other noise sources, then determines the achievable SNR.

Voltage Reference

A temperature compensated internal voltage reference provides the reference charges used in the successive approximation operations. The full scale range of each ADC is proportional to the reference voltage. The nominal value of the voltage reference is 1.25V.

Digital Outputs

The digital outputs are in CML format, and feature analog and digital characteristics compliant with the JESD204 standard requirements.

Power Dissipation

The power dissipated by the device is dependent on the ADC sample rate and the number of active lanes in the link. There is a fixed bias current drawn from the analog supply for the ADC, along with a fixed bias current drawn from the digital supply for each active lane. The remaining power dissipation is linearly related to the sample rate.

Nap/Sleep

Portions of the device may be shut down to save power during times when operation of the ADC is not required. Two power saving modes are available: Nap and Sleep. Nap mode reduces power dissipation significantly while taking a very short time to return to functionality. Sleep mode reduces power consumption drastically while taking longer to return to functionality.

In Nap mode the JESD204 lanes will continue to produce valid encoded data, allowing the link to remain active and thus return to a functional state quickly. The data transmitted over the lanes in nap mode is the last valid ADC sample, repeated until leaving nap mode. The 8b/10b encoder's running disparity will prevent the potentially long time repetition of this last valid sample from creating DC bias on the lane. In sleep mode, the JESD204 lanes will be deactivated to conserve power. Thus, sometime after wake up code group alignment will be required to reestablish the link.

The input clock should remain running and at a fixed frequency during Nap or Sleep and CSB should be high. The JESD204 link will only remain established during nap mode if the input clock continues to remain stable during the nap period.

By default after the device is powered on, the operational state is controlled by the NAPSLP pin as shown in Table 2. Please note that power on calibration occurs at power-up time regardless of the state of the NAPSLP pin; immediately following this power-on calibration routine, the device will enter nap or sleep state if the NAPSLP pin voltage dictates it is to do so.

TABLE 2. NAPSLP PIN SETTINGS

NAPSLP PIN	MODE
AVSS	Normal
Float	Nap
AVDD	Sleep

The power-down mode can also be controlled through the SPI port, which overrides the NAPSLP pin setting. Details on this are contained in "Serial Peripheral Interface" on page 26.

Data Format

Output data can be presented in three formats: two's complement(default), Gray code and offset binary. The data format can be controlled through the SPI port by writing to address 0x73. Details on this are contained in "Serial Peripheral Interface" on page 26.

Offset binary coding maps the most negative input voltage to code 0x000 (all zeros) and the most positive input to 0xFFF (all ones). Two's complement coding simply complements the MSB of the offset binary representation.

When calculating Gray code the MSB is unchanged. The remaining bits are computed as the XOR of the current bit position and the next most significant bit. Figure 50 shows this operation.

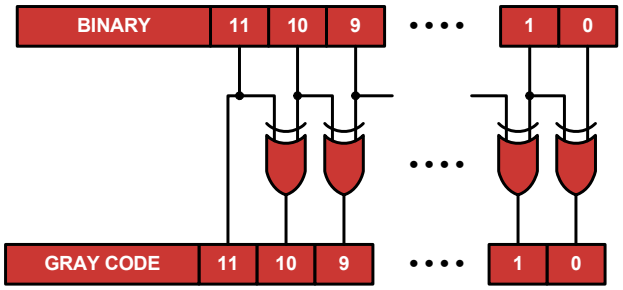


FIGURE 50. BINARY TO GRAY CODE CONVERSION

Converting back to offset binary from Gray code must be done recursively, using the result of each bit for the next lower bit as shown in Figure 51.

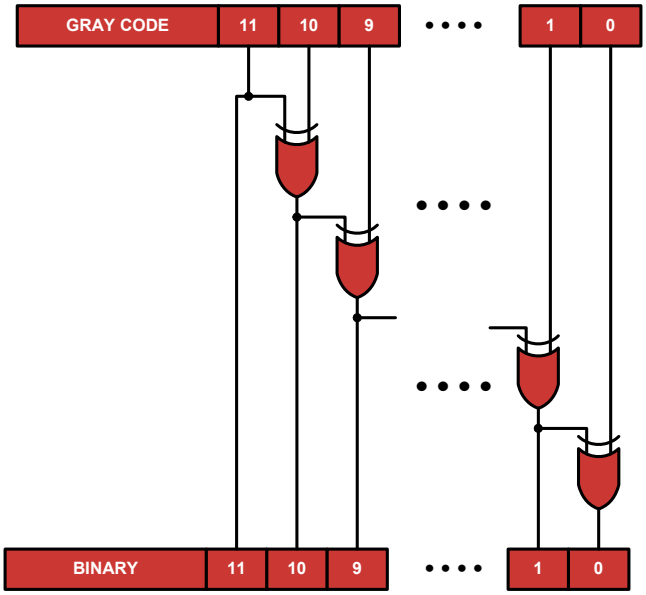


FIGURE 51. GRAY CODE TO BINARY CONVERSION

Mapping of the input voltage to the various data formats is shown in Table 3.

TABLE 3. INPUT VOLTAGE TO OUTPUT CODE MAPPING

INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT	GRAY CODE
-Full Scale	0000 0000 0000	1000 0000 0000	0000 0000 0000
-Full Scale +LSB	0000 0000 0001	1000 0000 0001	0000 0000 0001
Mid Scale	1000 0000 0000	0000 0000 0000	1100 0000 0000
+Full Scale -1LSB	1111 1111 1110	0111 1111 1110	1000 0000 0001
+Full Scale	1111 1111 1111	0111 1111 1111	1000 0000 0000

Clock Divider Synchronous Reset

The function of clock divider synchronous reset is available as a SPI-programmable overloaded function on the SYNCP and SYNCN pins. Given that the clock divider reset and SYNC features have the same electrical and timing requirements, this overloading allows the system to generate only a single well timed signal with respect to the ADC sample clock. Thus selects the ADC's interpretation of the signal as a SPI-programmable option (see SPI register 0x77 description for more information). By default the SYNCP and SYNCN pins will function as the JESD204 SYNC~.

The use of clock divider reset function is a requirement in a system that uses the ISLA214S50, ISLA214S35, or CLKDIV = 2 or 4 and also requires time alignment or deterministic latency of multiple devices. Please contact Intersil sales support with your needs about this feature and its usage.

Soft Reset

Soft reset is a function intended to be used when the power-on reset is to be re-run. An application may decide to issue a soft calibration command after significant temperature change or after a change in the sample rate frequency to optimize performance under the new condition.

Soft reset is issued by writing the soft reset bit at SPI address 0x00. Soft reset is a self-resetting bit in that will automatically return to 0 once the power on calibration has completed.

JESD204 Transmitter

Overview

The conversion data is presented by a JESD204B-compliant SERDES interface. The SERDES lane data rate supports typical speeds up to 4.375Gbps, exceeding the 3.125Gbps maximum specified by the JESD204 rev A standard. Two packing modes are supported: Efficient and Simple. A SYNC input is included, which is used for lane initialization as well as time alignment of multiple converter devices. AC coupling of the SERDES lane(s) on-the-board is required. A block diagram of this SERDES transmitter is shown in Figure 52.

For more information about the standardized characteristics and features of a JESD204 interface, please see JESD204 rev A and rev B standards. For application design support, including evaluation kit schematics and layout, reference FPGA project(s), and simulation models for functionality and signal integrity, please contact Intersil sales support with your needs and/or view application notes on the Intersil website.

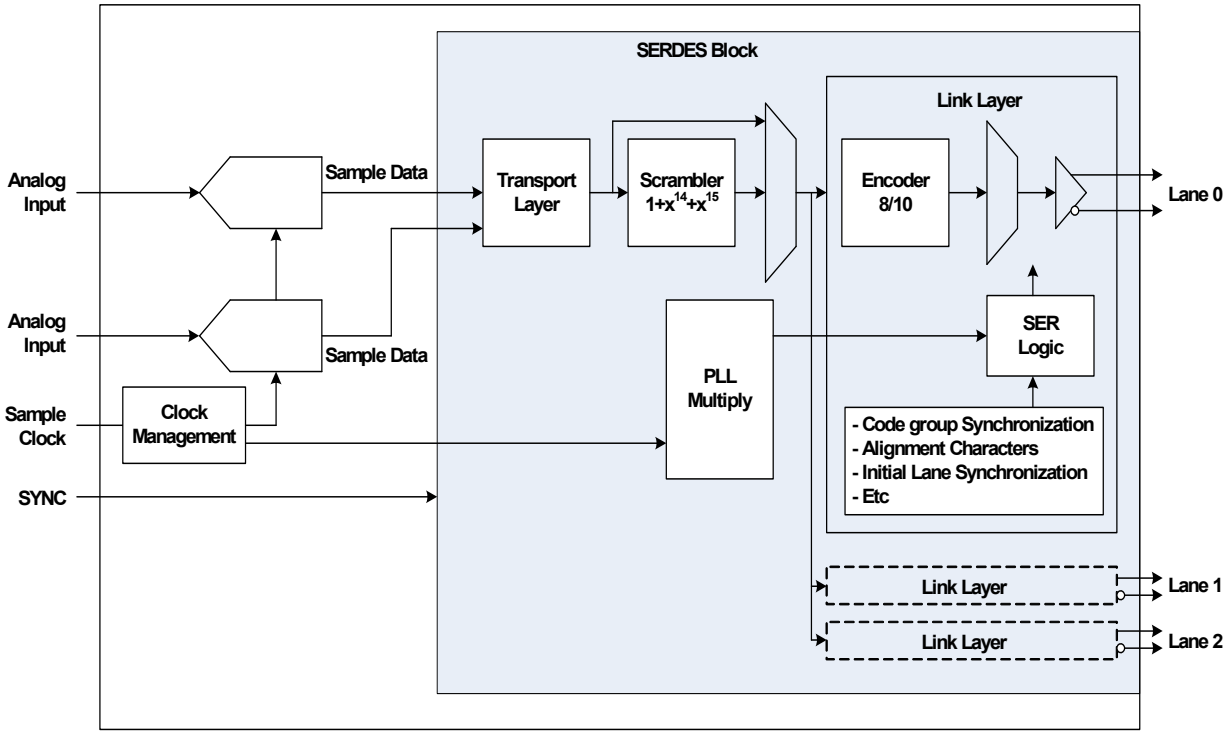


FIGURE 52. SERDES TRANSMITTER BLOCK DIAGRAM

To maximize flexibility at the system level, two transport layer packing modes are supported: simple and efficient. These two modes allow the system designer flexibility to trade off between the number of lanes to support a given throughput, the data rate of these lanes and the complexity of the receiver. This translates directly into providing system level trade-offs between cost, power and resource usage of the receiver and complexity of the solution.

Simple mode packs informationless bits onto each ADC sample to form full 16-bit data. In simple mode packing, the frame clock and ADC sample clock are the same frequency, easing frequency scaling requirements at the system level, but decreasing the payload efficiency of the lanes. Decreased payload efficiency of the lanes increases the lane data rate required to support a given throughput and may require additional lanes to support a given configuration. The degree of payload efficiency loss is dependent on the ADC resolution.

Efficient mode packs sequential ADC samples into a contiguous block of an integer number of octets and then slices the block into the octets for transport. This mode always achieves the theoretical maximum payload of the lanes (80%) regardless of the resolution of the ADC and the number of lanes used. This mode provides the minimum number of lanes at the minimum data rate that is theoretically possible given the 8b/10b encoding used in JESD204 systems. In efficient packing mode, frame clock and the ADC sample clock have an M/N relationship, where M and N are small integers and vary depending on the ADC resolution and number of lanes selected. Efficient mode packing may require additional frequency scaling elements (internal FPGA PLLs or discrete frequency scaling devices) to generate the frame clock for the receiving device.

The default configuration for this device is efficient packing mode. Reconfiguration into the simple packing mode is accomplished by programming the JESD204 parameters via the SPI bus. See Table 5 on page 23 for the full list of parameters values for each mode and product. Via SPI, the JESD204 transmitter is highly configurable, supporting efficient to simple mode packing reconfiguration as well as “downgrading” a given product’s JESD204 interface. For example, reconfiguring a 3-lane product into 2 lanes (with each running faster than with 3 lanes), or reducing the resolution of the ADC(s) to slow down the lane data rate in systems where the full ADC resolution is not required, are supported. Please contact Intersil sales support for a full list of downgradeable configurations that are supported.

Signal integrity plots, including data eye, BER bathtub curves, and edge histogram plots versus lane data rate can be found in the “Typical Performance Curves” beginning on page 10.

Initial Lane Alignment

The link initialization process is started by asserting the SYNC~ signal to the ADC device. This assertion causes the JESD204 transmitter to generate comma characters, which are used by the receiver to accomplish code group synchronization (bit and octet alignment, respectively). Once code group synchronization is detected in the receiver, it deasserts the SYNC~ signal, causing the JESD204 transmitter to generate the Initial Lane Alignment sequence (ILA). The ILA is comprised of 4 multiframes of data in a standard format, with the length of each multiframe determined by the *K* parameter as programmed into the SPI JESD204 parameter table. The ILA includes standard control character markers that can be used to perform channel bonding in the receiving device if desired. The 2nd multiframe includes the full JESD204 parameter

data, allowing the receiver to auto-detect the lane configuration if desired.

After completion of the ILA the JESD204 transmitter begins transmitting ADC sample data. Continuous link and lane alignment monitoring is accomplished via an octet substitution scheme. The last octet in each frame, if identical to the last octet in the previous frame, is replaced with a specific control character. If both sides of the link support lane synchronization, the last octet in each multiframe, if identical to the last octet in the previous frame, is replaced with a different specific control character. A more complete description of the link initialization sequence including finite state machine implementation, can be found in the JESD204 rev A standard.

LANE DATA RATE

The lane data rate for this product family is a function of the ADC sample rate, the number of SERDES lanes used and packing mode selected in the SERDES transmitter. Figure 53 illustrates the relationship between ADC sample rate and SERDES lane rate for various transmitter configurations. The SERDES can typically operate from lane rates of 1 to over 4.375Gbs. For each ADC speed grade, the SERDES lanes are tested at its maximum ADC sample rate using three lane efficient packing as well as two-lane, efficient packing for the 250 and 200MSPS speed versions and one-lane, efficient packing for 125MSPS speed version.

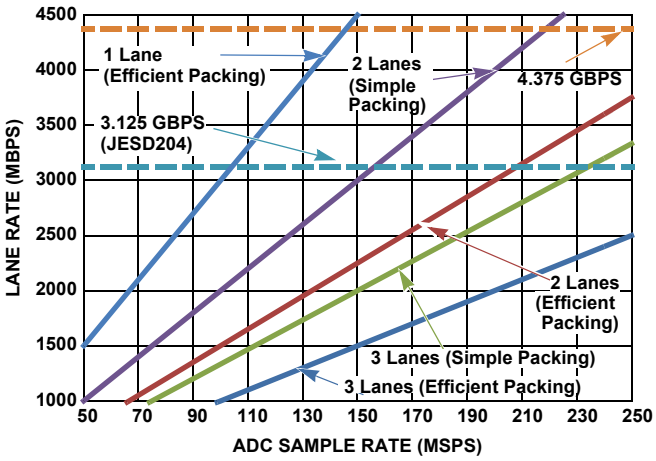


FIGURE 53. LANE DATA RATE AS A FUNCTION OF ADC SAMPLE RATE, PACKING

SCRAMBLER

The bypassable scrambler is compliant with the scrambler defined in the JESD204 rev A standard.

This implementation seeds the scrambler with the initial lane alignment sequence, such that the first two octets following the sequence can be properly descrambled if the receiver also passes the lane alignment sequence through its descrambler. Even if the receiver does not implement this detail, the 3rd and subsequent octets can be descrambled to yield ADC data due to the self-synchronizing nature of the scrambler used.

MULTI-CHIP TIME ALIGNMENT

The JESD204 standard (in various revisions) provides the capability to time align multiple JESD204 ADC devices to a single logic device (FPGA or ASIC). This feature is critical in many applications that cannot tolerate the variable latency of the JESD204 link and that must process pipeline depth correct data from more than one ADC device.

Time alignment of multiple devices provides the capability to align samples from multiple JESD204 ADC devices in the system in a pipeline-depth correct manner, thus enabling the system to analyze the ADC data from multiple devices while eliminating the variable latency of the JESD204 link as a concern. This capability enables configurations of JESD204 ADCs as IQ, interleave and/or simultaneously-sampled converters.

This ADC family uses the asserted to deasserted SYNC~ transition as the absolute time event with which to generate a known sequence of characters at the JESD204 transmitter of equal pipeline depth between all ADC devices in the system to be time aligned. This is consistent with the JESD204 rev B subclass 2 device definition.

Test Patterns

The complexity of the JESD204 interface merits much more test pattern capability than less complex parallel interfaces. This device family consequently supports a much wider range of test patterns than previous ADC families.

Supported test patterns include both transport and link layer patterns. Transport layer patterns are passed through the transport layer of the JESD204 transmitter, following the same sequence of being packed and sliced into octets as the ADC sample data. Link layer test patterns bypass the transport layer and are injected directly into the 8b/10b encoder, serialized and sent out of the physical media. Test pattern generation is controlled through SPI register 0xC0.

Link layer PRBS patterns are standard PRBS patterns that can be used with built-in standard PRBS checkers in, for example, FPGA SERDES-capable pins.

All transport layer test patterns reinitialize their phase when the SYNC~ deassertion occurs; consequently, a system that provides a well timed SYNC~ signal with respect to the ADC sample clock can expect transport layer test patterns to have consistent phase with respect to that deassertion, which can be a significant aid when debugging the system.

TABLE 4. JESD204 CONFIGURATIONS AND CLOCK FREQUENCIES

ADC SAMPLE CLOCK RANGE (MHz)	LANE DATA RATE MULTIPLIER FROM ADC SAMPLE CLOCK RATE	LANE DATA RATE (GBPS)
100 to 250 (Efficient Packing) 3 Lanes	(12-bits)*(2 ADC channels)*(10/8 encoder overhead)/(3 lanes) = (240/24) = 10.0	1.00 to 2.50
66.67 to 250 (Efficient Packing) 2 Lanes	(12-bits)*(2 ADC channels)*(10/8 encoder overhead)/(2 lanes) = (240/16) = 15	1.00 to 3.75
50 to 218.75(Simple Packing) 2 Lanes	(12-bits+4-bit tail)*(2 ADC channels)*(10/8 encoder overhead)/(2 lanes) = (320/16) = 20	1.00 to 4.375
40 to 145.8 (Efficient Packing) 1 Lane	(12-bits)*(2 ADC channels)*(10/8 encoder overhead)/(1 lane) = (240/8) = 30	1.20 to 4.375
40 to 109.375(Simple Packing) 1 Lane	(12-bits+4-bit tail)*(2 ADC channels)*(10/8 encoder overhead)/(1 lane) = (320/8) = 40	1.60 to 4.375

TABLE 5. JESD204 PARAMETERS

PACKING MODE	NUMBER OF LANES	JESD204 PARAMETER	ENCODED	JESD204 PARAMETERS AND FRAME MAP (Notes 16, 17, 18)						
Efficient	3	CF = 0	0							
		CS = 0	0	C0S0[11:4	C0S0[3:0]	C0S1[7:0]	C0S2[11:4]	C0S2[3:0]	C0S3[7:0]	
		F = 6	5		C0S1[11:8]			C0S3[11:8]		
		HD = 0	0							
		L = 3	2	C0S4[11:4]	C0S4[3:0]	C0S5[7:0]	C1S0[11:4]	C1S0[3:0]	C1S1[7:0]	
		M = 2	1		C0S5[11:8]			C1S1[11:8]		
		N = 12	11							
		N' = 12	11	C1S2[11:4]	C1S2[3:0]	C1S3[7:0]	C1S4[11:4]	C1S4[3:0]	C1S5[7:0]	
		S = 6	5		C1S3[11:8]			C1S5[11:8]		
		K ≥ 3	≥2							
Efficient	2	CF = 0	0							
		CS = 0	0	C0S0[11:4]	C0S0[3:0]	C0S1[7:0]				
		F = 3	2		C0S1[11:8]					
		HD = 0	0							
		L = 2	1	C1S0[11:4]	C1S0[3:0]	C1S1[7:0]				
		M = 2	1		C1S1[11:8]					
		N = 12	11							
		N' = 12	11							
		S = 2	1							
		K ≥ 6	≥5							

TABLE 5. JESD204 PARAMETERS (Continued)

PACKING MODE	NUMBER OF LANES	JESD204 PARAMETER	ENCODED	JESD204 PARAMETERS AND FRAME MAP (Notes 16, 17, 18)						
Simple	2	CF = 0	0							
		CS = 0	0	C0S0[11:4]	C0S0[3:0]					
		F = 2	1		TTTT					
		HD = 0	0							
		L = 2	1	C1S0[11:4]	C1S0[3:0]					
		M = 2	1		TTTT					
		N = 12	11							
		N' = 16	15							
		S = 1	0							
		K ≥ 9	≥8							
Efficient	1	CF = 0	0							
		CS = 0	0	C0S0[11:4]	C0S0[3:0]	C0S1[7:0]	C1S0[11:4]	C1S0[3:0]	C1S1[7:0]	
		F = 6	5		C0S1[11:8]			C1S1[11:8]		
		HD = 0	0							
		L = 1	0							
		M = 2	1							
		N = 12	11							
		N' = 12	11							
		S = 2	1							
		K ≥ 3	≥2							
Simple	1	CF = 0	0							
		CS = 0	0	C0S0[11:4]	C0S0[3:0]	C1S0[11:4]	C1S0[3:0]			
		F = 4	3		TTTT		TTTT			
		HD = 0	0							
		L = 1	0							
		M = 2	1							
		N = 12	11							
		N' = 16	15							
		S = 1	0							
		K ≥ 5	≥4							

NOTES:

16. The JESD204 parameters are shown as their actual values, with the JESD204 encoded values (i.e., the values that are programmed into the SPI registers) in the next column over. Typically values that must always be greater than 1 are encoded as value minus 1, and so on.
17. Frame map format decoder: "CxSy[a:b]" = Converter x, Sample y, bits a through b. For example, "C0S0[13:6]" = Converter 0, Sample 0, bits 13 through 6, etc. "T" = Tail bit (information-less bit packed in the transport layer mapping to form octets).
18. The topmost lane in the graphical frame map is Lane0, followed by Lane1 and Lane 2 (for 3-lane configurations).

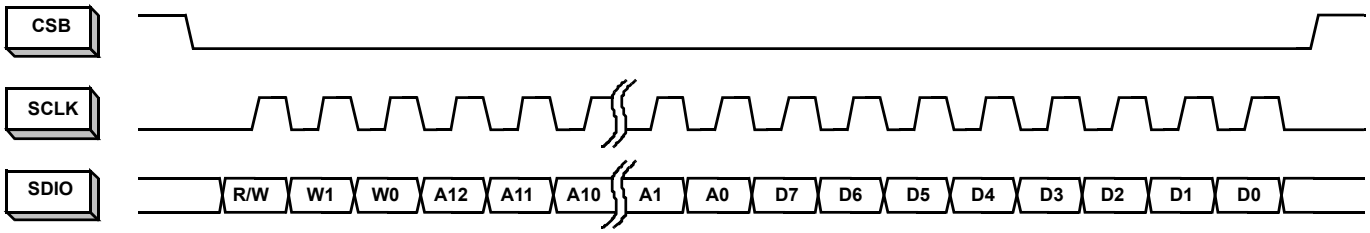


FIGURE 54. MSB-FIRST ADDRESSING

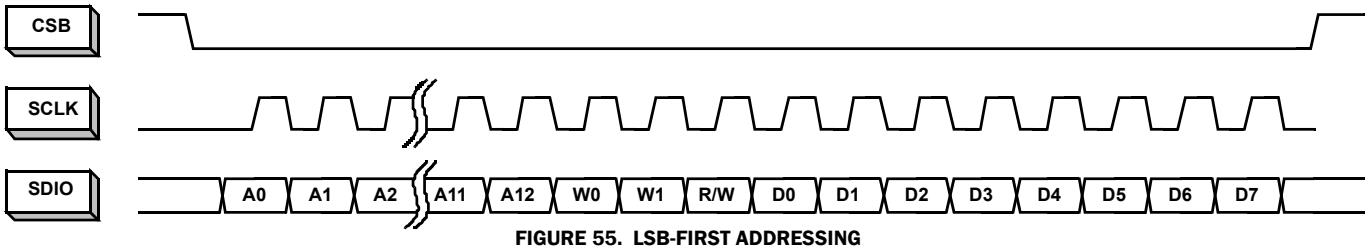
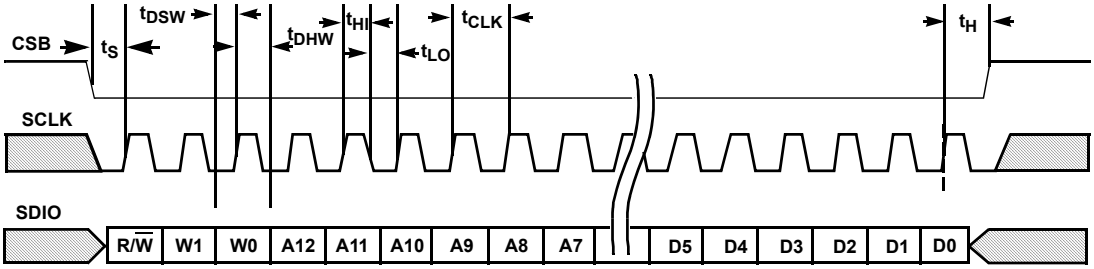
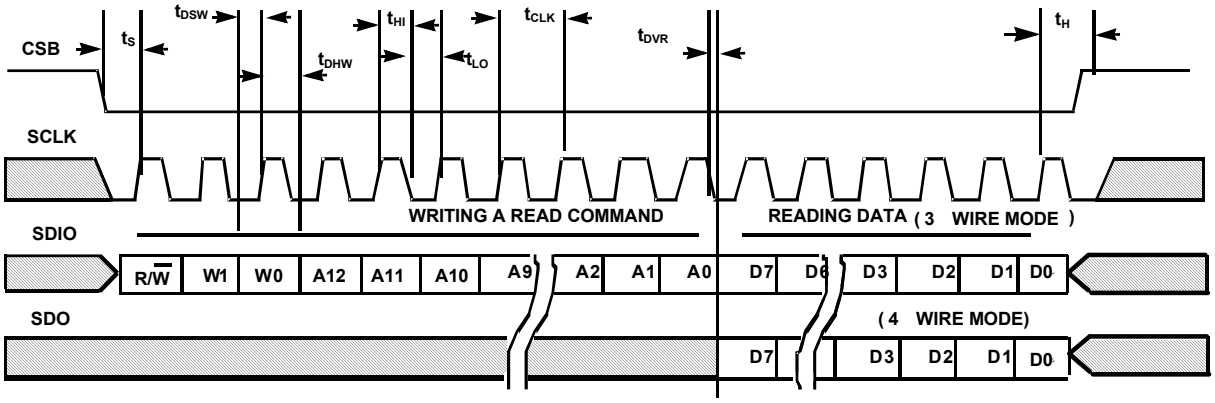


FIGURE 55. LSB-FIRST ADDRESSING



SPI WRITE

FIGURE 56. SPI WRITE



SPI READ

FIGURE 57. SPI READ

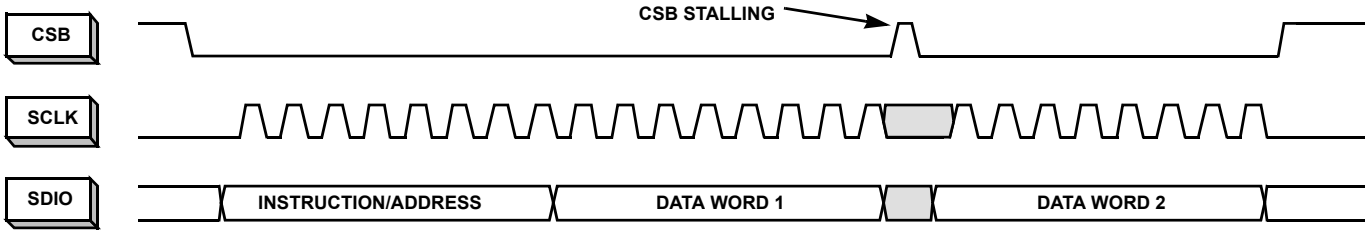


FIGURE 58. 2-BYTE TRANSFER

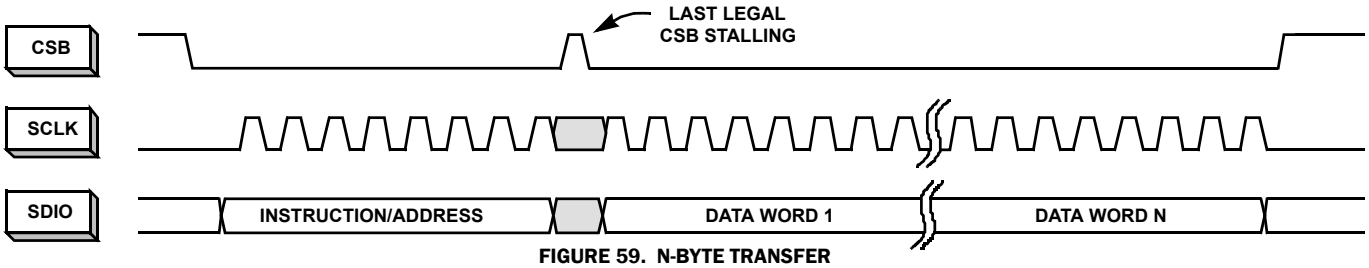


FIGURE 59. N-BYTE TRANSFER

Serial Peripheral Interface

A Serial Peripheral Interface (SPI) bus is used to facilitate configuration of the device and to optimize performance. The SPI bus consists of chip select (CSB), serial clock (SCLK) Serial Data Output (SDO), and Serial Data Input/Output (SDIO). The maximum SCLK rate is equal to the ADC sample rate (f_{SAMPLE}) divided by 7 for write operations and f_{SAMPLE} divided by 16 for reads. There is no minimum SCLK rate.

The following sections describe various registers that are used to configure the SPI or adjust performance or functional parameters. Many registers in the available address space (0x00 to 0xFF) are not defined in this document. Additionally, within a defined register there may be certain bits or bit combinations that are reserved. Undefined registers and undefined values within defined registers are reserved and should not be selected. Setting any reserved register or value may produce indeterminate results.

SPI Physical Interface

The serial clock pin (SCLK) provides synchronization for the data transfer. By default, all data is presented on the Serial Data Input/Output (SDIO) pin in three-wire mode. The state of the SDIO pin is set automatically in the communication protocol (described in the following). A dedicated Serial Data Output pin (SDO) can be activated by setting 0x00[7] high to allow operation in four-wire mode.

The SPI port operates in a half duplex master/slave configuration, with the ADC functioning as a slave. Multiple slave devices can interface to a single master in three-wire mode only, since the SDO output of an unaddressed device is asserted in four-wire mode.

The Chip-select Bar (CSB) pin determines when a slave device is being addressed. Multiple slave devices can be written to concurrently, but only one slave device can be read from at a given time (again, only in three-wire mode). If multiple slave devices are selected for reading at the same time, the results will be indeterminate.

The communication protocol begins with an instruction/address phase. The first rising SCLK edge following a high-to-low transition on CSB determines the beginning of the two-byte instruction/address command; SCLK must be static low before the CSB transition. Data can be presented in MSB-first order or LSB-first order. The default is MSB-first, but this can be changed by setting 0x00[6] high. Figures 54 and 55 show the appropriate bit ordering for the MSB-first and LSB-first modes, respectively. In MSB-first mode, the address is incremented for multi-byte transfers, while in LSB-first mode it's decremented.

In the default mode, the MSB is R/W, which determines if the data is to be read (active high) or written. The next two bits, W1 and W0, determine the number of data bytes to be read or written (see Table 6 on page 27). The lower 13 bits contain the first address for the data transfer. This relationship is illustrated in Figure 56, and timing values are given in "Switching Specifications" on page 8.

After the instruction/address bytes have been read, the appropriate number of data bytes are written to or read from the ADC (based on the R/W bit status). The data transfer will continue as long as CSB remains low and SCLK is active. Stalling of the CSB pin is allowed at any byte boundary (instruction/address or data) if the number of bytes being transferred is three or less. For transfers of four bytes or more, CSB is allowed to stall in the middle of the instruction/address bytes or before the first data byte. If CSB transitions to a high state after that point the state machine will reset and terminate the data transfer.

TABLE 6. BYTE TRANSFER SELECTION

[W1:W0]	BYTES TRANSFERRED
00	1
01	2
10	3
11	4 or more

Figures 58 and 59 illustrate the timing relationships for 2-byte and N-byte transfers, respectively. The operation for a 3-byte transfer can be inferred from these diagrams.

SPI Configuration

ADDRESS 0X00: CHIP_PORT_CONFIG

Bit ordering and SPI reset are controlled by this register. Bit order can be selected as MSB to LSB (MSB first) or LSB to MSB (LSB first) to accommodate various microcontrollers.

Bit 7 SDO Active

Bit 6 LSB First

Setting this bit high configures the SPI to interpret serial data as arriving in LSB to MSB order.

Bit 5 Soft Reset

Setting this bit high resets all SPI registers to default values.

Bit 4 Reserved

This bit should always be set high.

Bits 3:0 These bits should always mirror bits 4:7 to avoid ambiguity in bit ordering.

ADDRESS 0X02: BURST_END

If a series of sequential registers are to be set, burst mode can improve throughput by eliminating redundant addressing. The burst is ended by pulling the CSB pin high. Setting the burst_end address determines the end of the transfer. During a write operation, the user must be cautious to transmit the correct number of bytes based on the starting and ending addresses.

Bits 7:0 Burst End Address

This register value determines the ending address of the burst data.

Device Information

ADDRESS 0X08: CHIP_ID

ADDRESS 0X09: CHIP_VERSION

The generic die identifier and a revision number, respectively, can be read from these two registers.

Device Configuration/Control

A common SPI map, which can accommodate single-channel or multi-channel devices, is used for all Intersil ADC products.

ADDRESS 0X20: OFFSET_COARSE_COREA

ADDRESS 0X21: OFFSET_FINE_COREA

The input offset of the ADC core can be adjusted in fine and coarse steps. Both adjustments are made via an 8-bit word as detailed in Table 7. The data format is two's complement.The data format is two's complement. Bit 0 in register 0xFE must be set high to enable updates written to 0x20 and 0x21 to be used by the ADC (see description for 0xFE).

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

TABLE 7. OFFSET ADJUSTMENTS

CoreA CoreB PARAMETER	0x20[7:0] 0x26[7:0] COARSE OFFSET	0x21[7:0] 0x27[7:0] FINE OFFSET
Steps	255	255
–Full Scale (0x00)	-133LSB (-47mV)	-5LSB (-1.75mV)
Mid–Scale (0x80)	0.0LSB (0.0mV)	0.0LSB
+Full Scale (0xFF)	+133LSB (+47mV)	+5LSB (+1.75mV)
Nominal Step Size	1.04LSB (0.37mV)	0.04LSB (0.014mV)

ADDRESS 0X22: GAIN_COARSE_COREA

ADDRESS 0X23: GAIN_MEDIUM_COREA

ADDRESS 0X24: GAIN_FINE_COREA

Gain of the ADC core can be adjusted in coarse, medium and fine steps. Coarse gain is a 4-bit adjustment while medium and fine are 8-bit. Multiple coarse gain bits can be set for a total adjustment range of ±4.2%. ('0011' ≅ -4.2% and '1100' ≅ +4.2%). It is recommended to use one of the coarse gain settings (-4.2%, -2.8%, -1.4%, 0, 1.4%, 2.8%, 4.2%) and fine-tune the gain using the registers at 0x23 and 0x24.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register. Bit 0 in register 0xFE must be set high to enable updates written to 0x23 and 0x24 to be used by the ADC (see description for 0xFE).

TABLE 8. COARSE GAIN ADJUSTMENT

0x22[3:0] CoreA 0x26[3:0] CoreB	NOMINAL COARSE GAIN ADJUST (%)
Bit 3	+2.8
Bit 2	+1.4
Bit 1	-2.8
Bit 0	-1.4

TABLE 9. MEDIUM AND FINE GAIN ADJUSTMENTS

CoreA CoreB PARAMETER	0x23[7:0] 0x29[7:0] MEDIUM GAIN	0x24[7:0] 0x2A[7:0] FINE GAIN
Steps	256	256
–Full Scale (0x00)	-2%	-0.20%
Mid-scale (0x80)	0.00%	0.00%
+Full Scale (0xFF)	+2%	+0.2%
Nominal Step Size	0.016%	0.0016%

ADDRESS 0X25: MODES

Two distinct reduced power modes can be selected. By default, the tri-level NAPSLP pin can select normal operation, nap or sleep modes (refer to"Nap/Sleep" on page 19). This functionality can be overridden and controlled through the SPI. This register is not changed by a soft reset.

TABLE 10. POWER-DOWN CONTROL

VALUE	0x25[2:0] POWER DOWN MODE
000	Pin Control
001	Normal Operation
010	Nap Mode
100	Sleep Mode

ADDRESS 0X26: OFFSET_COARSE_COREB

ADDRESS 0X27: OFFSET_FINE_COREB

The input offset of ADC CoreB can be adjusted in fine and coarse steps in the same way that offset for CoreB can be adjusted. Both adjustments are made via an 8-bit word as detailed in Table 7. The data format is two's complement. Bit 0 in register 0xFE must be set high to enable updates written to 0x26 and 0x27 to be used by the ADC (see description for 0xFE).

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

ADDRESS 0X28: GAIN_COARSE_COREB

ADDRESS 0X29: GAIN_MEDIUM_COREB

ADDRESS 0X2A: GAIN_FINE_COREB

Gain of ADC CoreB can be adjusted in coarse, medium and fine steps in the same way that CoreA can be adjusted. Coarse gain is a 4-bit adjustment while medium and fine are 8-bit. Multiple Coarse Gain Bits can be set for a total adjustment range of ±4.2%. Bit 0 in register 0xFE must be set high to enable updates written to 0x29 and 0x2A to be used by the ADC (see description for 0xFE).

Global Device Configuration/Control

ADDRESS 0X71: PHASE_SLIP

When using the clock_divide feature, the sample clock edge that the ADC uses to sample the analog input signal can be one of several different edges on the incoming higher frequency sample clock. For example, in clock_divide = 2 mode, every other incoming sample clock edge gets used by the ADC to sample the analog input. The phase_slip feature allows the system to control which edge of the incoming sample clock signals gets used to cause the sampling event, by "slipping" the sampling event by one input clock period each time phase_slip is asserted.

The clkdivrst feature can work in conjunction with phase_slip. After well-timed assertion of the clkdivrst signal (via overloading on the SYNC inputs), the sampling edge position with respect to the incoming clock rate will have been reset, allowing the system to "slip" whatever desired number of incoming clock periods from a known state.

ADDRESS 0X72: CLOCK_DIVIDE

The ADC has a selectable clock divider that can be set to divide by two or one (no division). By default, CLOCK_DIVIDE is set to divide by 1. This functionality can be overridden and controlled through the SPI, as shown in Table 11. This register is not changed by a soft reset.

TABLE 11. CLOCK DIVIDER SELECTION

VALUE	0x72[2:0] CLOCK DIVIDER
000	Pin Control
001	Divide by 1 (Default)
010	Divide by 2
other	Not Allowed

ADDRESS 0X73: OUTPUT_MODE_A

The output_mode_A register controls the logical coding of the sample data. Data can be coded in three possible formats: two's complement(default), Gray code or offset binary. See Table 12.

This register is not changed by a soft reset.

TABLE 12. OUTPUT FORMAT CONTROL

VALUE	0x73[2:0] OUTPUT FORMAT
000	Two's Complement (Default)
010	Gray Code
100	Offset Binary

ADDRESS 0X74: OUTPUT_MODE_B

Bit 6 DLL Range

This bit sets the DLL operating range to fast (default) or slow.

Internal clock signals are generated by a Delay-locked Loop (DLL), which has a finite operating range. Table 13 shows the allowable sample rate ranges for the slow and fast settings.

TABLE 13. DLL RANGES

DLL RANGE	MIN	MAX	UNIT
Slow	40	100	MSPS
Fast	80	250	MSPS

ADDRESS 0X77: SYNC_FUNCTION

BIT 0 CLKDIVRST

This bit controls the functionality of the SYNCP, SYNCN pins on this device. By default, this bit equals ‘0’, which means that the functionality of the SYNCP, SYNCN pins is the JESD204 SYNC. Setting this bit equal to ‘1’ modifies the functionality of the SYNCP, SYNCN pins to be CLKDIVRST, which is a synchronous divider reset on all internal dividers in the device. Usage of this CLKDIVRST functionality is required to support multichip time alignment and deterministic latency for devices that use interleaved product configurations (ISLA214S50 and ISLA214S35), and for any other product configuration that uses CLKDIV > 1. In both states, the setup and hold times with respect to the sample clock remain the same. Contact Intersil sales support for more details.

ADDRESS 0XB6: CALIBRATION STATUS

The LSB at address 0xB6 can be read to determine calibration status. The bit is ‘0’ during calibration and goes to a logic ‘1’ when calibration is complete. This register is unique in that it can be read after POR at calibration, unlike the other registers on chip, which can’t be read until calibration is complete.

DEVICE TEST

The device can produce preset or user defined patterns on the digital outputs to facilitate in-situ testing. A user can pick from preset built-in patterns by writing to the output test mode field [7:4] at 0xC0 or user defined patterns by writing to the user test mode field [2:0] at 0xC0. The user defined patterns should be loaded at address space 0xC1 through 0xD0, see the “SPI Memory Map” on page 31 for more detail. The test mode is enabled asynchronously to the sample clock, therefore several sample clock cycles may elapse before the data is present on the output bus.

ADDRESS 0XC0: TEST_IO

Bits 7:4 Output Test Mode

These bits set the test mode according to the description in “SPI Memory Map” on page 31.

Bits 2:0 User Test Mode

The three LSBs in this register determine the test pattern in combination with registers 0xC1 through 0xD0. Refer to the “SPI Memory Map” on page 31.

ADDRESS 0XC1: USER_PATT1_LSB

ADDRESS 0XC2: USER_PATT1_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 1.

ADDRESS 0XC3: USER_PATT2_LSB

ADDRESS 0XC4: USER_PATT2_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 2

ADDRESS 0XC5: USER_PATT3_LSB

ADDRESS 0XC6: USER_PATT3_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 3.

ADDRESS 0XC7: USER_PATT4_LSB

ADDRESS 0XC8: USER_PATT4_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 4.

ADDRESS 0XC9: USER_PATT5_LSB

ADDRESS 0XCA: USER_PATT5_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 5.

ADDRESS 0XCB: USER_PATT6_LSB

ADDRESS 0XCC: USER_PATT6_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 6.

ADDRESS 0XCD: USER_PATT7_LSB

ADDRESS 0XCE: USER_PATT7_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 7.

ADDRESS 0XCF: USER_PATT8_LSB

ADDRESS 0XD0: USER_PATT8_MSB

These registers define the lower and upper eight bits, respectively, of the user-defined pattern 8.

ADDRESS 0xDF - 0xF3: JESD204 Registers

Address 0xDF-0xEE: JESD204 Parameter Interface

This set of registers controls the JESD204 transmitter configuration. By programming these parameters, the system can select between efficient and simple packing, select the number of powered up SERDES lanes, choose the ADC resolution transmitted and so on. The JESD204 parameters for standard dual channel products are shown in Table 4 on page 23. This is a small subset of the total number of configurations supported; contact Intersil sales support for details.

0xE0 through 0xED are the JESD204 parameter registers. These parameters are written to set the transport layer mapping of the JESD204 transmitter in this product family. These registers can be written to shift between efficient and simple packing, to enable or bypass scrambling, and to reduce the number of powered up lanes used in the link. Each speed graded product

allows downgrading of the JESD204 link (such as reducing the number of lanes, reducing the converter resolution, etc), but not upgrading. These parameters are communicated on every lane of the link during the 2nd multiframe of the initial lane alignment sequence, and therefore can be used by a generic JESD204 receiver the supports the given configuration. See the JESD204 specification for additional information on how these registers are used in a JESD204 system, including encoding rules.

ADDRESS 0XDF: JESD204_UPDATE_CONFIG_START

Bit 0 Update_start

This self-resetting bit is used to indicate that some or all the JESD204 parameters (addresses 0xE0 through 0xED) are going to be written. Writing a '1' to this bit will hold the JESD204 PLL and transmitter in a reset state while these parameters are written, because these parameters can affect the transmitter's dynamic behavior (such as modifying the PLL's frequency multiplication). The bit will automatically reset to a '0' once a '1' is written to address 0xEE Bit[0] "update_config W1TC". The recommended sequence for modifying the JESD204 transmitter is as follows:

1. Write a '1' to 0xDF Bit[0]
2. Write some or all modified values to 0xE0 through 0xEC
3. Write a '1' to 0xEE Bit[0]. Note: 0xDF Bit[0] and 0xEE Bit[0] will automatically be reset to a '0' once configuration has been applied to the circuitry.

ADDRESS 0XE0: JESD204_CONFIG_0

Bits 7:0 "DID", JESD204 Device ID number.

ADDRESS 0XE1: JESD204_CONFIG_1

Bits 3:0 "BID", JESD204 Bank ID.

ADDRESS 0XE2: JESD204_CONFIG_2

Bits 4:0 "LID" JESD204 Lane ID.

ADDRESS 0XE3: JESD204_CONFIG_3

Bit 7 "SCR", JESD204 SCR controls if scrambling across the SERDES lane(s) is enabled ('1' means enabled).

Bits 4:0 "L", JESD204 L is the number of SERDES lanes in the link.

ADDRESS 0XE4: JESD204_CONFIG_4

Bits 7:0 "F", JESD204 Number of octets per frame period.

ADDRESS 0XE5: JESD204_CONFIG_5

Bits 4:0 "K" JESD204 Number of frame periods per multi-frame period. This product family supports the full programmable range of K (decimal 0 through 31), although note that the JESD204 standard dictates a minimum number for this parameter that is configuration dependent.

ADDRESS 0XE6: JESD204_CONFIG_6

Bits 7:0 "M" JESD204 Number of converters per device.

ADDRESS 0XE7: JESD204_CONFIG_7

Bits 7:6 "CS", JESD204 CS is the number of control bits per sample (Always '0' for this product family).

Bits 4:0 "N", JESD204 N is the converter resolution.

ADDRESS 0XE8: JESD204_CONFIG_8

Bits 4:0 "N'", JESD204 N' is the total number of bits per sample.

ADDRESS 0XE9: JESD204_CONFIG_9

Bits 4:0 "S", JESD204 Number of samples per converter per frame cycle.

ADDRESS 0XEA: JESD204_CONFIG_10

Bit 7 "HD", JESD204 HD indicates if a converter's sample can be split across multiple lanes in the link (always '0' for this product family).

Bits 4:0 "CF", JESD204 CF is the number of control fames per frame clock (always '0' for this product family).

ADDRESS 0XEB: JESD204_CONFIG_11

Bits 7:0 "RES1", JESD204 reserved for future use.

ADDRESS 0XEC: JESD204_CONFIG_12

Bits 7:0 "RES2", JESD204 reserved for future use.

ADDRESS 0XED: JESD204_CONFIG_13

Bits 7:0 "FCHK" JESD204 checksum (unsigned sum MOD 256) of all the other JESD204 parameter register values. This is a read-only register, as the checksum is calculated by the device.

ADDRESS 0XEE: JESD204_UPDATE_CONFIG_COMPLETE

Bit 0 Update_complete

This self-resetting bit is used to indicate that all the modifications to the JESD204 parameters are complete.

ADDRESS 0XEF: JESD204_PLL_MONITOR_RESET

Bit 0 "pll_lock_mon_rst", This self resetting register resets the state of the 0xF0 Bit[0] "latched_pll_lockn" bit. The purpose of this pair of bits is as a debugging feature to the system designer. The "latched_pll_lockn" bit indicates if the JESD204 transmitter PLL inside the device has at any time lost lock since the last '1' was written to the "pll_lock_mon_rst" bit. This can be used to help identify the source of intermittent link lost errors in the system.

ADDRESS 0XF0: JESD204_STATUS

Bit 2 "op_cfg_wrong" indicates if the JESD204 parameters (registers 0xE0 through 0xED) are supported by the JESD204 transmitter (a '1' indicates they are not supported, a '0' indicates they are supported).

Bit 1"pll_lockn" indicates if the JESD204 transmitter PLL is currently locked (a '1' indicates it is not locked, a '0' indicates it is locked).

Bit 0 "latched_pll_lockn" indicates if the JESD204 transmitter PLL has lost lock since the last assertion of the "pll_lock_mon_rst" (see register 0xEF description for more information).

ADDRESS 0XF1: JESD204_SYNC

Bit 0 "sync_req" this register provides a SPI-programmable interface that can be used to assert and deassert the JESD204 SYNC~ functionality. Certain systems may benefit from the elimination of SYNC~ as a separate board-level LVDS signal (and the power, PCB space and pins it consumes), and these systems can use this register to functionally assert and deassert SYNC~. For this bit to have any effect, a '1' must have previously been written to the SYNC_FUNCTION (Address 0x77, bit 0).

A '1' written to this bit will result in behavior identical to the assertion of SYNC~ (comma character generation) and '0' will result in the behavior identical to the deassertion of SYNC~ (initial lane alignment sequence followed by converter data). Usage of this SPI SYNC~ capability may compromise the system's ability to perform multi-chip time alignment, as the SYNC~ asserted to deasserted transition using this register is not well timed with respect to sample clock.

ADDRESS 0XF2: JESD204_TRANS_PAT_CONFIG

Bit 0 "no_mf_lane_sync", By default, this device family assumes that both sides of the link support lane synchronization. As per the JESD204 rev A standard, in this case continuous frame alignment monitoring via character substitution (section 5.3.3.4) is modified such that a different control character is substituted when the octet reoccurrence happens at the end of a multiframe. This behavior occurs when Bit 0 is '0' (the power on default). Writing a '1' to Bit 0 will inform the JESD204 transmitter than the receiving device does not support lane synchronization, and therefore the transmitter will no longer substitute this different control character when reoccurrence of octets occurs at the end of a multi-frame.

Bit 1 "trans_pat_max_len" There is some ambiguity of the proper length of the JESD204 rev A section 5.1.6.2 required transport layer test pattern. Specifically, that the description perhaps should have "max()" in place of "min()" for the equation defining the length of the pattern. Setting Bit 1 in this register to a '0' (also the power-on default) and issuing this test pattern by writing to 0xC0 will cause the pattern to assume a "min()" interpretation of the pattern described in section 5.1.6.2. Setting the bit to a '1' will assume a "max()" interpretation of the described pattern.

ADDRESS 0XF3: JESD204_CML_POLARITY

0xF3 Bit[2:0]: "TX polarity flip lane x" This register allows the system designer to invert the sense of the SERDES pins on a per lane basis. For example, writing a '1' to Bit[0] causes LANE0N to functionally become LANE0P and LANE0P to become LANE0N. This feature allows the system designer to avoid having to crossover P and N sides of the CML pair on the board to match pin out and layout of the transmitter and receiver. Typically, a trace crossover would require vias, which can degrade the signal integrity of the high-speed SERDES lanes.

ADDRESS 0XFE: OFFSET/GAIN_ADJUST_ENABLE

Bit 0 at this register must be set high to enable adjustment of offset coarse and fine adjustments (0x20 and 0x21) and gain medium and gain fine adjustments(0x23 and 0x24). It is recommended that new data be written to the offset and gain adjustment registers (0x20, 0x21, 0x23, 0x24) while Bit 0 is a '0'. Subsequently, Bit 0 should be set to '1' to allow the values written to the aforementioned registers to be used by the ADC. Bit 0 should be set to a '0' upon completion.

SPI Memory Map

	ADDR. (HEX)	PARAMETER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEF. VALUE (HEX)
SPI Config/Control	00	port_config	SDO Active	LSB First	Soft Reset			Mirror (Bit 5)	Mirror (Bit 6)	Mirror (Bit 7)	00h
	01	Reserved	Reserved								
	02	burst_end	Burst end address [7:0]								00h
	03-07	Reserved	Reserved								
DUT Info	08	chip_id	Chip ID #								Read only
	09	chip_version	Chip Version #								Read only
	0A-0F	Reserved	Reserved								

SPI Memory Map (Continued)

	ADDR. (HEX)	PARAMETER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEF. VALUE (HEX)
Device Config/Control	10-1F	Reserved	Reserved								
	20	offset_coarse_CoreA	Coarse Offset								cal. value
	21	offset_fine_CoreA	Fine Offset								cal. value
	22	gain_coarse_CoreA	Reserved				Coarse Gain				cal. value
	23	gain_medium_CoreA	Medium Gain								cal. value
	24	gain_fine_CoreA	Fine Gain								cal. value
	25	modes_CoreA	Reserved					Power Down Mode CoreA [2:0] 000 = Pin Control 001 = Normal Operation 010 = Nap 100 = Sleep Other codes = Reserved			00h NOT reset by soft reset
	26	offset_coarse_CoreB	Coarse Offset								cal. value
	27	offset_fine_CoreB	Fine Offset								cal. value
	28	gain_coarse_CoreB	Reserved				Coarse Gain				cal. value
	29	gain_medium_CoreB	Medium Gain								cal. value
	2A	gain_fine_CoreB	Fine Gain								cal. value
	2B	modes_CoreB	Reserved					Power Down Mode CoreB [2:0] 000 = Pin Control 001 = Normal Operation 010 = Nap 100 = Sleep Other codes = Reserved			00h NOT reset by soft reset
	2C-6F	Reserved	Reserved								
	70	skew_diff	Differential Skew								80h
	71	phase_slip	Reserved							Next Clock Edge	00h
	72	clock_divide						Clock Divide [2:0] 000 = Pin Control 001 = divide by 1 010 = divide by 2 100 = divide by 4 Other codes = Reserved			01h NOT reset by soft reset
Device Config/Control	73	output_mode_A						Output Format [2:0] 000 = Two's Complement (Default) 010 = Gray Code 100 = Offset Binary Other codes = Reserved			00h NOT reset by soft reset
	74	output_mode_B		DLL Range 0 = Fast 1 = Slow Default='0'							00h NOT reset by soft reset
	75-76	Reserved	Reserved								
	77	SYNC_function								Clkdivrst	
	78-B5	Reserved	Reserved								
	B6	cal_status	Reserved							Calibration Done	Read only
	B7-BF	Reserved									

SPI Memory Map (Continued)

	ADDR. (HEX)	PARAMETER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEF. VALUE (HEX)
Device Test	C0	test_io	Output Test Mode [7:4]				JESD Test	User Test Mode [2:0]			00h
			<7:4> = Output Test, <3> = JESD Test JESD Test = 0 Output Test = 0x0 = Output Test Mode Off. During calibration MSB justified constant output 0xCCCC 0x1 = Midscale adjusted by numeric format 0x2 = Plus full scale, adjusted by numeric format 0x3 = Minus full scale adjusted by numeric format 0x4 = Checkboard output - 0xAAAA, 0x5555 0x5 = reserved 0x6 = reserved 0x7 = 0xFFFF, 0x0000 all on pattern 0x8 = User pattern 8 deep, MSB justified with output 0x9 = reserved 0xA, Count-up ramp 0xB, PRBS-9 0xC, PRBS-15 0xD, PRBS-23 0xE, PRBS-31 0xF = reserved JESD Test=1 Output Test = 0x0 = Link Layer Repeat K28.5+Lane Alignment Sequence 0x1, Link Layer Repeat K28.5 0x2, Link Layer Repeat D21.5 0x3, Link Layer Repeat K28.7 0x4, Link Layer PRBS-7 0x5, Link Layer PRBS-23 0x6, Link Layer All Zeros 0x7, Link Layer All Ones 0x8 - 0xE, reserved 0xF, JESD204 section 5.1.6.2 Transport Layer Test Pattern					User Test Mode (Single ADC products only) 0 = user pattern 1 only 1 = cycle pattern 1 through 2 2 = cycle pattern 1 through 3 3 = cycle pattern 1 through 4 4 = cycle pattern 1 through 5 5 = cycle pattern 1 through 6 6 = cycle pattern 1 through 7 7 = cycle pattern 1 through 8 User Test Mode (Dual and interleaved ADC products only) 0 = cycle pattern 1 through 2 1 = cycle pattern 1 through 4 2 = cycle pattern 1 through 6 3 = cycle pattern 1 through 8 4 through 7 = NA			
	C1	user_patt1_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	C2	user_patt1_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	C3	user_patt2_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	C4	user_patt2_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	C5	user_patt3_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	C6	user_patt3_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	C7	user_patt4_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	C8	user_patt4_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	C9	user_patt5_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	CA	user_patt5_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	CB	user_patt6_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	CC	user_patt6_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	CD	user_patt7_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	CE	user_patt7_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	CF	user_patt8_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h
	D0	user_patt8_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h
	D1-DE	Reserved	Reserved								

SPI Memory Map (Continued)

	ADDR. (HEX)	PARAMETER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEF. VALUE (HEX)
JESD204 Interface	DF	JESD204_update_config_start								update_ start	00h
	E0	JESD204_config_0	*DID* (Device ID Number)								00h
	E1	JESD204_config_1					*BID* (Bank ID Number)				See Description for Default Settings
	E2	JESD204_config_2				*LID* (Lane ID Number)					
	E3	JESD204_config_3	SCR			*L* (Number of Lanes per Device)					
	E4	JESD204_config_4	*F* (Number of Octets per Frame)								
	E5	JESD204_config_5				K (Number of frames per multiframe)					
	E6	JESD204_config_6	*M* (Number of Converters per Device)								
	E7	JESD204_config_7	*CS* (Number of Control bits per Sample)			*N* (Converter Resolution in bits)					
	E8	JESD204_config_8				*N'* (Total number of bits per Sample)					
	E9	JESD204_config_9				*S* (Number of Samples per Converter per Frame)					
	EA	JESD204_config_10	HD			*CF* (Number of Control Words per Frame per Link)					
	EB	JESD204_config_11	RES1								
	EC	JESD204_config_12	RES2								
	ED	JESD204_config_13	*FCHK* (Checksum)								
	EE	JESD204_update_config_ complete								update_ complete	00h
	EF	JESD204_PLL_monitor_reset								pll_lock_ mon_rst	00h
	F0	JESD204_status						op_confg_ wrong	pll_lockn	latched_ pll_lockn	00h
	F1	JESD204_sync								sync_req	
	F2	JESD204_trans_pat_config							trans_pat_ max_len	no_mf_ lane_sync	
	F3	JESD204_CML_polarity						lane_2_ polarity	lane_1_ polarity	lane_0_ polarity	00h
	F4-FD	Reserved	Reserved								
	FE	Offset/Gain_Adjust_Enable								Enable ‘1’=Enable	00h
	FF	Reserved	Reserved								

Equivalent Circuits

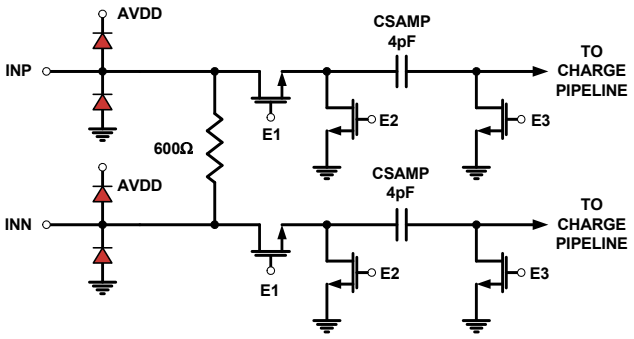


FIGURE 60. ANALOG INPUTS

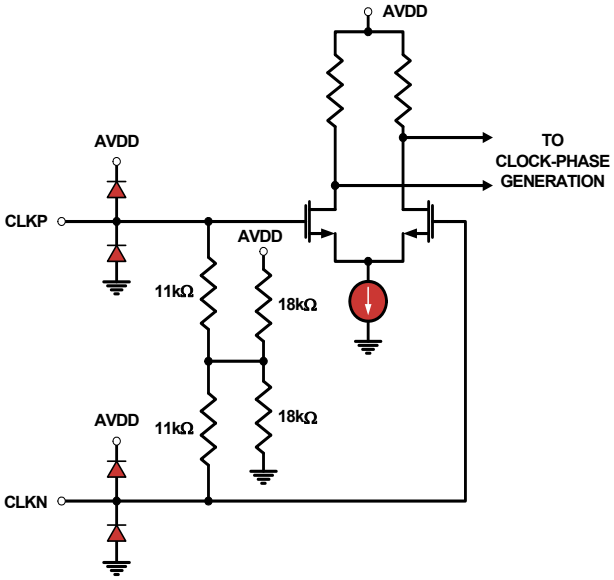


FIGURE 61. CLOCK INPUTS

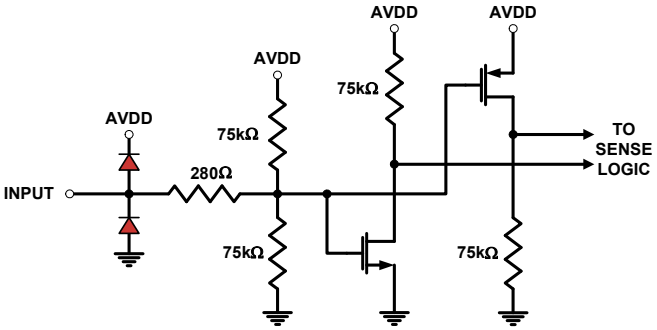


FIGURE 62. TRI-LEVEL DIGITAL INPUTS

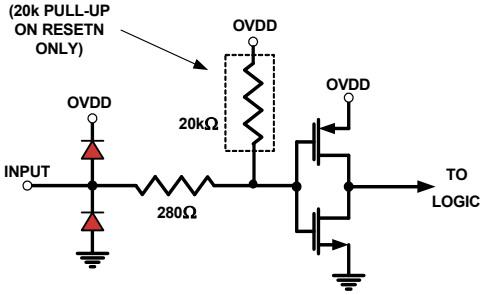


FIGURE 63. DIGITAL INPUTS

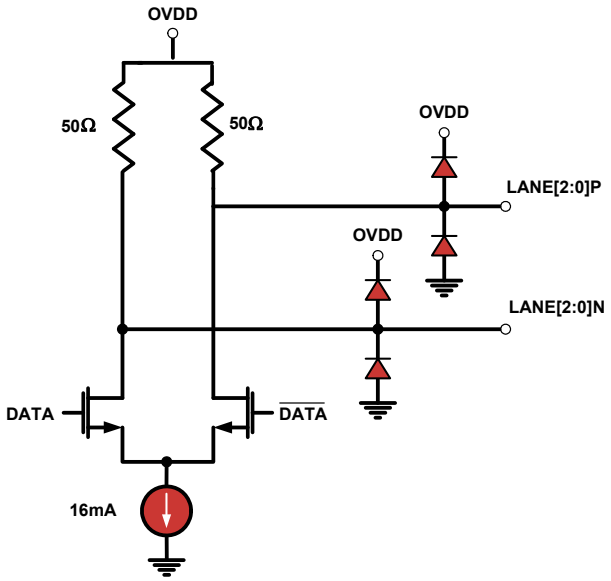


FIGURE 64. CML OUTPUTS

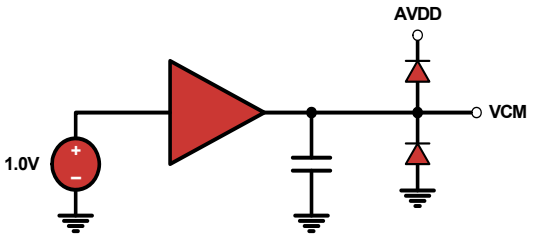


FIGURE 65. VCM_OUT OUTPUT

ADC Evaluation Platform

Intersil offers ADC Evaluation platforms, which can be used to evaluate any of Intersil's high speed ADC products. Each platform consists of a FPGA based data capture motherboard and a family of ADC daughtercards. The USB interface and evaluation platform control software allow a user to quickly evaluate the ADC's performance at a user's specific application frequency requirements. More information is available at http://www.intersil.com/converters/adc_eval_platform/

Layout Considerations

Split Ground and Power Planes

Data converters operating at high sampling frequencies require extra care in PC board layout. Many complex board designs benefit from isolating the analog and digital sections. Analog supply and ground planes should be laid out under signal and clock inputs. Locate the digital planes under outputs and logic pins. Grounds should be joined under the chip.

Clock Input Considerations

Use matched transmission lines to the transformer inputs for the analog input and clock signals. Locate transformers and terminations as close to the chip as possible.

Exposed Paddle

The exposed paddle must be electrically connected to analog ground (AVSS) and should be connected to a large copper plane using numerous vias for optimal thermal performance.

Bypass and Filtering

Bulk capacitors should have low equivalent series resistance. Tantalum is a good choice. For best performance, keep ceramic bypass capacitors very close to device pins, as longer traces between the ceramic bypass capacitors and the device pins will increase inductance, which can result in diminished dynamic performance. Best practices bypassing is especially important on the AVDD and OVDD(PLL) power supply pins. Whenever possible, each supply pin should have its own 0.1µF bypass capacitor. Make sure that connections to ground are direct and low impedance. Avoid forming ground loops.

CML Outputs

Output traces and connections must be designed for 50Ω (100Ω differential) characteristic impedance. Keep traces direct and short, and minimize bends and vias where possible. Avoid crossing ground and power-plane breaks with signal traces. Keep good clearance (at least 5 trace widths) between the SERDES traces and other signals. Given the speed of these outputs and importance of maintaining an open eye to achieve low BER, signal integrity simulations are recommended, especially when the data lane rate exceeds 3Gbps and/or the trace or cable length between the ADC and the receiver gets larger than 20cm.

Unused Inputs

Standard logic inputs (RESETN, CSB, SCLK, SDIO, SDO) which will not be operated, do not require connection to ensure optimal ADC performance. These inputs can be left floating if they are not used. Tri-level inputs (NAPSLP) accept a floating input as a valid state and therefore should be biased according to the desired functionality.

Definitions

Analog Input Bandwidth is the analog input frequency at which the spectral output power at the fundamental frequency (as determined by FFT analysis) is reduced by 3dB from its full scale low-frequency value. This is also referred to as Full Power Bandwidth.

Aperture Delay or Sampling Delay is the time required after the rise of the clock input for the sampling switch to open, at which time the signal is held for conversion.

Aperture Jitter is the RMS variation in aperture delay for a set of samples.

Clock Duty Cycle is the ratio of the time the clock wave is at logic high to the total time of one clock period.

Differential Non-Linearity (DNL) is the deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB) is an alternate method of specifying Signal to Noise-and-Distortion Ratio (SINAD). In dB, it is calculated as: ENOB = (SINAD - 1.76)/6.02

Gain Error is the ratio of the difference between the voltages that cause the lowest and highest code transitions to the full scale voltage less than 2 LSB. It is typically expressed in percent.

I2E The Intersil Interleave Engine. This highly configurable circuitry performs estimates of offset, gain, and sample time skew mismatches between the core converters, and updates analog adjustments for each to minimize interleave spurs.

Integral Non-Linearity (INL) is the maximum deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Least Significant Bit (LSB) is the bit that has the smallest value or weight in a digital word. Its value in terms of input voltage is $V_{FS}/(2^N - 1)$ where N is the resolution in bits.

Missing Codes are output codes that are skipped and will never appear at the ADC output. These codes cannot be reached with any input value.

Most Significant Bit (MSB) is the bit that has the largest value or weight.

Pipeline Delay is the number of clock cycles between the initiation of a conversion and the appearance at the output pins of the data.

Power Supply Rejection Ratio (PSRR) is the ratio of the observed magnitude of a spur in the ADC FFT, caused by an AC signal superimposed on the power supply voltage.

Signal-to-Noise and Distortion (SINAD) is the ratio of the RMS signal amplitude to the RMS sum of all other spectral components below one half the clock frequency, including harmonics but excluding DC.

Signal-to-Noise Ratio (without Harmonics) is the ratio of the RMS signal amplitude to the RMS sum of all other spectral components below one-half the sampling frequency, excluding harmonics and DC.

SNR and SINAD are either given in units of dB when the power of the fundamental is used as the reference, or dBFS (dB to full scale) when the converter's full scale input power is used as the reference.

Spurious-Free-Dynamic Range (SFDR) is the ratio of the RMS signal amplitude to the RMS value of the largest spurious spectral component. The largest spurious spectral component may or may not be a harmonic.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
July 6, 2015	FN8302.1	Removed Product Availability column from "Pin-compatible Family" on page 1. Removed "Coming Soon" from parts in ordering information on page 4 and changed ADCMB-HSFMC-EV1Z to ADCMB-HSFMCEV1Z Changed default value for register 72 from 00h to 01h in "SPI Memory Map" on page 32. Under "Address 0x72: clock_divide" on page 28, replaced the sentence "By default, the tri-level CLKDIV pin selects the divisor." with the sentence "By default, CLOCK_DIVIDE is set to divide by 1. In Table 11 on page 28, added the phrase "(Default)" to the right of "Divide by 1" in the second row.
May 1, 2012	FN8302.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

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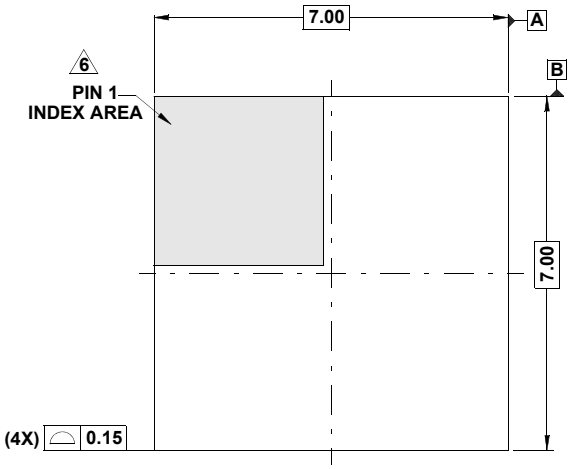
Package Outline Drawing

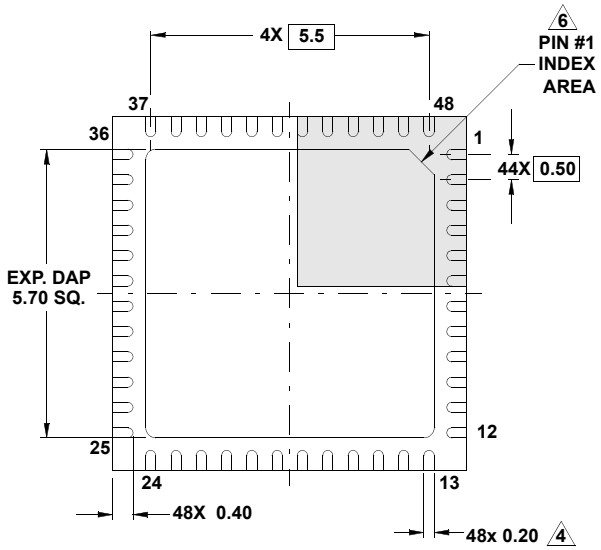
L48.7x7G

48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

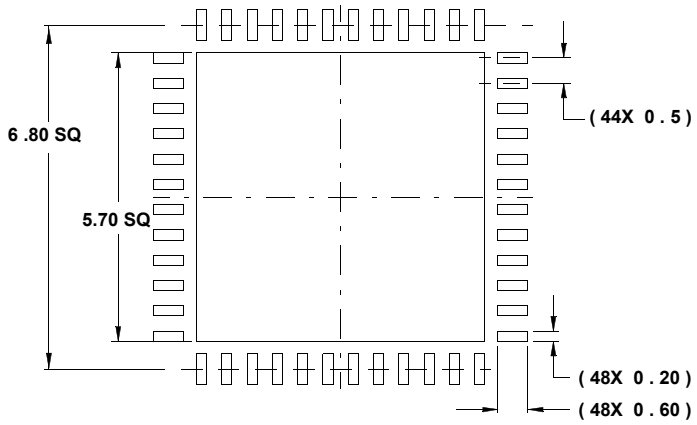
Rev 0, 1/10



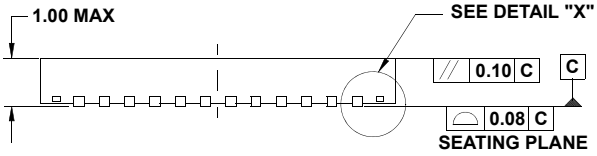
TOP VIEW



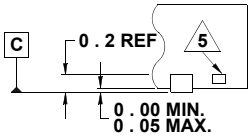
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.015mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.