MP3312L

2.7V-5.5V Input , 38V OVP, Dual-Channel White LED Driver

The Future of Analog IC Technology

DESCRIPTION

The MP3312L is a dual-channel, step-up WLED driver with an integrated 40V MOSFET. It supports a 2.7V to 5.5V power supply input and uses peak current mode to regulate the LED current, which is set by an external resistor.

The MP3312L employs a 600kHz fixed switching frequency. It supports both PWM input analog dimming and digital analog dimming to regulate the dimming current accurately.

The MP3312L integrates a current source to balance the LED current, which leads to good ILED matching and accuracy performance.

In addition, the MP3312L has both LED open and short protection, cycle-by-cycle current limit protection, and thermal shutdown protection. It is available in a tiny WLCSP1.35x1.35-9mm package.

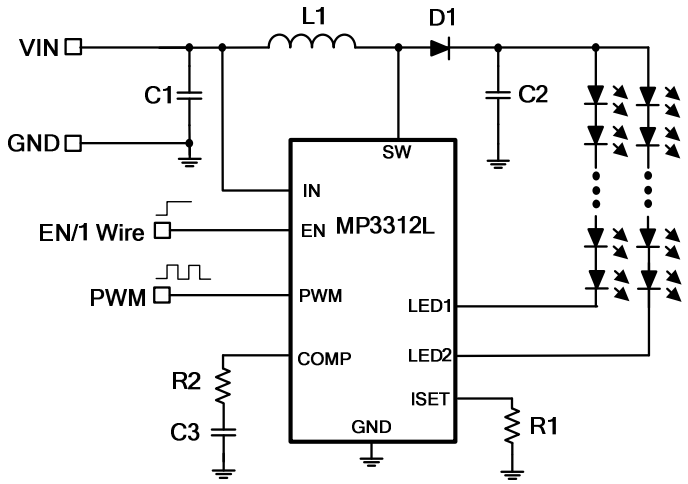
FEATURES

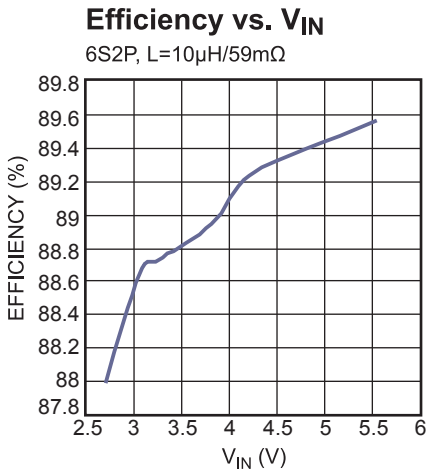
- 2.7V~5.5V Input Voltage
- 600kHz Switching Frequency
- Dual Channels Support up to 30mA/String
- 1% Current Matching between LED Channels
- +/-2% Current Accuracy
- 38V OVP
- PWM Input Analog Dimming Mode
- 5kHz to100kHz PWM Input Analog Dimming
- 1-Wire Interface for Digital Dimming
- 9-Bit Dimming Resolution
- Internal Soft Start to Reduce Inrush Current
- Available in WLCSP1.35x1.35-9mm Package

APPLICATIONS

- Feature Phones and Smart Phones
- Tablets
- GPS Receivers
- <10 Inch LCD Video Displays with One-Cell Li-Ion Battery

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP3312LGC	WLCSP1.35x1.35-9mm	*See Below*

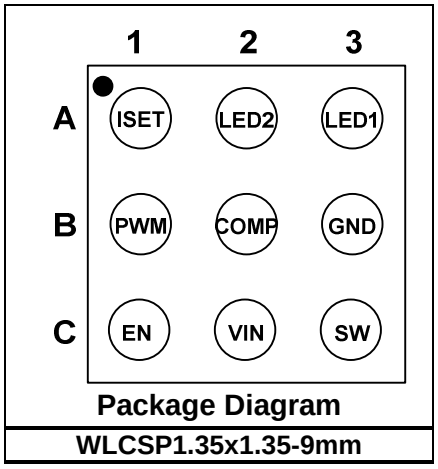
* For Tape & Reel, add suffix –Z (e.g. MP3312LGC–Z)

TOP MARKING

DMY
LLL

DM: Product code of MP3312LGC
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



Package Diagram

WLCSP1.35x1.35-9mm

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +6V
V_{SW} ..... -1V to +40V
V_{LED1}, V_{LED2} ..... -0.3V to +40V
All other pins ..... –0.3V to +6V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (T_A = 25°C) (2)
WLCSP1.35x1.35-9mm 1.04W

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.7V to 5.5V
Operating junction temp. ..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

WLCSP1.35x1.359mm ..... 120 ..... 12.. °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.7V, V_{EN} = V_{PWM} = high, typical values are at T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Power Supply						
Operating input voltage	V_{IN}		2.7		5.5	V
Supply current (quiescent)	I_Q	V_{IN} = 3.7V, V_{EN} = V_{PWM} = high, no load with switching		1	2	mA
Supply current (shutdown)	I_{ST}	V_{EN} = 0V, V_{IN} = 3.7V			1	μA
Input UVLO threshold	V_{IN_UVLO}	Rising edge		2.4	2.6	V
Input UVLO hysteresis				200		mV
Oscillator						
Switching frequency	f_{SW}		500	600	720	kHz
Maximum duty cycle	D_{MAX}		93	95		%
Minimum on time(5)	T_{ON_MIN}			100		ns
Power Switch						
Main switch on resistance	R_{DSON_M}	VIN = 3.7V		0.2		Ω
Error Amplifier						
Error amplifier transconductance	gm			370		μS
Max sink/source current				42		μA
Current Regulation						
VLEDx regulation voltage	V_{REG}	ILED1 = ILED2 = 20mA		240		mV
ISET voltage	V_{ISET}		1.207	1.232	1.247	V
Current multiplier	K_{ISET}			1020		
Current accuracy		I_{ISET} = 20μA, ($\|I_{MIN}-I_{ISET}\|/I_{ISET}$,$\|I_{MAX}-I_{ISET}\|/I_{ISET}$)	-2		2	%
Current matching		I_{ISET} = 20μA, ($I_{MAX} - I_{MIN}$) /I_{AVG}		1	2	%
Current sink max output current			30			mA
EN & PWM Logic						
PWM input high threshold	V_{PWM_HI}	V_{PWM} rising	1.2			V
PWM input low threshold	V_{PWM_LO}	V_{PWM} falling			0.4	V
EN high voltage	V_{EN_HIGH}	V_{EN} rising	1.2			V
EN low voltage	V_{EN_LOW}	V_{EN} falling			0.4	V
EN & PWM pull-down resistor	R_{PD}			800		kΩ
EN low logic to shutdown time	T_{SD_EN}	EN high to low	2.5			ms
PWM low logic to shutdown time	T_{SD_PWM}	PWM high to low	20			ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.7V, V_{EN} = V_{PWM} = high, typical values are at T_A = 25°C, unless otherwise noted.

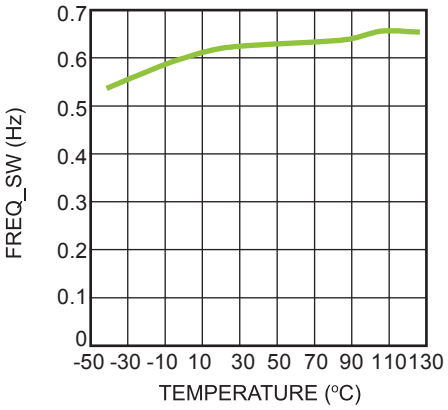
Parameters	Symbol	Condition	Min	Typ	Max	Unit
Protection						
OVP voltage	V_{OVP}		37	38	39.5	V
Cycle-by-cycle current limit	I_{LIM}	Max duty cycle	1.2	1.8		A
Start-up current limits(5)	I_{LIM_START}	Max duty cycle		1		A
Time step for half current limit(5)	T_{LIM_HALF}			6		ms
LEDx threshold when no switching				560		mV
LEDx over-voltage threshold	V_{OVP_LED}		4.5	5	5.5	V
Thermal shutdown threshold	T_{ST}			150		°C
Thermal shutdown hysteresis				25		°C
1-Wire Interface						
1-wire detection delay time	t_{DELAY}		100			µs
1-wire detection time	$t_{DETECTION}$		260			µs
1-wire detection window	t_{WIN}		1			ms
Start time of program stream	t_{START}		2			µs
End time of program stream	t_{EOS}		2		360	µs
High time of logic 0 bit	t_{H_LB}		5		180	µs
Low time of logic 0 bit	t_{L_LB}		3* t_{H_LB}		360	µs
High time of logic 1 bit	t_{H_HB}		3* t_{L_HB}		360	µs
Low time of logic 1 bit	t_{L_HB}		5		180	µs
Acknowledge valid time	t_{ACKval}				2	µs
Duration of acknowledge signal	t_{ACK}				512	µs
Acknowledge output voltage low(6)	V_{ACKL}	Open drain, R_{PULLUP} = 15kΩ to V_{IN}			0.4	V

NOTES:

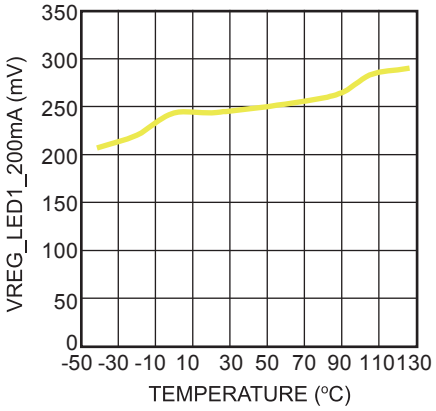
5) Guaranteed by design and characterization.
6) ACK signal is active 0 (when ACK signal is true, the data line is pulled down by the chip). This signal only replies when the RFA bit is set to 1. If you want to use the ACK signal, the master should have an open-drain output, and the data line should be pulled high by the master with a resistor load.

TYPICAL CHARACTERISTICS

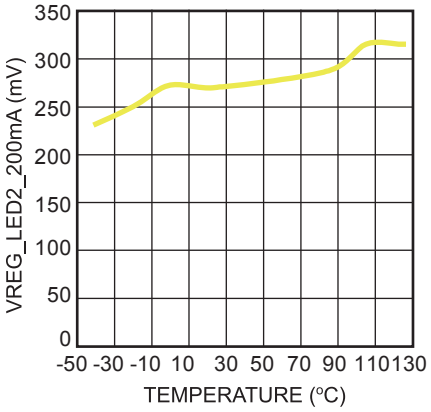
Freq_SW vs. Temperature Chart



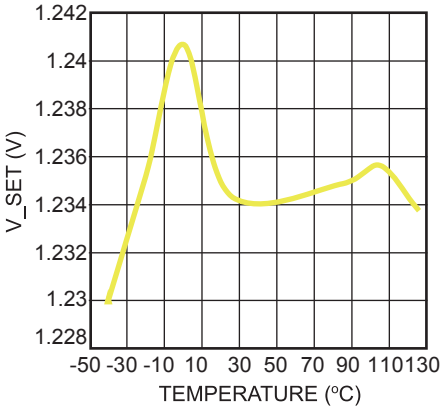
V_LED1(20mA) vs. Temperature Chart



V_LED2(20mA) vs. Temperature Chart



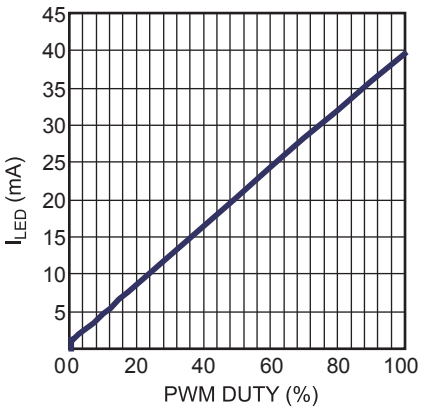
V_ISET(20mA) vs. Temperature Chart



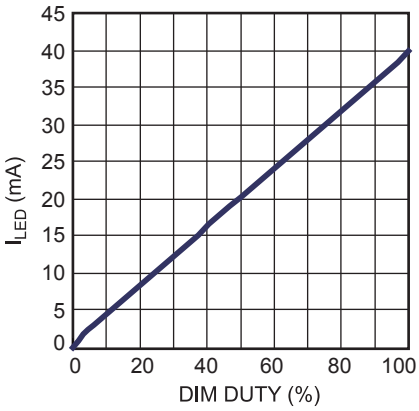
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.7V, 6*LEDs/string, ILED1 = ILED2 = 20mA, L = 10µH, T_A = 25°C, unless otherwise noted.

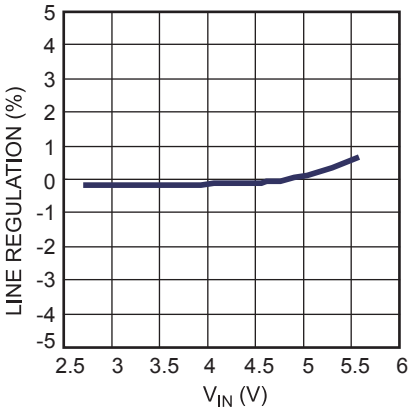
Analog Dimming Curve



1-Wire Dimming Curve

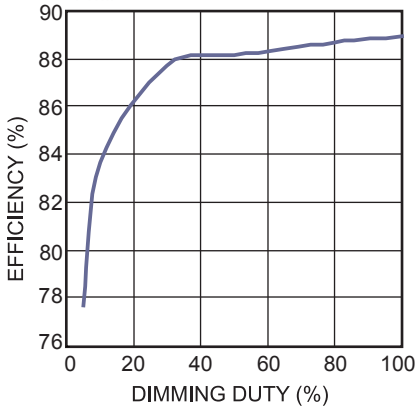


Line Regulation



Efficiency when Dimming

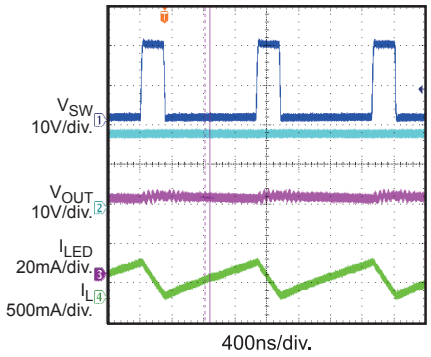
F_{PWM}=25kHz, L=10µH/59mΩ



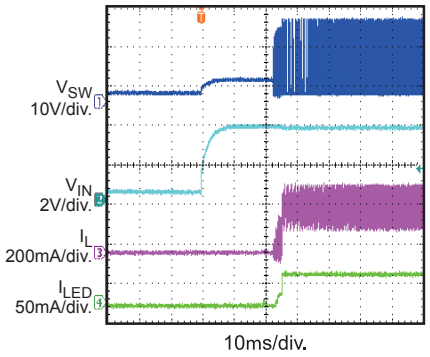
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.7V, 6*LEDs/string, ILED1 = ILED2 = 20mA, L = 10µH, T_A = 25°C, unless otherwise noted.

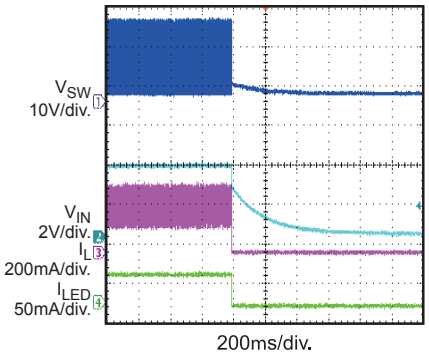
Steady State



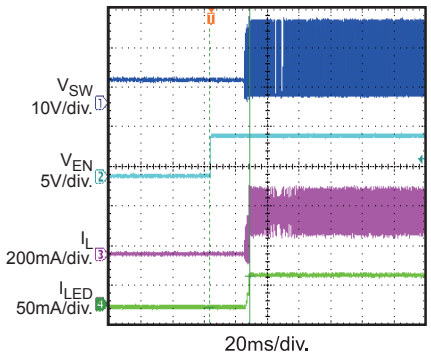
V_{IN} Power On



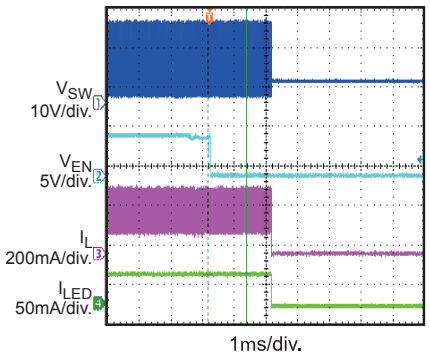
V_{IN} Power Off



En Power On

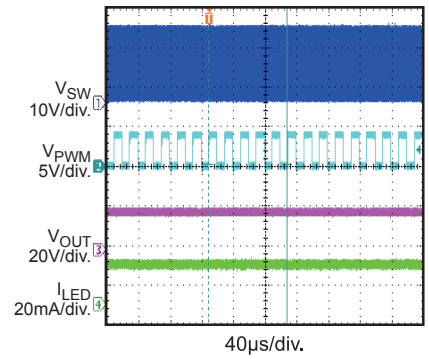


En Power Off

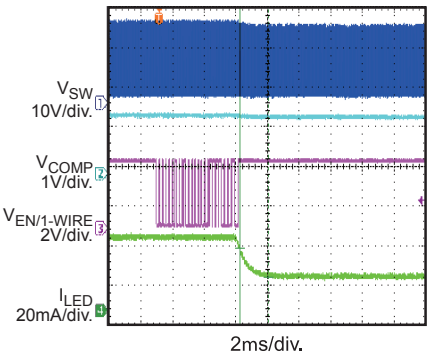


PWM Input Analog Dimming

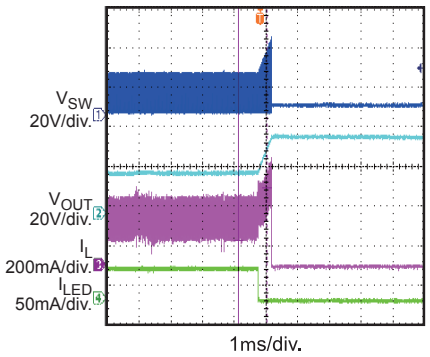
f_{PWM}=50kHz



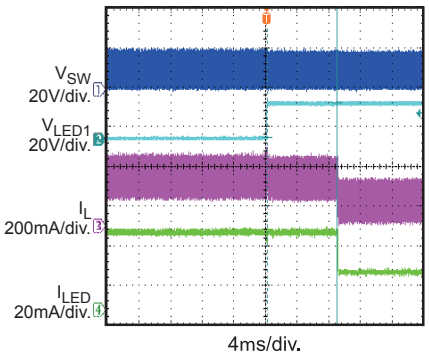
1-Wire Dimming (01FF to 0100)



Open-Load Protection



Short 1-String Protection



PIN FUNCTIONS

Pin #	Name	Description
A1	ISET	**Full scale LED current set.** Connecting a resistor between ISET and GND sets the full scale current.
A2	LED2	**LED2 current sink.**
A3	LED1	**LED1 current sink.**
B1	PWM	**PWM signal input.** A 5kHz to 100kHz PWM signal is recommended for PWM for analog current dimming. Low logic for >20ms shuts down the IC.
B2	COMP	**Internal error amplifier output .** Connect a capacitor to compensate the system.
B3	GND	**Ground.**
C1	EN	**Enable and 1-wire input.** Logic high enables the IC, and low logic >2.5ms shuts down the IC.
C2	VIN	**Power supply input.** Connect a ceramic capacitor close to VIN to bypass the IC.
C3	SW	**Drain connection of the internal N-channel power MOSFET.**

FUNCTIONAL BLOCK DIAGRAM

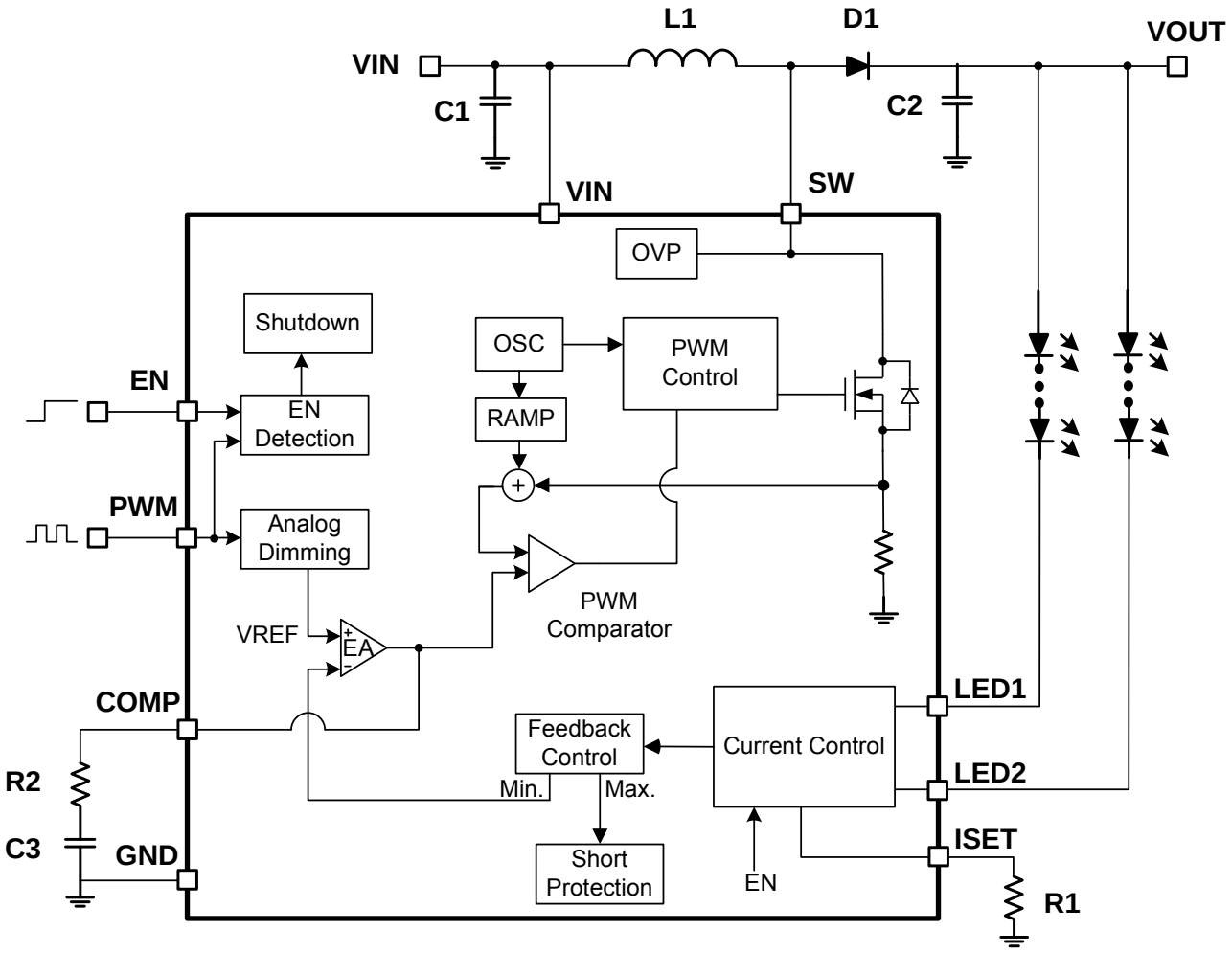


Figure 1: Functional Block Diagram

OPERATION

The MP3312L employs a fixed switching frequency, peak-current-mode control architecture, and two regulated current sinks to power the LED array (see Figure 1).

System Start-Up

Pulling EN and PWM high enables the IC while pulling EN to GND for >2.5ms (or pulling PWM to GND for >20ms) shuts down the IC.

When enabled, the MP3312L checks the topology connection first. Also, the MP3312L checks UVLO and over-temperature protection (OTP). If all the protections pass, the chip starts boosting the step-up converter with an internal soft start.

It is recommended that the enable signal occurs after the establishment of the input voltage and PWM dimming signal during the start-up sequence to avoid large inrush current.

Switching Operation

At the start of each oscillator cycle, the main low-side FET (M1) is turned on through the control circuitry. To prevent sub-harmonic oscillation at a duty cycle greater than 50%, a stabilizing ramp is added to the output of the current sense amplifier; the result is fed into the positive input of the PWM generation comparator. When this voltage equals the output voltage of the error amplifier, the main power FET is turned off. Then the inductor current flows through the free-wheeling diode, which forces the inductor current to decrease. The output voltage of the internal error amplifier is an amplified signal of the difference between the reference voltage and the feedback voltage. The converter chooses the lowest active LEDX pin voltage automatically to provide a high enough bus voltage to power all the LED arrays.

If the feedback voltage drops below the reference, the output of the error amplifier increases. This results in more current flowing through the MOSFET, thus increasing the power delivered to the output. This forms a closed loop that regulates the output voltage.

Dimming Control

The MP3312L supports analog dimming and 1-wire digital set dimming mode to regulate the WLED current.

For analog dimming, apply a PWM signal to PWM by adjusting the LED current amplitude. The internal filter is integrated, and the PWM signal (5k~100kHz range) is supported. The internal dimming signal duty detection circuit changes the internal reference linearly to regulate the current automatically.

In addition, EN supports a 1-wire interface for current dimming control.

1-Wire Interface

1-wire interface is based on a master-slave structure, which is designed for digital dimming. EN is a multipurpose single port that receives LED brightness data. The rate to detect the bit ranges from 1.39kit/sec to 50kBit/sec.

The command sent to the chip (slave) contains 24 bits and 9-bit dimming data. Also, an 8-bit device address and RFA bit are included. The chip detects the bit in the series and transmits the LSB first and the MSB last.

Refer to Figure 2 and the description of the control bits below:

- D0-D8 are the dimming data bits, which achieve a 9-bit dimming resolution.
- Bit 9 and bit 11-bit 15 are reserved. Set to 0.
- The RFA bit indicates if the master needs to request acknowledgment or not.
- The device address byte is DA0-DA7. The device address byte is set to 0x8F.

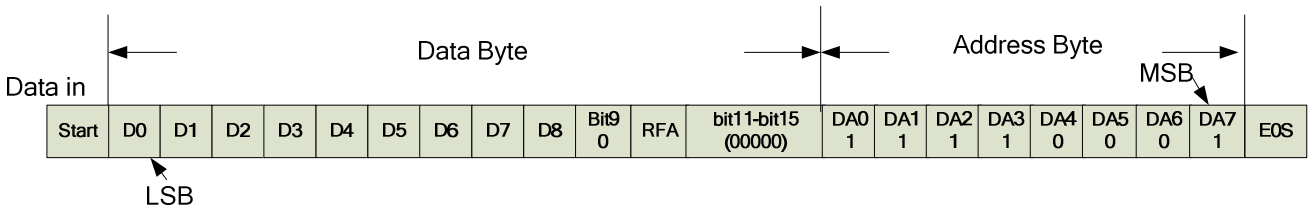


Figure 2: 1-Wire Command Structure

The 1-wire interface defines logic 0 and logic 1 by comparing the time between the signal's low level and high level; 1 cycle means 1 logic bit. The bit detection starts with a falling edge on EN and ends with the next falling edge. Low logic (logic 0): t_{LOW}≥3* t_{HIGH}. High logic (logic 1): t_{HIGH}≥3* t_{LOW} (see Figure 3).

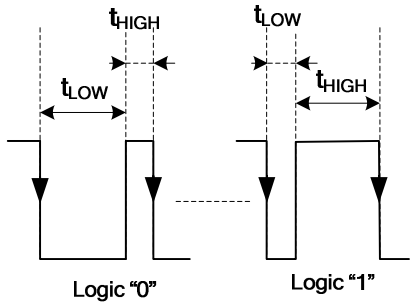


Figure 3: 1-Wire Bit Definition

EN must distinguish the EN signal and the digital dimming signal when setting up the boost driver. The chip only receives the 1-wire signal when the EN signal matches the 1-wire protocol during the 1ms 1-wire detection window. The 1-wire dimming sequence is described below and shown in Figure 4.

1. VIN and PWM are pulled high.
2. The data line is pulled from low to high for t_{DELAY} (1-wire detection delay time, 100μs). This rising edge is the start of the 1-wire detection window.
3. After the 1-wire detection delay time, the data line pulls low for more than $t_{DETECTION}$ (1-wire detection time, 260μs). Then the data line pulls high.
4. The sum of the 1-wire detection delay time and the 1-wire detection time should be less than t_{WIN} (the time of 1-wire detection window, 1ms).

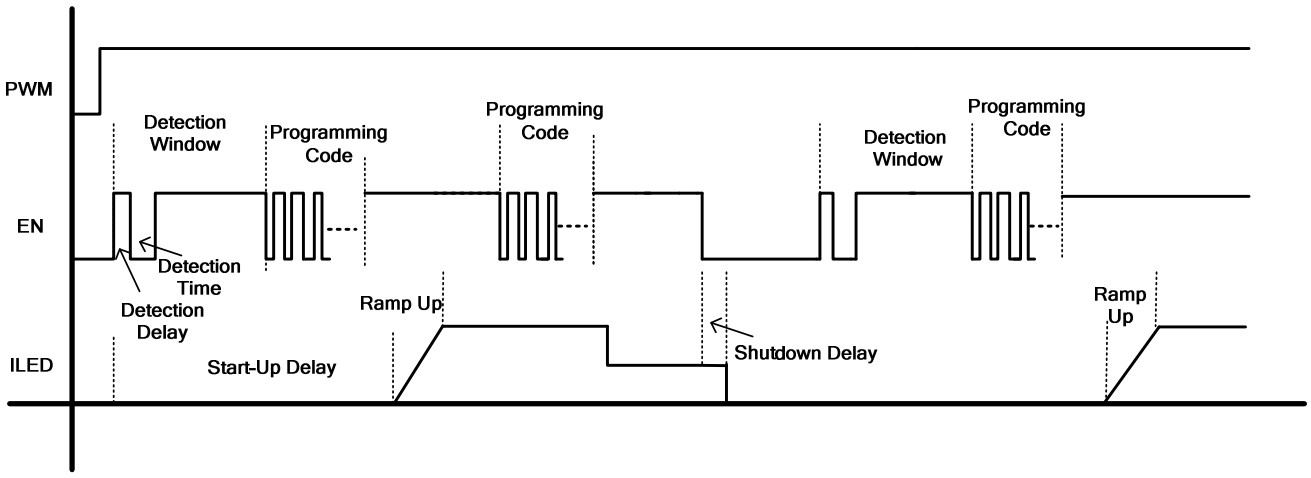


Figure 4: 1-Wire Dimming Sequence

In addition, before the chip starts to receive each command with the first falling edge, the data line should remain high for t_{START} (minimum, 2μs). The transmission of each command is completed with low levels for t_{EOS} (minimum 2μs). See Figure 5.

Whether the ACK signal feedback is sent to the master or not is dependent on the RFA bit. If ACK is needed, the master should have an open-drain output, and the data line should be pulled high by the master with a resistor load.

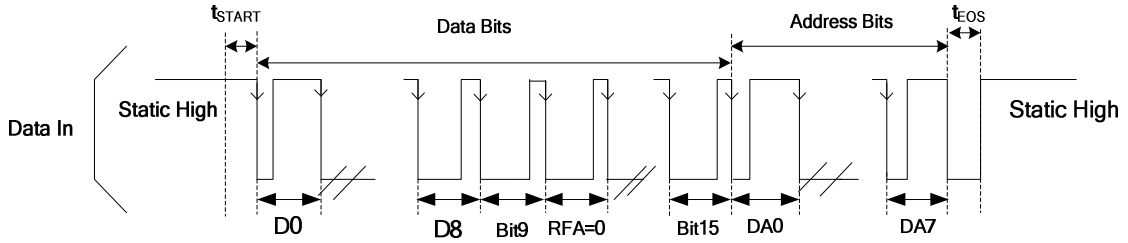


Figure 5: Data-Line Timing When RFA = 0

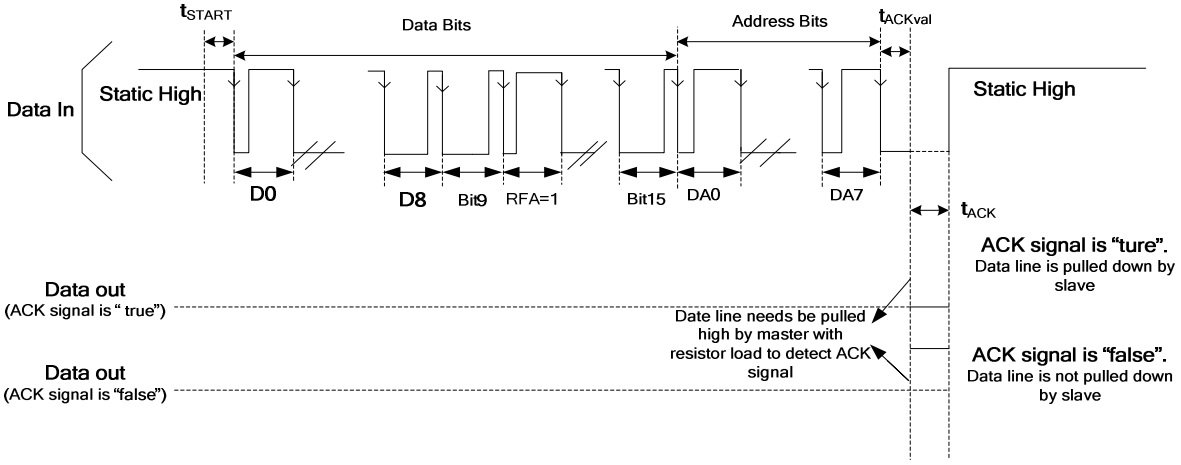


Figure 6: Data-Line Timing When RFA=1

If RFA = 0, there is no ACK signal feedback. After all 24 bits of data are transferred, the data line remains low for a t_{EOS} (minimum 2μs) delay, and then it is pulled to static high (see Figure 5).

If RFA = 1, the ACK signal feedback is sent to the master. After all 24 bits of data are transferred, the data line remains low for t_{ACKval} (maximum, 2μs), then the data line should be released to output high impedance. After this occurs, the master is ready to detect the ACK signal from the slave. After t_{ACKval}, if the ACK signal is "false" (1-wire data is not received successfully), the data line will be pulled high directly. After t_{ACKval}, if the ACK signal is "true" (1-wire data is received successfully), the data line is pulled low continuously (V_{ACKL} (max. 0.4V)) by the slave for t_{ACK} (max. 512μs). If the master reads this low logic, it means the chip has received the 1-wire data successfully, and the data line is pulled to static high (see Figure 6).

The MP3312L has a 9 bit DAC for digital dimming control; the dimming resolution is 1/511. The default code value of D0 (LSB)-D8(MSB) is "111111111" when the device is first enabled. The LED current is dependent on the internal register value D0-D8 according to Equation (1):

$$ILED = ILED_{full} \times \frac{code}{511} \quad (1)$$

$ILED_{full}$ is the full scale output current set by R_{ISET} to ISET. The code is the DEC value of the resolution bit (D0-D8).

Cycle-by-Cycle Current Limit Protection

The MP3312L provides cycle-by-cycle current limit protection to avoid damage caused by too large of a current rating. During start-up, the current limit is clamped to 1A for around 6ms to avoid output overshoot and inrush current. After start-up, the current limit returns back to a normal 1.8A.

Open-String Protection

Open-string protection is achieved by detecting VOUT. If the LED string is open, the feedback voltage is lower than the reference voltage, and thus the COMP rises up and keeps the charge of the output capacitor until VOUT hits the protection point OVP. Then the IC stops switching and shuts down until VIN and EN are reset for enable.

Unused LED Channel

In some cases, if one LED current channel is not used, LEDX must be connected to the corresponding GND to remove it from the control loop.

Short-String Protection

The MP3312L monitors the LEDX voltage to detect if the short string has occurred. If one string is short, the respective LEDX pin is pulled up to the boost output and tolerates high voltage stress. If the LEDX voltage is higher than 5V and the LED current is larger than the 8% of the full-scale setting current, the short-string condition is detected. If this condition lasts longer than 8ms, the fault string current source is disabled until VIN and EN are reset for enable.

Thermal Shutdown Protection

To prevent the IC from operating at exceedingly high temperatures, thermal shutdown is implemented in this chip by detecting the silicon die temperature. When the die temperature exceeds the upper threshold (150°, typically), the IC shuts down. It resumes normal operation once the die temperature drops below the lower threshold. Typically, the hysteresis value is 25°C.

APPLICATION INFORMATION

Setting the LED Current

The full scale LED current is set through the current-setting resistor on FB using Equation (2).

$$ILED(mA) = \frac{V_{ISET}(V)}{R_{ISET}(k\Omega)} * 1020 \quad (2)$$

For V_{ISET} = 1.232V and R_{ISET} = 63.4kΩ, the LED current is set to 20mA. Please do NOT leave ISET open.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be much less than the input source impedance to prevent the high-frequency switching current from passing through to the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients. For most applications, a 1μF~4.7μF ceramic capacitor will suffice.

Selecting the Inductor

The MP3312L requires an inductor to supply a higher output voltage while being driven by the input voltage. A larger value inductor results in less ripple current, resulting in lower peak inductor current, which reduces stress on the internal N-channel MOSFET. However, the larger value inductor has a larger physical size, a higher series resistance, and a lower saturation current.

Choose an inductor that does not saturate under the worst-case load conditions. Select the minimum inductor value to ensure that the boost converter works in continuous conduction mode with high efficiency and good EMI performance. Calculate the required inductance value using Equation (3) and Equation (4):

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times f_{SW} \times I_{LOAD}} \quad (3)$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad (4)$$

Where V_{IN} and V_{OUT} are the input and output voltages, f_{SW} is the switching frequency, I_{LOAD} is the total LED load current, and η is the efficiency. The switching current is used for the peak-current-mode control.

In order to avoid hitting the current limit, the worst-case inductor peak current should be less than 80% of the current limit (I_{LIM}). Generally, a 4.7μH~10μH inductor will suffice for most applications. Note that the system efficiency is dependent on the DC resistance of the inductor, and a larger DC resistance causes more power loss.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance must be low at the switching frequency. Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. Please note that ceramic capacitance is also dependent on the voltage rating; DC bias voltage and the value can lose as much as 50% of its capacitance at its rated voltage rating. Please leave a high enough voltage rating margin when selecting the component. However, if the capacitance is too low, it will cause loop instability. For most applications, a 1μF~4.7μF ceramic capacitor will suffice.

Selecting the External Schottky Diode

To optimize efficiency, a high-speed and low-reverse recovery current Schottky diode is recommended. Make sure the diode's average and peak current ratings exceed the output average LED current and the peak inductor current. In addition, the diode's breakdown voltage rating should be larger than the maximum voltage across the diode. Usually, unexpected high-frequency spikes in the voltage can be seen across the diode when the diode turns off. When selecting a diode, always leave a sufficient voltage rating margin to guarantee normal, long-term operation.

PCB Layout Guidelines

Efficient PCB layout is critical to prevent noise and electromagnetic interference. If the loop of MP3312L's internal low-side MOSFET, Schottky diode, and output capacitor flows with a high frequency ripple current, it MUST be minimized. The input and output capacitor should be placed as close to the IC as possible.

TYPICAL APPLICATION CIRCUITS

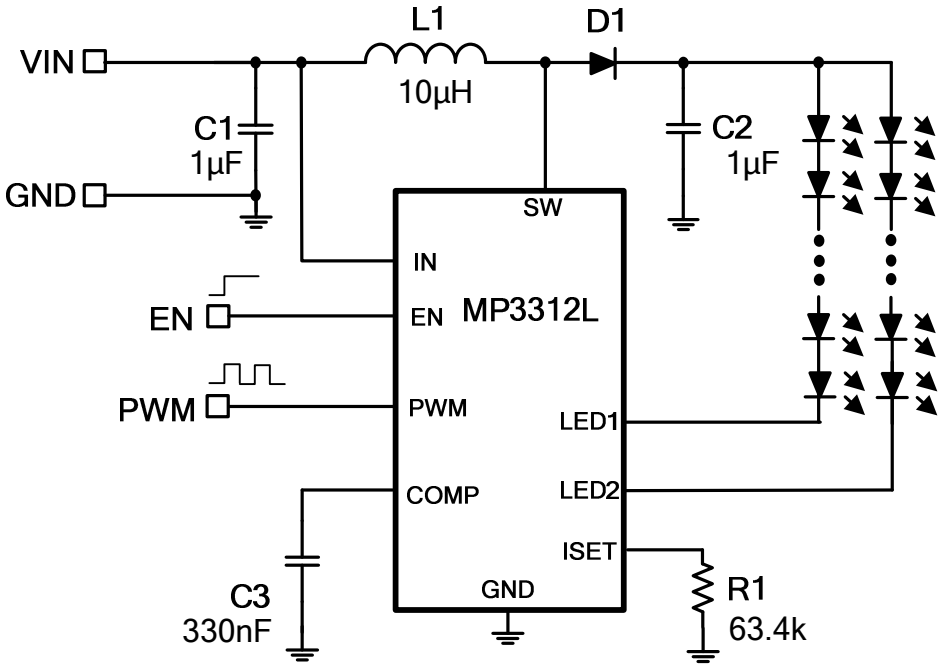
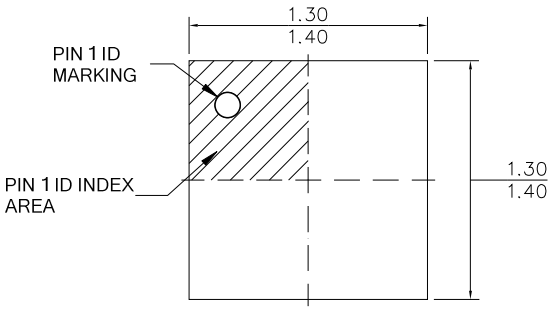


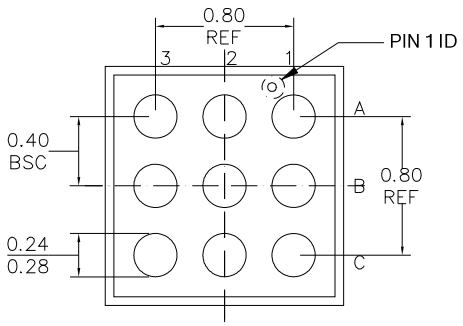
Figure 7: Typical Application for Dual String 6 LEDs, 20mA/String

PACKAGE INFORMATION

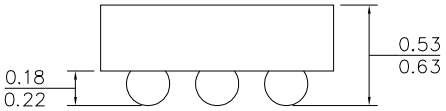
WLCSP1.35X1.35-9



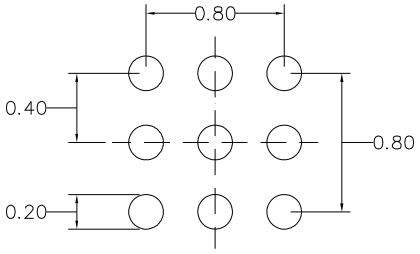
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211, VARIATION BC.
4) DRAWING IS NOT TO SCALE.