BLP0427M9S20; BLP0427M9S20G

Power LDMOS transistor

AMPLEON

Rev. 2 — 16 July 2021

Product data sheet

1. Product profile

1.1 General description

20 W plastic LDMOS power transistor for general purpose applications at frequencies from 400 MHz to 2700 MHz.

Table 1. Application performance (multiple frequencies)

Typical RF performance at T_{case} = 25 °C; I_{Dq} = 180 mA; in a class-AB demo board, tested on gull wing lead device.

Test signal	f	I_{Dq}	V_{DS}	$P_{L(AV)}$	$P_{L(1dB)}$	G_p	η_D
	(MHz)	(mA)	(V)	(dBm)	(dBm)	(dB)	(%)
pulsed	960 to 1215	100	28	-	43	17	>55
1-carrier	1805 to 1880	180	28	35	-	19	21
CW	30 to 512	150	28	-	43	19	>50

Table 2. Application performance

Typical RF performance at T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 100 mA; t_p = 300 μs; δ = 10 %; in a class-AB demo board, tested on straight lead device.

Test signal	f	P_L	G_p	$P_{L(1dB)}$	η_D	RL_{in}
	(MHz)	(dBm)	(dB)	(dBm)	(%)	(dB)
pulsed RF	1200 to 1400	43	19	43	63	–9

1.2 Features and benefits

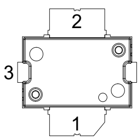
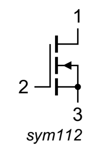
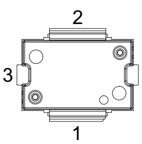
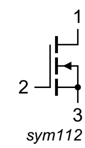
- High efficiency
- Excellent ruggedness
- Designed for broadband operation
- Excellent thermal stability
- High power gain
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Radars & avionics
- Communications
- Broadcast transmitter applications
- Industrial, scientific and medical applications

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLP0427M9S20 (SOT1482-1)			
1	drain		
2	gate		
3	source [1]		
BLP0427M9S20G (SOT1483-1)			
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 4. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT1482-1	BLP0427M9S20Z	9349 601 09515	TR13; 500-fold; 24 mm; dry pack	500
	BLP0427M9S20XY	9349 601 09538	TR7; 100-fold; 24 mm; dry pack	100
SOT1483-1	BLP0427M9S20GZ	9349 601 08515	TR13; 500-fold; 24 mm; dry pack	500
	BLP0427M9S20GXY	9349 601 08538	TR7; 100-fold; 24 mm; dry pack	100

4. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 3 W	1.1	K/W

6. Characteristics

Table 7. DC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.3 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 30 mA	1.5	2.0	-	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 180 mA	1.6	2.1	2.6	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V	-	6	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 30 mA	-	300	-	mS
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 1.05 A	-	500	-	mΩ

Table 8. RF characteristics

A derivative functional RF test is performed in production. The performance as mentioned below is verified by design and characterization in a class AB production board.

Test signal: pulsed CW; δ = 10%; t_p = 100 μs; V_{DS} = 28 V; I_{Dq} = 180 mA; T_{case} = 25 °C; f = 1842.5 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 35 dBm	17	19	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 35 dBm	18	22	-	%
RL_{in}	input return loss	$P_{L(AV)}$ = 35 dBm	-	–10	–6	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		-	42.5	-	dBm
$P_{L(3dB)}$	output power at 3 dB gain compression		-	43	-	dBm

7. Test information

7.1 Ruggedness in Doherty operation

The BLP0427M9S20 and BLP0427M9S20G are capable of withstanding a load mismatch corresponding to a VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; P_L = 20 W (CW); f = 728 MHz and 1805 MHz on development board.

7.2 Impedance information

Table 9. Typical impedance of BLP0427M9S20G

Measured load-pull data; I_{Dq} = 180 mA; V_{DS} = 28 V.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
740	0.5 + j0.1	10.6 – j1.0	37	55.1	22.8
880	0.6 – j1.4	3.8 + j2.0	49	70.9	22.8
1810	1.6 – j5.5	3.4 – j1.0	43	62.2	19.0
1840	1.3 – j5.8	3.0 – j1.2	43	62.7	19.1

Table 9. Typical impedance of BLP0427M9S20G *…continued*

Measured load-pull data; I_{Dq} = 180 mA; V_{DS} = 28 V.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
1880	1.3 – j6.2	2.6 – j1.5	42	61.2	18.7
2110	5.3 – j9.6	2.6 – j2.5	41	58.2	17.7
2170	6.2 – j8.1	2.6 – j2.5	41	60.4	18.2
Maximum drain efficiency load					
740	0.5 + j0.1	6.0 + j10.0	20	74.1	24.8
880	0.6 – j1.4	3.7 + j5.9	26	82.7	24.7
1810	1.6 – j5.5	1.9 + j0.2	31	70.9	20.9
1840	1.3 – j5.8	1.7 + j0.0	29	69.8	21.3
1880	1.3 – j6.2	1.6 – j0.2	28	69.8	21.3
2110	5.3 – j9.6	1.7 – j1.5	32	65.6	19.5
2170	6.2 – j8.1	1.6 – j1.7	30	65.9	20.2

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

Table 10. Typical impedance of BLP0427M9S20

Measured load-pull data; I_{Dq} = 180 mA; V_{DS} = 28 V.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
740	0.6 + j0.6	10.6 – j1.0	39	56.8	22.7
880	0.6 – j0.7	4.0 + j1.6	51	70.9	22.1
1810	1.8 – j5.4	3.0 – j1.2	44	60.9	19.1
1840	1.6 – j5.8	3.0 – j1.2	44	62.6	19.6
1880	1.8 – j6.1	2.9 – j1.6	44	60.9	19.1
2110	7.3 – j8.2	2.6 – j2.5	41	57.7	17.8
2170	8.7 – j6.8	2.6 – j2.5	43	62.1	18.7
Maximum drain efficiency load					
740	0.6 + j0.6	6.0 + j10.0	22	77.0	24.6
880	0.6 – j0.7	3.7 + j5.9	26	85.3	24.4
1810	1.8 – j5.4	1.9 + j0.0	33	69.4	20.9
1840	1.6 – j5.8	1.9 + j0.0	31	69.4	21.7
1880	1.8 – j6.1	1.8 – j0.2	32	70.7	21.6
2110	7.3 – j8.2	1.5 – j1.4	30	65.3	19.9
2170	8.7 – j6.8	1.4 – j1.6	29	69.3	21.3

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

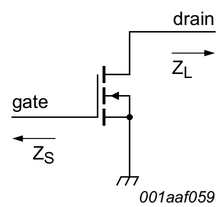
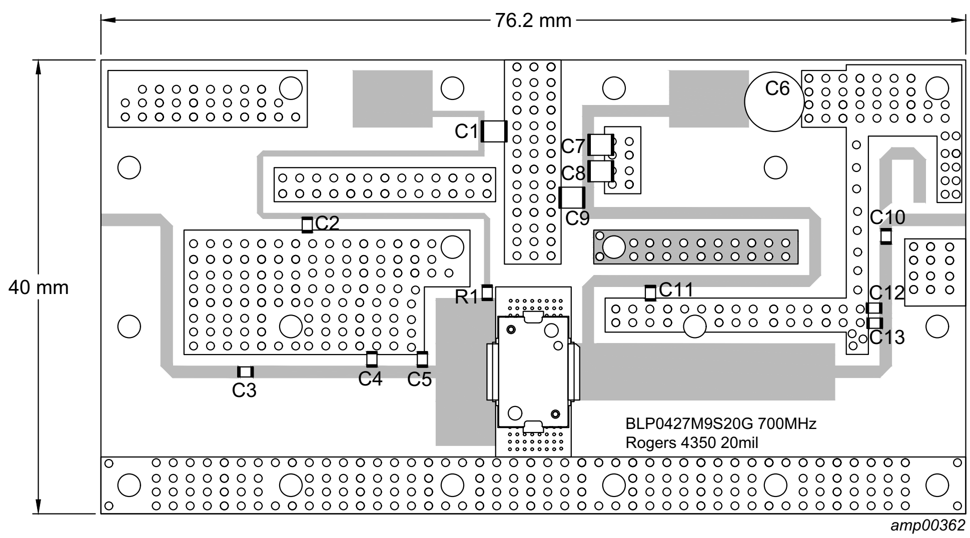


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; thickness = 0.508 mm.

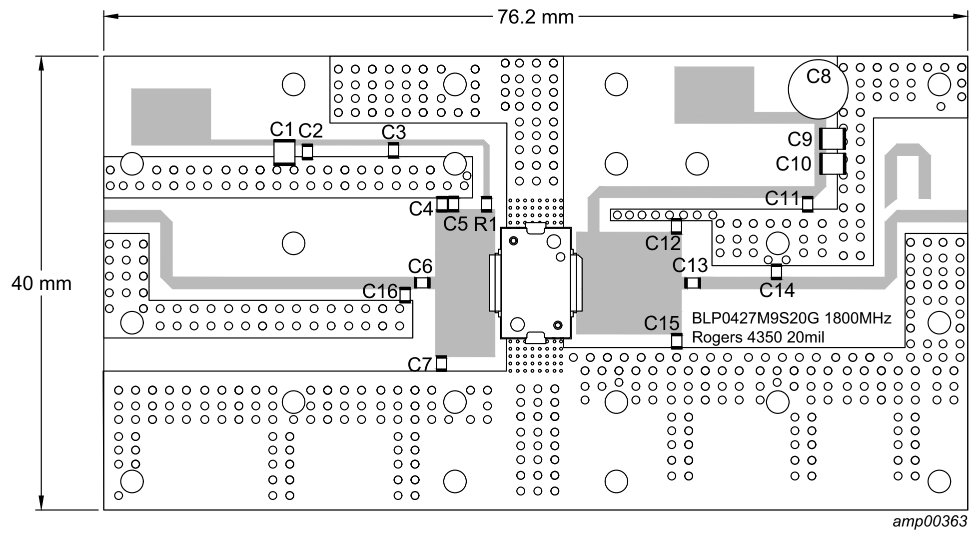
See Table 11 for a list of components.

Fig 2. Component layout for test circuit at 740 MHz

Table 11. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C7, C8, C9	multilayer ceramic chip capacitor	10 μF, 50 V	Murata
C2, C3, C10, C11	multilayer ceramic chip capacitor	36 pF	ATC 600F
C4, C5	multilayer ceramic chip capacitor	15 pF	ATC 600F
C6	electrolytic capacitor	2200 μF, 50 V	
C12	multilayer ceramic chip capacitor	5.6 pF	ATC 600F
C13	multilayer ceramic chip capacitor	0.2 pF	ATC 600F
R1	resistor	5.1 Ω	SMD 0805



Printed-Circuit Board (PCB): Rogers RO4350B; thickness = 0.508 mm.

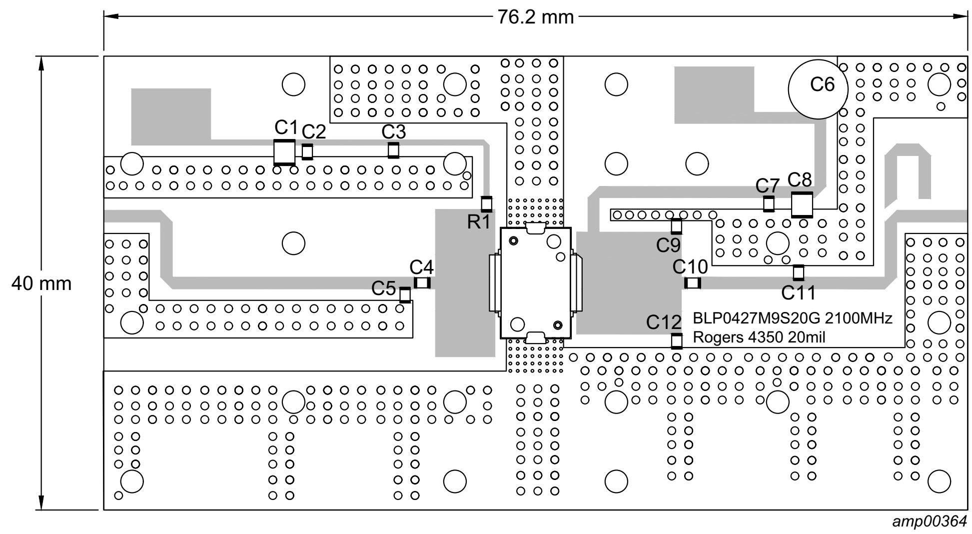
See Table 12 for a list of components.

Fig 3. Component layout for test circuit at 1800 MHz

Table 12. List of components

See Figure 3 for component layout.

Component	Description	Value	Remarks
C1, C9, C10	multilayer ceramic chip capacitor	10 μF, 50 V	Murata
C2, C3, C11, C13	multilayer ceramic chip capacitor	12 pF	ATC 600F
C4, C5	multilayer ceramic chip capacitor	0.8 pF	ATC 600F
C6	multilayer ceramic chip capacitor	6.2 pF	ATC 600F
C7	multilayer ceramic chip capacitor	2 pF	ATC 600F
C8	electrolytic capacitor	2200 μF, 50 V	
C12, C15	multilayer ceramic chip capacitor	0.3 pF	ATC 600F
C14	multilayer ceramic chip capacitor	2.2 pF	ATC 600F
C16	multilayer ceramic chip capacitor	0.3 pF	ATC 600F
R1	resistor	5.1 Ω	SMD 0805



Printed-Circuit Board (PCB): Rogers RO4350B; thickness = 0.508 mm.

See Table 13 for a list of components.

Fig 4. Component layout for test circuit at 2100 MHz

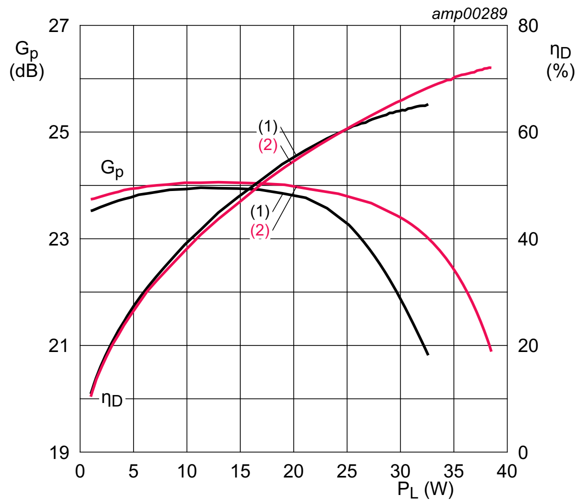
Table 13. List of components

See Figure 4 for component layout.

Component	Description	Value	Remarks
C1, C8	multilayer ceramic chip capacitor	10 μF, 50 V	Murata
C2, C7, C10	multilayer ceramic chip capacitor	12 pF	ATC 600F
C3	multilayer ceramic chip capacitor	62 pF	ATC 600F
C4	multilayer ceramic chip capacitor	5.6 pF	ATC 600F
C5	multilayer ceramic chip capacitor	0.5 pF	ATC 600F
C6	electrolytic capacitor	2200 μF, 50 V	
C9	multilayer ceramic chip capacitor	2.2 pF	ATC 600F
C11	multilayer ceramic chip capacitor	1.2 pF	ATC 600F
C12	multilayer ceramic chip capacitor	1.8 pF	ATC 600F
R1	resistor	5.1 Ω	SMD 0805

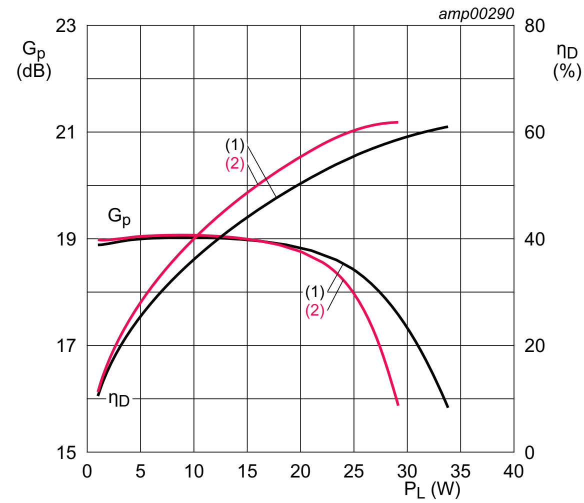
7.4 Graphical data

7.4.1 CW



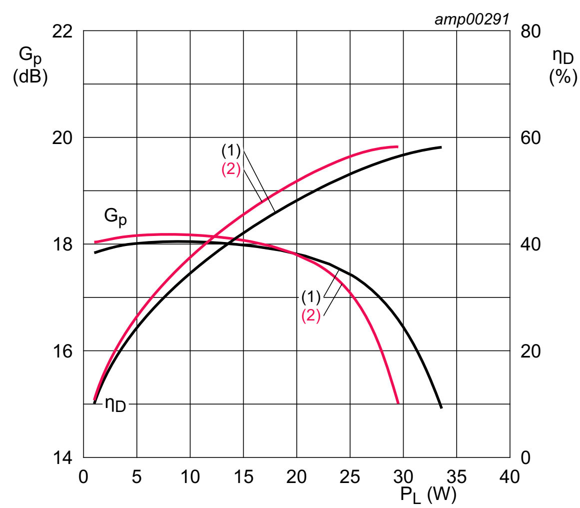
V_{DS} = 28 V; I_{Dq} = 180 mA.
(1) f = 728 MHz
(2) f = 768 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 180 mA.
(1) f = 1805 MHz
(2) f = 1880 MHz

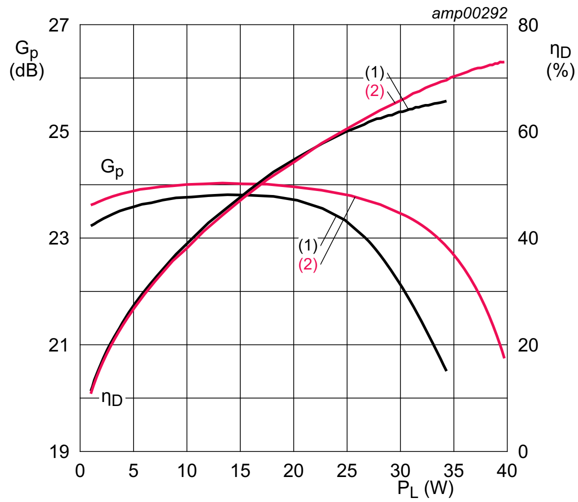
Fig 6. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 180 mA.
(1) f = 2110 MHz
(2) f = 2170 MHz

Fig 7. Power gain and drain efficiency as function of output power; typical values

7.4.2 Pulsed CW

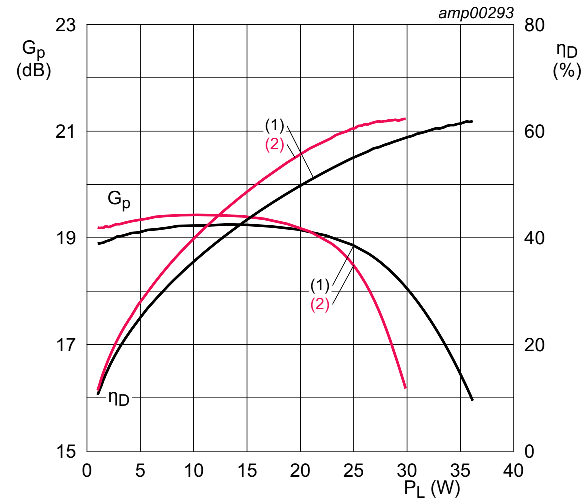


V_{DS} = 28 V; I_{Dq} = 180 mA.

(1) f = 728 MHz

(2) f = 768 MHz

Fig 8. Power gain and drain efficiency as function of output power; typical values

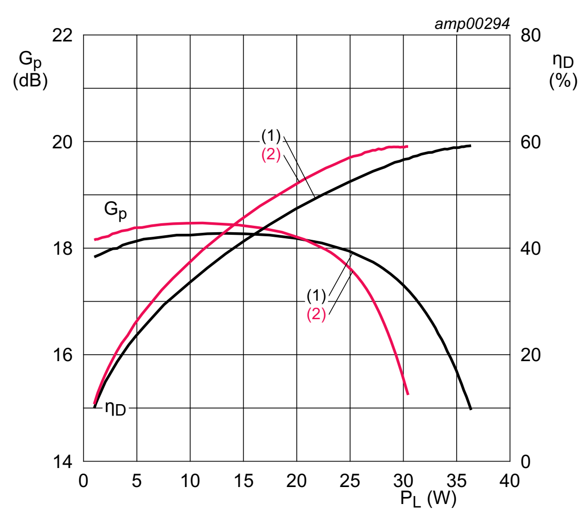


V_{DS} = 28 V; I_{Dq} = 180 mA.

(1) f = 1805 MHz

(2) f = 1880 MHz

Fig 9. Power gain and drain efficiency as function of output power; typical values



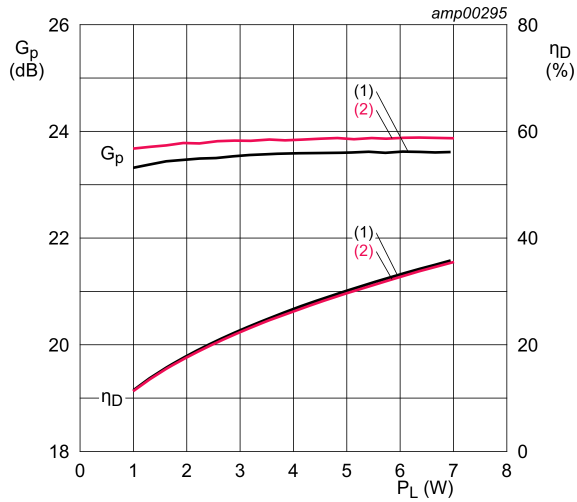
V_{DS} = 28 V; I_{Dq} = 180 mA.

(1) f = 2110 MHz

(2) f = 2170 MHz

Fig 10. Power gain and drain efficiency as function of output power; typical values

7.4.3 1-Carrier W-CDMA

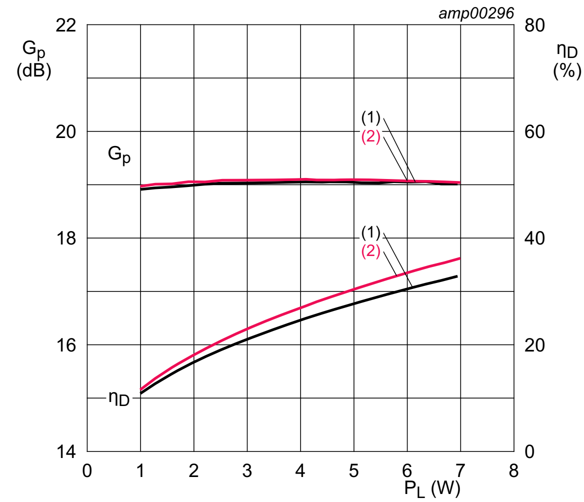


V_{DS} = 28 V; I_{Dq} = 180 mA.

(1) f = 728 MHz

(2) f = 768 MHz

Fig 11. Power gain and drain efficiency as function of output power; typical values

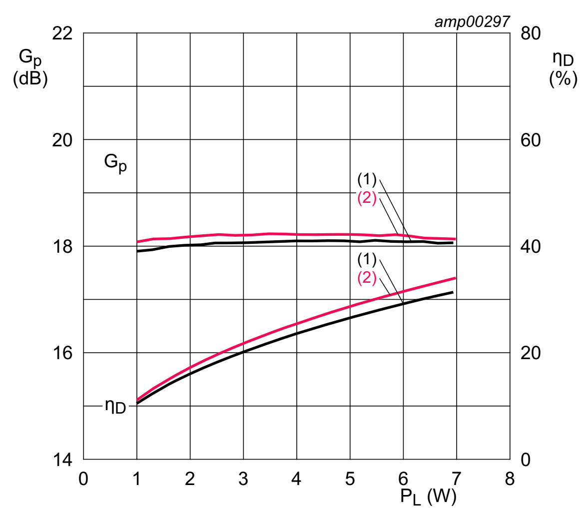


V_{DS} = 28 V; I_{Dq} = 180 mA.

(1) f = 1805 MHz

(2) f = 1880 MHz

Fig 12. Power gain and drain efficiency as function of output power; typical values

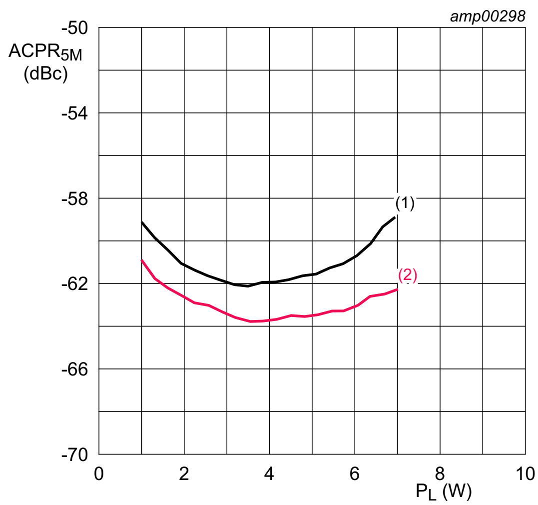


V_{DS} = 28 V; I_{Dq} = 180 mA.

(1) f = 2110 MHz

(2) f = 2170 MHz

Fig 13. Power gain and drain efficiency as function of output power; typical values

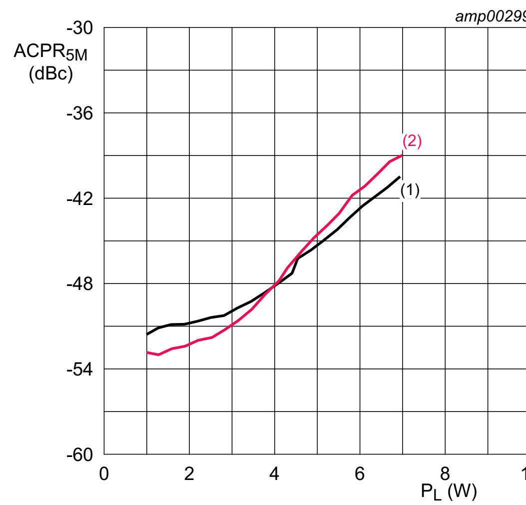


V_{DS} = 28 V; I_{Dq} = 180 mA.

(1) f = 728 MHz

(2) f = 768 MHz

Fig 14. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

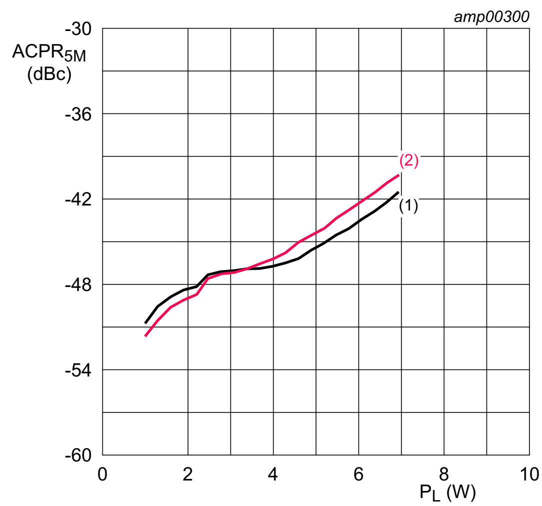


V_{DS} = 28 V; I_{Dq} = 180 mA.

(1) f = 1805 MHz

(2) f = 1880 MHz

Fig 15. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



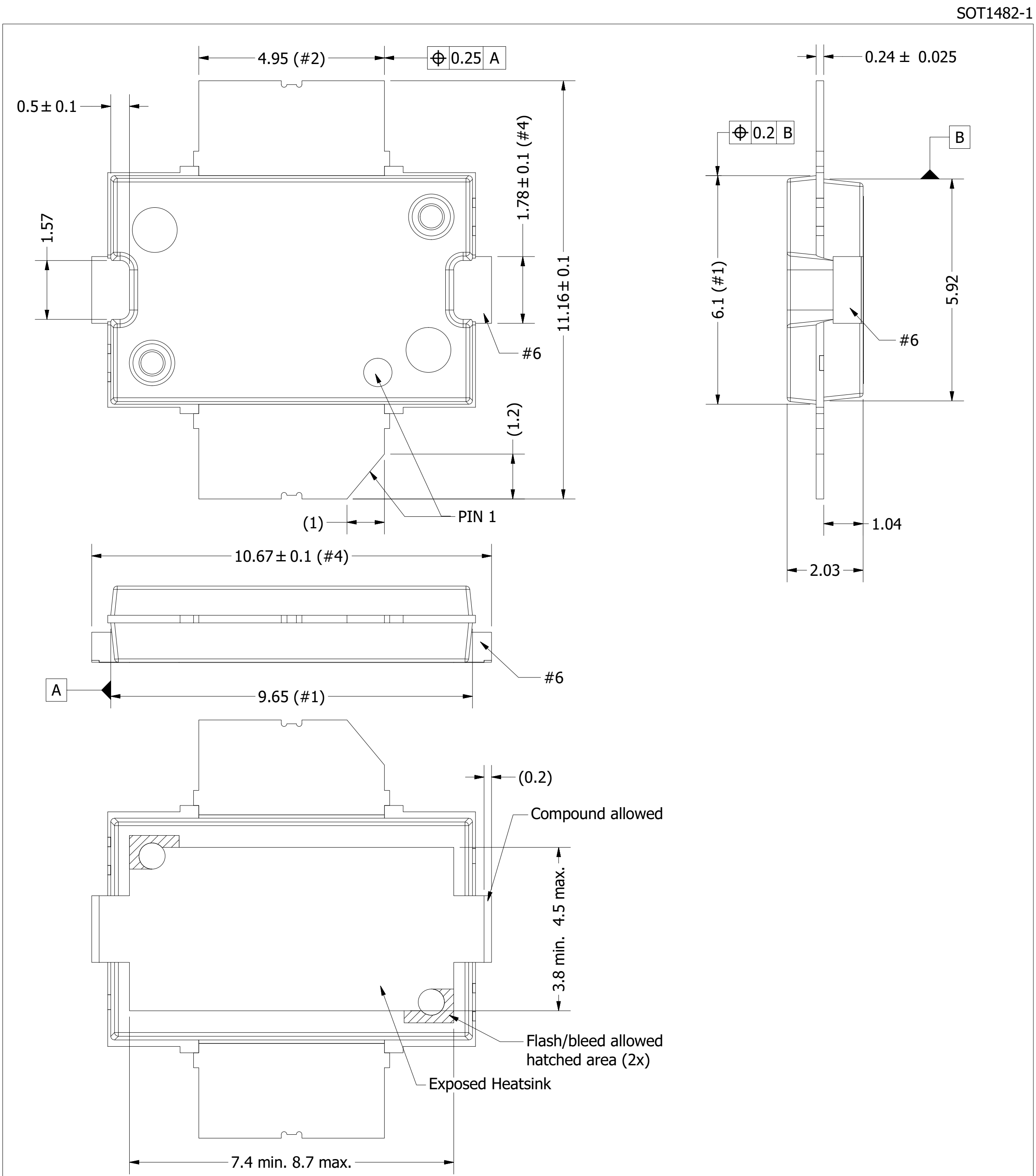
V_{DS} = 28 V; I_{Dq} = 180 mA.

(1) f = 2110 MHz

(2) f = 2170 MHz

Fig 16. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

8. Package outline

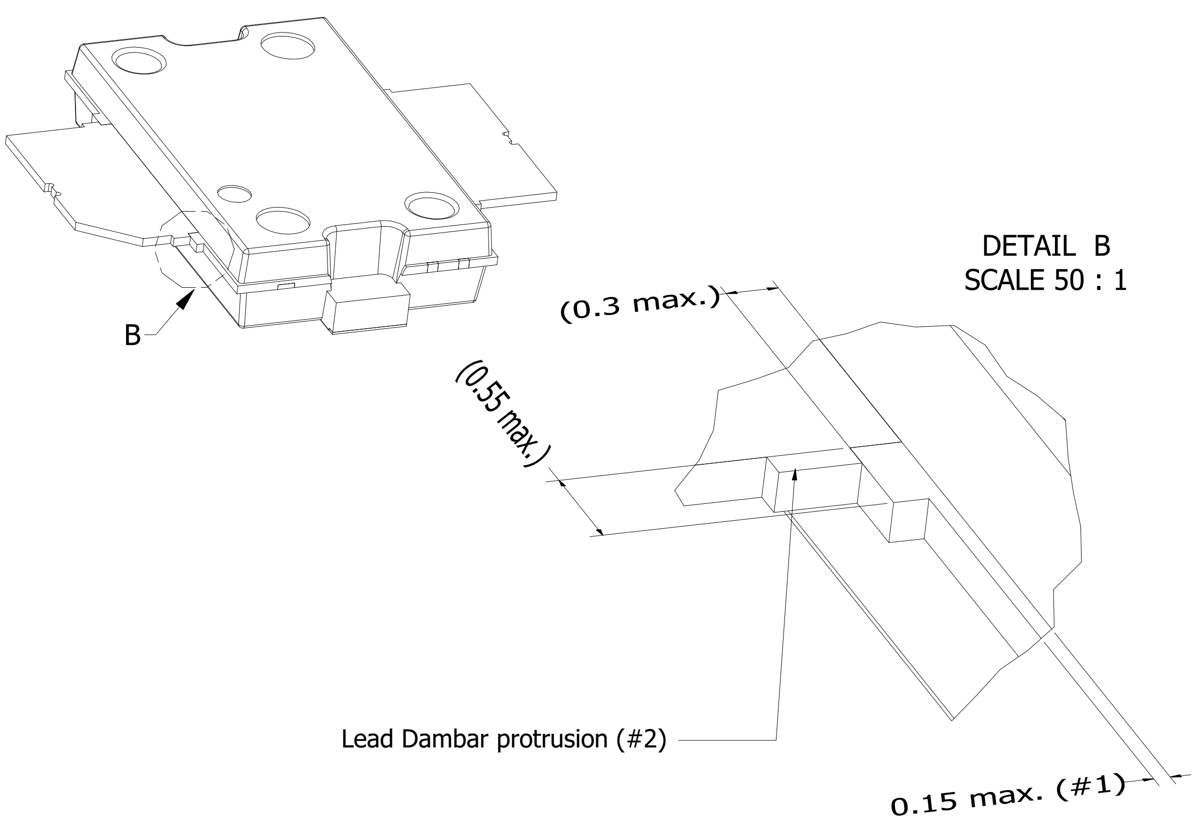


Package outline drawing: SOT1482-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 6 Revision date: 1/4/2017
		Third angle projection	Sheet 1 of 2

Fig 17. Package outline SOT1482-1 (sheet 1 of 2)

SOT1482-1

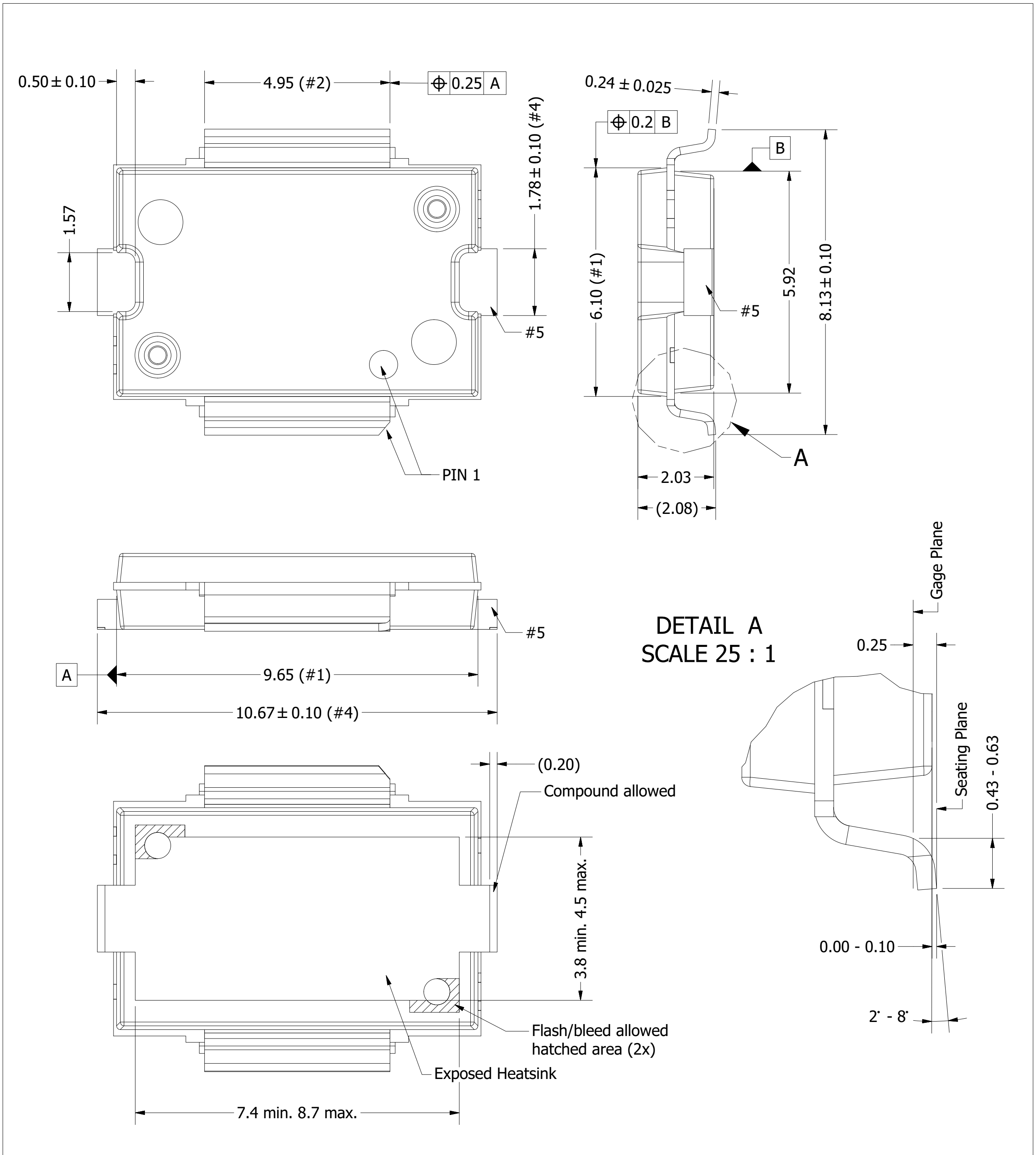
Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. The mold protrusion is maximum 0.15 mm per side. See also detail B. In the dambar area max. protrusion is 0.55 mm. max. in length and 0.3 mm. max. in width (4x). See also detail B.
(2)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(3)	The leads and exposed heatsink are plated with matte Tin (Sn).
(4)	Dimensions (Heatsink ears) 10,67 and 1,78 do not include mouldprotrusion. Overall Max. dimensions incl. mould protrusions is 10.92 mm. (max.) and 2.03 mm. (max.)
(5)	Lead coplanarity over the leads is 0,1 mm. maximum.
(6)	Surfaces may remain unplated (not solderable surfaces)



Package outline drawing: SOT1482-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 6 Revision date: 1/4/2017
		Third angle projection	Sheet 2 of 2

Fig 18. Package outline SOT1482-1 (sheet 2 of 2)

SOT1483-1

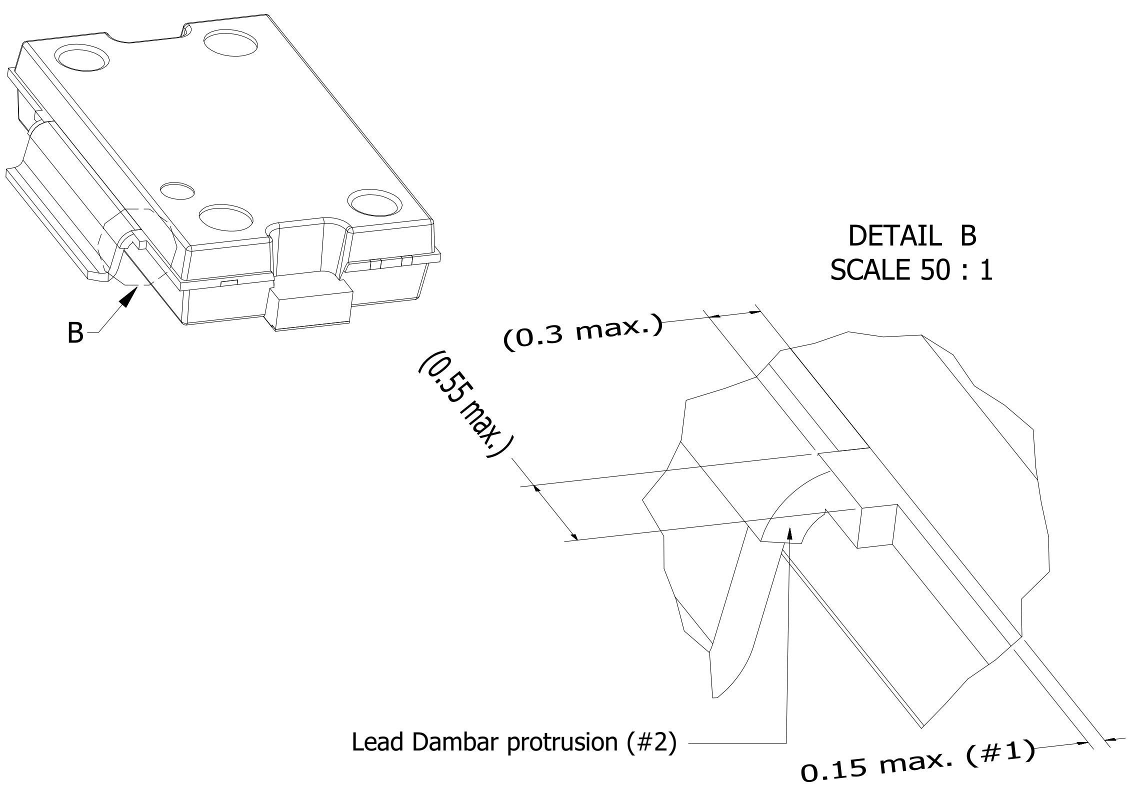


Package outline drawing: SOT1483-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 7 Revision date: 2/21/2017
		Third angle projection	Sheet 1 of 2

Fig 19. Package outline SOT1483-1 (sheet 1 of 2)

SOT1483-1

Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. The mold protrusion is maximum 0.15 mm per side. See also detail B. In the dambar area max. protrusion is 0.55mm max. in lenght and 0.3 mm max. in width (4x) See also detail B.
(2)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(3)	The leads and exposed heatsink are plated with matte Tin (Sn).
(4)	Dimensions (Heatsink ears) 10,67 and 1,78 do not include mouldprotrusion. Overall Max. dimensions incl. mould protrusions is 10,92 mm. (max.) and 2,03 mm. (max.).
(5)	Surfaces may remain unplated (not solderable surfaces).



Package outline drawing: SOT1483-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 7 Revision date: 2/21/2017
		Third angle projection	Sheet 2 of 2

Fig 20. Package outline SOT1483-1 (sheet 2 of 2)

9. Handling information

CAUTION
This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 14. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 15. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
SMD	Surface Mounted Device
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP0427M9S20_0427M9S20G v.2	20210716	Product data sheet	-	BLP0427M9S20_0427M9S20G v.1
Modifications:	• Table 4 on page 2: updated table with orderable part numbers			
BLP0427M9S20_0427M9S20G v.1	20180116	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contents

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