

HSMC Adapter for DC890-Compatible Demo Boards

DESCRIPTION

Demonstration circuit 2511A is a gasket adapter board that allows DC890-compatible data converter eval boards to interface with FPGA boards that have an HSMC connector, such as the SoCkit Cyclone 5 SoC board from Arrow Electronics.

Design files for this circuit board are available at <http://www.linear.com/demo/DC2511A>

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BOARD PHOTO

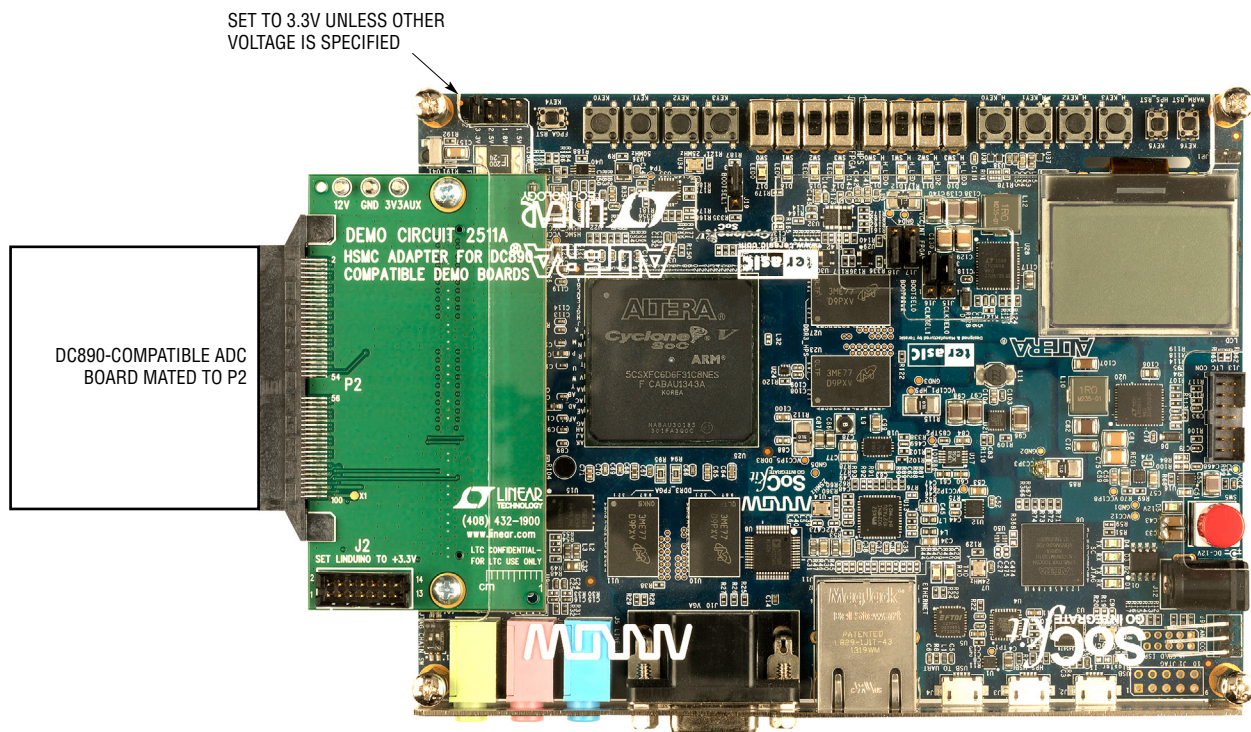


Figure 1. Basic Connections

QUICK START PROCEDURE

DC2511 was designed to mate to the Arrow SoCkit board. DC2511 may work with other HSMC-compatible FPGA boards, but the pin connections and voltages should be verified.

Carefully mate the HSMC connector on the reverse side of the DC2511 to the SoCkit board. Use high-quality, 5mm spacers such as Harwin R30-6200514, and M3 × 12 or 4-40 × 1/2” pan-head screws.

Most FPGA loads intended for use with the DC2511 require 3.3V I/O voltage. Unless the test script or other experiment documentation indicates otherwise, set the

SoCkit’s I/O voltage to 3.3V by placing the JP2 jumper on the SoCkit board in the 3.3V position (closest to the edge of the board). Mate the ADC demo board to P2 on DC2511. Observe proper power-sequencing: the best practice is to power up the SoCkit before applying power to the ADC demo board.

A complete example of a typical evaluation setup is covered in the blog, “Data Converter Evaluation with the Arrow/Altera SoCkit FPGA board”:

<http://www.linear.com/solutions/7704>

EXTERNAL CONNECTIONS

Mapping of individual pins is shown in Table 1.

P2: 100-pin Samtec MEC8 receptacle, compatible with ADC demo boards that are used with the DC890 capture board. Signals include conversion clock, up to 32 data lines, I²C signals for identification, and 3.3V auxiliary power.

J2: 2 × 7 QuikEval™/Linduino® connector. Not used for basic ADC evaluation. Allows the FPGA board to control

QuikEval-compatible demo boards for experiments or application development.

J1: Test pads for additional HSMC signals.

12V, GND, 3.3V Turret Posts: 12V and 3.3V, supplied through the HSMC connector. May be used to power additional circuitry, refer to SoCkit documentation for maximum current. Do NOT apply power to these points.

Table 1. Pin Mapping

DC2511 Header/Pin	DC2511 Signal Name	HSMC Signal Name	SoCkit FPGA Pin No.
		HSMC_CLK_IN0	PIN_J14
P2, Pin 50	CCLK+	HSMC_CLKIN_p1	PIN_AA26
P2, Pin 52	CCLK-	HSMC_CLKIN_n1	PIN_AB27
		HSMC_CLKIN_p2	PIN_H15
		HSMC_CLKIN_n2	PIN_G15
		HSMC_CLK_OUT0	PIN_AD29
J1, Pin 29		HSMC_CLKOUT_p1	PIN_E7
J1, Pin 31		HSMC_CLKOUT_n1	PIN_E6
		HSMC_CLKOUT_p2	PIN_A11
		HSMC_CLKOUT_n2	PIN_A10
J2, Pin 4	SCK/SCL	HSMC_D[0]	PIN_C10
J2, Pin 7	MOSI/SDA	HSMC_D[1]	PIN_H13
J2, Pin 6	CS#	HSMC_D[2]	PIN_C9
J2, Pin 5	MISO	HSMC_D[3]	PIN_H12

EXTERNAL CONNECTIONS

Table 1. Pin Mapping (Continued)

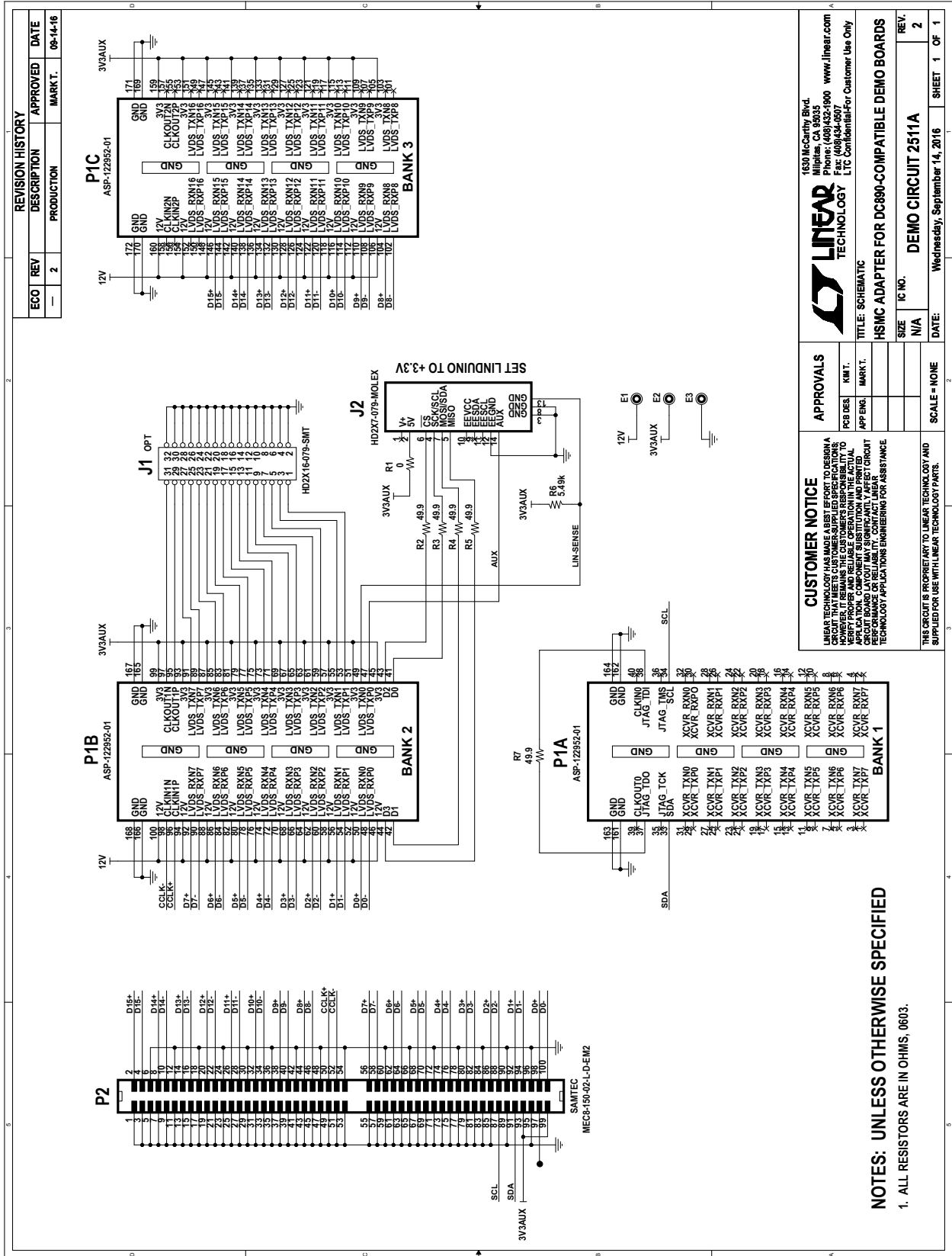
DC2511 Header/Pin	DC2511 Signal Name	HSMC Signal Name	SoCkit FPGA Pin No.
P2, Pin 87	SCL	HSMC_SCL	PIN_AA28
P2, Pin 91	SDA	HSMC_SDA	PIN_AE29
P2, Pin 100	D0-	HSMC_RX_p[0]	PIN_G12
P2, Pin 98	D0+	HSMC_RX_n[0]	PIN_G11
P2, Pin 94	D1-	HSMC_RX_p[1]	PIN_K12
P2, Pin 92	D1+	HSMC_RX_n[1]	PIN_J12
P2, Pin 88	D2-	HSMC_RX_p[2]	PIN_G10
P2, Pin 86	D2+	HSMC_RX_n[2]	PIN_F10
P2, Pin 82	D3-	HSMC_RX_p[3]	PIN_J10
P2, Pin 80	D3+	HSMC_RX_n[3]	PIN_J9
P2, Pin 76	D4-	HSMC_RX_p[4]	PIN_K7
P2, Pin 74	D4+	HSMC_RX_n[4]	PIN_K8
P2, Pin 70	D5-	HSMC_RX_p[5]	PIN_J7
P2, Pin 68	D5+	HSMC_RX_n[5]	PIN_H7
P2, Pin 64	D6-	HSMC_RX_p[6]	PIN_H8
P2, Pin 62	D6+	HSMC_RX_n[6]	PIN_G8
P2, Pin 58	D7-	HSMC_RX_p[7]	PIN_F9
P2, Pin 56	D7+	HSMC_RX_n[7]	PIN_F8
P2, Pin 46	D8-	HSMC_RX_p[8]	PIN_F11
P2, Pin 44	D8+	HSMC_RX_n[8]	PIN_E11
P2, Pin 40	D9-	HSMC_RX_p[9]	PIN_B6
P2, Pin 38	D9+	HSMC_RX_n[9]	PIN_B5
P2, Pin 34	D10-	HSMC_RX_p[10]	PIN_E9
P2, Pin 32	D10+	HSMC_RX_n[10]	PIN_D9
P2, Pin 28	D11-	HSMC_RX_p[11]	PIN_E12
P2, Pin 26	D11+	HSMC_RX_n[11]	PIN_D12
P2, Pin 22	D12-	HSMC_RX_p[12]	PIN_D11
P2, Pin 20	D12+	HSMC_RX_n[12]	PIN_D10
P2, Pin 16	D13-	HSMC_RX_p[13]	PIN_C13
P2, Pin 14	D13+	HSMC_RX_n[13]	PIN_B12
P2, Pin 10	D14-	HSMC_RX_p[14]	PIN_F13
P2, Pin 8	D14+	HSMC_RX_n[14]	PIN_E13
P2, Pin 4	D15-	HSMC_RX_p[15]	PIN_H14
P2, Pin 2	D15+	HSMC_RX_n[15]	PIN_G13
		HSMC_RX_p[16]	PIN_F15
		HSMC_RX_n[16]	PIN_F14
		HSMC_TX_p[0]	PIN_A9
		HSMC_TX_n[0]	PIN_A8
J1, Pin 1		HSMC_TX_p[1]	PIN_E8
J1, Pin 3		HSMC_TX_n[1]	PIN_D7

EXTERNAL CONNECTIONS

Table 1. Pin Mapping (Continued)

DC2511 Header/Pin	DC2511 Signal Name	HSMC Signal Name	SoCkit FPGA Pin No.
J1, Pin 5		HSMC_TX_p[2]	PIN_G7
J1, Pin 7		HSMC_TX_n[2]	PIN_F6
J1, Pin 9		HSMC_TX_p[3]	PIN_D6
J1, Pin 11		HSMC_TX_n[3]	PIN_C5
J1, Pin 13		HSMC_TX_p[4]	PIN_D5
J1, Pin 15		HSMC_TX_n[4]	PIN_C4
J1, Pin 17		HSMC_TX_p[5]	PIN_E3
J1, Pin 19		HSMC_TX_n[5]	PIN_E2
J1, Pin 21		HSMC_TX_p[6]	PIN_E4
J1, Pin 23		HSMC_TX_n[6]	PIN_D4
J1, Pin 25		HSMC_TX_p[7]	PIN_C3
J1, Pin 27		HSMC_TX_n[7]	PIN_B3
		HSMC_TX_p[8]	PIN_E1
		HSMC_TX_n[8]	PIN_D1
		HSMC_TX_p[9]	PIN_D2
		HSMC_TX_n[9]	PIN_C2
		HSMC_TX_p[10]	PIN_B2
		HSMC_TX_n[10]	PIN_B1
		HSMC_TX_p[11]	PIN_A4
		HSMC_TX_n[11]	PIN_A3
		HSMC_TX_p[12]	PIN_A6
		HSMC_TX_n[12]	PIN_A5
		HSMC_TX_p[13]	PIN_C7
		HSMC_TX_n[13]	PIN_B7
		HSMC_TX_p[14]	PIN_C8
		HSMC_TX_n[14]	PIN_B8
		HSMC_TX_p[15]	PIN_C12
		HSMC_TX_n[15]	PIN_B11
		HSMC_TX_p[16]	PIN_B13
		HSMC_TX_n[16]	PIN_A13

SCHEMATIC DIAGRAM



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DEMO MANUAL DC2511A

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