

# BLC10G22XS-400AVT

Power LDMOS transistor

Rev. 1 — 30 April 2018

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

400 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 2110 MHz to 2200 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in an asymmetrical Doherty production test circuit.

$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 800\text{ mA}$  (main);  $V_{GS(amp)peak} = 1.0\text{ V}$ , unless otherwise specified.

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	2110 to 2200	28	56	17.0	47.0	-29.6 <a href="#">[1]</a>

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

### 1.2 Features and benefits

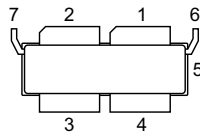
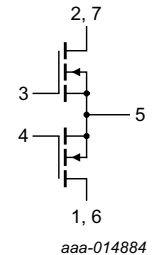
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 2110 MHz to 2200 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source <a href="#">[1]</a>		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC10G22XS-400AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1258-4

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		-6	+9	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		-6	+9	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		<a href="#">[1]</a>	225	°C
$T_{case}$	case temperature	operating	<a href="#">[1]</a>	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$V_{DS} = 28\text{ V}; I_{Dq} = 800\text{ mA (main)};$ $V_{GS(amp)peak} = 1.0\text{ V}; T_{case} = 80\text{ °C}$		
		$P_L = 56\text{ W}$	0.29	k/W
		$P_L = 74\text{ W}$	0.27	k/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Main device</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.44\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 144\text{ mA}$	1.5	2.0	2.5	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 800\text{ mA}$	-	2.2	-	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$	-	26.5	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 9\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 7.2\text{ A}$	-	15.0	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 5.04\text{ A}$	-	93	128	$\text{m}\Omega$
<b>Peak device</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.98\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 298\text{ mA}$	1.5	2.0	2.5	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 1600\text{ mA}$	-	2.2	-	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$	-	47	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 14.9\text{ A}$	-	28.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 10.43\text{ A}$	-	50	74	$\text{m}\Omega$

**Table 7. RF characteristics**

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH;  $f_1 = 2112.5\text{ MHz}; f_2 = 2167.5\text{ MHz}$ ; RF performance at  $V_{DS} = 28\text{ V}; I_{Dq} = 800\text{ mA}$  (main);  $V_{GS(amp)peak} = 1.0\text{ V}; T_{case} = 25\text{ °C}$ ; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 2110 MHz to 2200 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 56\text{ W}$	15.3	16.3	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 56\text{ W}$	-	-14	-9	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 56\text{ W}$	42	46	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 56\text{ W}$	-	-29	-24	dBc

**Table 8. RF characteristics**

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH;  $f_1 = 2112.5\text{ MHz}; f_2 = 2167.5\text{ MHz}$ ; RF performance at  $V_{DS} = 28\text{ V}; I_{Dq} = 800\text{ mA}$  (main);  $V_{GS(amp)peak} = 1.0\text{ V}; T_{case} = 25\text{ °C}$ ; unless otherwise specified; in an asymmetrical Doherty production test circuit at a frequency of 2200 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$PAR_O$	output peak-to-average ratio	$P_{L(AV)} = 56\text{ W}$	6.3	6.9	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)} = 56\text{ W}$	380	440	-	W

## 7. Test information

### 7.1 Ruggedness in Doherty operation

The BLC10G22XS-400AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 32\text{ V}$ ;  $I_{Dq} = 800\text{ mA}$ ;  $V_{GS(amp)peak} = 1.0\text{ V}$ ;  $f = 2112.5\text{ MHz}$ ;  $P_L = 155\text{ W}$  (5 dB OBO); 100 % clipping

### 7.2 Impedance information

**Table 9. Typical impedance of main device**

Measured load-pull data of main device;  $I_{Dq} = 800\text{ mA}$  (main);  $V_{DS} = 28\text{ V}$ ; pulsed CW ( $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\text{ %}$ ).

f (MHz)	Z <sub>S</sub> [1] (Ω)	Z <sub>L</sub> [1] (Ω)	P <sub>L</sub> [2] (W)	η <sub>D</sub> [2] (%)	G <sub>p</sub> [2] (dB)
<b>Maximum power load</b>					
2110	1.6 – j6.1	1.5 – j2.9	205	61.5	17.2
2140	2.1 – j6.5	1.5 – j2.9	205	62.0	17.3
2170	2.6 – j7.0	1.4 – j3.3	205	60.0	17.2
<b>Maximum drain efficiency load</b>					
2110	1.6 – j6.1	2.4 – j2.4	160	68.0	19.1
2140	2.1 – j6.5	2.4 – j2.3	158	67.5	19.2
2170	2.6 – j7.0	2.0 – j2.2	160	67.0	19.1

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] At 3 dB gain compression.

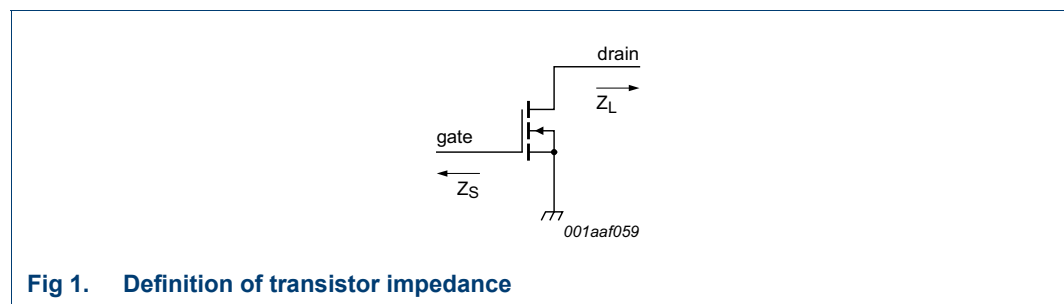
**Table 10. Typical impedance of peak device**

Measured load-pull data of peak device;  $I_{Dq} = 1600 \text{ mA (peak)}$ ;  $V_{DS} = 28 \text{ V}$ ; pulsed CW ( $t_p = 100 \mu\text{s}$ ;  $\delta = 10 \%$ ).

f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]	P <sub>L</sub> [2]	η <sub>D</sub> [2]	G <sub>p</sub> [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
<b>Maximum power load</b>					
2110	1.9 – j5.4	1.3 – j3.3	390	60.0	16.2
2140	2.4 – j5.7	1.4 – j3.5	390	57.5	16.3
2170	3.1 – j6.1	1.3 – j3.7	390	55.0	16.1
<b>Maximum drain efficiency load</b>					
2110	1.9 – j5.4	1.8 – j2.7	340	63.6	17.6
2140	2.4 – j5.7	1.9 – j2.6	315	63.4	18.1
2170	3.1 – j6.1	1.9 – j2.7	320	63.6	18.2

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] At 3 dB gain compression.



**Fig 1. Definition of transistor impedance**

### 7.3 Recommended impedances for Doherty design

**Table 11. Typical impedance of main at 1 : 1 load**

Measured load-pull data of main device;  $I_{Dq} = 800 \text{ mA (main)}$ ;  $V_{DS} = 28 \text{ V}$ ; pulsed CW ( $t_p = 100 \mu\text{s}$ ;  $\delta = 10 \%$ ).

f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]	P <sub>L</sub> [2]	η <sub>D</sub> [2]	G <sub>p</sub> [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2110	1.7 – j5.5	2.1 – j3.8	165	38.0	20.8
2140	2.0 – j5.8	2.1 – j3.5	170	38.0	20.8
2170	2.3 – j6.1	2.0 – j3.3	175	38.5	21.1

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] At P<sub>L(AV)</sub> = 56 W.

**Table 12. Typical impedance of main device at 1 : 2.5 load**

Measured load-pull data of main device;  $I_{Dq} = 800 \text{ mA (main)}$ ;  $V_{DS} = 28 \text{ V}$ ; pulsed CW ( $t_p = 100 \mu\text{s}$ ;  $\delta = 10 \%$ ).

f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]	P <sub>L</sub> [2]	η <sub>D</sub> [2]	G <sub>p</sub> [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2110	1.7 – j5.5	3.6 – j0.8	85	53.2	23.5
2140	2.0 – j5.8	3.5 – j0.6	78	53.4	23.5
2170	2.3 – j6.1	3.3 – j0.4	70	53.2	24.0

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] At P<sub>L(AV)</sub> = 56 W.

**Table 13. Typical impedance of peak device at 1 : 1 load**

Measured load-pull data of peak device;  $I_{Dq} = 1600 \text{ mA (peak)}$ ;  $V_{DS} = 28 \text{ V}$ ; pulsed CW ( $t_p = 100 \mu\text{s}$ ;  $\delta = 10 \%$ ).

f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]	P <sub>L</sub> [2]	η <sub>D</sub> [2]	G <sub>p</sub> [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2110	1.7 – j4.8	1.8 – j3.5	350	25.5	19.7
2140	2.0 – j5.0	1.8 – j3.2	345	25.8	19.9
2170	2.4 – j5.2	1.8 – j3.1	340	26.4	20.4

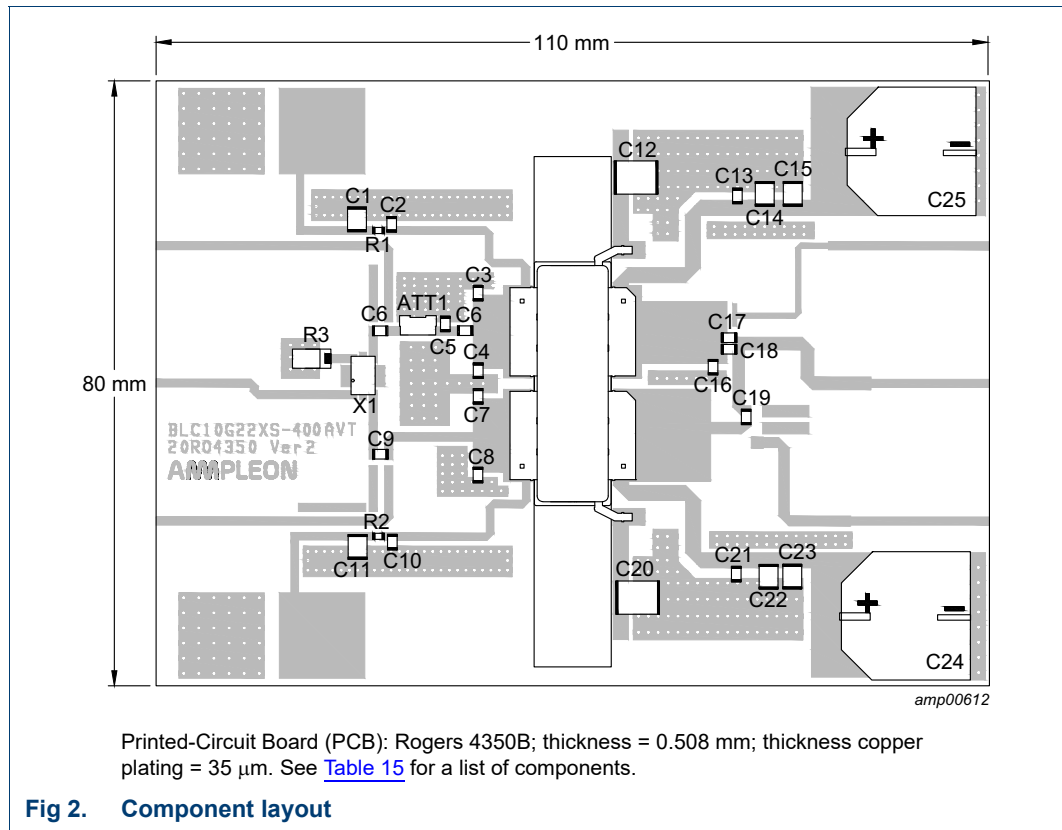
[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] At P<sub>L(AV)</sub> = 56 W.

**Table 14. Off-state impedances of peak device**

f	Z <sub>off</sub>
(MHz)	(Ω)
2110	2.9 – j2.9
2140	2.3 – j1.8
2170	2.0 – j1.0

7.4 Test circuit

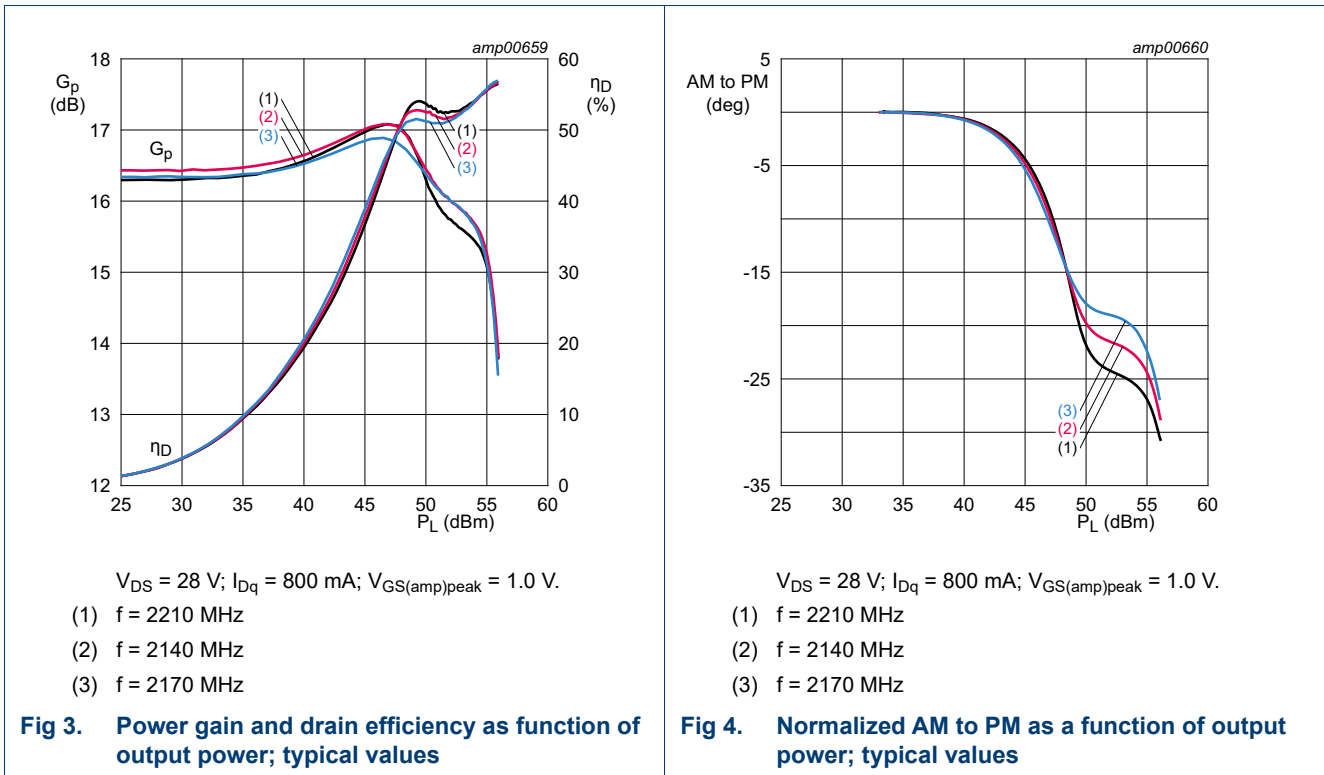


**Table 15. List of components**  
See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1, C11, C14, C15, C22, C23,	multilayer ceramic chip capacitor	10 $\mu\text{F}$ , 50 V	Murata: GRM32ER71H106KA12L, SMD 1210
C2, C6, C9, C10, C13, C19, C21	multilayer ceramic chip capacitor	15 pF, 250 V	Murata: GQM2195C2E150FB15, SMD 805
C3, C4, C7, C8	multilayer ceramic chip capacitor	1.0 pF, 250 V	Murata: GQM2195C2E1ROBB15, SMD 0805
C5	multilayer ceramic chip capacitor	0.8 pF, 250 V	Murata: GQM2195C2E1ROBB15, SMD 0805
C12, C20	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$ , 100 V	C5750X7R2A475KT/A
C16	multilayer ceramic chip capacitor	0.5 pF, 250 V	Murata: GQM2195C2E1ROBB15, SMD 0805
C17, C18	multilayer ceramic chip capacitor	1.8 pF, 250 V	Murata: GQM2195C2E1R8BB15, SMD 0805
C24, C25	electrolytic capacitor	470 $\mu\text{F}$ , 63 V	
R1, R2	resistor	5.1 $\Omega$ , 1 %	SMD 805
R3	resistor	50 $\Omega$ , 25 W	Anaren: C16A50Z4
X1	hybrid coupler	2 dB, 90°	Anaren: Xinger III, X3C20F1-02
ATT1	attenuator	1 dB	Anaren: D10AA1Z4

7.5 Graphical data

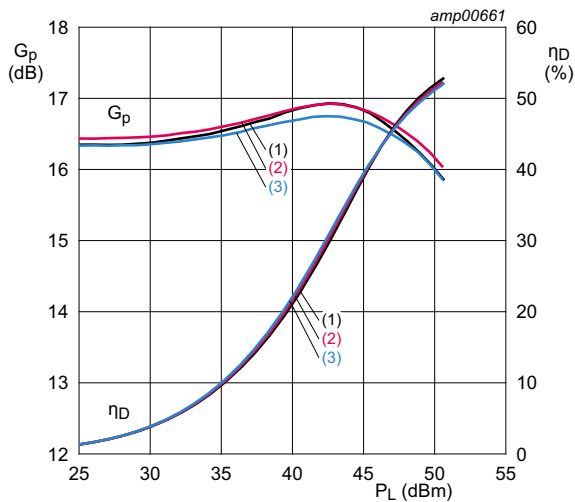
7.5.1 Pulsed CW





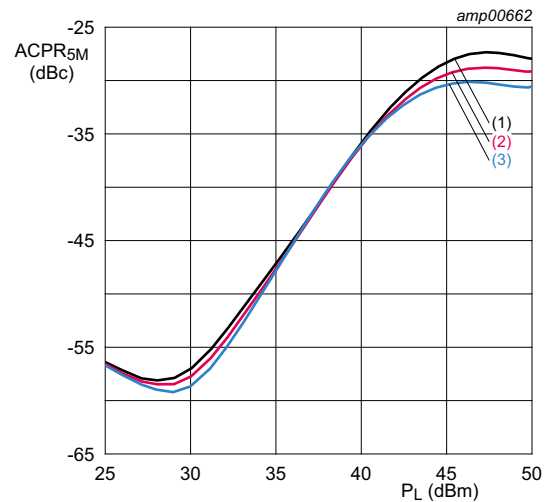
7.5.2 1-Carrier W-CDMA

Test signal: 3GPP test model 1; 1 to 64 DPCH (100 % clipping): PAR = 7.5 dB per carrier at 0.01 % probability on CCDF per carrier.



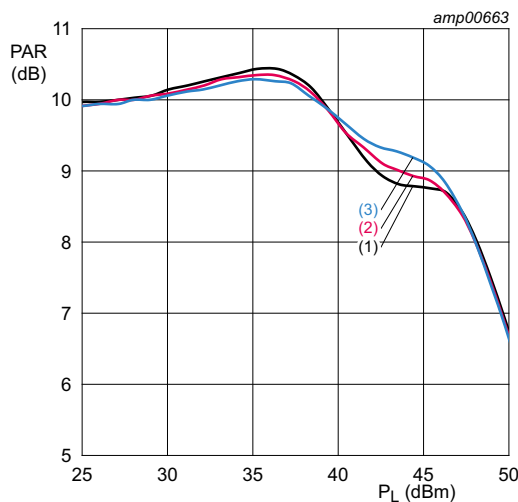
$V_{DS} = 28\text{ V}; I_{Dq} = 800\text{ mA}; V_{GS(amp)peak} = 1.0\text{ V}.$   
 (1)  $f = 2210\text{ MHz}$   
 (2)  $f = 2140\text{ MHz}$   
 (3)  $f = 2170\text{ MHz}$

Fig 5. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 28\text{ V}; I_{Dq} = 800\text{ mA}; V_{GS(amp)peak} = 1.0\text{ V}.$   
 (1)  $f = 2210\text{ MHz}$   
 (2)  $f = 2140\text{ MHz}$   
 (3)  $f = 2170\text{ MHz}$

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

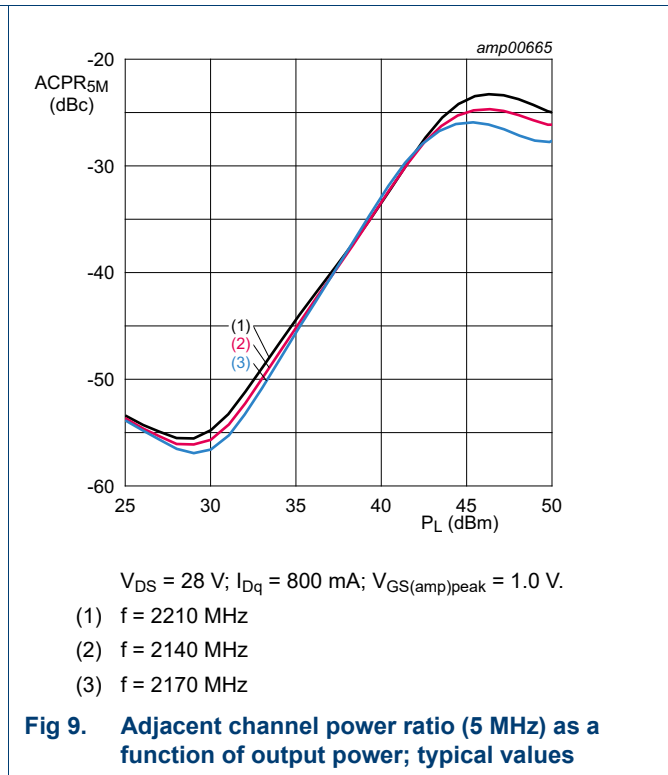
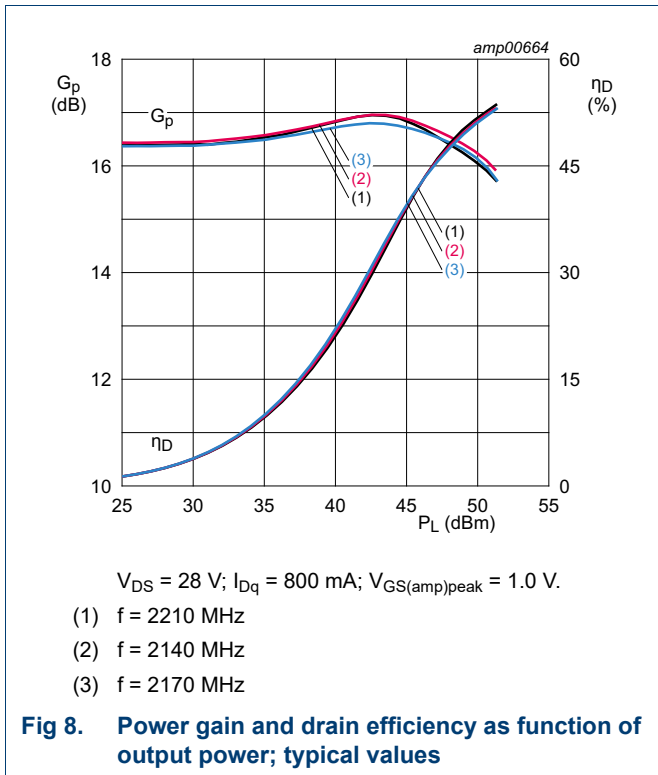


$V_{DS} = 28\text{ V}; I_{Dq} = 800\text{ mA}; V_{GS(amp)peak} = 1.0\text{ V}.$   
 (1)  $f = 2210\text{ MHz}$   
 (2)  $f = 2140\text{ MHz}$   
 (3)  $f = 2170\text{ MHz}$

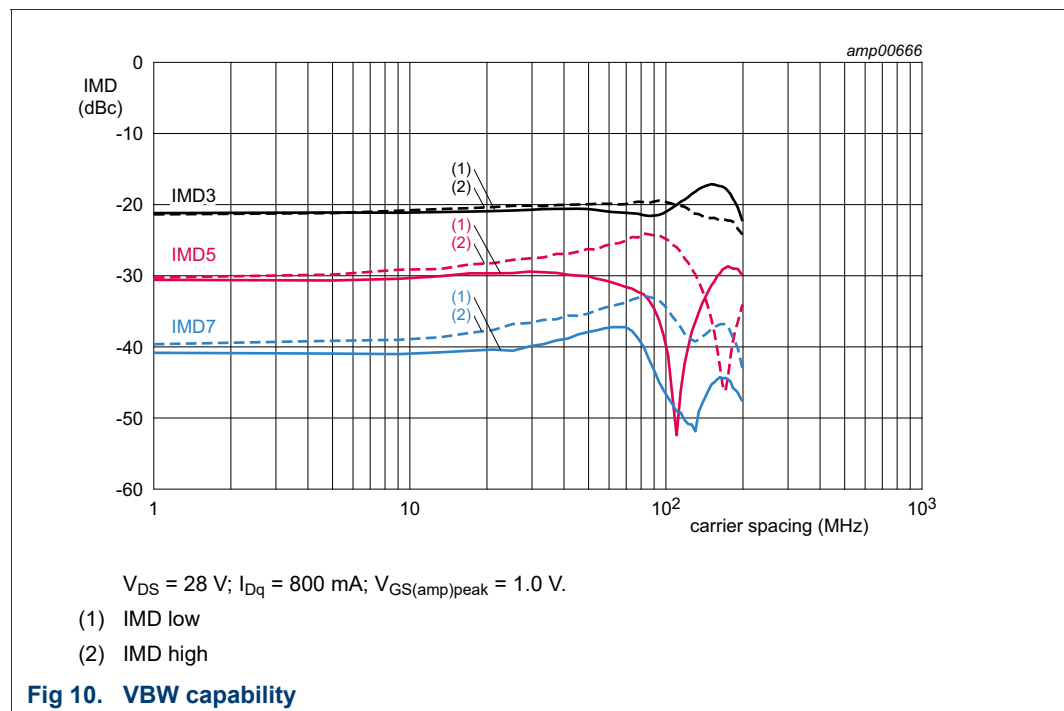
Fig 7. Peak-to-average power ratio as a function of output power; typical values

7.5.3 2-Carrier W-CDMA

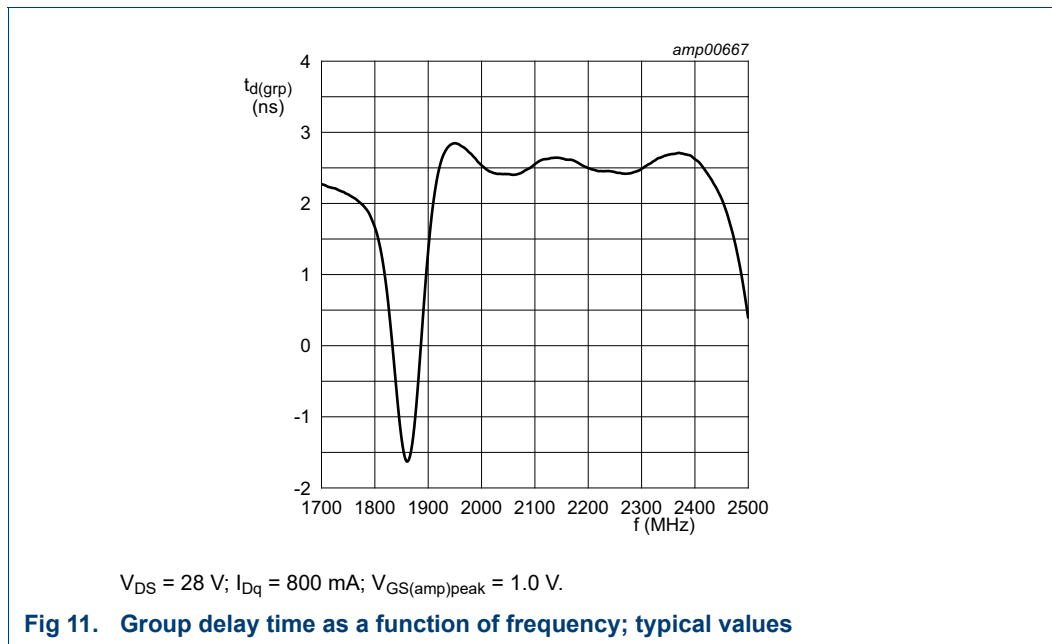
Test signal: 3GPP test model 1; 1 to 64 DPCH (46 % clipping): PAR = 7.5 dB per carrier at 0.01 % probability on CCDF per carrier.



7.5.4 2-Tone VBW



7.5.5 Group delay



8. Package outline

Air cavity plastic earless flanged package; 6 leads

SOT1258-4

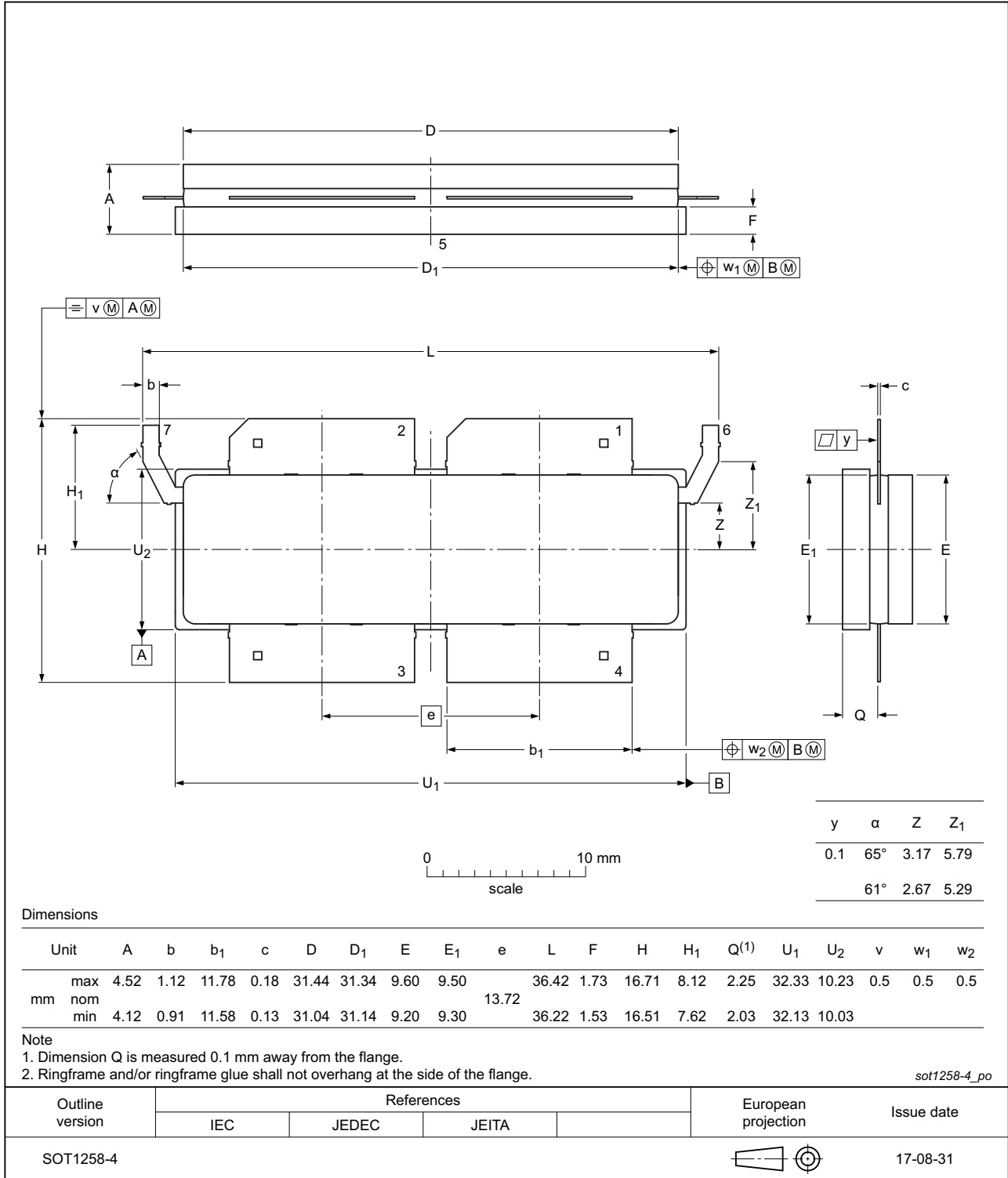


Fig 12. Package outline SOT1258-4

## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 16. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[2]</a>

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

## 10. Abbreviations

**Table 17. Abbreviations**

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

**Table 18. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC10G22XS-400AVT v.1	20180430	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.ampleon.com>.

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## 13. Contact information

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