SCOPE: 8-CHANNEL/DUAL 4-CHANNEL CMOS, ANALOG SWITCHES

Device Type	Generic Number	SMD Number
01	DG408A(x)/883B	5962-9204201
02	DG409A(x)/883B	5962-9204202

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter		Mil-Std-1835	Case Outline	Package Code
Maxim	SMD			
K	E	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
L	X	CDFP3-F16	16 LEAD FLATPACK	F16
Z	2	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings

Voltage Referenced to V^-
- V^+ to V^- 44V
- V^- to GND 25V
- Digital Inputs Overvoltage Range 1/ ..... .(V^- -2V) to (V^+ +2V) or 20mA whichever occurs first.
- Continuous Current, Any terminal except S or D 30mA
- Continuous Current, S or D 20mA
- Current, S or D (Pulsed at 1ms, 10% duty cycle max) 40mA

Lead Temperature (soldering, 10 seconds) ..... +300°C

Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C

16 lead CERDIP(derate 10.0mW/°C above +70°C) 800mW

16 lead FLATPACK(derate 6.1mW/°C above +70°C) 485mW

20 lead LCC(derate 9.1mW/°C above +70°C) 727mW

Junction Temperature T_J ..... +150°C

Thermal Resistance, Junction to Case, ΘJC:
- Case Outline 16 lead CERDIP..... 50°C/W
- Case Outline 16 lead FLATPACK ..... 65°C/W
- Case Outline 20 lead LCC ..... 55°C/W

Thermal Resistance, Junction to Ambient, ΘJA:
- Case Outline 16 lead CERDIP..... 100°C/W
- Case Outline 16 lead FLATPACK ..... 165°C/W
- Case Outline 20 lead LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C

Positive Supply Voltage (V^+) ..... +15V

Negative Supply Voltage (V^-) ..... -15V

1/ Signals on S, D or IN exceeding V^+ or V^- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+15V, V^-=-15V, GND=0V V_{AH}=2.4V, V_{AL}=0.8V, V_{EN}=2.4V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
SWITCH							
Analog-Signal Range	V_{ANALOG}	NOTE 2	1,2,3	All	-15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S=-10mA, V_D=±10V	1,3 2	All		100 125	Ω
$r_{DS(ON)}$ Matching Between Channels	$\Delta r_{DS(ON)}$	I_S=-10mA, V_D=±10V, NOTE 3	1	All		15	Ω
Source-OFF Leakage Current	$I_{S(OFF)}$	V_S=±10V, V_D=±10V, V_{EN}=0V	1 2	All	-0.5 -50	0.5 50	nA
Drain-OFF Leakage Current	$I_{D(OFF)}$	V_S=±10V, V_D=±10V, V_{EN}=0V	1 2 2	All 01 02	-1.0 -100 -50	1.0 100 50	nA
Drain-ON Leakage Current	$I_{D(ON)+}$ $I_{S(ON)}$	V_S=±10V, V_D=±10V, sequence each switch on	1 2 2	All 01 02	-1.0 -100 -50	1.0 100 50	nA
INPUT							
Input Current/Voltage High	I_{AH}	V_A= 2.4V, 15V	1,2,3	All	-10	10	µA
Input Current/Voltage Low	I_{AL}	V_A=0V, V_{EN}= 0V, 2.4V	1,2,3	All	-10	10	µA
Standby Positive Supply Current	$+I_{SBY}$	V_A=0V, V_{EN}= 0V	1,2,3	All		75	µA
Standby Negative Supply Current	$-I_{SBY}$	V_A=0V, V_{EN}= 0V	1,2,3	All	-75		µA
SUPPLY							
Positive Supply Current	I+	V_A=0V, V_{EN}= 2.4V	1,3 2	All		0.5 2.0	mA
Negative Supply Current	I-	V_A=0V, V_{EN}= 2.4V	1,2,3	All	-0.5		mA
DYNAMIC							
Transition Time	t_{TRANS}	Figure 2	9,10,11	All		250	ns
Break Before Make Time	t_{OPEN}	Figure 4	9	All	10		ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3	9,11 10	All		150 225	ns
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3	9,10,11	All		150	ns

NOTE 2: Guaranteed by design.

NOTE 3: $\Delta r_{DS(ON)} = \Delta r_{DS(ON)}max - \Delta r_{DS(ON)}min$

FIGURE 2: TRANSITION TIME TEST CIRCUIT: See Commercial Data Sheet
FIGURE 3: ENABLE SWITCHING TIME: See Commercial Data Sheet
FIGURE 4: BREAK-BEFORE-MAKE INTERVAL: See Commercial Data Sheet

ORDERING INFORMATION:

	SMD NUMBER	CIRCUIT FUNCTION	PKG CODE
DG408AK/883B	5962-9204201MEA	8-channel analog multiplexer	16 CERDIP
DG408AL/883B	5962-9204201MXC	8-channel analog multiplexer	16 FLATPACK
DG408AZ/883B	5962-9204201M2C	8-channel analog multiplexer	20 LCC
DG409AK/883B	5962-9204202MEA	Dual 4-channel analog multiplexer	16 CERDIP
DG409AL/883B	5962-9204202MXC	Dual 4-channel analog multiplexer	16 FLATPACK
DG409AZ/883B	5962-9204202M2C	Dual 4-channel analog multiplexer	20 LCC

TRUTH TABLES: **TERMINAL CONNECTION**

A2	A1	A0	EN	DG408A ON SWITCH	Terminal Number	DG408	DG408	DG409	DG409
X	X	X	L	None		J16 & F16	LCC20	J16 & F16	LCC20
L	L	L	H	1	1	A0	NC	A0	NC
L	L	H	H	2	2	EN	A0	EN	A0
L	H	L	H	3	3	V-	EN	V-	EN
L	H	H	H	4	4	S1	V-	S1a	V-
H	L	L	H	5	5	S2	S1	S2a	S1a
H	L	H	H	6	6	S3	NC	S3a	NC
H	H	L	H	7	7	S4	S2	S4a	S2a
H	H	H	H	8	8	D	S3	Da	S3a
					9	S8	S4	Db	S4a
				DG409A	10	S7	D	S4b	DA
				ON SWITCH	11	S6	NC	S3b	NC
	X	X	X	None	12	S5	S8	S2b	DB
	L	L	H	1	13	V+	S7	S1b	S4b
	L	H	H	2	14	GND	S6	V+	S3b
	H	L	H	3	15	A2	S5	GND	S2b
	H	H	H	4	16	A1	NC	A1	NC
					17		V+		S1b
					18		GND		V+
					19		A2		GND
					20		A1		A1

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 7, 8, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 7**, 8**, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** Subgroups 7 and 8 tests shall be sufficient to verify the truth table.