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CCG1 Datasheet

USB Type-C Port Controller with Power Delivery

THIS PRODUCT IS NOT RECOMMENDED FOR NEW DESIGNS

General Description

CCG1 provides a complete USB Type-C and USB Power Delivery port control solution. The core architecture of CCG1 enables a base Type-C solution that can scale to a complete 100-W USB Power Delivery with Alternate Mode multiplex support. CCG1 is also a Type-C cable ID IC for active and passive cables. The CCG1 controller detects connector insert, plug orientation and VCONN switching signals. CCG1 makes it easier to add USB Power Delivery to any architecture because it provides control signals to manage external VBUS and V_{CONN} power management solutions and external mux controls for most single cable-docking solutions.

The CCG1 family of devices are fixed-function parts that use a configuration table to control their operation in different applications. The functionality is implemented in firmware and will be certified against USB Implementers Forum (USB-IF) compliance tests when available. The programmability allows CCG1 devices to track any USB Specification changes. For information on accessing the source code, contact Cypress support. CCG1 devices are not recommended for new designs. However, customers may continue to purchase these CCG1 devices for their existing designs already in production.

Applications

- Notebooks, tablets, monitors, docking stations
- Power adapters, USB Type-C cables

Features

32-bit MCU Subsystem

- 48-MHz ARM Cortex-M0 CPU with 32-KB flash and 4-KB SRAM

Integrated analog blocks

- 12-bit, 1-Msps ADC for VBUS voltage and current monitoring
- Dynamic overcurrent and overvoltage protection

Integrated digital blocks

- Two configurable 16-bit TCPWM blocks
- One I^2C master or slave

Type-C Support

- Integrated transceiver (BB PHY)
- Supports up to two USB ports with PD
- Supports routing of all protocols through an external mux

PD Support

- Supports Provider and Consumer roles
- Supports all power profiles

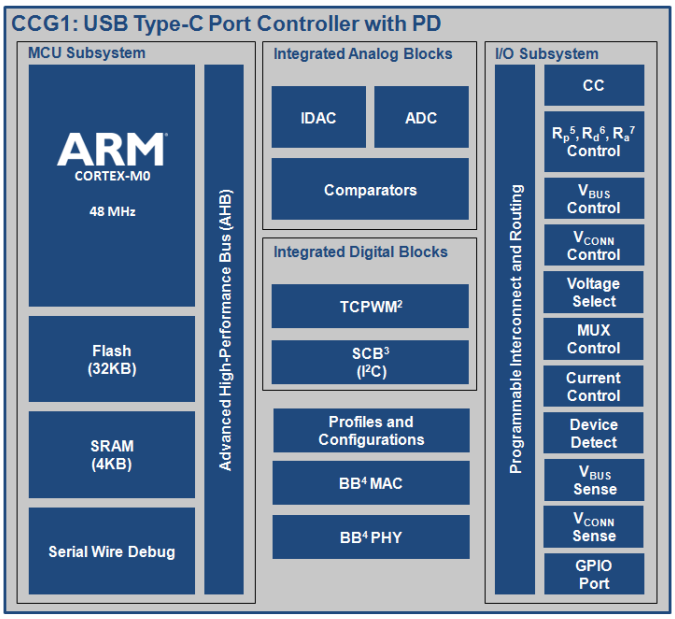
Low-Power Operation

- 3.2 V to 5.5 V operation
- Sleep 1.3 mA, Deep Sleep 1.3 μA[1]

Packages

- 40-pin QFN
- 16-pin SOIC
- 35-ball wafer-level CSP (WLCSP)

Figure 1. CCG1 Block Diagram[2, 3, 4, 5, 6, 7]



Notes
1. Values measured for CCG1 silicon only. Application specific power numbers may be higher.
2. Timer, counter, pulse-width modulation block.
3. Serial communication block configurable as I^2C.
4. Base band.
5. Termination resistor denoting a Downstream Facing Port (DFP).
6. Termination resistor denoting a Upstream Facing Port (UFP).
7. Termination resistor denoting an Electronically Marked Cable Assembly (EMCA).

Contents

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the CCG1 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for CCG1 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The CCG1 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section Power on page 12. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) or interrupts (Low Voltage Detect (LVD)). The CCG1 operates with a single external supply over the range of 3.2 V to 5.5 V operation and has three different power modes: Active, Sleep, and Deep Sleep; transitions between modes are managed by the power system.

Serial Communication Blocks (SCB)

The CCG1 has one SCB, which can implement an I^2C interface. The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZ-I^2C that creates a mailbox address range in the memory of the CCG1 and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripheral is compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices, as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

The CCG1 is not completely compliant with the I^2C spec in the following respects:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8 mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.
- When the SCB is an I^2C Master, it interposes an IDLE state between NACK and Repeated Start; the I^2C spec defines Bus free as following a Stop condition so other Active Masters do not intervene but a Master that has just become activated may start an Arbitration cycle.
- When the SCB is in the I^2C Slave mode, and Address Match on External Clock is enabled (EC_AM = 1) along with operation in the internally clocked mode (EC_OP = 0), then its I^2C address must be even.

GPIO

The CCG1 has up to 30 GPIOs, which are configured for various functions. Refer to the pinout tables for the definitions. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode).
- Selectable slew rates for dV/dt related noise control to improve EMI.

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network, known as a high-speed I/O matrix, is used to multiplex between various signals that may connect to an I/O pin.

Pin Definitions

Table 1 provides the pin definition for 35-Ball WLCSP for the Cable/EMCA application. Refer to Table 23 for part numbers to package mapping.

Table 1. Pin Definitions for 35-ball WLCSP for EMCA Cable Application

Functional Pin Name	CYPD1103-35FNXIT Balls	Type	Description
CC1_RX	C4	I	CC1 control 0: TX enabled z: RX sense
CC1_TX	D7	O	Configuration Channel 1
SWD_IO	D1	I/O	SWD I/O
SWD_CLK	C1	I	SWD clock
I2C_SCL	B1	I/O	I^2C clock signal
I2C_SDA	B2	I/O	I^2C data signal
XRES	B6	I	Reset
VCCD	A7	POWER	Regulated digital supply output. Connect a 1 to 1.6-µF capacitor. No external source should be connected
VDDD	C7	POWER	Power supply for both analog and digital sections
VSSA	B7	GND	Analog ground
CC_VREF	C5	I	Data reference signal for CC lines
TX_U	B3	O	Signals for internal use only. The TX_U output signal should be connected to the TX_M signal
TX_M	B5	I	_
TX_REF_IN	D3	I	Reference signal for internal use. Connect to TX_REF output via a 2.4K 1% resistor
TX_GND	A3	I	Connect to GND via 2K 1% resistor
TX_REF_OUT	D4	O	Reference signal generated by connecting internal current source to two 1K external resistors
RA_DISCONNECT	E4	O	Optional control signal to remove RA after assertion of VCONN 0: RA disconnected 1: RA connected
VCONN_DET	C6	I	Local VCONN detection signal 0: VCONN is not locally applied 1: VCONN is locally applied
CC1_LPREF	A5	I	Reference signal for internal use. Connect to the output of resistor divider from VDDD.
RA_FAR_DISCONNECT	E5	O	Optional control signal to remove RA after assertion of VCONN (NC for 2 chip/cable) 0: RA disconnected 1: RA connected
BYPASS	D5	I	Bypass capacitor for internal analog circuits
CC1_LPRX	C3	I	Configuration channel 1 RX signal for Low Power States
GPIO	A1, A2, A4, A6, B4, C2, D2, D6, E1, E2, E3, E6, E7	–	General-purpose I/Os

Table 2 provides the pin definitions for 40-pin QFN and 35-ball WLCSP for the notebook, tablet, smartphone, and monitor applications. Refer to Table 23 on page 23 for part numbers to package mapping.

Table 2. Pin Definitions for 40-QFN and 35-ball WLCSP for Notebook, Tablet, SmartPhone and Monitor Applications

Functional Pins	CYPD 1122-40LQXI Pins[8]	CYPD 1121-40LQXI Pins[9]	CYPD 1131-35FNXIT Balls[10]	Type	Description
MUXSEL_1	1	1	D5	O	External Data Mux Select signal 1
MUXSEL_2	2	2	D6	O	External Data Mux Select signal 2
CC1_CTRL	3	3	D3	I/O	CC1 control 0: TX enabled z: RX sense
CC2_CTRL	4	4	E4	I/O	CC2 control 0: TX enabled z: RX sense
MUXSEL_3	5	5	E5	O	External Data Mux Select signal 3
MUXSEL_4	6	6	E6	O	External Data Mux Select signal 4
CS_P	7	7	E3	I	Current Sensing Plus input
CS_M	8	8	E2	I	Current Sensing Minus input I
VSS	9	9	–	GND	Ground
CC1	10	10	-	I/O	Configuration Channel 1
CC_SEL_REF_1	11	11	E1	O	CC Reference Select signal
SWD_IO	12	12	D1	I/O	SWD IO
SWD_CLK	13	13	C1	I	SWD Clock
HOTPLUG_DET	14	14	C2	I/O	HotPlug Detection for Display Port Alternate Mode
GPIO1	15	–	–	I/O	General-purpose I/O
VSEL2	–	15	–	O	Voltage Select signal 2 for selecting output voltage
GPIO2	16	–	–	I/O	General-purpose I/O
GPIO3	17	–	–	I/O	General-purpose I/O
IFAULT	–	17	–	I	Current Fault Indication 0: No fault 1: Current fault
I2C_SCL	18	18	B1	I/O	I2C Clock signal
I2C_SDA	19	19	B2	I/O	I2C Data signal
I2C_INT	20	20	A2	O	I2C Interrupt
CC_SEL_REF_2	21	21	A1	O	CC Reference Select signal
CC1_RD	22	22	C3	O	Open Drain signal to connect RD to CC 1 line z: RD not connected 0: RD connected for Monitor application 1: RD connected for Notebook application
CC1_RP	23	23	A5	O	Open Source signal to connect RP to CC 1 line z: RP not connected 1: RP connected

Notes
8. Pinout for Notebook DRP application for 40-QFN.
9. Pinout for Monitor DRP application for 40-QFN.
10. Pinout for Notebook DRP application for 35-CSP.

Table 2. Pin Definitions for 40-QFN and 35-ball WLCSP for Notebook, Tablet, SmartPhone and Monitor Applications *(continued)*

Functional Pins	CYPD 1122-40LQXI Pins[8]	CYPD 1121-40LQXI Pins[9]	CYPD 1131-35FNXIT Balls[10]	Type	Description
CC1_VCONN_CTRL	24	24	A4	O	Open Drain signal to control a PFET power switch for VCONN on CC 1 line 0: VCONN switch closed z: VCONN switch open
VBUS_DISCHARGE	25	25	A3	O	Signal used for discharging VBUS line during voltage change
CC2	26	26	B3	O	Configuration Channel 2
CC2_RD	27	27	A6	O	Open Drain signal to connect RD to CC 2 line z: RD not connected 0: RD connected for Monitor application 1: RD connected for Notebook application
CC2_RP	28	28	B4	O	Open Source signal to connect RP to CC 2 line z: RP not connected 1: RP connected
CC2_VCONN_CTRL	29	29	B5	O	Open Drain signal to control a PFET power switch for VCONN on CC 2 line 0: VCONN switch closed z: VCONN switch open
XRES	30	30	B6	I	Reset
VCCD	31	31	A7	POWER	Regulated digital supply output. Connect a 1 to 1.6-µF capacitor. No external source should be connected
VDDD	32	32	C7	POWER	Power supply for digital sections
VDDA	33	33	C7	POWER	Power Supply for analog sections
VSSA	34	34	B7	GND	Analog ground pin
VBUS_VMON	35	35	C4	I	VBUS Overvoltage Protection monitoring signal
VBUS_VREF	36	36	C5	I	VBUS reference signal for Overvoltage Protection detection
VSEL1	–	37	–	O	Voltage Select signal 1 for selecting the output voltage
CC_SEL_REF_3	37	16	C6	O	CC Reference Select signal
VBUS_C_CTRL	38	–	D7	O	Full rail control signal for enabling/disabling Consumer load FET
VBUS_OK	–	38	–		VBUS_OK=1 - VBUS Voltage ok VBUS_OK=0 - VBUS Overvoltage detected
CC_VREF	39	39	D4	I	Data reference signal for CC lines
VBUS_P_CTRL	40	40	E7	O	Full rail control signal for enabling/disabling Provider load FET

Notes
8. Pinout for Notebook DRP application for 40-QFN.
9. Pinout for Monitor DRP application for 40-QFN.
10. Pinout for Notebook DRP application for 35-CSP.

Table 3 provides the pin definition for 40-pin QFN for Notebook (DFP) application. Refer to Table 23 for part numbers to package mapping.

Table 3. Pin Definitions for 40-Pin QFN for Notebook (DFP)

Functional Pin Name	Active HIGH/ LOW	Drive Mode	CYPD 1134-40LQXI Pins	Type	Description
MUXSEL_1	–	Open drain, drives low	1	O	External Data Mux Select signal 1
MUXSEL_2	–	Open drain, drives low	2	O	External Data Mux Select signal 2
CC1_CTRL	–	Analog input/Strong drive (push pull)	3	IO	CC1 control 0:Tx enabled z: RX sense
CC2_CTRL	–	Analog input/Strong drive (push pull)	4	IO	CC2 control 0: TX enabled z: RX sense
MUXSEL_3	–	Open drain, drives low	5	O	External Data Mux Select signal 3
MUXSEL_4	–	Open drain, drives low	6	O	External Data Mux Select signal 4
CS_P	–	Analog input	7	I	Current Sensing Plus input
CS_M	–	Analog input	8	I	Current Sensing Minus input
VSS	–	_	9	GND	Ground
CC1	–	Strong drive (push pull)	10	O	Configuration Channel 1
CC1_RP_1.5	Active HIGH	Open drain, drives high	11	O	Open Drain signal to connect RP to CC1 line (1.5A current) z: RP not connected 1: RP connected
SWD_IO	–	_	12	IO	SWD IO
SWD_CLK	–	_	13	I	SWD Clock
CC1_RP_3.0	Active HIGH	Open drain, drives high	14	O	Open Source signal to connect RP to CC1 line (3A current) z: RP not connected 1: RP connected
CC1_RP_DEF	Active HIGH	Open drain, drives high	15	O	Open Drain signal to connect RP to CC1 line (Default current) z: RP not connected 1: RP connected
CC2_RP_DEF	Active HIGH	Open drain, drives high	16	O	Open Drain signal to connect RP to CC2 line (Default current) z: RP not connected 1: RP connected
CC2_RP_1.5	Active HIGH	Open drain, drives high	17	O	Open Drain signal to connect RP to CC2 line (1.5A current) z: RP not connected 1: RP connected
I2C_SCL	Active LOW	Open drain, drives low	18	IO	I^2C Clock signal
I2C_SDA	Active LOW	Open drain, drives low	19	IO	I^2C Data signal
I2C_INT	Active LOW	Open drain, drives low	20	O	I^2C Interrupt

Table 3. Pin Definitions for 40-Pin QFN for Notebook (DFP) *(continued)*

Functional Pin Name	Active HIGH/ LOW	Drive Mode	CYPD 1134-40LQXI Pins	Type	Description
CC2_RP_3.0	Active HIGH	Open drain, drives high	21	O	Open Source signal to connect RP to CC2 line (3A current) z: RP not connected 1: RP connected
CC1_LPRX	–	Analog input	22	I	Configuration channel 1 RX signal for Low Power states
CC1_LPREF	–	Analog input	23	I	Reference signal for internal use.
CC2_LPRX	–	Analog input	24	I	Configuration channel 2 RX signal for Low Power states
CC2_LPREF	–	Analog input	25	I	Reference signal for internal use.
CC2	–	Strong drive (push pull)	26	O	Configuration Channel 2
CC1_VCONN_CTRL	Active LOW	Open drain, drives low	27	O	Open Drain signal to control a PFET power switch for VCONN on CC1 line 0: VCONN switch closed z: VCONN switch open
CC2_VCONN_CTRL	Active LOW	Open drain, drives low	28	O	Open Drain signal to control a PFET power switch for VCONN on CC2 line 0: VCONN switch closed z: VCONN switch open
IFAULT	Active HIGH	Digital input	29	I	Current Fault Indication on VBUS 0: No fault 1: Over Current fault
XRES	Active LOW	Analog input	30	I	Reset
VCCD	–	_	31	POWER	Connect 1uf Capacitor between VCCD and Ground
VDDD	–	_	32	POWER	5-V Supply
VDDA	–	_	33	POWER	5-V Supply
VSSA	–	_	34	GND	–
E-PAD	–	_	E-PAD	GND	–
VBUS_VMON	–	Analog input	35	I	VBUS Over-voltage Protection monitoring signal
VBUS_VREF	–	Analog input	36	I	VBUS reference signal for Over-voltage Protection detection
VBUS_P_CTRL	Active HIGH	Strong drive (Push Pull)	37	O	Full rail control signal for enabling/disabling Provider load FET
HOTPLUG_DET	Active HIGH	Open drain, drives low	38	IO	HotPlug Detection for Display Port Alternate Mode
CC_VREF/ VBUS_DISCHARGE	-/Active HIGH	Analog input/Strong drive (Push Pull)	39	IO	Data reference signal for CC lines / Signal used for discharging VBUS line during voltage change
MUXSEL_5	–	Open drain, drives low	40	O	External Data Mux Select signal 5

Table 4 provides the pin definition for 16-pin SOIC for the Power Adapter application. Refer to Table 23 on page 23 for part numbers to package mapping.

Table 4. Pin Definitions for 16-pin SOIC for Power Adapter Application

Functional Pin Name	CYPD 1132-16SXI Pins	Type	Description
SWD_CLK	1	I	SWD Clock
VBUS_P_CTRL	2	O	Full rail control signal for enabling/disabling provider load FET
VBUS_VMON	3	I	VBUS over-voltage protection monitoring signal
VBUS_VREF	4	I	VBUS reference signal for over-voltage protection detection
XRES	5	–	Active Low Reset
VCCD	6	–	Connect 1 µF capacitor between VCCD and GROUND
VSSD	7	–	Ground
VDDD	8	–	Power 3.3 V/5 V
VSSA	9	–	Ground
CC_VREF/VBUS_DISCHARGE	10	I/O	Data reference signal for CC line (0.55 Volt) / Signal used for discharging VBUS line during voltage decrease
CC_CTRL	11	I/O	CC1 control 0: TX enabled z: RX sense
CS	12	I	Low Side Current Sense
VSEL1	13	O	Voltage select signal for selecting the output voltage 5/12/20 V
VSEL2	14	O	Voltage select signal for selecting the output voltage 5/12/20 V
CC	15	I/O	Configuration Channel TX/RX
SWD_IO	16	I/O	SWD I/O

Pinouts

Figure 2. Pinout for CYPD1122-40LQXI/CYPD1121-40LQXI

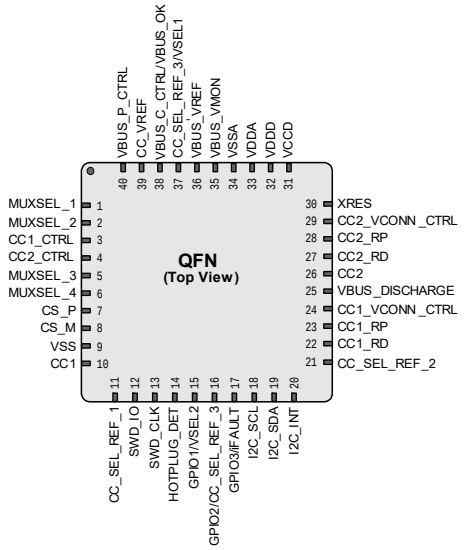


Figure 3. Pinout for CYPD1134-40LQXI

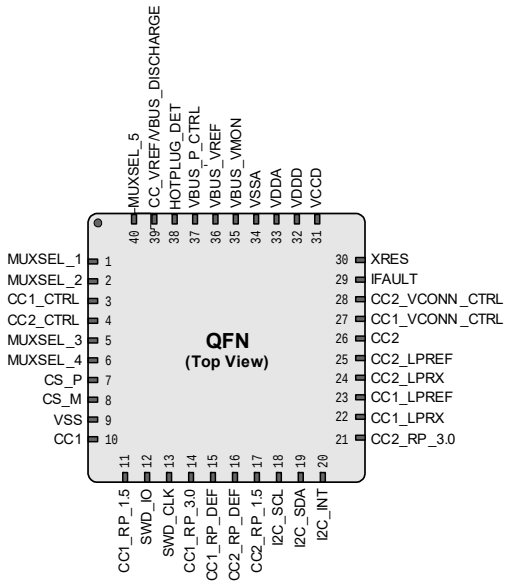


Figure 4. Pinout for CYPD1132-16SXI

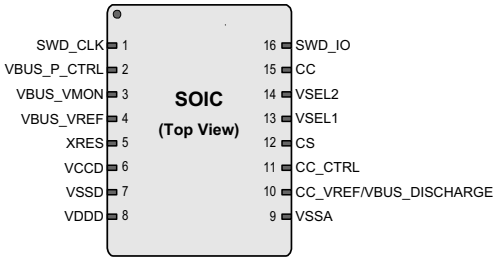
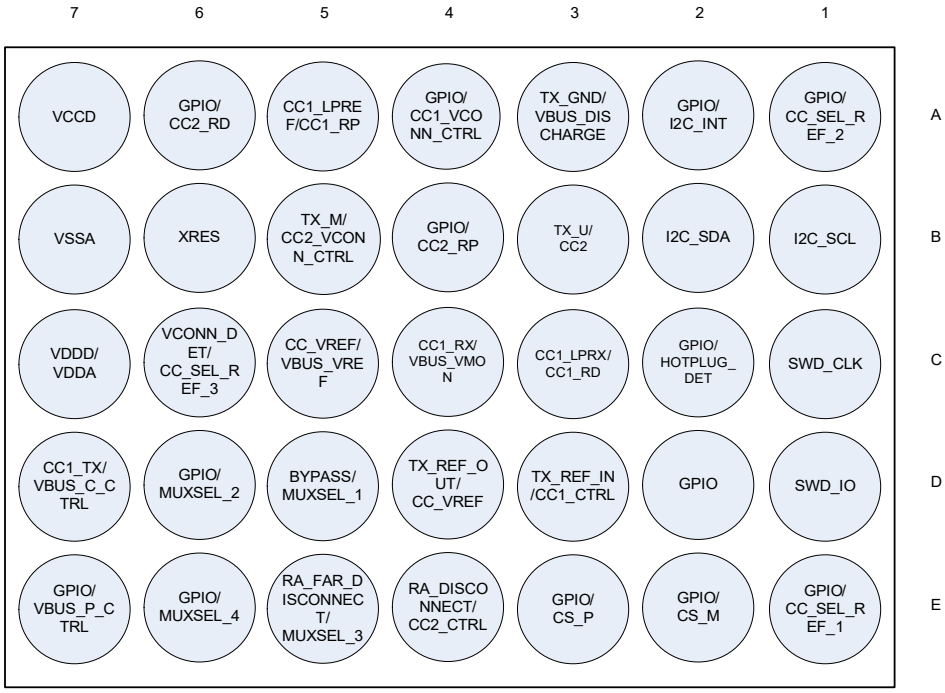


Figure 5. Pinout for CYPD1103-35FNXIT/CYPD1131-FNXIT



Power

The following power system diagram shows the minimum set of power supply pins as implemented for the CCG1. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the VDDA input. There is a separate regulator for the Deep Sleep mode. There is a separate low-noise regulator for the bandgap. The supply voltage range is 3.2 V to 5.5 V with all functions and circuits operating over that range.

VDDA and VDDD must be shorted together; the grounds, VSSA and VSS must also be shorted together. Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Refer to Application Diagrams for bypassing schemes.

Electrical Specifications

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings[11]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID1	V_{DDD_ABS}	Digital supply relative to V_{SSD}	–0.50	–	6.00	V	Absolute max
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.50	–	1.95	V	Absolute max
SID3	V_{GPIO_ABS}	GPIO voltage	–0.50	–	V_{DDD}+0.50	V	Absolute max
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25.00	–	25.00	mA	Absolute max
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.50	–	0.50	mA	Absolute max, current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200.00	–	–	V	–
BID45	ESD_CDM	Electrostatic discharge charged device model	500.00	–	–	V	–
BID46	LU	Pin current for latch-up	–200.00	–	200.00	mA	–

Device-Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C for 35-CSP and 40-QFN package options. Specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C for 16-SOIC package options. Specifications are valid for 3.2 V to VDD's maximum value, depending on the type of application.

Table 6. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID53	V_{DDD}	Power supply input voltage	3.20	–	5.20	V	Notebook, tablet, monitor and power adapter applications
SID53_A	V_{DDD}	Power supply input voltage	3.20	–	5.50	V	EMCA applications
SID54	V_{CCD}	Output voltage (for core logic)	–	1.80	–	V	–
SID55	C_{EFC}	External regulator voltage bypass	1.00	1.30	1.60	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply decoupling capacitor	–	1.00	–	µF	X5R ceramic or better
Active Mode, V_{DDD} = 3.2 to 5.5 V. Typical values measured at V_{DD} = 3.3 V.							
SID19	I_{DD14}	Execute from flash; CPU at 48 MHz	–	12.80	–	mA	T = 25 °C
SID20	I_{DD15}	Execute from flash; CPU at 48 MHz	–	–	13.80	mA	–
Sleep Mode, V_{DDD} = 3.2 to 5.5 V							–
SID25A	I_{DD20A}	I^2C wakeup and comparators on	–	1.70	2.2 0	mA	–
Deep Sleep Mode, V_{DDD} = 3.2 to 3.6 V (Regulator on)							
SID31	I_{DD26}	I^2C wakeup on	–	1.30	–	µA	T = 25 °C, 3.6 V
SID32	I_{DD27}	I^2C wakeup on	–	–	50.00	µA	T = 85 °C
Deep Sleep Mode, V_{DDD} = 3.6 to 5.5 V							
SID34	I_{DD29}	I^2C wakeup	–	15.00	–	µA	T = 25 °C, 5 V
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2.00	5.00	mA	–

Note

11. Usage above the absolute maximum conditions listed in Table 5 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 7. AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID48	F_{CPU}	CPU frequency	DC	–	48.00	MHz	$3.2 \le V_{DD} \le 5.5$
SID49	T_{SLEEP}	Wakeup from sleep mode	–	0.00	–	µs	Guaranteed by characterization
SID50	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	25.00	µs	24-MHz IMO. Guaranteed by characterization
SID52	$T_{RESETWIDTH}$	External reset pulse width	1.00	–	–	µs	Guaranteed by characterization

I/O

Table 8. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID57	V_{IH}[12]	Input voltage high threshold	0.70 × V_{DDD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.30 × V_{DDD}	V	CMOS Input
SID243	V_{IH}[12]	LVTTL input	2.00	–	–	V	–
SID244	V_{IL}	LVTTL input	–	–	0.80	V	–
SID59	V_{OH}	Output voltage high level	V_{DDD} – 0.60	–	–	V	I_{OH} = 4 mA at 3 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.60	V	I_{OL} = 8 mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.40	V	I_{OL} = 3 mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.50	5.60	8.50	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.50	5.60	8.50	kΩ	–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2.00	nA	25 °C, V_{DDD} = 3.0 V
SID65A	I_{IL_CTBM}	Input leakage current (absolute value) for analog pins	–	–	4.00	nA	–
SID66	C_{IN}	Input capacitance	–	–	7.00	pF	–
SID67	V_{HYSTTL}	Input hysteresis LVTTL	15.00	40.00	–	mV	$V_{DDD} \ge 2.7$ V. Guaranteed by characterization
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	200.00	–	–	mV	$V_{DDD} \ge 4.5$ V. Guaranteed by characterization
SID69	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100.00	µA	Guaranteed by characterization
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200.00	mA	Guaranteed by characterization

Table 9. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time	2.00	–	12.00	ns	3.3-V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time	2.00	–	12.00	ns	3.3-V V_{DDD}, Cload = 25 pF

Note
12. V_{IH} must not exceed V_{DDD} + 0.2 V.

XRES

Table 10. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID77	V_{IH}	Input voltage high threshold	0.70 × V_{DDD}	–	–	V	CMOS input
SID78	V_{IL}	Input voltage low threshold	–	–	0.30 × V_{DDD}	V	CMOS input
SID79	R_{PULLUP}	Pull-up resistor	3.50	5.60	8.50	kΩ	–
SID80	C_{IN}	Input capacitance	–	3.00	–	pF	–
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100.00	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100.00	µA	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for VSEL and CUR_LIM Pins

Table 11. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID140	$T_{PWMFREQ}$	Operating frequency	–	–	48.00	MHz	–
SID141	$T_{PWMPWINT}$	Pulse width (internal)	42.00	–	–	ns	–
SID142	T_{PWMEXT}	Pulse width (external)	42.00	–	–	ns	–
SID143	$T_{PWMKILLINT}$	Kill pulse width (internal)	42.00	–	–	ns	–
SID144	$T_{PWMKILLEXT}$	Kill pulse width (external)	42.00	–	–	ns	–
SID145	$T_{PWMEINT}$	Enable pulse width (internal)	42.00	–	–	ns	–
SID146	$T_{PWMENEXT}$	Enable pulse width (external)	42.00	–	–	ns	–
SID147	$T_{PWMRESWINT}$	Reset pulse width (internal)	42.00	–	–	ns	–
SID148	$T_{PWMRESWEXT}$	Reset pulse width (external)	42.00	–	–	ns	–

I^2C

Table 12. Fixed I^2C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135.00	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310.00	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.40	µA	–

Table 13. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1.00	Mbps	–

Memory

Table 14. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	3.20	–	5.50	V	–

Table 15. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$[13]	Row (block) write time (erase and program)	–	–	20.00	ms	Row (block) = 128 bytes
SID175	$T_{ROWERASE}$[13]	Row erase time	–	–	13.00	ms	–
SID176	$T_{ROWPROGRAM}$[13]	Row program time after erase	–	–	7.00	ms	–
SID178	$T_{BULKERASE}$[13]	Bulk erase time (32 KB)	–	–	35.00	ms	–
SID180	$T_{DEVPROG}$[13]	Total device program time	–	–	7.00	seconds	Guaranteed by characterization
SID181	F_{END}	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F_{RET}[14]	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A	–	Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	–	Flash retention. 85 °C < $T_A \leq 105$ °C, 10K P/E cycles	3	–	–	years	Guaranteed by characterization

System Resources

Power-on-Reset (POR) with Brown Out

Table 16. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.40	V	Guaranteed by characterization
SID187	$V_{IPORHYST}$	Hysteresis	15.0	–	200.0	mV	Guaranteed by characterization

Table 17. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.64	–	–	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.40	–	–	V	Guaranteed by characterization

Notes

13. It can take as much as 20 milliseconds to write to flash. During this time the device should not be Reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
14. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +105 °C ambient temperature range. Contact customercare@cypress.com.

SWD Interface

Table 18. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	3.2 V ≤ V_{DDD} ≤ 5.5 V	–	–	14.00	MHz	SWDCLK ≤1/3 CPU clock frequency
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50*T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 19. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000.00	µA	–

Table 20. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation	–	–	±2.00	%	With API-called calibration
SID226	$T_{STARTIMO}$	IMO startup time	–	–	12.00	µs	–
SID229	$T_{JITRMSIMO3}$	RMS Jitter at 48 MHz	–	139.00	–	ps	–

Internal Low-Speed Oscillator

Table 21. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	ILO operating current at 32 kHz	–	0.30	1.05	µA	Guaranteed by characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2.00	15.00	nA	Guaranteed by design

Table 22. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	2.00	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40.00	50.00	60.00	%	Guaranteed by characterization
SID237	$F_{ILOTRIM1}$	32-kHz trimmed frequency	15.00	32.00	50.00	kHz	±60% with trim

Applications in Detail

Figure 6. Single Chip/Cable, Component Count = 19

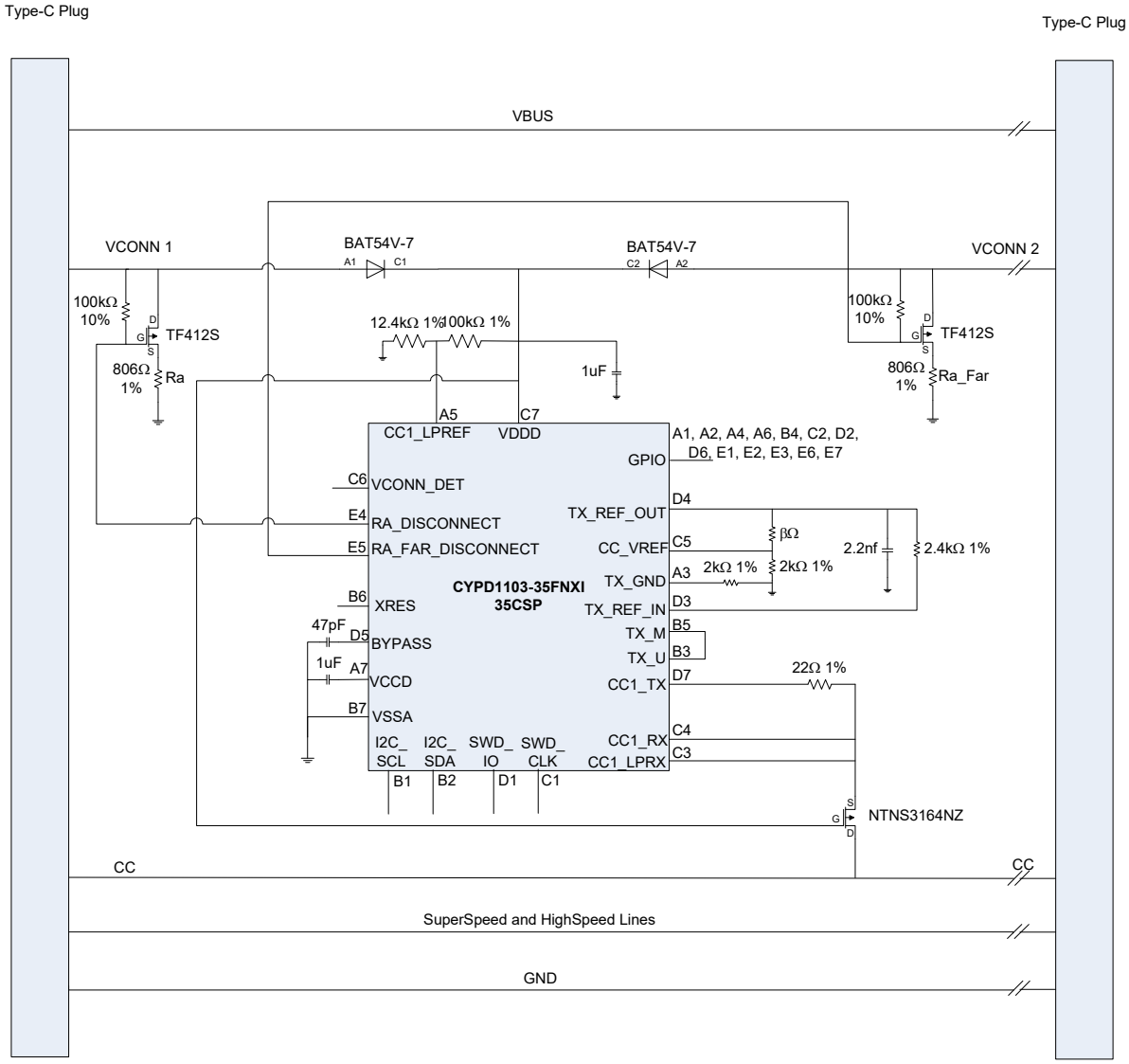


Figure 7. Two Chip/Cable, Component Count = 15/paddle

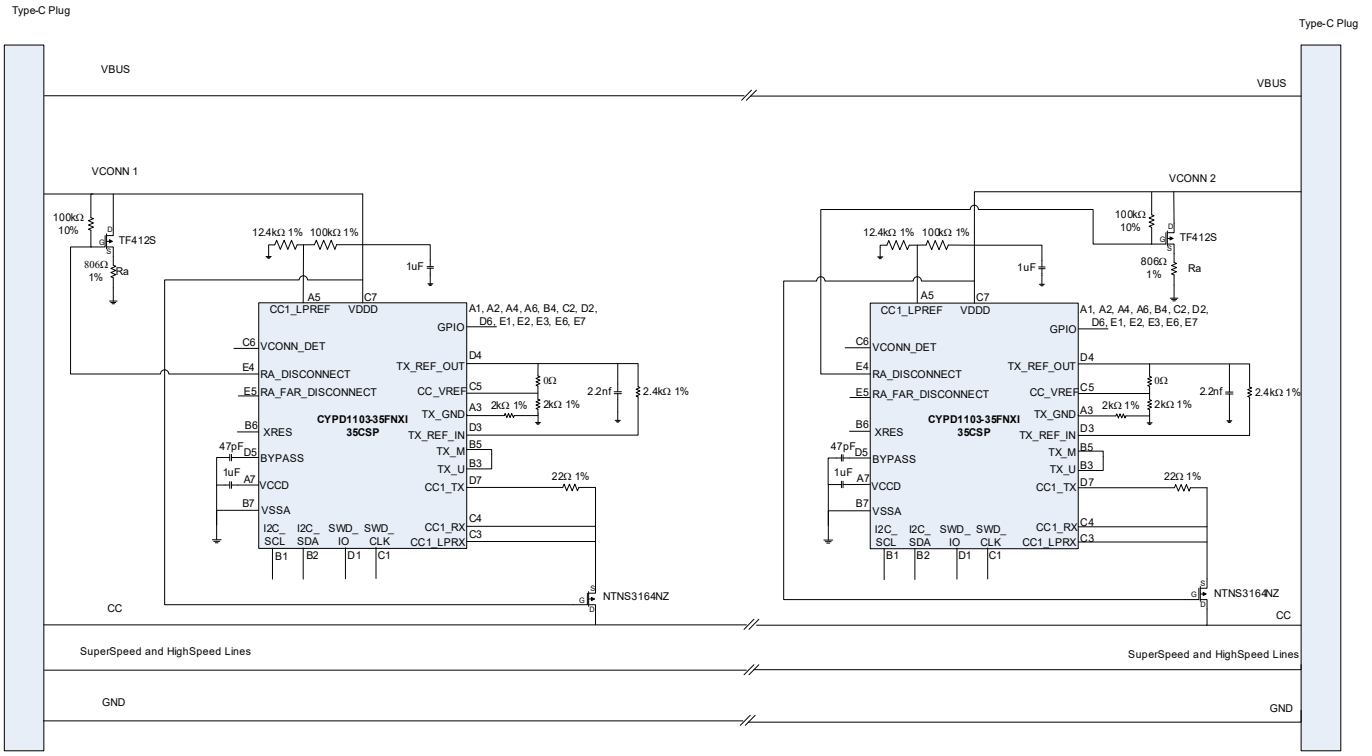


Figure 8. 16-pin SOIC Power Adapter Application Diagram

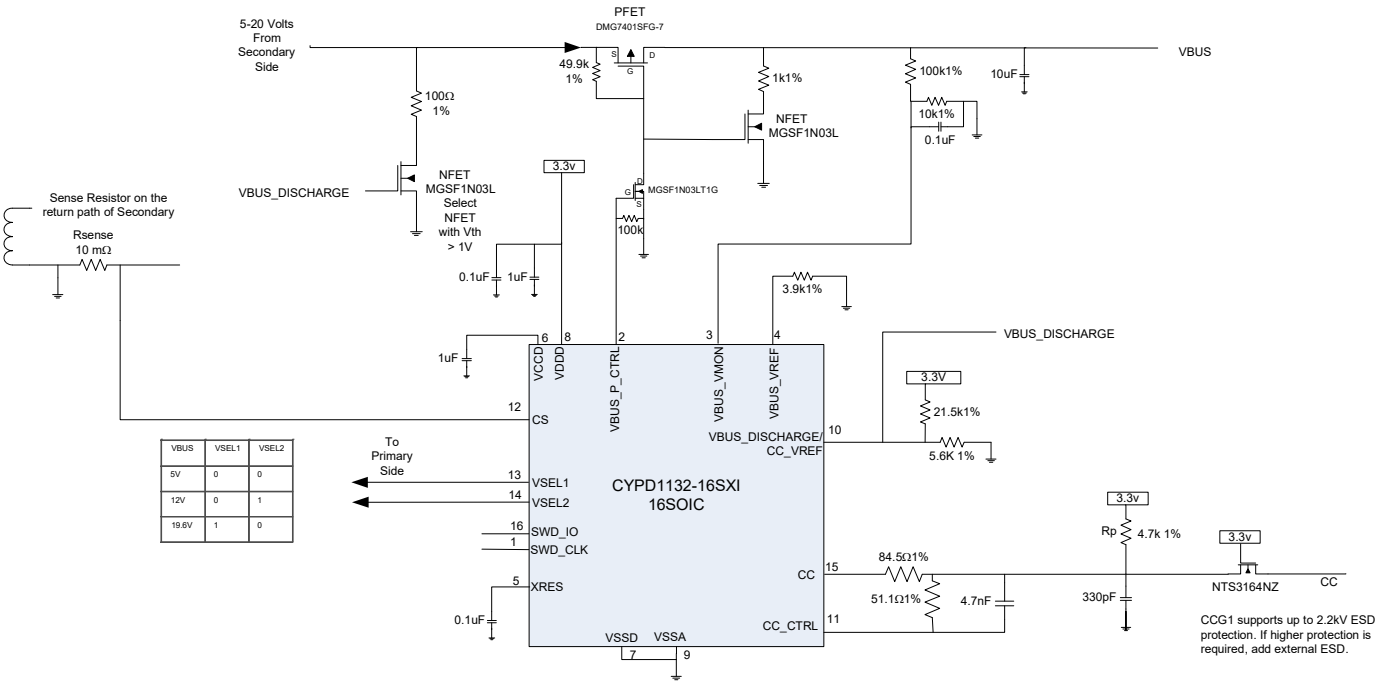


Figure 9. Notebook (DRP) Application Diagram

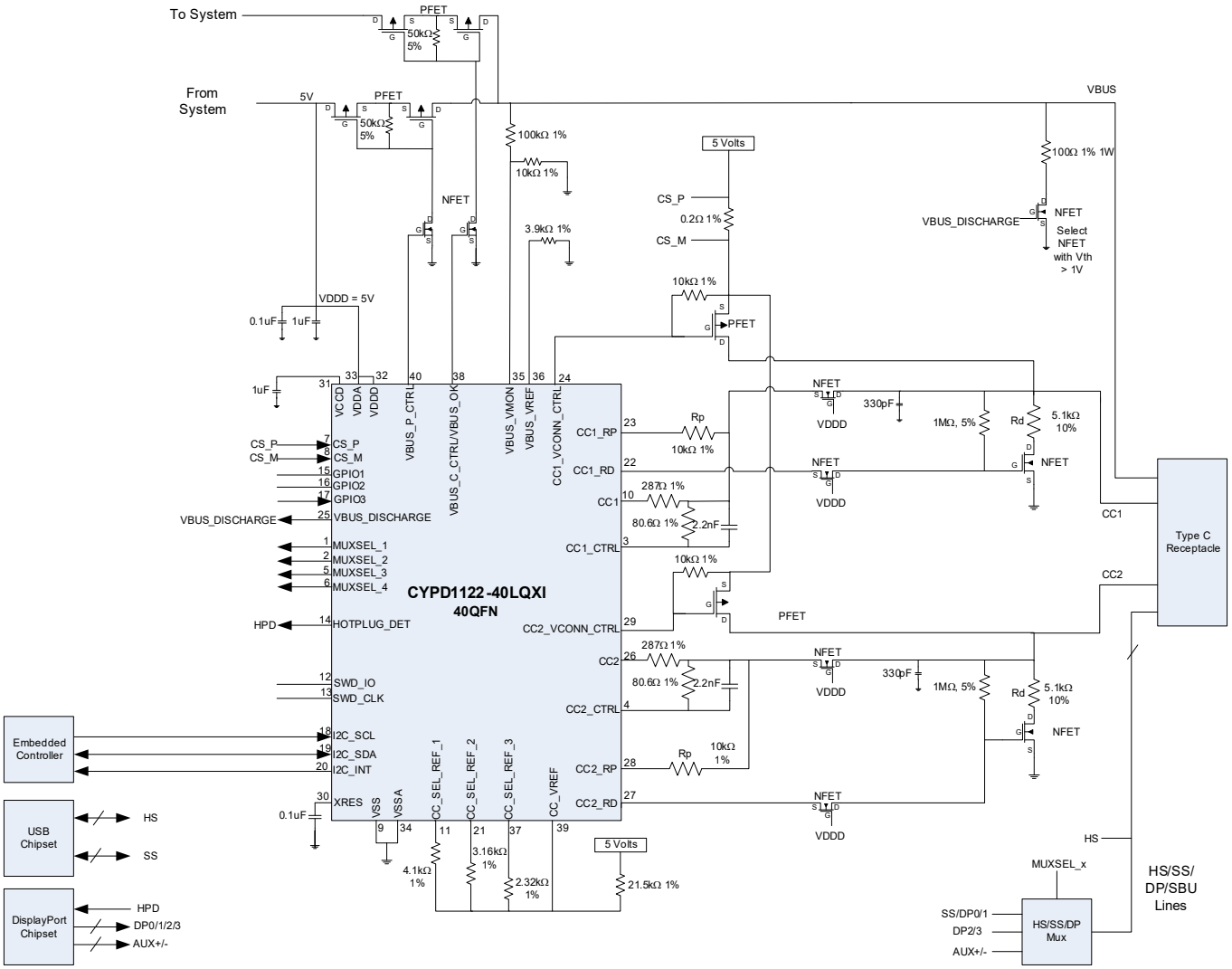


Figure 10. Notebook (DFP) Application Diagram

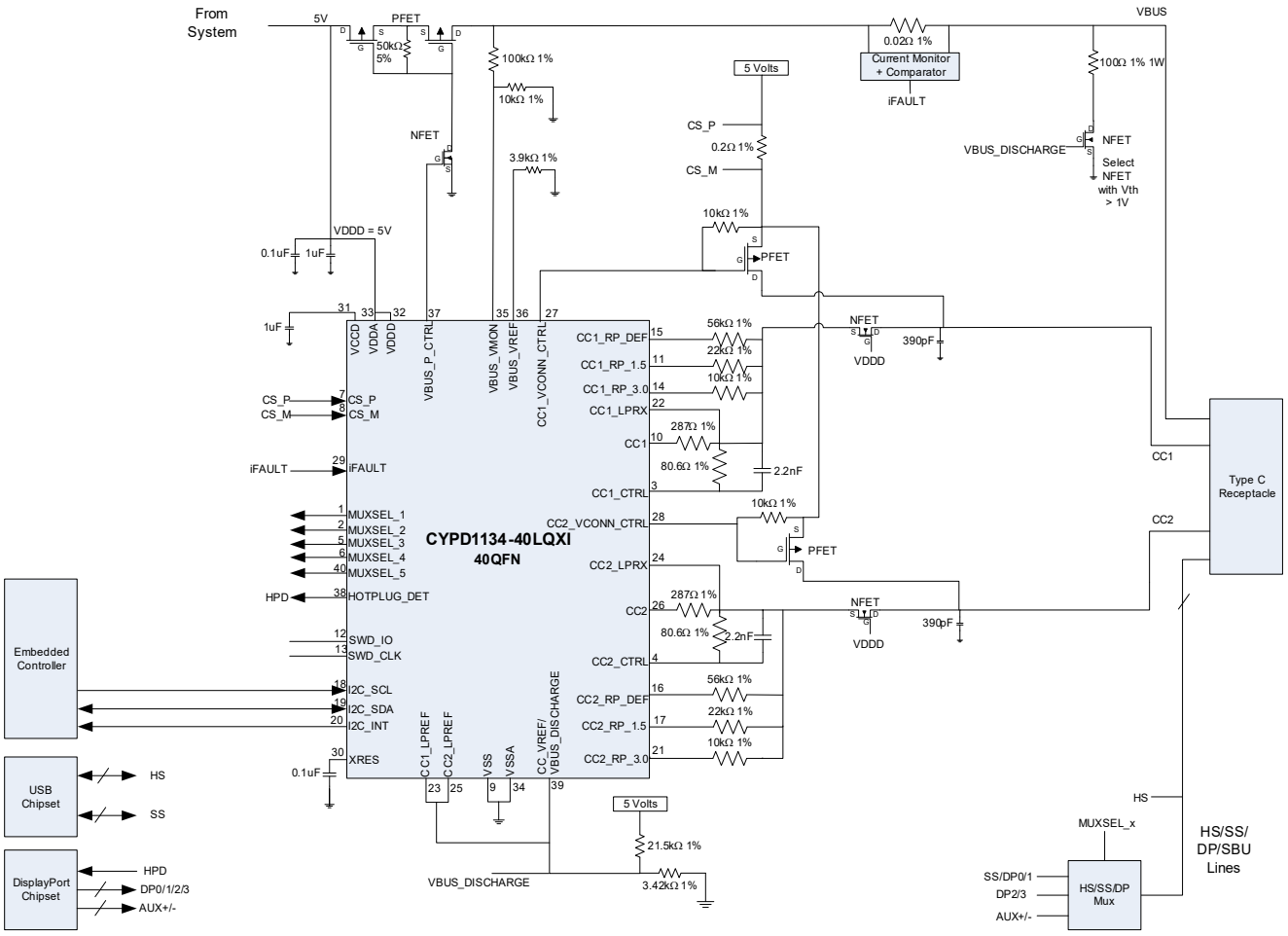
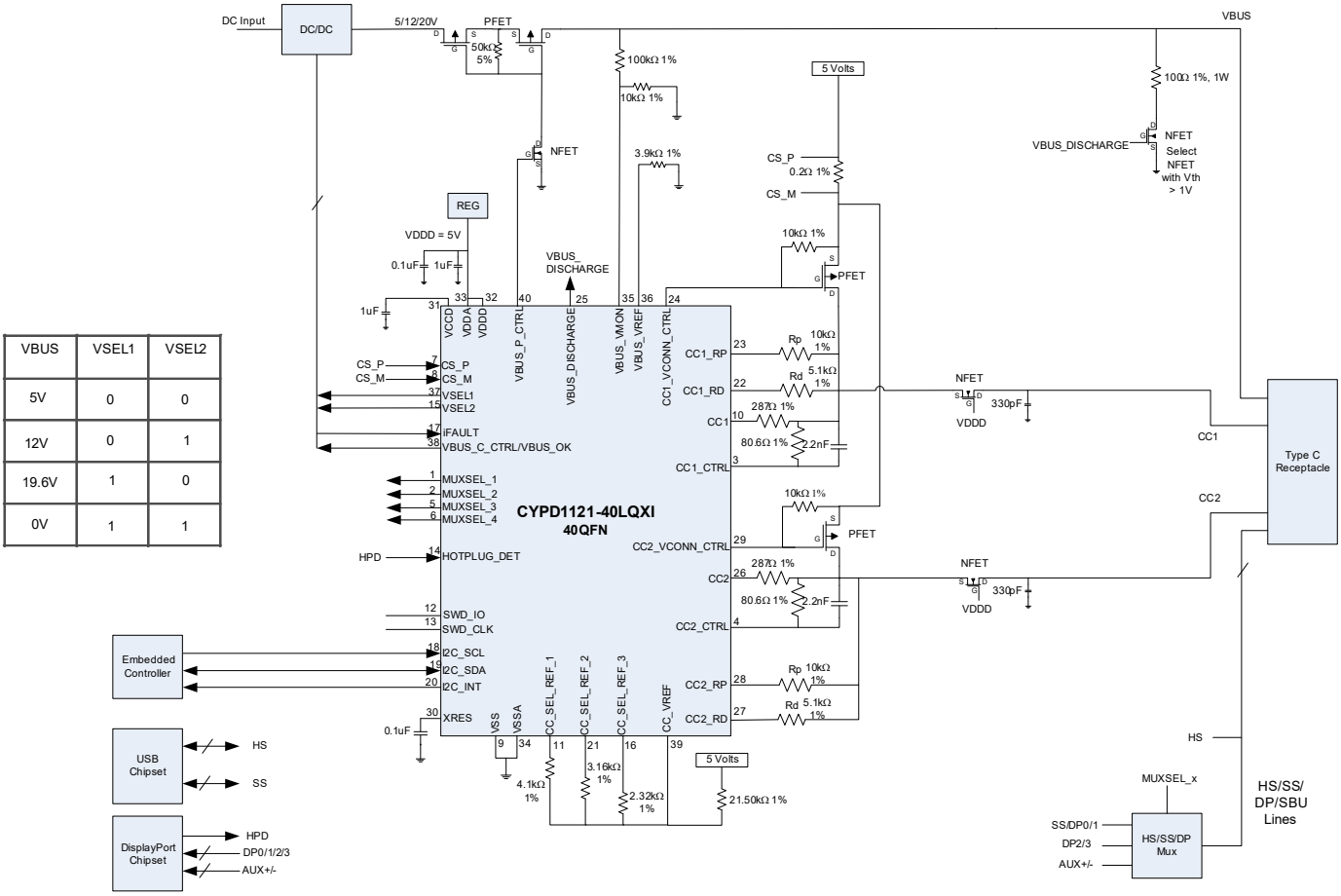


Figure 11. Monitor Application Block Diagram



VBUS	VSEL1	VSEL2
5V	0	0
12V	0	1
19.6V	1	0
0V	1	1

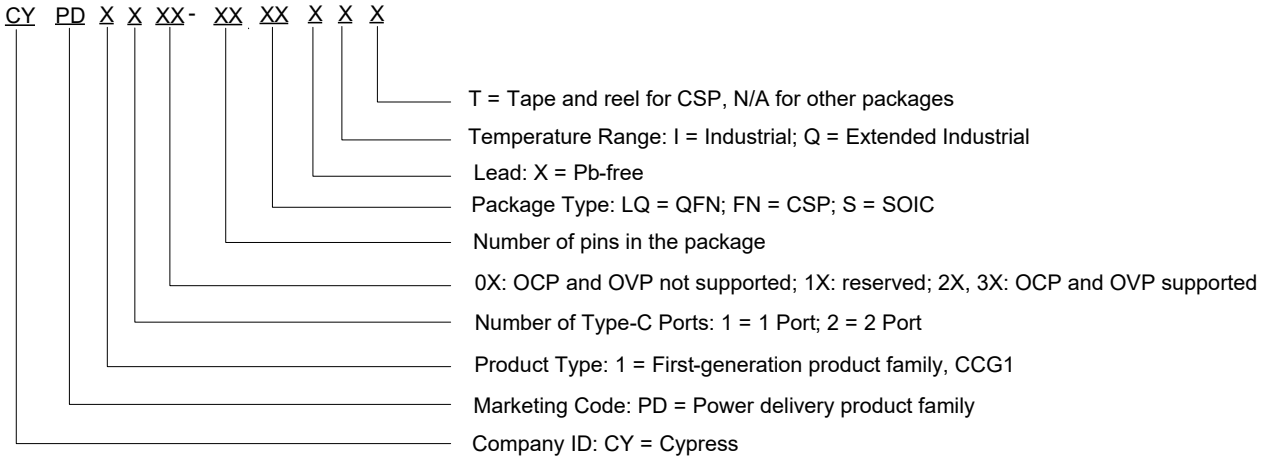
Ordering Information

The CCG1 part numbers and features are listed in the following table.

Table 23. CCG1 Ordering Information

Part Number[15]	Application	Type-C Ports[16]	Overcurrent Protection	Overvoltage Protection	Termination Resistor[17]	Role[18]	Package	Si ID
CYPD1103-35FNXIT	Cable, EMCA	1	No	No	R_a[19]	Cable	35-WLCSP[20]	0490
CYPD1131-35FNXIT	Notebook, Tablet, Smartphone	1	Yes	Yes	R_p[23], R_d[21]	DRP[24]	35-WLCSP[22]	0491
CYPD1121-40LQXI	Monitor	1	Yes	Yes	R_p[23], R_d[21]	DRP[24]	40-QFN	0489
CYPD1122-40LQXI	Notebook	1	Yes	Yes	R_p[23], R_d[21]	DRP[24]	40-QFN	048A
CYPD1134-40LQXI	Notebook, Desktop	1	Yes	Yes	R_p[23]	DFP	40-QFN	048B
CYPD1132-16SXI	Power Adapter	1	Yes	Yes	R_p[23]	DFP	16-SOIC	0498
CYPD1132-16SXQ	Power Adapter	1	Yes	Yes	R_p[23]	DFP	16-SOIC	0498

Ordering Code Definitions



Notes
15. All part numbers support: Input voltage range from 3.2 V to 5.5 V. Industrial parts support -40 °C to +85 °C, Extended Industrial parts support -40 °C to 105 °C.
16. Number of USB Type-C Ports supported .
17. Default V_{CONN} termination.
18. PD Role.
19. Type-C Cable Termination.
20. 35-WLCSP #1 pinout.
21. USB Device Termination.
22. 35-WLCSP #2 pinout.
23. USB Host Termination.
24. Dual Role Port.

Packaging

Table 24. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A (40-QFN, 35-CSP)	Operating ambient temperature	–	–40	25.00	85.00	°C
T_J (40-QFN, 35-CSP)	Operating junction temperature	–	–40	–	100.00	°C
T_A (16-SOIC)	Operating ambient temperature	–	–40	25.00	105.00	°C
T_J (16-SOIC)	Operating junction temperature	–	–40	–	120.00	°C
T_{JA}	Package θ_{JA} (40-pin QFN)	–	–	15.34	–	°C/Watt
T_{JA}	Package θ_{JA} (35-CSP)	–	–	28.00	–	°C/Watt
T_{JA}	Package θ_{JA} (16-SOIC)	–	–	85.00	–	°C/Watt
T_{JC}	Package θ_{JC} (40-pin QFN)	–	–	02.50	–	°C/Watt
T_{JC}	Package θ_{JC} (35-CSP)	–	–	00.40	–	°C/Watt
T_{JC}	Package θ_{JC} (16-SOIC)	–	–	49.00	–	°C/Watt

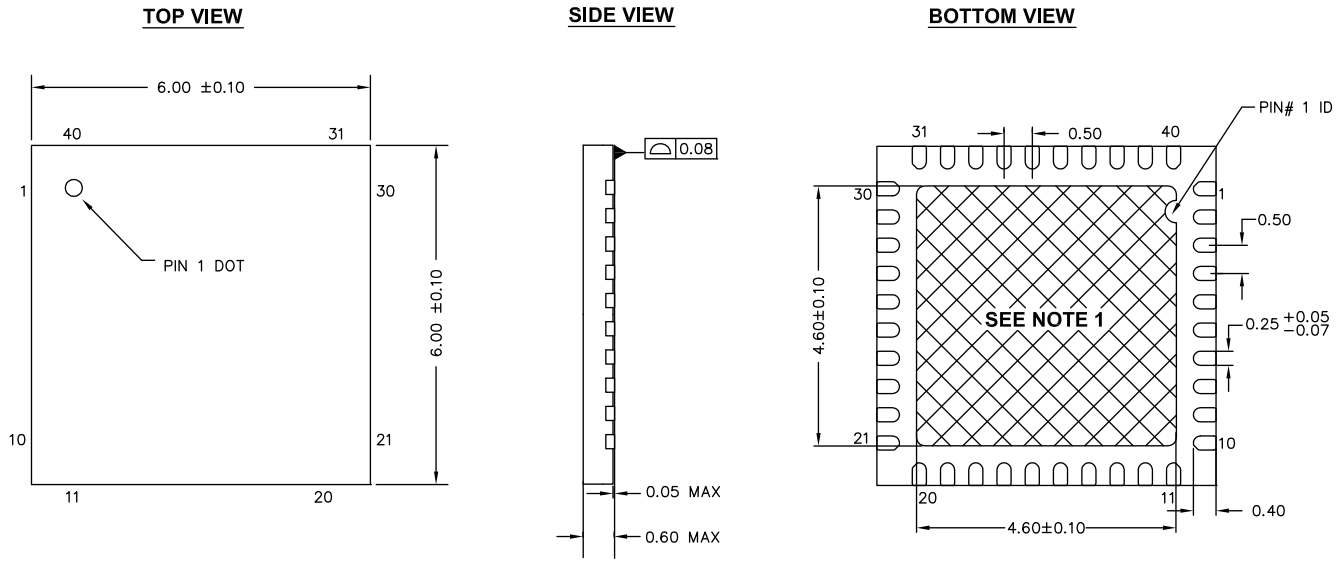
Table 25. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
16-pin SOIC	260 °C	30 seconds
40-pin QFN	260 °C	30 seconds
35-ball WLCSP	260 °C	30 seconds

Table 26. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
16-pin SOIC	MSL 3
40-pin QFN	MSL 3
35-ball WLCSP	MSL 1

Figure 12. 40-pin QFN Package Outline, 001-80659



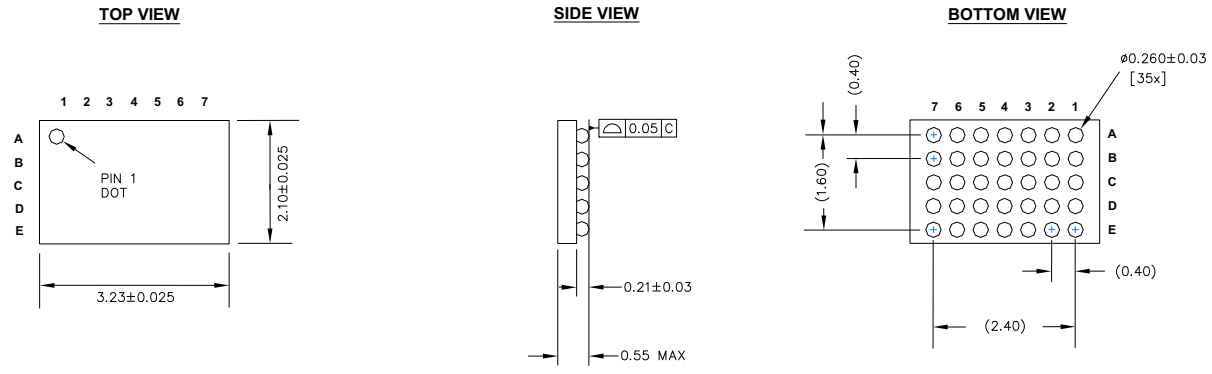
NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

Figure 13. 35-Ball WLCSP Package Outline, 001-93741

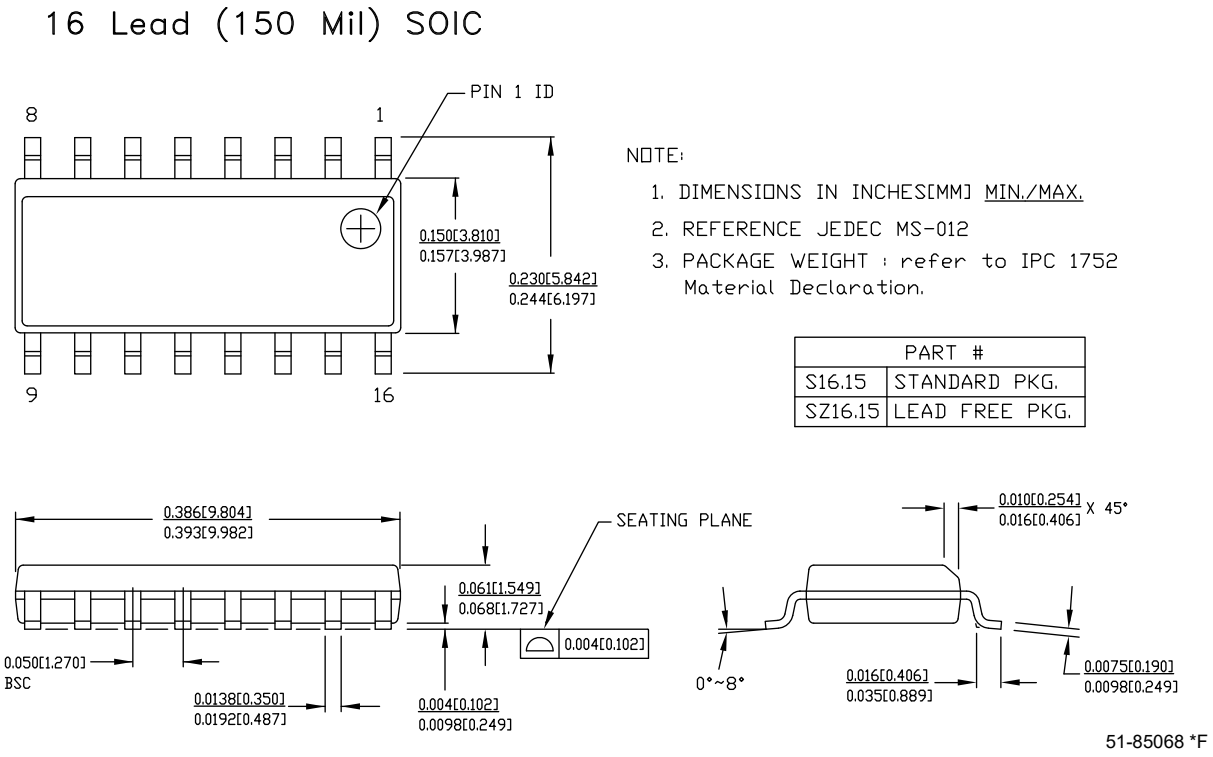


NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-93741 **

Figure 14. 16-pin SOIC (150 Mils) S16.15/SZ16.15 Package Outline, 51-85068



Acronyms

Table 27. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
CC	Configuration Channel
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	Current Sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO, DIO, SIO, USBIO
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller

Table 27. Acronyms Used in this Document *(continued)*

Acronym	Description
opamp	operational amplifier
OCP	Overcurrent protection
OVP	Overvoltage protection
PCB	printed circuit board
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UFP	upstream facing port
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 28. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision History

Description Title: CCG1 Datasheet USB Type-C Port Controller with Power Delivery Document Number: 001-93639			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	4520316	09/30/2014	New datasheet
*A	4531795	10/13/2014	Updated Functional Definition. Updated Figure 8, Figure , Figure 7, Figure , Figure 14, Figure 9. Added Figure 11. Updated Pinouts. Updated Power. Updated Figure , Figure 8. Updated Ordering Information Added Note 24 and referred the same note in 40-pin QFN corresponding to CYPD1122-40LQXI. Added Note 27 and referred the same note in 40-pin QFN corresponding to CYPD1134-40LQXI.
*B	4569912	11/21/2014	Updated Features. Added 16-pin SOIC related information. Updated Functional Definition. Updated Pin Definitions. Added Table 2. Updated Pinouts. Updated Figure 2, Figure 5. Added Figure 4. Updated Power. Updated Figure , Figure 8. Added Figure 6. Updated Electrical Specifications. Updated Device-Level Specifications. Updated Memory. Added Note 14 and referred the same note in F_{RET} parameter. Added details corresponding to spec ID SID182B under F_{RET} parameter. Updated Figure 14, Figure 9, Figure 11. Added Figure 8 and Figure 10. Updated Ordering Information. Updated part numbers. Added a column “Si ID”. Updated Packaging. Updated Table 24. Updated details in maximum value column corresponding to T_A and T_J parameters. Added 16-pin SOIC related information. Updated Table 25.
*C	4596141	12/14/2014	Updated Figure 6, Figure 14, Figure 16. Updated Table 8, Table 23.
*D	4646123	02/04/2015	Updated pin definitions for 40-pin QFN and 35-ball WLCSP. Updated Pinout for CYPD1122-40LQXI/CYPD1121-40LQXI and Ordering Information. Updated conditions for Device-Level Specifications. Updated diagrams in Applications in Detail section.
*E	4686050	03/13/2015	Removed information about 28-pin SSOP. Updated Table 3, Table 23, Table 24, Table 25, Table 26, Table 27. Updated Figure 2, Figure .
*F	4747272	05/13//2015	Updated General Description. Added Note 1 and referenced it in Features. Updated Figure 6, Figure 8 through Figure 11. Removed Figure 9. Single Chip/Cable, Component Count = 13. Removed Figure 11. Two Chip/Cable, Component Count = 11/paddle.

Revision History *(continued)*

Description Title: CCG1 Datasheet USB Type-C Port Controller with Power Delivery Document Number: 001-93639			
Revision	**ECN**	**Submission Date**	**Description of Change**
*G	4800534	07/02/2015	Updated Low-Power Operation. Updated the number of GPIOs to “up to 30” in GPIO. Updated “1.8 to 5.5 V” to “3.2 V to 5.5 V” in Low-Power Operation, Power System, Power, Device-Level Specifications and Note 15. Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 14 and Table 18. Added table footnotes 8, 9 and 10. Deleted footnotes 25 through 28. Updated Figure 2 and Figure 8 through Figure 11. Added Figure 3. Updated the following in Power: Removed Figures 5 through 8. Updated the section.
*H	4939764	09/29/2015	Removed specs SID241 and 242. Updated 40-pin QFN package to current revision.
*I	5179365	03/17/2016	Updated max value of I_{I2C1} from 10.50 µA to 50 µA. Updated copyright information and sales links at the end of the document.
*J	5459633	10/03/2016	Added compliance information regarding the USB Specification. Updated copyright notice to include WICED. Added IoT link in Sales, Solutions, and Legal Information.
*K	5725038	05/03/2017	Updated Cypress logo. Updated Copyright information.
*L	7036611	12/03/2020	Updated General Description: Added “THIS PRODUCT IS NOT RECOMMENDED FOR NEW DESIGNS” on page 1. Updated Figure 14 in Packaging (spec 51-85068 *E to *F).

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

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