Development Board EPC90142 Quick Start Guide

100 V Half-bridge with Gate Drive, Using EPC23101 and EPC2302

Revision 1.0

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC90142 development board is a 100 V maximum device voltage, 65 A maximum output current, half bridge featuring the EPC23101 Integrated ePower™ FET and EPC2302 eGaN®FET. The purpose of this development board is to simplify the evaluation process of the EPC23101 by including all the critical components on a single board that can be easily connected into the majority of existing converter topologies.

The EPC90142 development board measures 2" x 2" and contains one EPC23101 Integrated ePower™ FET in a half bridge configuration. The board also contains all critical components and the layout supports optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A block diagram of the circuit is given in figure 1.

For more information on the FETs associated with this board, please refer to their datasheets available on EPC's website: EPC23101 and EPC2302. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (T_A = 25°C) EPC90142

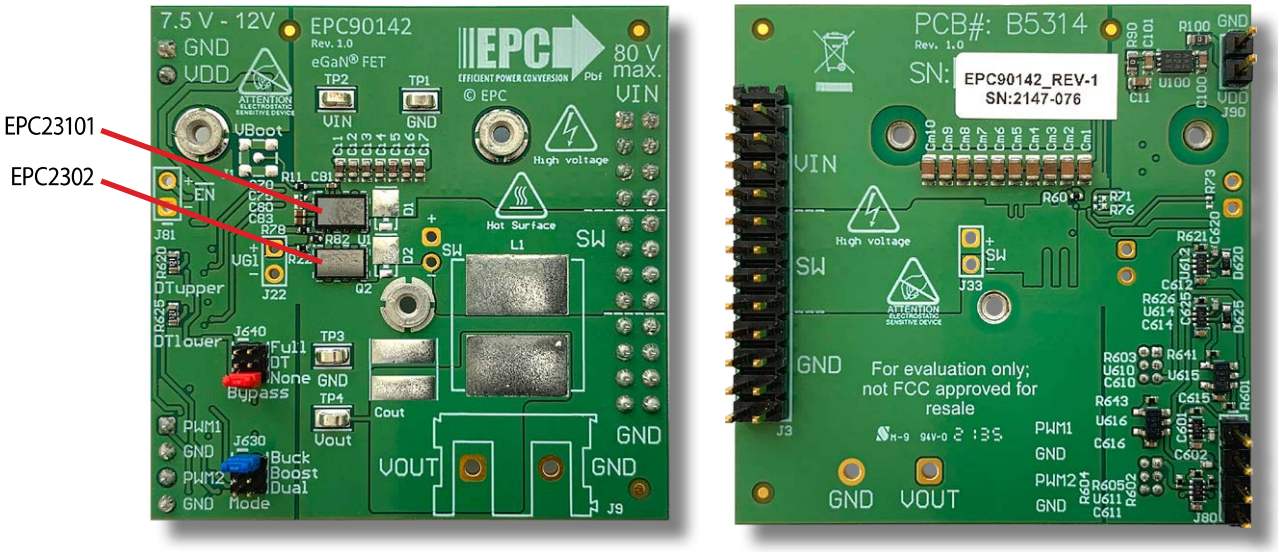
Symbol	Parameter	Conditions	Min	Nominal	Max	Units
V_{DD}	Gate Drive Input Supply Range		7.5		12	V
V_{IN}	Bus Input Voltage Range(1)				80	V
I_{OUT}	Switch Node Output Current (2)				65	A
V_{PWM}	PWM Logic Input Voltage Threshold (3)	Input 'High' Input 'Low'	3.5 0		5.5 1.5	V V
	Minimum 'High' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	50			ns
	Minimum 'Low' State Input Pulse Width (4)	V_{PWM} rise and fall time < 10ns	200			ns

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 100 V for EPC23101.

(2) Maximum current depends on die temperature – actual maximum current is affected by switching frequency, bus voltage and thermal cooling.

(3) When using the on board logic buffers, refer to the EPC23101 datasheet when bypassing the logic buffers.

(4) Limited by time needed to 'refresh' high side bootstrap supply voltage.



Front view Back view

EPC90142 development board

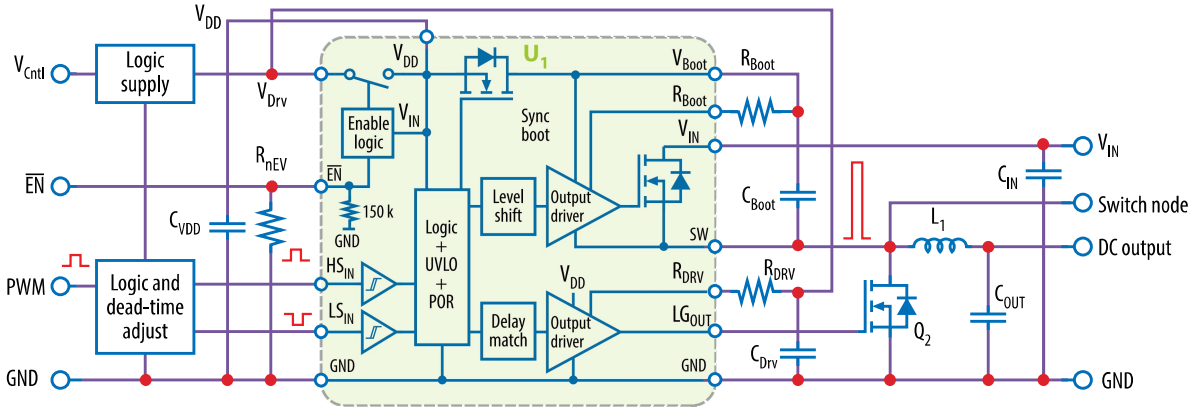


Figure 1: Block diagram of EPC90142 development board

QUICK START PROCEDURE

The EPC90142 development board is easy to set up as a buck or boost converter to evaluate the performance of the two EPC23101 ePower™ FET. This board includes a logic PWM input signal polarity changer used to ensure positive PWM polarity for the switching device when configured in either the buck or boost modes, and can accommodate both single and dual PWM inputs. Furthermore, the board includes a dead-time generating circuit that adds a delay from when the gate signal of one FET is commanded to turn off, to when the gate signal of the other FET is commanded to turn on. In the default configuration, this dead time circuit ensures that both the high and low side FETs will not be turned on at the same time thus preventing a shoot-through condition. The dead-time and/or polarity changing circuits can be utilized or bypassed for added versatility.

Single/dual PWM signal input settings

There are two PWM signal input ports on the board, PWM1 and PWM2. Both input ports are used as inputs in dual-input mode where PWM1 connects to the upper FET and PWM2 connects to the lower FET. The PWM1 input port is used as the input in single-input mode where the circuit will generate the required complementary PWM for the FETs. The input mode is set by choosing the appropriate jumper positions for J630 (mode selection) as shown in figure 2(a) for a single-input buck converter (**blue** jumper across pins 1 & 2 of J630), (b) for a single-input boost converter (**blue** jumpers across pins 3 & 4 of J630), and (c) for a dual-input operation (**blue** jumpers across pins 5 & 6 of J630).

Note: In dual mode there is no shoot-through protection as both gate signals can be set high at the same time.

Dead-time settings

Dead-time is defined as the time between when one FET turns off and the other FET turns on, and for this board is referenced to the input of the gate driver. The dead-time can be set to a specific value where resistor R620 delays the turn on of the upper FET and resistor R625 delays the turn on of the lower FET as illustrated in figure 3.

The required resistance for the desired dead-time setting can be read off the graph in figure 4. An example for 10 ns dead-time setting shows that a 120 Ω resistor is needed.

Note: This is the default deadtime and resistor value installed. A minimum dead-time of is 5 ns and maximum of 15 ns is recommended.

Bypass settings

Both the polarity changer and the deadtime circuits can be bypassed using the jumper settings on J640 (Bypass), for direct access to the gate driver input. There are three bypass options: 1) No bypass, 2) Dead-time bypass, 3) Full bypass. The jumper positions for J640 for all three bypass options are shown in figure 5.

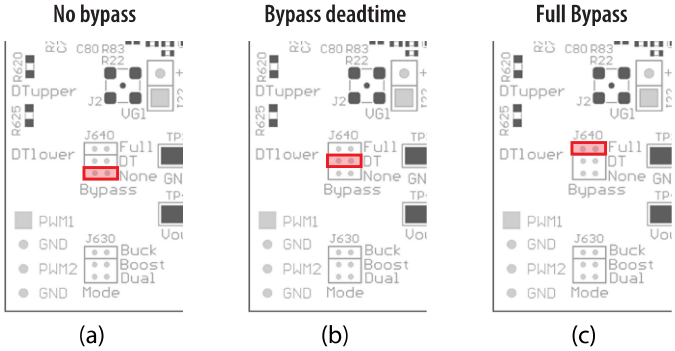


Figure 5: Bypass mode Jumper settings for J640

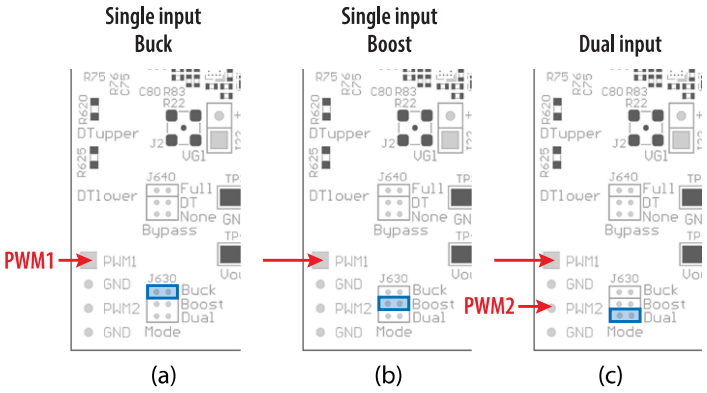


Figure 2: Input mode selection on J630

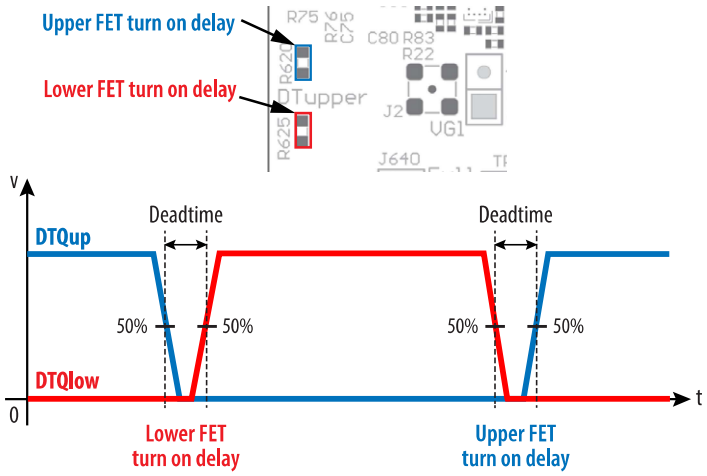


Figure 3: Definition of dead-time between the upper-FET gate signal (DTQup) and the lower-FET gate signal (DTQlow)



Figure 4: The required resistance values for R620 or R625 as a function of desired dead-time

In ***no-bypass mode***, figure 5(a) (**red** jumper across pins 5 & 6 of J640), both the on-board polarity and dead-time circuits are fully utilized. In ***dead-time bypass mode***, figure 5(b) (**red** jumpers across pins 3 & 4 of J640), only the on-board polarity changer circuit is utilized, effectively bypassing the dead-time circuit. In ***full bypass mode***, Figure 5(c) (**red** jumper across pins 1 & 2 of J640), the inputs to the gate driver are directly connected to the PWM1 and PWM2 pins and the on-board polarity and dead-time circuits are not utilized.

Bypass mode warnings

- ***It is important to provide the correct PWM signals that includes dead-time and polarity for either buck or boost operation when making use of bypass modes.***
- When operating in ***full bypass mode***, the input signal specifications revert to that of the EPC23101. Refer to the EPC23101 datasheet for details.

Buck converter configuration

To operate the board as a buck converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select ***Single Input Buck Mode***, the bypass jumper J640 ***must*** be set to the ***no-bypass mode***, the ***buck mode*** J630 ***must*** be selected as shown in figure 6(a).

To select ***Dual Input Buck Mode***, the bypass jumper J640 ***may*** be configured to any of the valid settings, the dual-input mode J630 ***must*** be selected as shown in figure 6(b).

Note: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in bypass mode.

Once the input source, dead-time settings and bypass configurations have be chosen and set, then the boards can be operated.

1. With power off, connect the input power supply bus to VIN and ground / return to GND.
2. With power off, connect the switch node (SW) of the half bridge to your circuit as required (half bridge configuration). Or use the provided pads for inductor (L1) and output capacitors (Cout), as shown in figure 6.
3. With power off, connect the gate drive supply to VDD (J1, Pin-1) and ground return to GND (J1, Pin-2 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J2 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is set between 7.5 V and 12 V.
6. Turn on the controller / PWM input source.
7. Making sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the required value (***do not exceed the absolute maximum voltage***). Probe switch-node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters.
9. For shutdown, please follow steps in reverse.

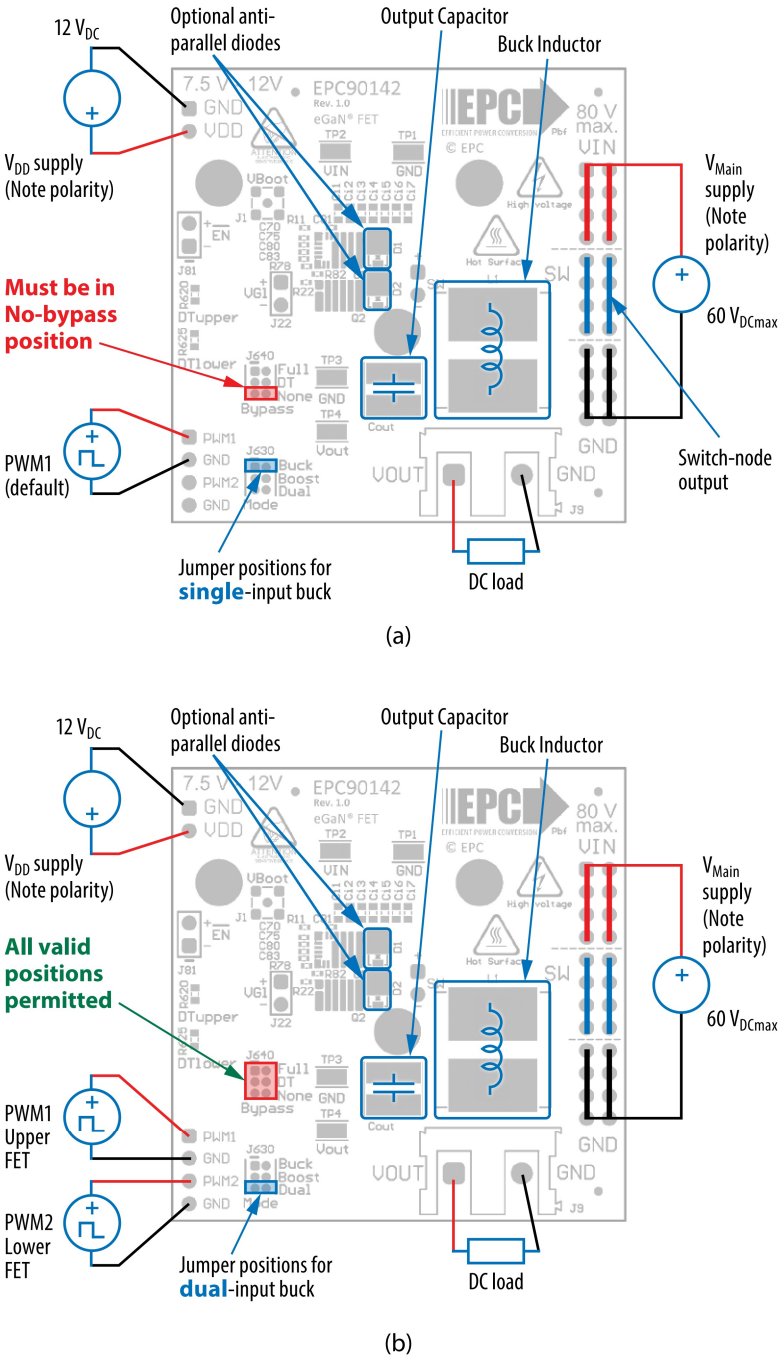


Figure 6: (a) Single-PWM input buck converter (b) Dual-PWM input buck converter configurations showing the supply, anti-parallel diodes, output capacitor, inductor, PWM, and load connections with corresponding jumper positions.

Boost Converter configuration

Warning: Never operate the boost converter mode without a load, as the output voltage can increase beyond the maximum ratings.

To operate the board as a boost converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select ***Single Input Boost Mode***, the bypass jumper J640 ***must*** be set to the ***no-bypass mode***, the boost mode J630 ***must*** be selected as shown in figure.7(a).

To select ***Dual Input Boost Mode***, the bypass jumper J640 ***may*** be configured to any of the valid settings, the ***dual-input mode*** J630 ***must*** be selected as shown in figure 7(b).

Note: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in bypass mode.

Once the input source, dead-time settings and bypass configurations have be chosen and set, then the boards can be operated.

1. The inductor (L1) and input capacitors (labeled as Cout) can either be soldered onto the board, as shown in figure 7, or provided off board. Anti-parallel diodes can also be installed using the additional pads on the right side of the EPC23101 FETs.
2. With power off, connect the input power supply bus to V_{OUT} and ground / return to GND, or externally across the capacitor if the inductor L1 and Cout are provided externally. Connect the output voltage (labeled as VIN) to your circuit as required, e.g., resistive load.
3. With power off, connect the gate drive supply to VDD (J1, Pin-1) and ground return to GND (J1, Pin-2 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J2 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is between 7.5 V and 12 V.
6. Turn on the controller / PWM input source.
7. Making sure the output is not open circuit, and the input supply voltage is initially 0 V, turn on the power and slowly increase the voltage to the required value (*do not exceed the absolute maximum voltage*). Probe switch-node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters. Observe device temperature for operational limits.
9. For shutdown, please follow steps in reverse.

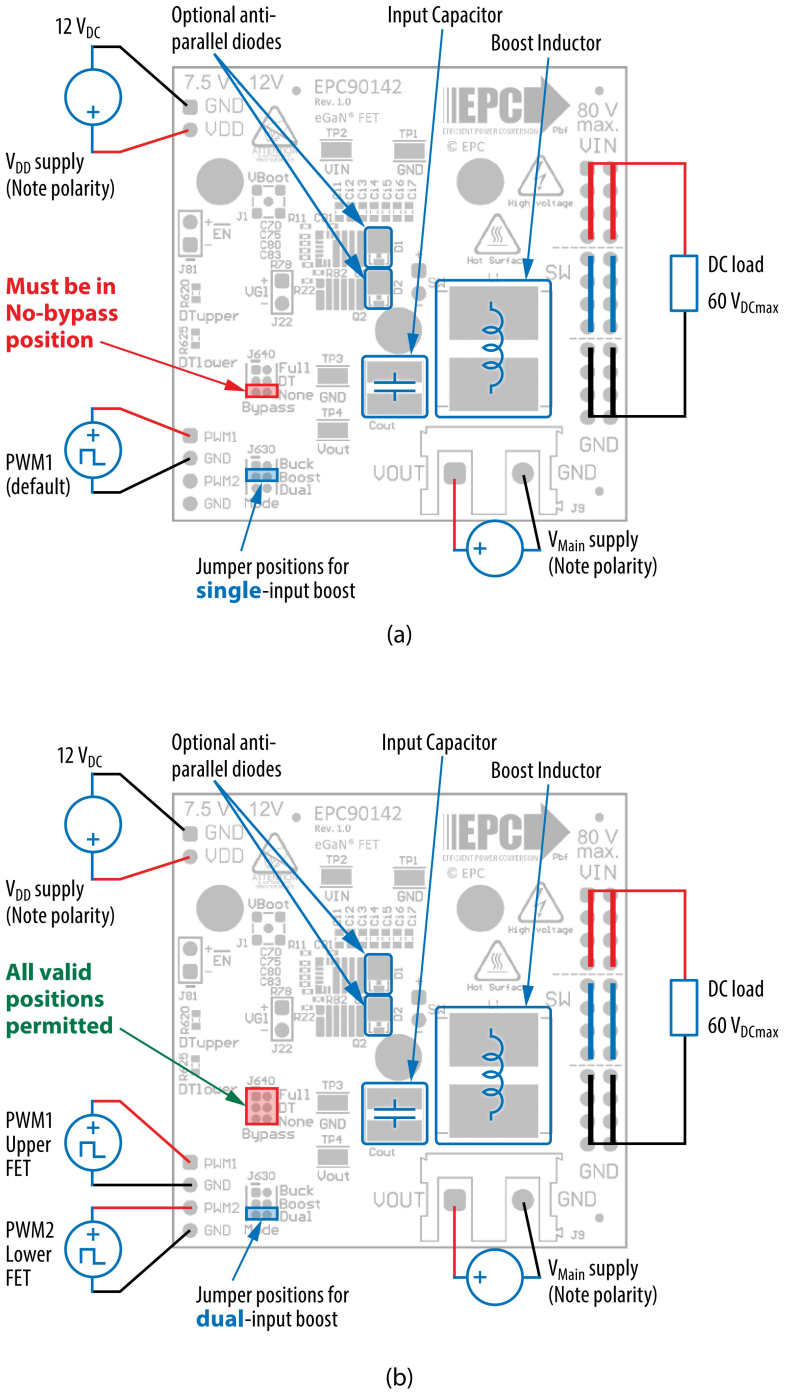


Figure 7: (a) Single-PWM input boost converter (b) Dual-PWM input boost converter configurations showing the supply, inductor, anti-parallel diodes, input capacitor, PWM, and load connections with corresponding jumper settings.

MEASUREMENT CONSIDERATIONS

Measurement connections are shown in figure 8. When measuring the switch node voltage containing high-frequency content, care must be taken to provide an accurate high-speed measurement. An optional two pin header (J33) is provided for switch-node measurement.

Differential probe is recommended for measuring the high-side bootstrap voltage (J1). IsoVu probes from Tektronix has mating MMCX connector.

For regular passive voltage probes (e.g. TPP1000) measuring switch node using MMCX connector, probe adaptor is available. PN: 206-0663-xx

NOTE. For information about measurement techniques, the EPC website offers: "AN023 Accurately Measuring High Speed GaN Transistors" and the How to GaN educational video series, including: HTG09-Measurement

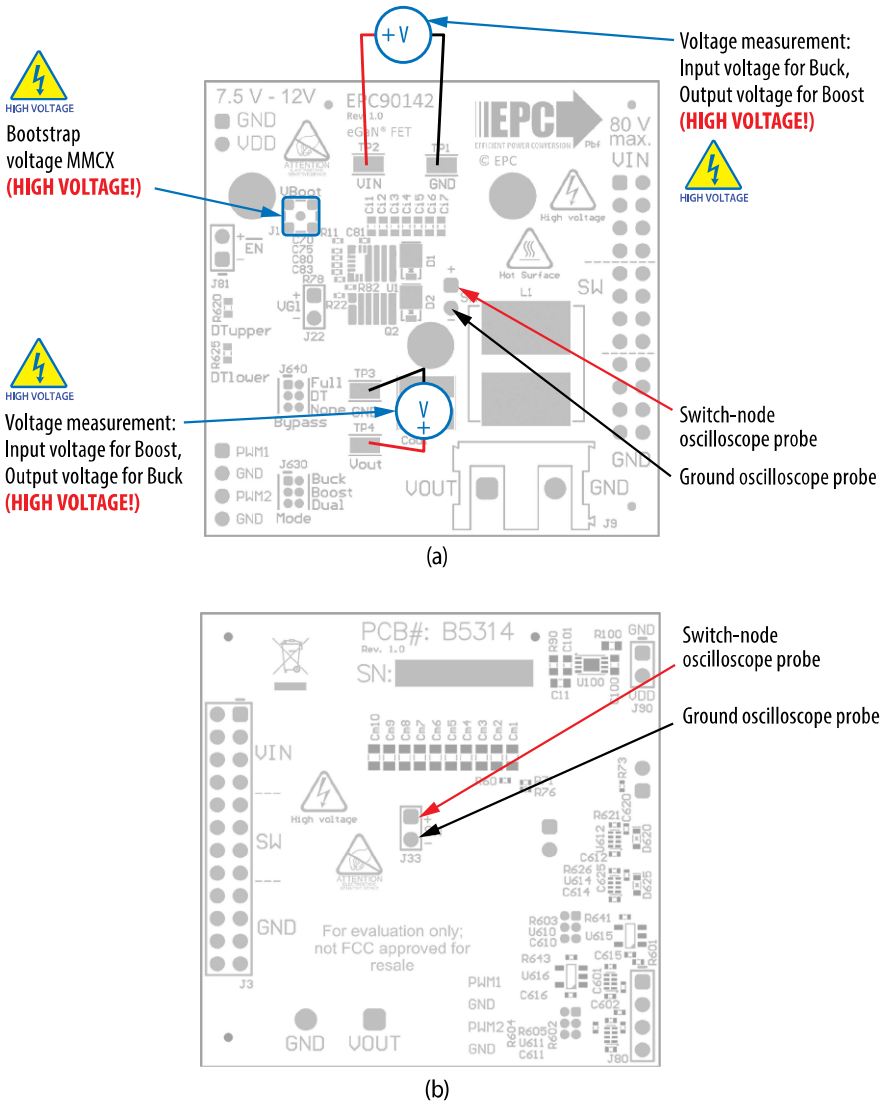
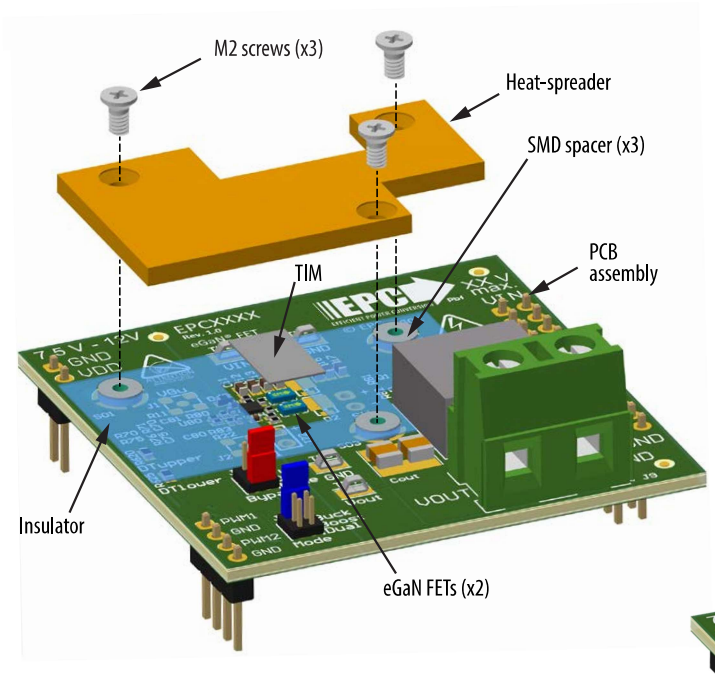


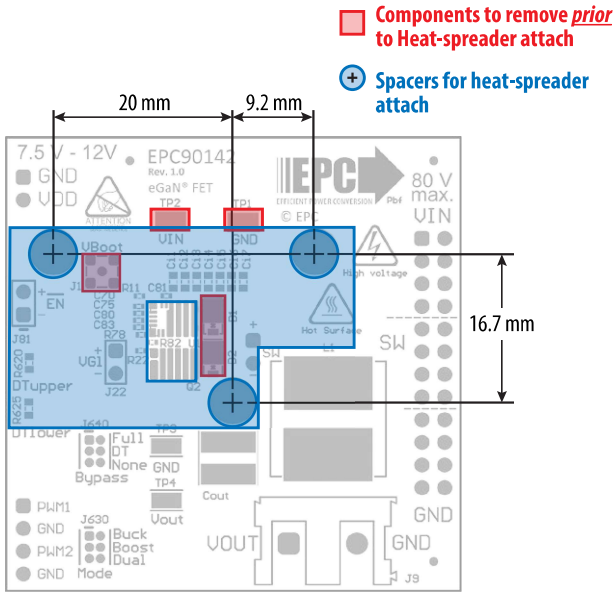
Figure 8: Measurement points (a) front side, (b) Back side

THERMAL CONSIDERATIONS

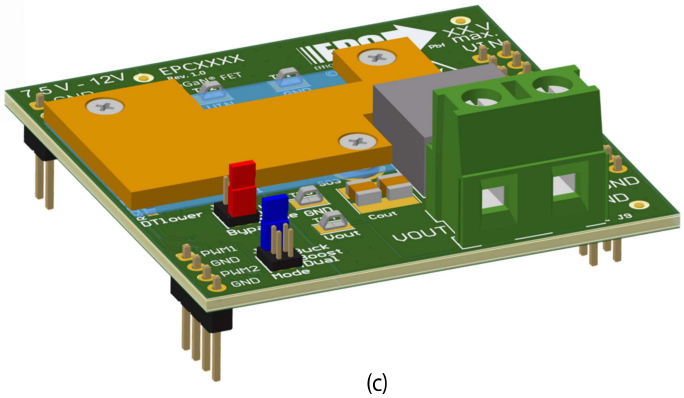
The EPC90142 board is equipped with three mechanical spacers that can be used to easily attach a heat-spreader or heatsink as shown in figure 9(a), and only requires a thermal interface material (TIM), a custom shape heat-spreader/ heatsink, and screws. Prior to attaching a heat-spreader, any component exceeding 1 mm in thickness under the heat-spreader area will need to be removed from the board as shown in figure 9 (b).



(a)



(b)



(c)

Figure 9: Details for attaching a heatsink to the development board. (a) 3D perspective, (b) top view details, (c) Assembled view with heat-spreader attached.

The design of the heat-spreader is shown in figure 10 and can be made using **aluminum** or **tellurium copper** for higher performance.

The heat-spreader is held in place using countersunk screws that fasten to the mechanical spacers which will accept M2 x 0.4 mm thread screws such as McMasterCarr 91294A002.

When assembling the heatsink, it may be necessary to add a thin insulation layer to prevent the heat-spreader from short circuiting with components that have exposed conductors such as capacitors and resistors, as shown in figure 11. ***Note that the heat-spreader is ground connected by the lower most mounting post***. A rectangular opening in the insulator must be provided to allow the TIM to be placed over the FETs to be cooled with a minimum clearance of 1 mm on each side of the rectangle encompassing the FETs. The TIM will then be similar in size or slightly smaller than the opening in the insulator shown by the red dashed outline in figure 11.

EPC recommends Laird P/N: A14692-30, Tgard™ K52 with thickness of 0.051 mm the for the insulating material.

A TIM is added to improve the interface thermal conductance between the FETs and the attached heat exchanger. The choice of TIM needs to consider the following characteristics:

- **Mechanical compliance** – During the attachment of the heat spreader, the TIM underneath is compressed from its original thickness to the vertical gap distance between the spacers and the FETs. This volume compression exerts a force on the FETs. A maximum compression of 2:1 is recommended for maximum thermal performance and to constrain the mechanical force which maximizes thermal mechanical reliability.
- **Electrical insulation** – The backside of the eGaN FET is a silicon substrate that is connected to source and thus the upper FET in a half-bridge configuration is connected to the switch-node. To prevent short-circuiting the switch-node to the grounded thermal solution, the TIM must be of high dielectric strength to provide adequate electrical insulation in addition to its thermal properties.
- **Thermal performance** – The choice of thermal interface material will affect the thermal performance of the thermal solution. Higher thermal conductivity materials is preferred to provide higher thermal conductance at the interface.

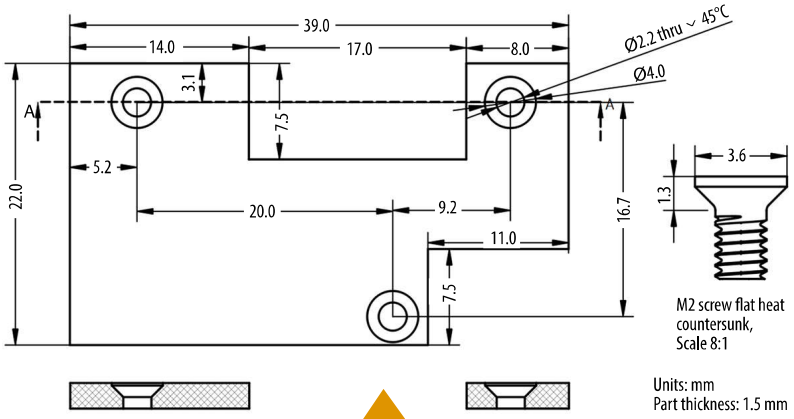
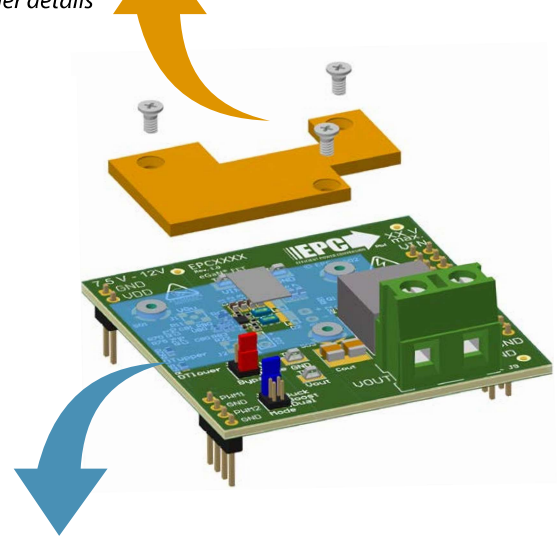


Figure 10: Heat-spreader details



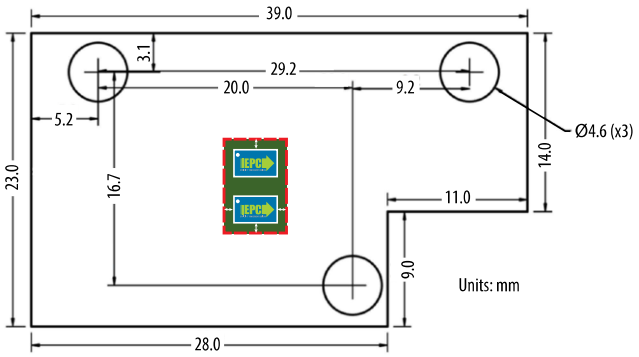


Figure 11: Insulator sheet details with opening for the TIM with location of the FETs

EPC recommends the following thermal interface materials:

- **t-Global** P/N: TG-A1780 X 0.5 mm (highest conductivity of 17.8 W/m·K)
- **t-Global** P/N: TG-A6200 X 0.5 mm (moderate conductivity of 6.2 W/m·K)
- **Bergquist** P/N: GP5000-0.02 (~0.5 mm with conductivity of 5 W/m·K)
- **Bergquist** P/N: GPTGP7000ULM-0.020 (conductivity of 7 W/m·K)

NOTE. The EPC90142 development board does not have any current or thermal protection on board. For more information regarding the thermal performance of EPC eGaN FETs, please consult:
D. Reusch and J. Glaser, ***DC-DC Converter Handbook, a supplement to GaN Transistors for Efficient Power Conversion,*** First Edition, Power Conversion Publications, 2015.

EXPERIMENTAL VALIDATION

The performance of EPC90142 was tested under the operating conditions given in table 2 unless otherwise specified.

A heat-spreader per figures 10 and 11 with t-Global TG-A1780 thermal interface material (TIM) and a heatsink from Wakefield Vette 567-24AB using the same TIM was added to the board prior to testing at high current.

Additional input and output capacitance are added to suppress input and output voltage ripple at high output current as shown in Table 2.

Table 2: Test conditions

Parameter	Max	Units
Regulated Input voltage	48	V
Regulated Output voltage	12	V
Switching frequency (f_S)	500 750 1000	kHz
Inductor (mounted on motherboard)	2.2	µH[1]
Additional Input capacitance (min.)	244	µF[2]
Additional Output capacitance (min.)	70.5	µF[3]
Maximum case temperature	110	°C
Dead time	10	ns
R_{boot} (R60)	2.2	Ω

[1] 2.2 µH inductor from Vishay, P/N IHTH1125KZEB2R2M5A.
[2] Capacitors used:
10 µF, 100 V, x15 (P/N: GRM32EC72A106KE05L),
47 µF, 80 V, x2 (P/N: 80SXV47M)
[3] Capacitors used:
4.7 µF, 100 V, x5 (P/N: GMC32X7R475K100NT)
47 µF, 80 V, x1 (P/N: 80SXV47M)

ELECTRICAL PERFORMANCE

Measure Waveforms

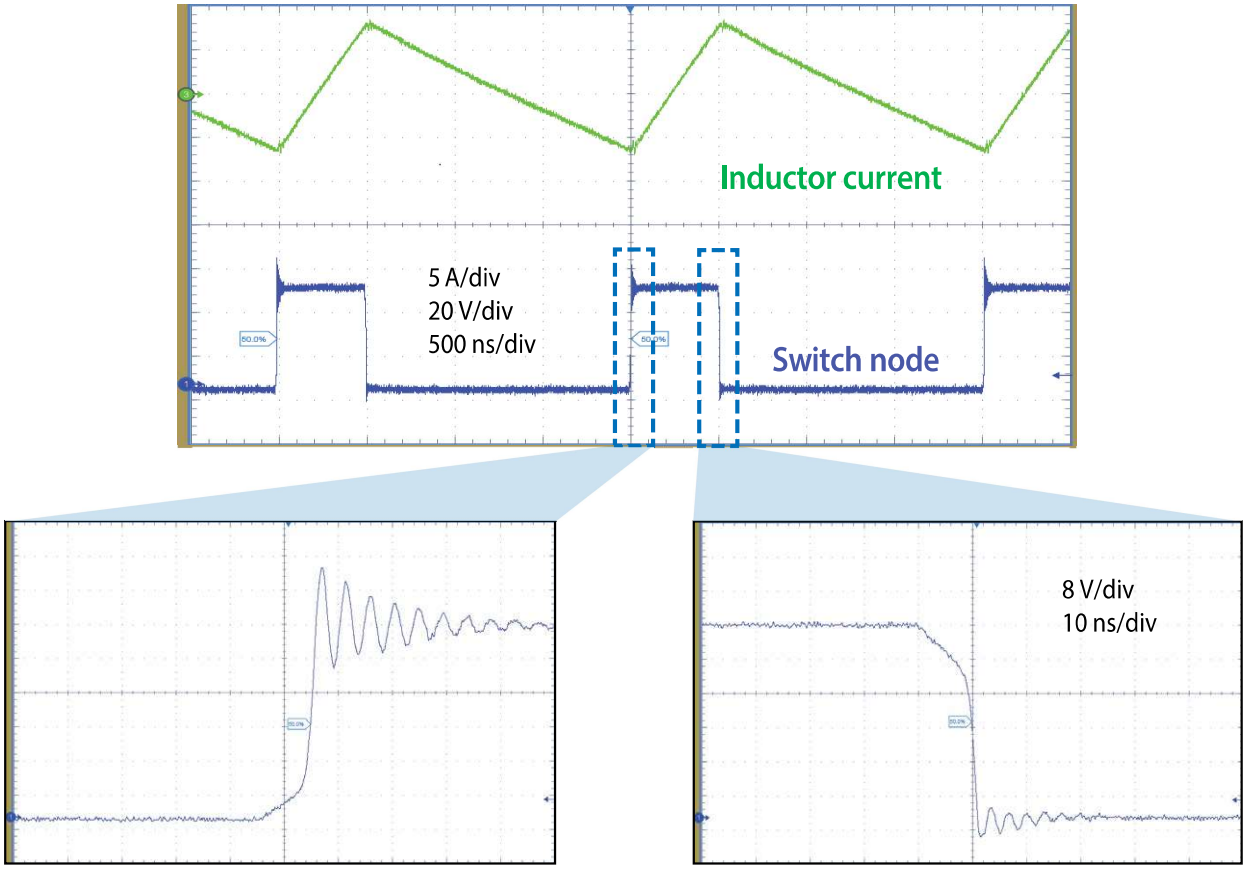


Figure 12: Measured inductor current and switch node waveforms when operating from 48 V at 500 kHz and delivering 0 A into a 12 V load

Measure Waveforms *(continued0*

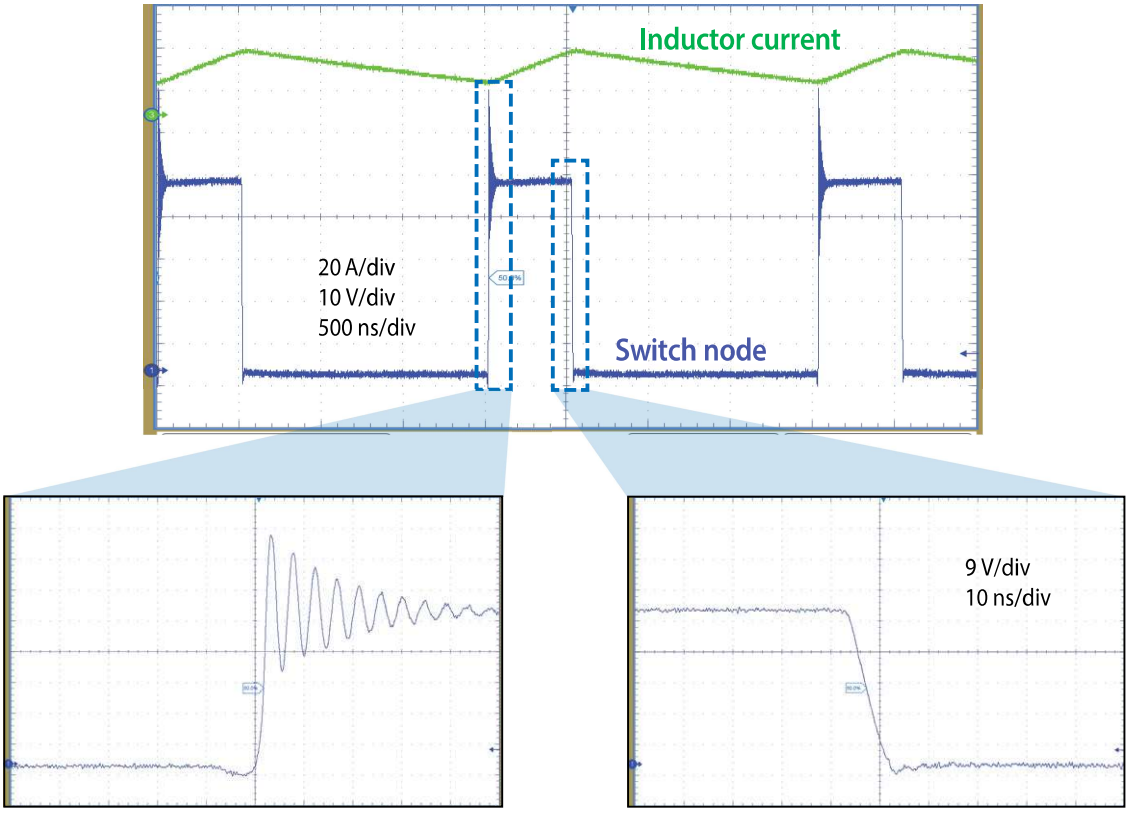


Figure 13: Measured inductor current and switch node waveforms when operating from 48 V at 500 kHz and delivering 10 A into a 12 V load

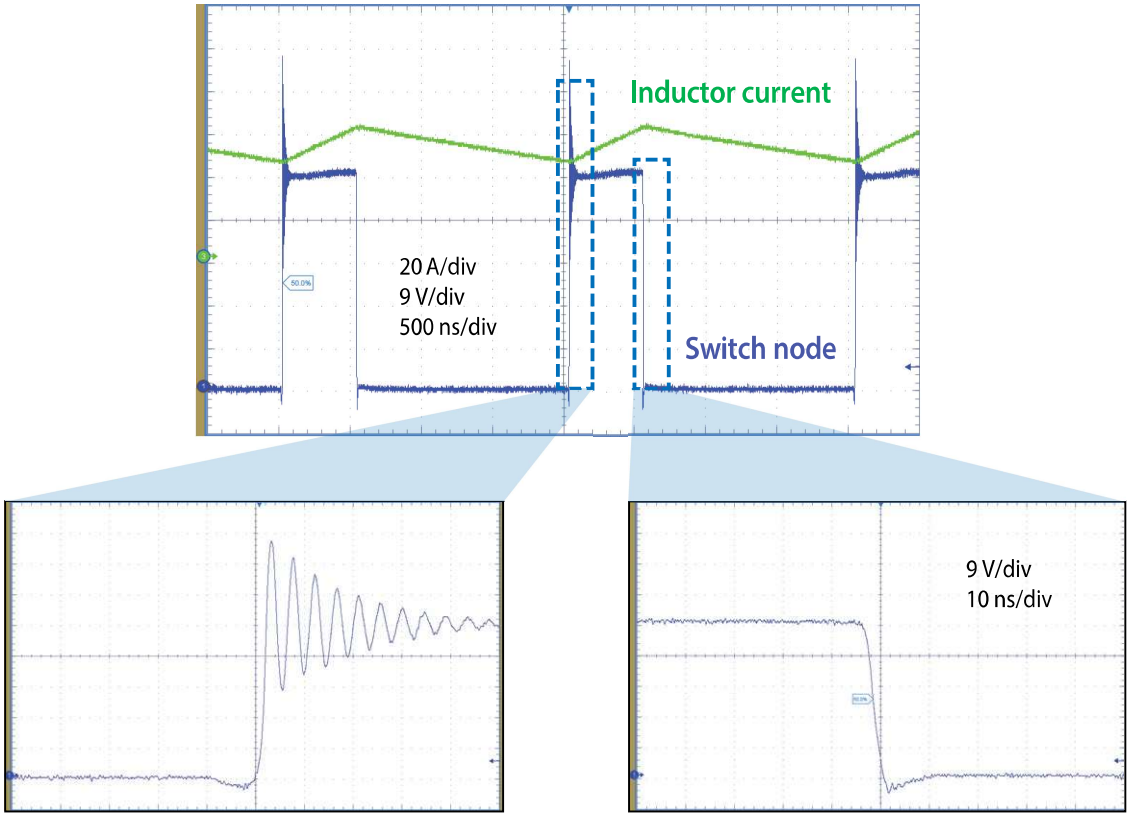


Figure 14: Measured inductor current and switch node waveforms when operating from 48 V at 500 kHz and delivering 25 A into a 12 V load

EFFICIENCY and POWER LOSSES

Figure 15 shows the efficiency and power loss results when operating from 48 V to 12 V at various switching frequencies using a 2.2 µH inductor.

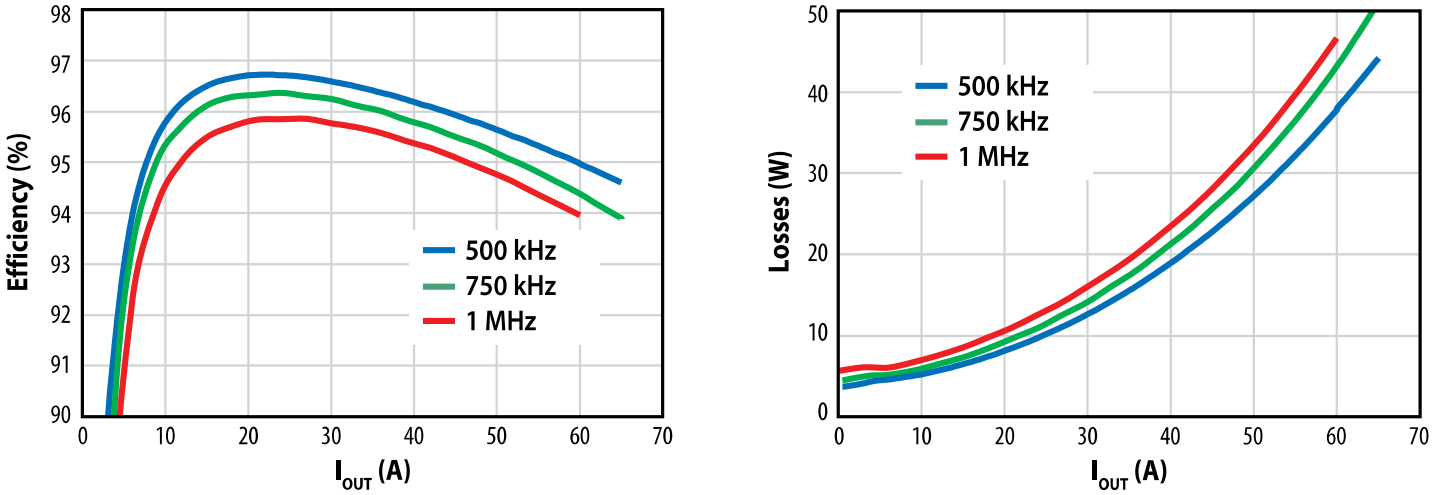


Figure 15: Measured efficiency and power loss operating at at various switching frequencies and using L = 2.2 µH

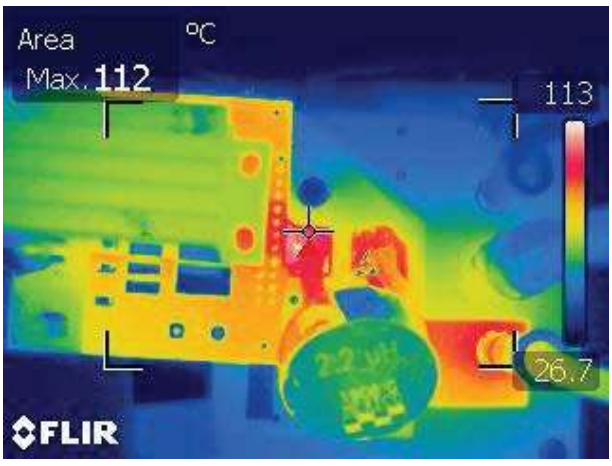
Table 3: Measured I_{DD} current (V_{DD} = 5 V) (5)

Setting\Condition	f_{SW} = 500 kHz	f_{SW} = 1 MHz
Enabled (nEN = low, V_{IN} = 48 V)	40 mA	58 mA
Disabled (nEN = high)	3.6 mA	5.1 mA

(5) Includes current consumption from dead-time logic circuit.

THERMAL PERFORMANCE

Figure 16 through 18 shows the thermal performance of the board fitted with a heatsink and heat-spreader when operating at 48 V delivering 12 V into the load with 1000-1500 LFM (high) airflow.



PCB with heatsink and heat-spreader

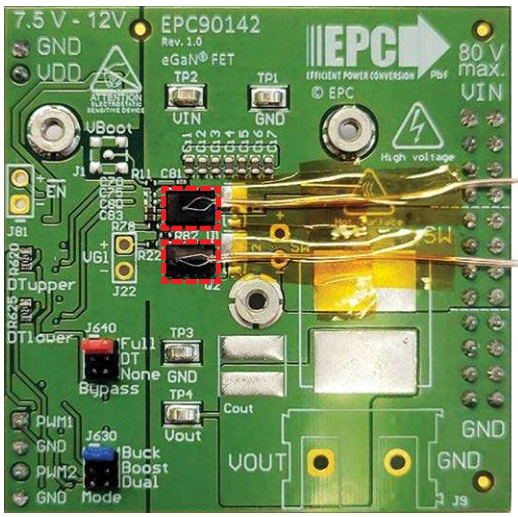
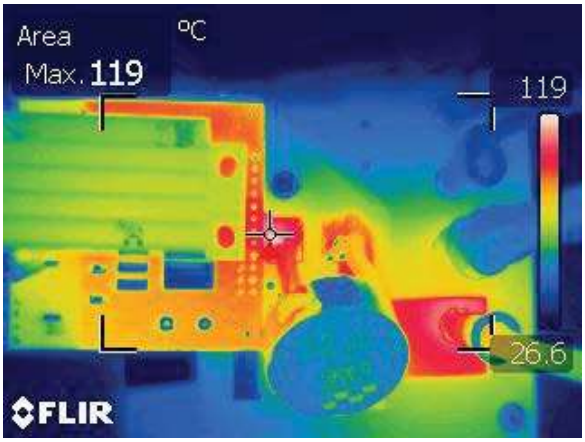


Figure 16: Measured thermal image and thermal couple readings of case temperature when operating under the following conditions: f_S = 500 kHz, I_{OUT} = 65 A output, 25°C ambient and high air flow



PCB with heatsink and heat-spreader

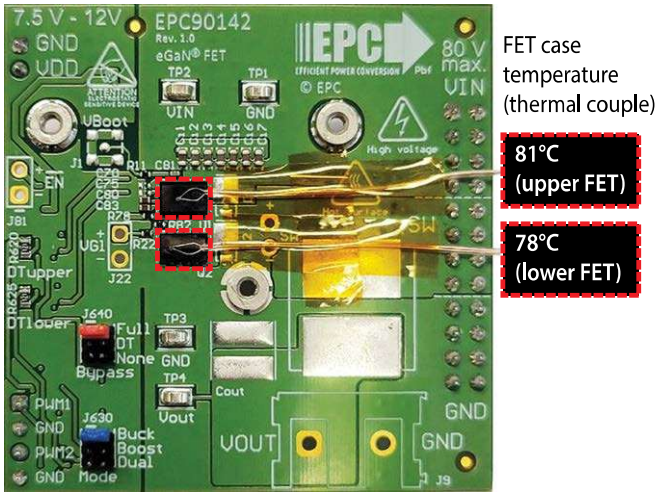
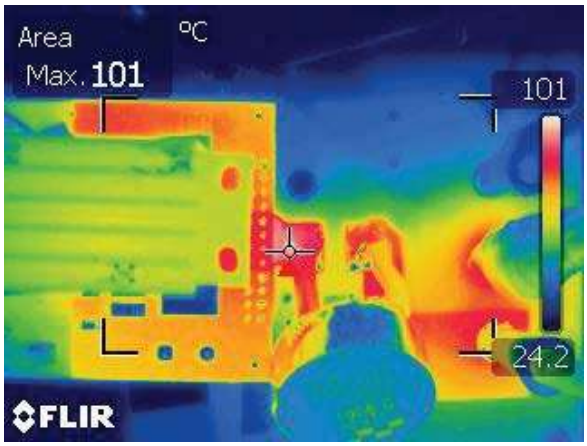


Figure 17: Measured thermal image and thermal couple readings of case temperature when operating under the following conditions: f_S = 750 kHz, I_{OUT} = 65 A output, 25°C ambient and high air flow



PCB with heatsink and heat-spreader

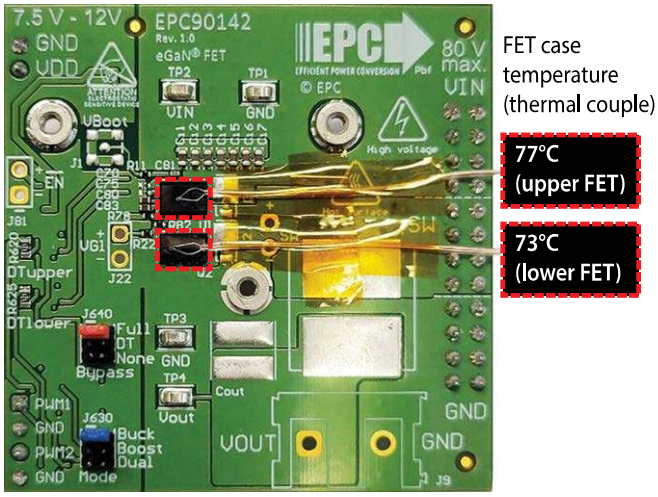


Figure 18: Measured thermal image and thermal couple readings of case temperature when operating under the following conditions: f_S = 1 MHz, I_{OUT} = 60 A output, 25°C ambient and high air flow

THERMAL DERATING

Using the thermal setup for the board, additional testing at 400 LFM and 1000 LFM was conducted to determine the ambient temperature derating for the board with and without a heatsink attached. The temperature rise as function of load current is measured and the derating curves generated for a maximum case temperature of 110°C and shown in figure 19 for various switching frequencies.

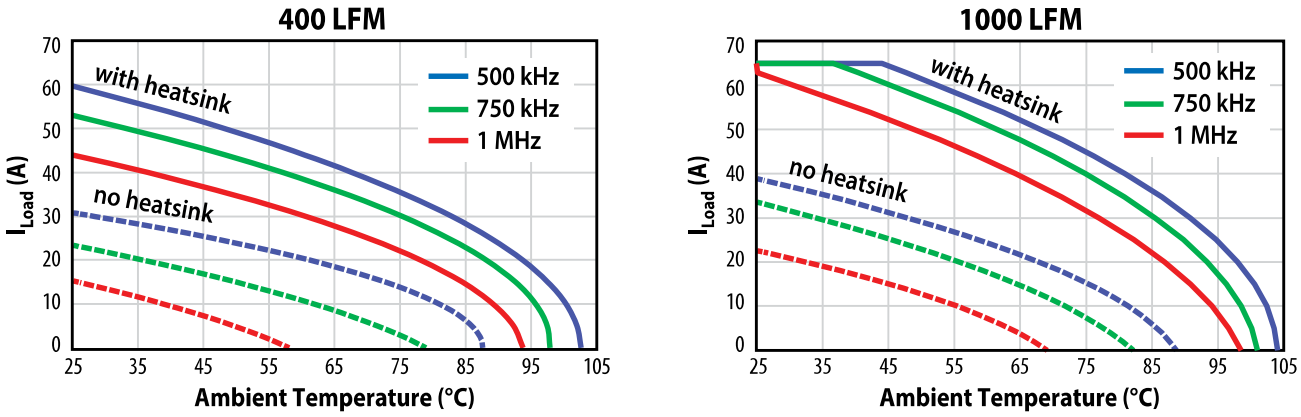


Figure 19: Typical thermal derating curve for two air flow rates, with and without a heatsink attached, measured with the board operating at various switching frequencies and using a 2.2 µH inductor

Table 4: Bill of Materials

Item	Qty	Reference	Part Description	Manufacturer	Part Number
1	3	C11, C100, C101	CAP CER 1 µF 25 V X7R 0603	TDK	C1608X7R1E105K080AB
2	2	C80, C83	CAP CER 2.2 µF 25 V X5R 0402	Murata	GRM155R61E225ME15D
3	7	C81, C610, C611, C612, C614, C615, C616	CAP CER 0.1 µF 25 V X7R 0402	Yageo	CC0402KRX7R8BB104
4	2	C601, C602	CAP CER 47 pF 50 V C0G/NPO 0402	Yageo	CC0402JRNPO9BN470
5	2	C620, C625	CAP CER 100 pF 50 V X7R 0402	Yageo	CC0402KRX7R9BB101
6	7	Ci1, Ci2, Ci3, Ci4, Ci5, Ci6, Ci7	CAP CER 0.22 µF 100 V X7S 0603	Taiyo Yuden	HMK107C7224KAHTE
7	10	Cm1, Cm2, Cm3, Cm4, Cm5, Cm6, Cm7, Cm8, Cm9, Cm10	CAP CER 1 µF 100 V X7R 0805	AVX	08051C105K4Z2A
8	2	D620, D625	DIODE SCHOTTKY 30 V 30 mA SOD523	Diodes Inc.	SDM03U40-7
9	1	J3	Header Male 100 mil 2 row, 12 pos., Thru Vert.	Amphenol	67997-272HLF
10	1	J80	Header Male 100 mil 1 row, 4 pos., Thru Vert.	Tyco	4-103185-0-04
11	1	J90	Header Male 100 mil 1 row, 2 pos., Thru Vert.	Tyco	4-103185-0-02
12	2	J630, J640	Header Male 50 mil 2 row, 3 pos., Thru Vert.	Sullins	GRPB032VWVN-RC
13	1	JP630	50 mil Jumper **Blue** with Handle	Harwin Inc	M50-2030005
14	1	JP640	50 mil Jumper **Red** with Handle	Harwin Inc	M50-2020005
15	1	Q2	100 V, 1.9 mΩ	EPC	EPC2302
16	2	R11, R22	RES 0 Ω JUMPER 1/16 W 0402	Stackpole	RMCF0402ZT0R00
17	1	R60	RES SMD 2.2 Ω JUMPER 1/16 W 0402	Yageo	RC0402JR-072R2L
18	2	R78, R82	RES SMD 0 Ω JUMPER 1/16 W 0402	Yageo	RC0402JR-070RL
19	2	R90, R100	RES SMD 0 Ω JUMPER 1/10 W 0603	Panasonic	ERJ-3GEY0R00V
20	9	R601, R602, R603, R604, R605, R621, R626, R641, R643	RES SMD 10 K Ω 1% 1/16 W 0402	Yageo	RC0402FR-0710KL
21	2	R620, R625	RES SMD 120 Ω 1% 1/10 W 0603	Yageo	RC0603FR-07120RL
22	3	SO1, SO2, SO3	Round Standoff Threaded M2x0.4 Steel 0.039" (1.00 mm)	Wurth	9774010243R
23	4	TP1, TP2, TP3, TP4	HookUP SMD	Keystone	5015
24	1	U1	100 V, 2.7 mΩ Upper FET HB driver IC with UVLO & ESDs	EPC	EPC23101
25	1	U100	5.0 V 250 mA DFN	MicroChip	MCP1703T-5002E/MC
26	4	U610, U611, U612, U614	Reconfig Logic	Nexperia	74LVC1G99GT,115
27	2	U615, U616	Bi directional SW 5E 5.5 V	Texas Instruments	SN74LVC1G66DBV

Table 5: Optional Components

Item	Qty	Reference	Part Description	Manufacturer	Part Number
1	2	C70, C75	CAP CER 100PF 50 V X7R 0402	Yageo	CC0402KRX7R9BB101
2	1	Cout	Custom	TBD	TBD
3	2	D1, D2	DIODE SCHOTTKY 100 V 2A DO220AA	Vishay	SS2PH10-M3
4	1	J1	MMCX Jack SMD Vert.	Molex	734152063
5	1	J9	7.62 mm 2 pos. Euro Block	Wurth	691216410002
6	1	J81	Header Male 100 mil 1 row, 2 pos., Thru Vert.	Tyco	4-103185-0-02
7	1	L1	Custom	TBD	TBD
8	3	R71, R73, R76	RES SMD 10 k Ω 1% 1/16 W 0402	Yageo	RC0402FR-0710KL

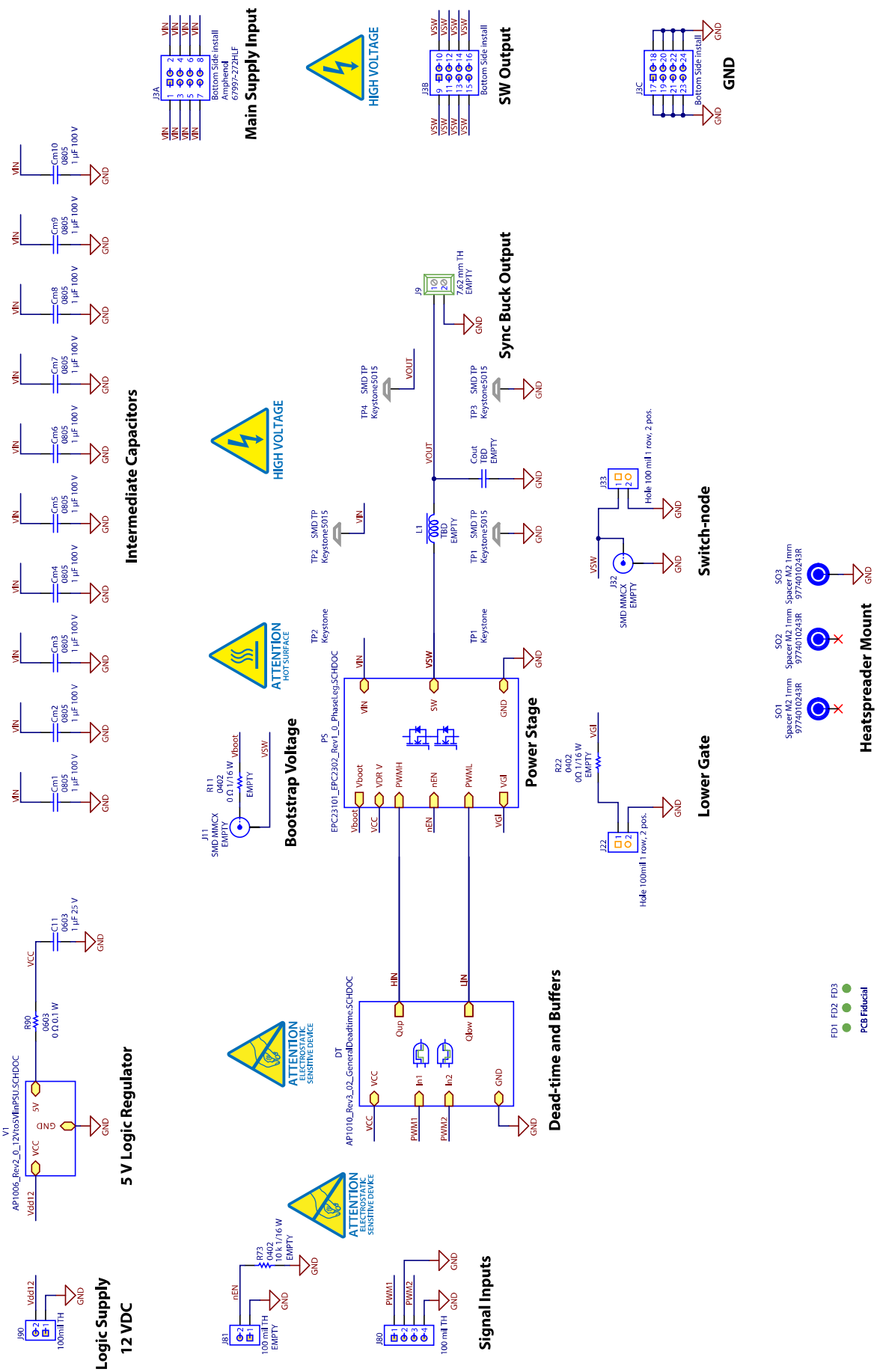


Figure 20: EPC90142 schematic

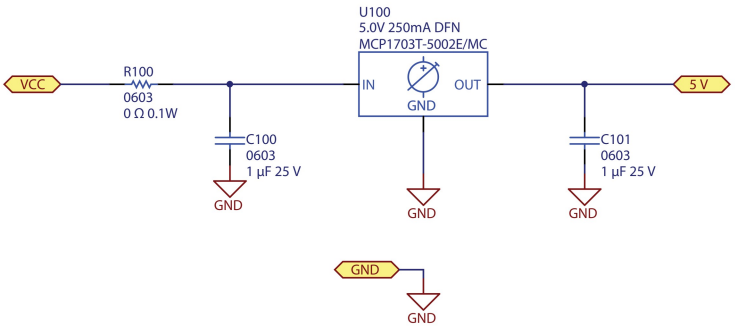


Figure 21: 5 V Regulator

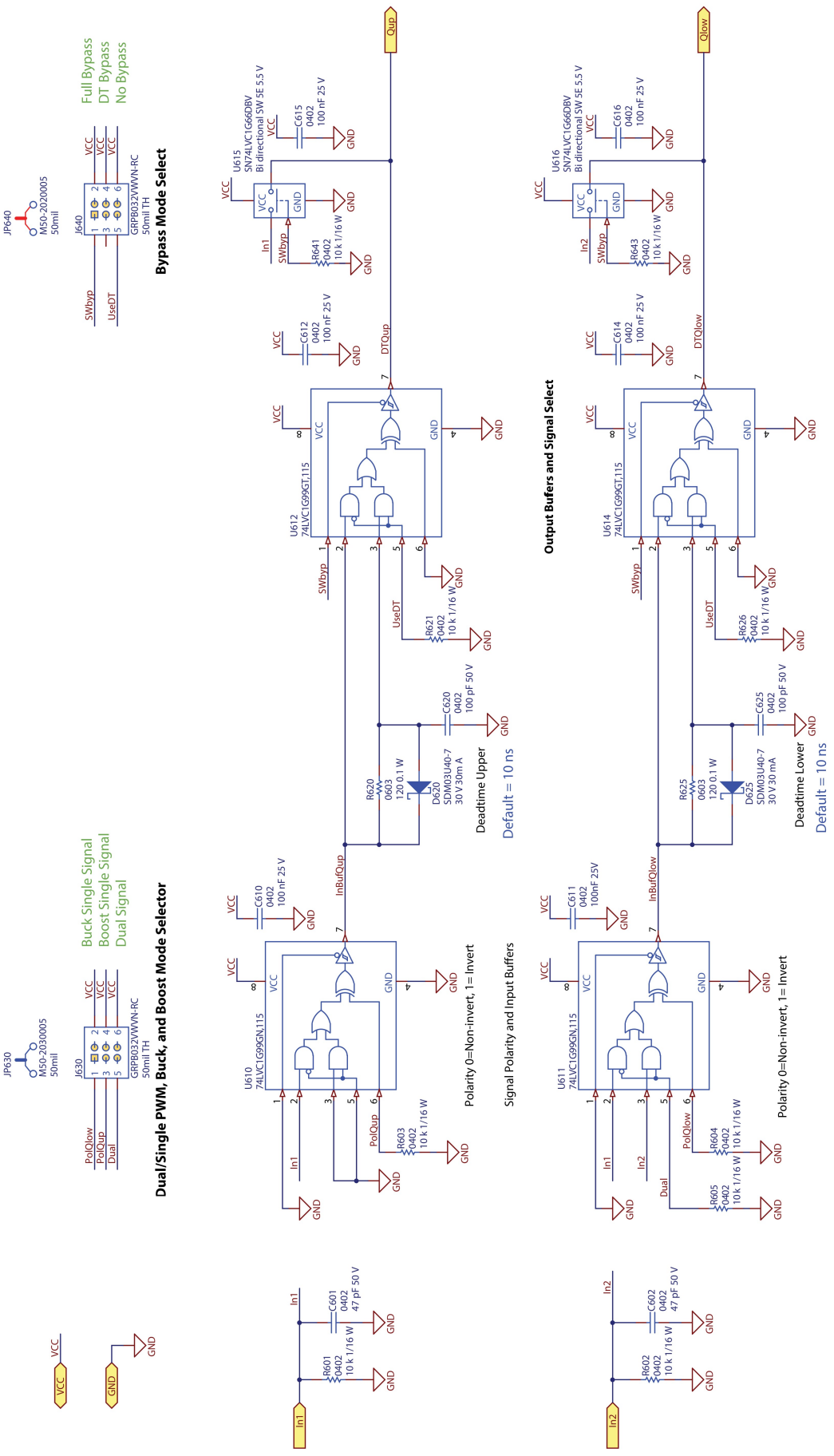


Figure 22: Dead-time and bypass circuit

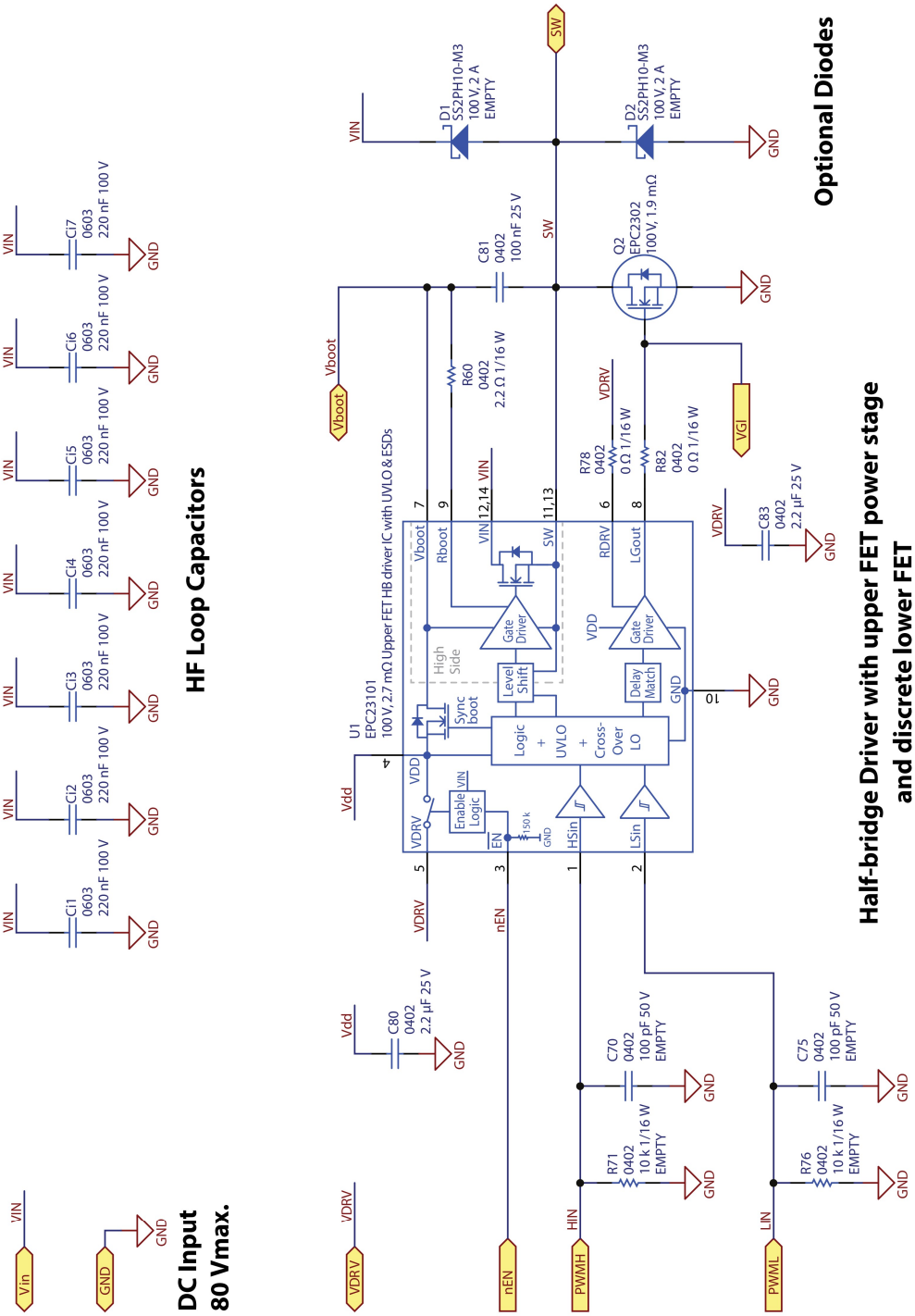


Figure 23: EPC23101 power stage circuit

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