

512K x 8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

NOVEMBER 2016

FEATURES

- High-speed access time: 35, 45, 55 ns
- CMOS low power operation
 - 36 mW (typical) operating
 - 9 μ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
 - 1.65V – 2.2V V_{DD} (IS62WV5128DALL)
 - 2.3V – 3.6V V_{DD} (IS62WV5128DBLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial and Automotive temperature support
- Lead-free available

DESCRIPTION

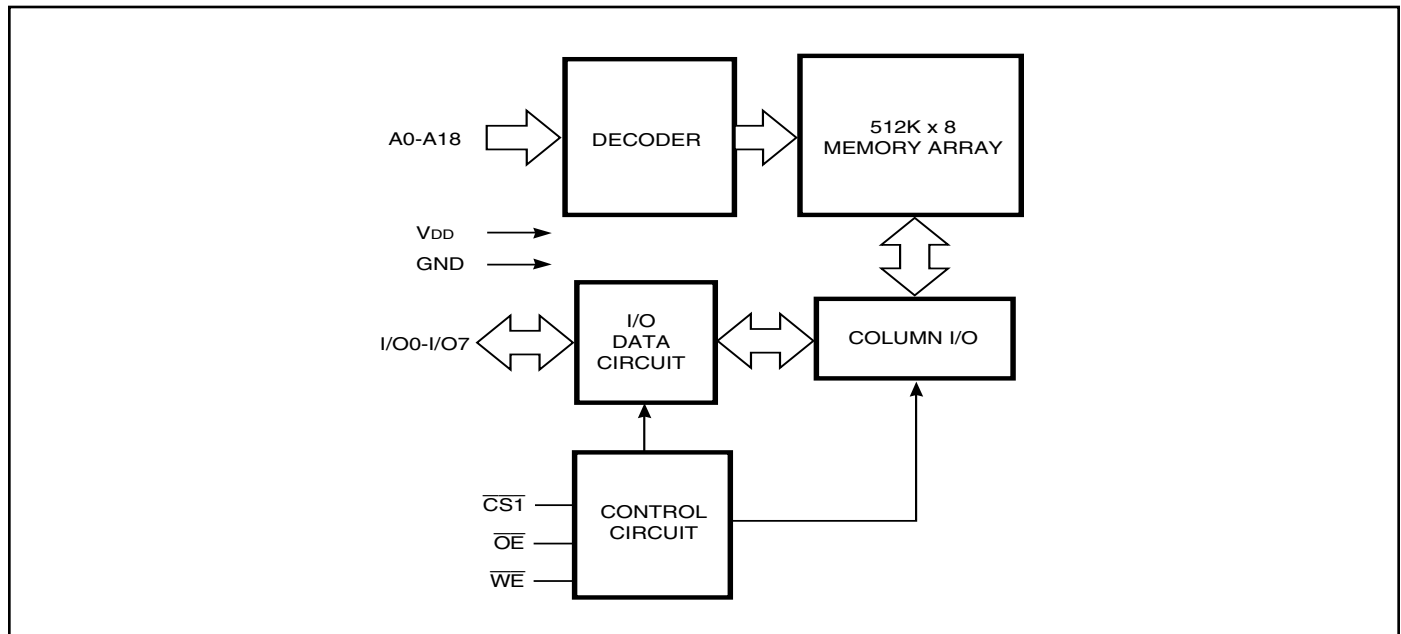
The *ISSI* IS62WV5128DALL / IS62WV5128DBLL are high-speed, 4M bit static RAMs organized as 512K words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory.

The IS62WV5128DALL and IS62WV5128DBLL are packaged in the JEDEC standard 32-pin TSOP (TYPE I), 32-pin sTSOP (TYPE I), 32-pin TSOP (Type II), 32-pin SOP and 36-pin mini BGA.

FUNCTIONAL BLOCK DIAGRAM



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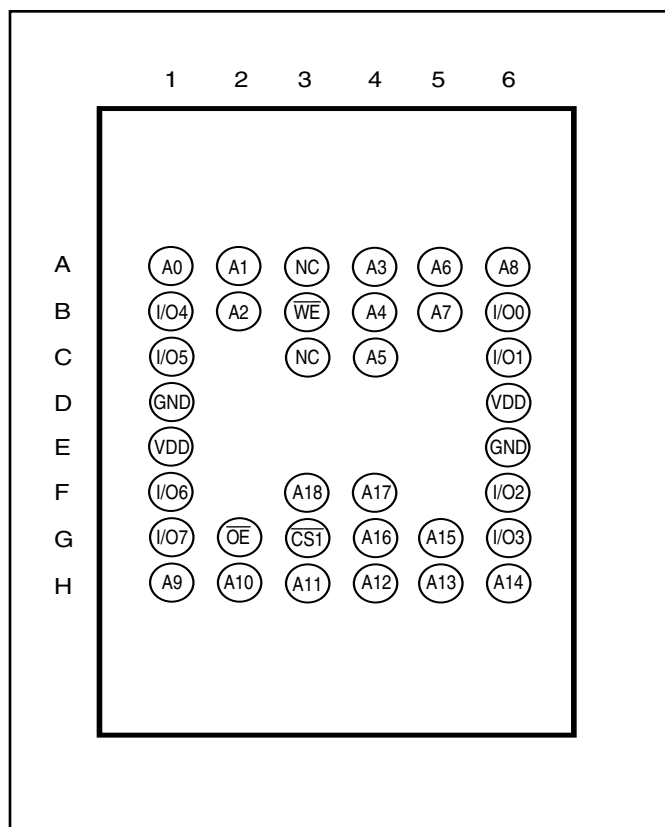
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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

PIN DESCRIPTIONS

| | |
|------------------|---------------------|
| A0-A18 | Address Inputs |
| $\overline{CS1}$ | Chip Enable 1 Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| I/O0-I/O7 | Input/Output |
| NC | No Connection |
| V _{DD} | Power |
| GND | Ground |

**36-pin mini BGA (B) (6mm x 8mm)
(Package Code B)**



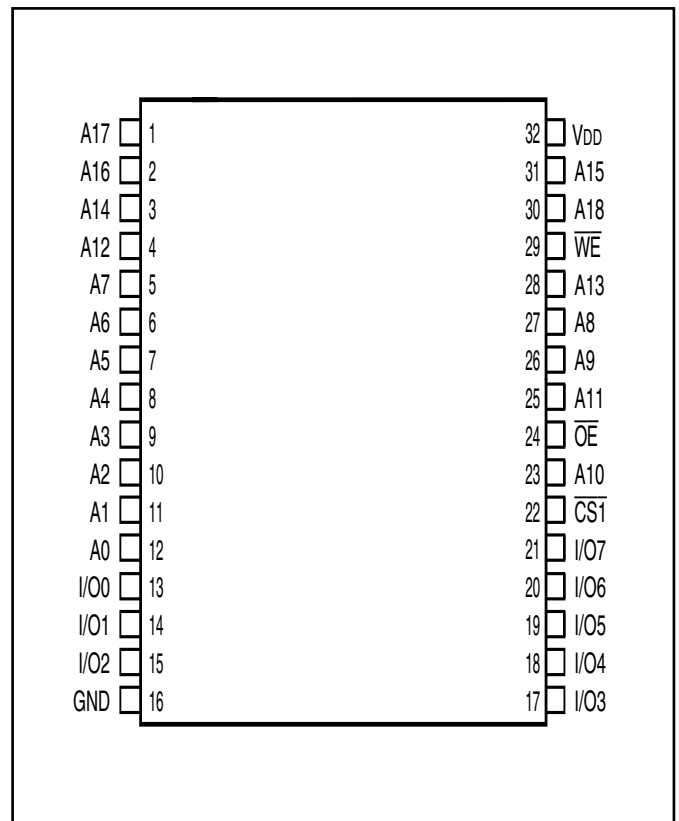
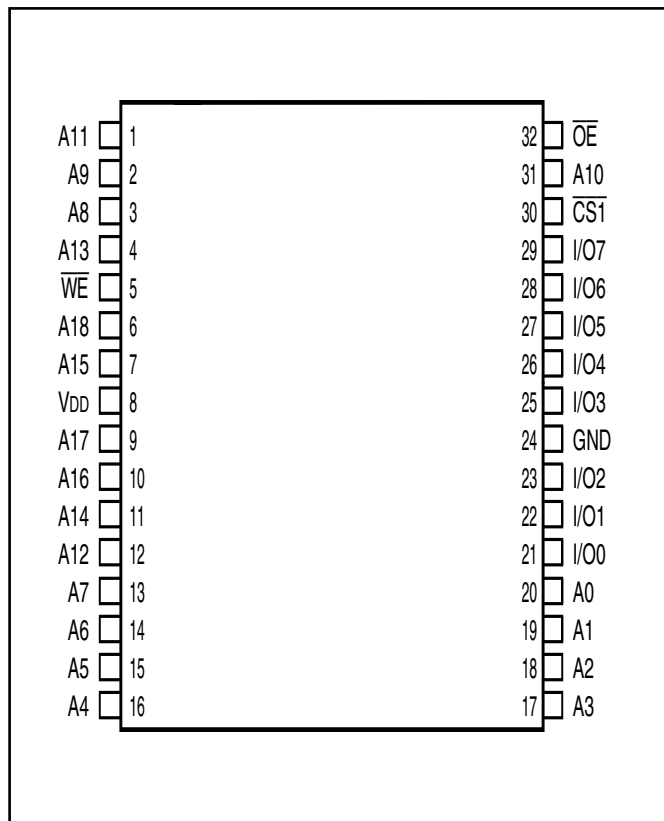
PIN DESCRIPTIONS

| | |
|-----------|---------------------|
| A0-A18 | Address Inputs |
| CS1 | Chip Enable 1 Input |
| OE | Output Enable Input |
| WE | Write Enable Input |
| I/O0-I/O7 | Input/Output |
| VDD | Power |
| GND | Ground |

PIN CONFIGURATION

32-pin TSOP (TYPE I), (Package Code T)
32-pin sTSOP (TYPE I) (Package Code H)

32-pin SOP (Package Code Q)
32-pin TSOP (TYPE II) (Package Code T2)



TRUTH TABLE

| Mode | \overline{WE} | $\overline{CS1}$ | \overline{OE} | I/O Operation | V _{DD} Current |
|------------------------------|-----------------|------------------|-----------------|------------------|-------------------------------------|
| Not Selected (Power-down) | X | H | X | High-Z | I _{SB1} , I _{SB2} |
| Output Disabled | H | L | H | High-Z | I _{CC} |
| Read | H | L | L | D _{OUT} | I _{CC} |
| Write | L | L | X | D _{IN} | I _{CC} |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|-------------------------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to V _{DD} + 0.5 | V |
| V _{DD} | V _{DD} Relates to GND | -0.3 to 4.0 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | W |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{I/O} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

AC TEST CONDITIONS

| Parameter | Unit (2.3V-3.6V) | Unit (3.3V ± 5%) | Unit (1.65V-2.2V) |
|--------------------------------------------------------------------|--------------------------------|--------------------------------|--------------------------------|
| Input Pulse Level | 0.4V to V _{DD} - 0.3V | 0.4V to V _{DD} - 0.3V | 0.4V to V _{DD} - 0.3V |
| Input Rise and Fall Times | 1V/ ns | 1V/ ns | 1V/ ns |
| Input and Output Timing and Reference Level (V _{Ref}) | V _{DD} /2 | $\frac{V_{DD}}{2} + 0.05$ | 0.9V |
| Output Load | See Figures 1 and 2 | See Figures 1 and 2 | See Figures 1 and 2 |
| R1 (Ω) | 1005 | 1213 | 13500 |
| R2 (Ω) | 820 | 1378 | 10800 |
| V _{TM} (V) | 3.0V | 3.3V | 1.8V |

AC TEST LOADS

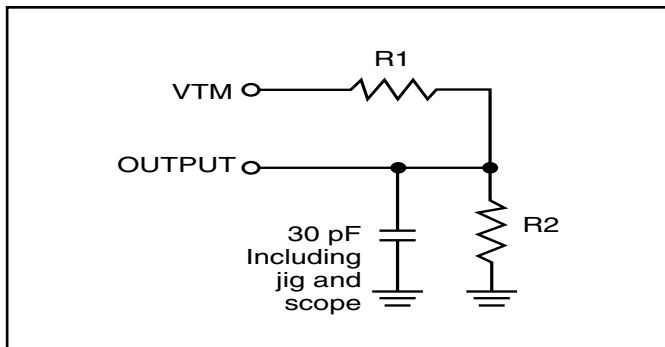


Figure 1.

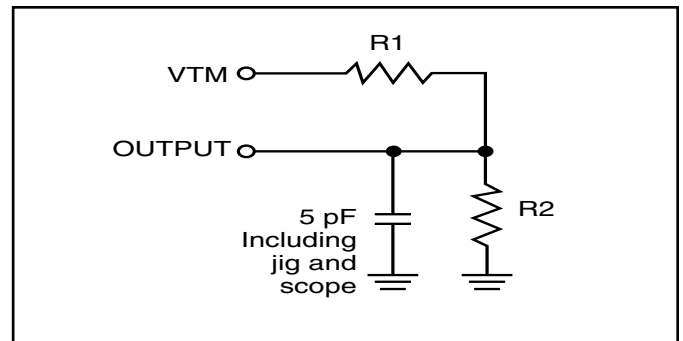


Figure 2.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 3.3V ± 5%

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------|----------------------------------|-------------------------------------------------------------|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | V _{DD} = Min., I _{OH} = -1 mA | 2.4 | — | V |
| V _{OL} | Output LOW Voltage | V _{DD} = Min., I _{OL} = 2.1 mA | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2 | V _{DD} + 0.3 | V |
| V _{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{DD} | -1 | 1 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled | -1 | 1 | μA |

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.3V-3.6V

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------|----------------------------------|-------------------------------------------------------------|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | V _{DD} = Min., I _{OH} = -1.0 mA | 1.8 | — | V |
| V _{OL} | Output LOW Voltage | V _{DD} = Min., I _{OL} = 2.1 mA | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.0 | V _{DD} + 0.3 | V |
| V _{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{DD} | -1 | 1 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled | -1 | 1 | μA |

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 1.65V-2.2V

| Symbol | Parameter | Test Conditions | V _{DD} | Min. | Max. | Unit |
|--------------------------------|---------------------|-------------------------------------------------------------|-----------------|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | I _{OH} = -0.1 mA | 1.65-2.2V | 1.4 | — | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 0.1 mA | 1.65-2.2V | — | 0.2 | V |
| V _{IH} | Input HIGH Voltage | | 1.65-2.2V | 1.4 | V _{DD} + 0.2 | V |
| V _{IL} ⁽¹⁾ | Input LOW Voltage | | 1.65-2.2V | -0.2 | 0.4 | V |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{DD} | | -1 | 1 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled | | -1 | 1 | μA |

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

OPERATING RANGE (V_{DD})

| Range | Ambient Temperature | V _{DD} | Speed |
|------------|---------------------|-----------------|-------|
| Commercial | 0°C to +70°C | 1.65V-2.2V | 45ns |
| Industrial | -40°C to +85°C | 1.65V-2.2V | 55ns |
| Automotive | -40°C to +125°C | 1.65V-2.2V | 55ns |

OPERATING RANGE (V_{DD})

| Range | Ambient Temperature | V _{DD} (45 ns) | V _{DD} (35 ns) |
|------------|---------------------|-------------------------|-------------------------|
| Commercial | 0°C to +70°C | 2.3V-3.6V | 3.3V±5% |
| Industrial | -40°C to +85°C | 2.3V-3.6V | 3.3V±5% |

OPERATING RANGE (V_{DD})

| Range | Ambient Temperature | V _{DD} (45 ns) |
|------------|---------------------|-------------------------|
| Automotive | -40°C to +125°C | 2.3V-3.6V |

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -35 | | -45 | | -55 | | Unit |
|------------------|--------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------|------|------|------|------|------|------|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| I _{CC} | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} $\overline{CE} = V_{IL}$ V _{IN} ≥ V _{DD} - 0.3V, or V _{IN} ≤ 0.4V | Com. | — | 20 | — | 15 | — | 15 | mA |
| | | | Ind. | — | 25 | — | 20 | — | 20 | |
| | | | Auto. | — | 30 | — | 25 | — | 25 | |
| | | | typ. ⁽²⁾ | 10 | | | | | | |
| I _{CC1} | Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = 0 $\overline{CE} = V_{IL}$ V _{IN} ≥ V _{DD} - 0.3V, or V _{IN} ≤ 0.4V | Com. | — | 3 | — | 3 | — | 3 | mA |
| | | | Ind. | — | 3 | — | 3 | — | 3 | |
| | | | Auto. | — | 3 | — | 3 | — | 3 | |
| | | | | | | | | | | |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. | — | 5 | — | 5 | — | 5 | μA |
| | | | Ind. | — | 10 | — | 10 | — | 10 | |
| | | | Auto. | — | 30 | — | 30 | — | 30 | |
| | | | typ. ⁽²⁾ | 2 | | | | | | |

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

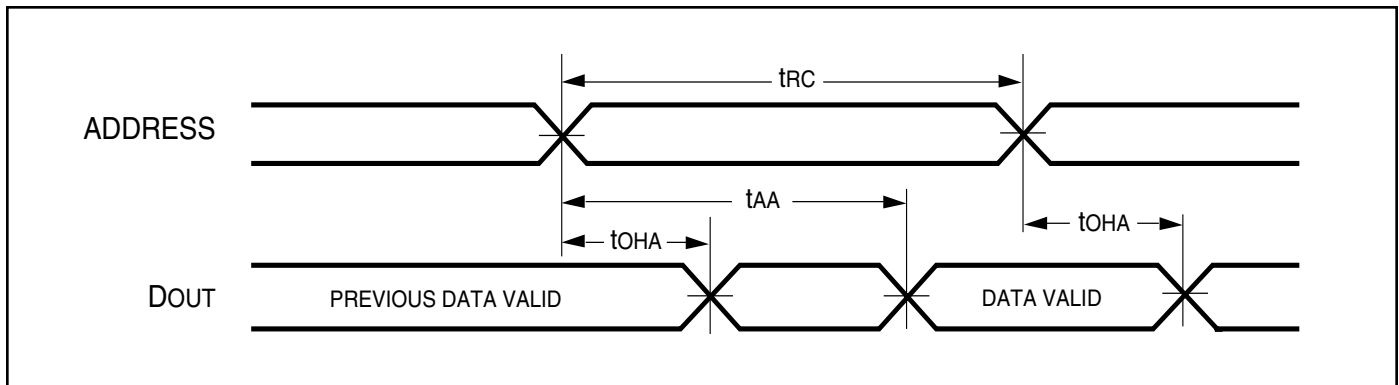
| Symbol | Parameter | 35 ns | | 45 ns | | 55 ns | | Unit |
|---------------------------------|-----------------------------------|-------|------|-------|------|-------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{RC} | Read Cycle Time | 35 | — | 45 | — | 55 | — | ns |
| t _{AA} | Address Access Time | — | 35 | — | 45 | — | 55 | ns |
| t _{OHA} | Output Hold Time | 10 | — | 10 | — | 10 | — | ns |
| t _{ACS1} | $\overline{CS1}$ Access Time | — | 35 | — | 45 | — | 55 | ns |
| t _{DOE} | \overline{OE} Access Time | — | 10 | — | 20 | — | 25 | ns |
| t _{HZOE⁽²⁾} | \overline{OE} to High-Z Output | — | 10 | — | 15 | — | 20 | ns |
| t _{LZOE⁽²⁾} | \overline{OE} to Low-Z Output | 3 | — | 5 | — | 5 | — | ns |
| t _{HZCS1} | $\overline{CS1}$ to High-Z Output | 0 | 10 | 0 | 15 | 0 | 20 | ns |
| t _{LZCS1} | $\overline{CS1}$ to Low-Z Output | 5 | — | 10 | — | 10 | — | ns |

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

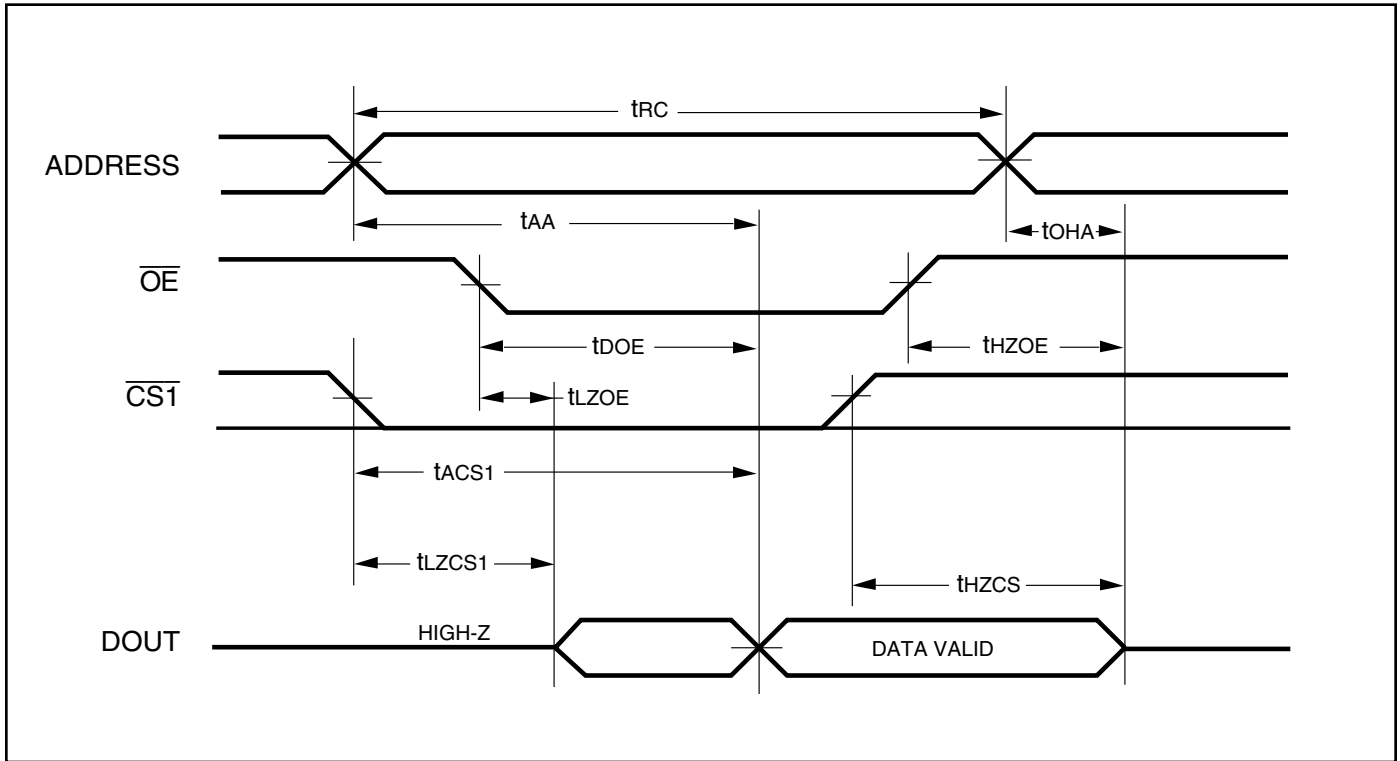
AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CS1} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



AC WAVEFORMS

READ CYCLE NO. 2^(1,3) ($\overline{CS1}$, \overline{OE} Controlled)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CS1} = V_{IL}$. $\overline{WE} = V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

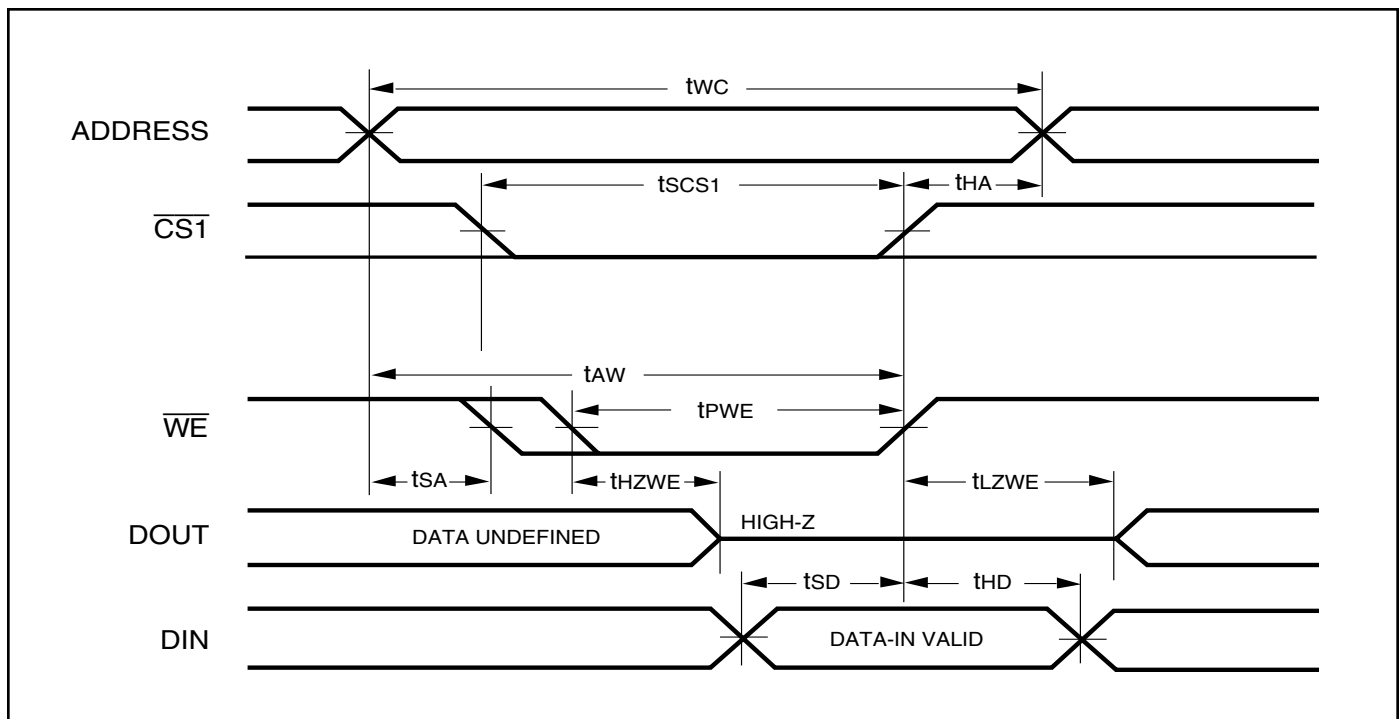
| Symbol | Parameter | 35ns | | 45ns | | 55 ns | | Unit |
|----------------------------------|--------------------------------------|------|------|------|------|-------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{wc} | Write Cycle Time | 35 | — | 45 | — | 55 | — | ns |
| t _{scs1} | $\overline{CS1}$ to Write End | 25 | — | 35 | — | 45 | — | ns |
| t _{aw} | Address Setup Time to Write End | 25 | — | 35 | — | 45 | — | ns |
| t _{ha} | Address Hold from Write End | 0 | — | 0 | — | 0 | — | ns |
| t _{sa} | Address Setup Time | 0 | — | 0 | — | 0 | — | ns |
| t _{pwe} | \overline{WE} Pulse Width | 25 | — | 35 | — | 40 | — | ns |
| t _{sd} | Data Setup to Write End | 20 | — | 20 | — | 25 | — | ns |
| t _{hd} | Data Hold from Write End | 0 | — | 0 | — | 0 | — | ns |
| t _{hzwe} ⁽³⁾ | \overline{WE} LOW to High-Z Output | — | 10 | — | 20 | — | 20 | ns |
| t _{lzwe} ⁽³⁾ | \overline{WE} HIGH to Low-Z Output | 3 | — | 5 | — | 5 | — | ns |

Notes:

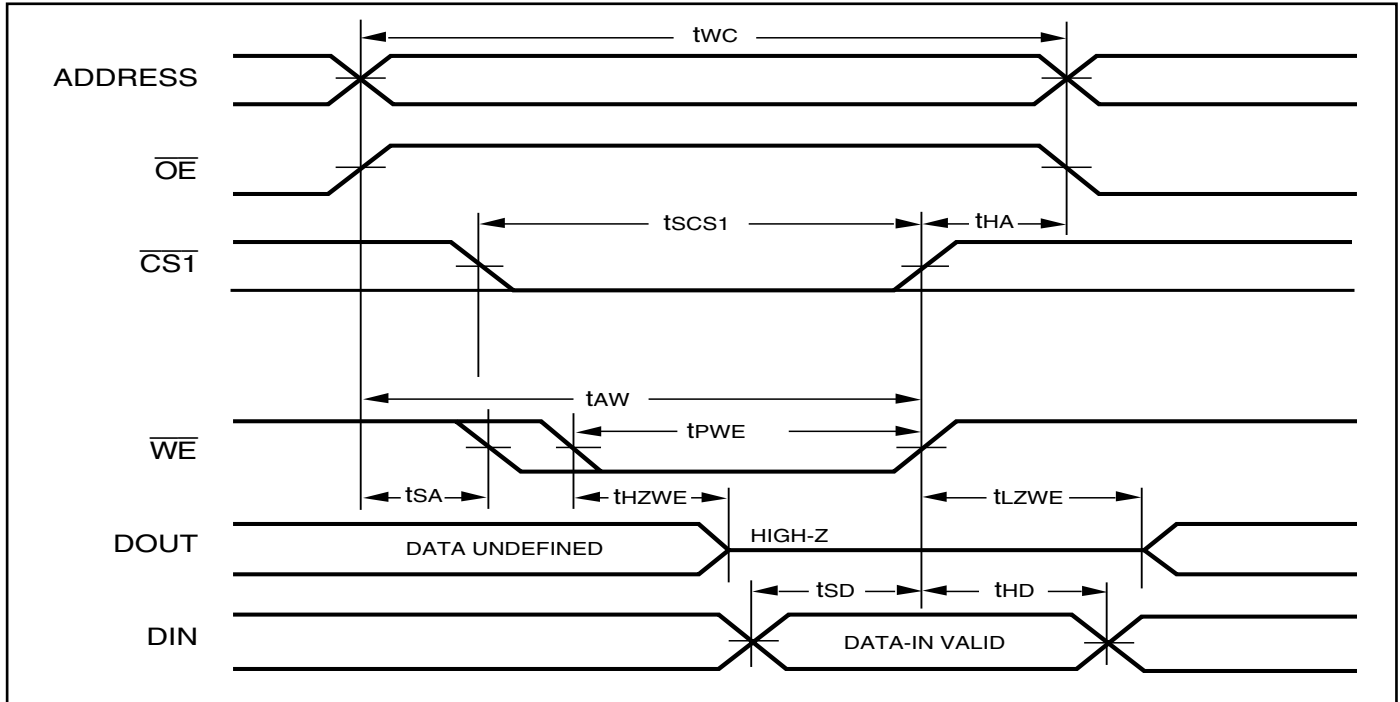
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4V to V_{DD}-0.2V/V_{DD}-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

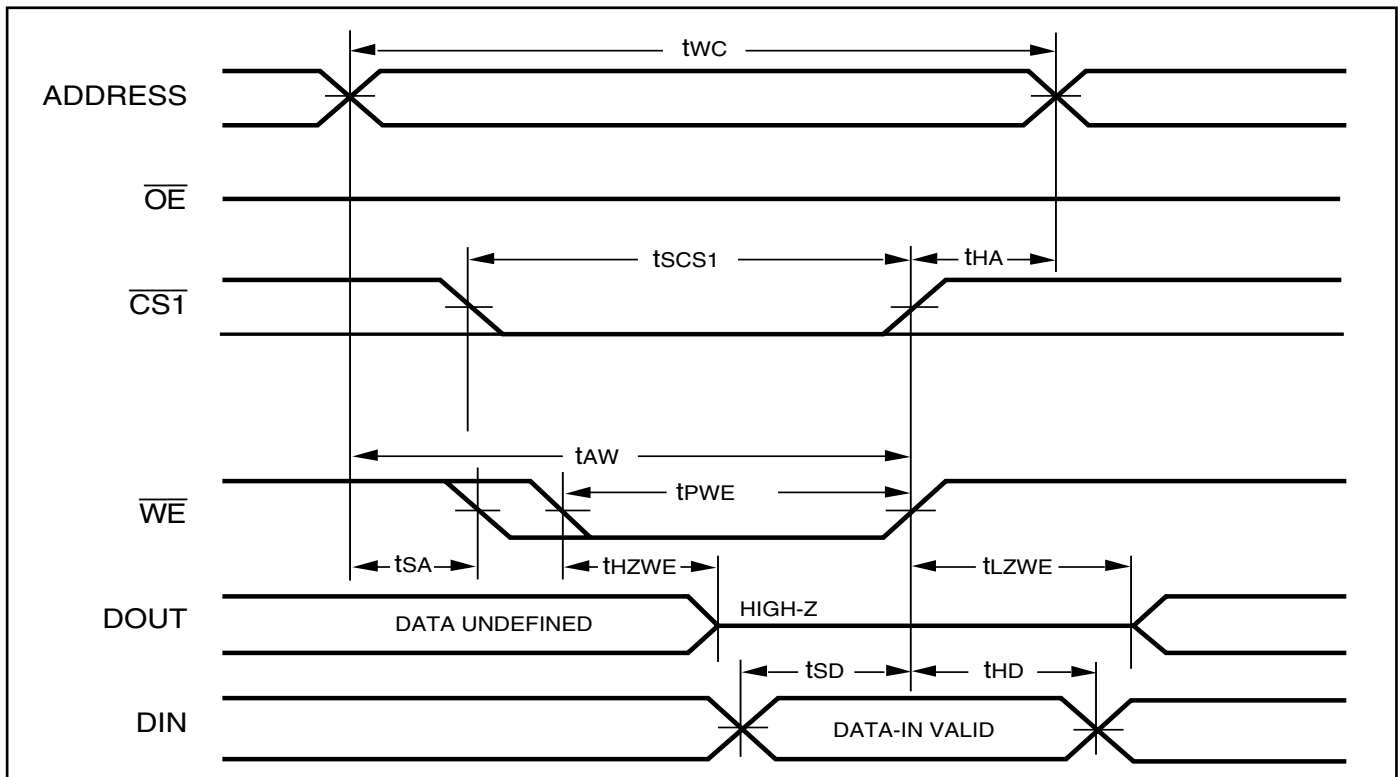
WRITE CYCLE NO. 1 ($\overline{CS1}$ Controlled, \overline{OE} = HIGH or LOW)



WRITE CYCLE NO. 2 (\overline{WE} Controlled: \overline{OE} is HIGH During Write Cycle)



WRITE CYCLE NO. 3 (\overline{WE} Controlled: \overline{OE} is LOW During Write Cycle)

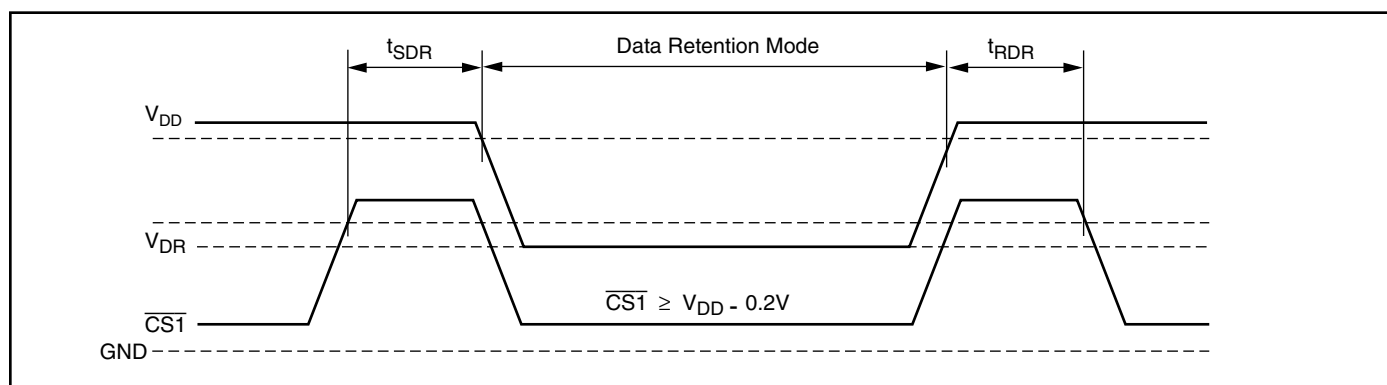


DATA RETENTION SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test Condition | Min. | Max. | Unit |
|------------------|------------------------------------|-------------------------------------------------------------|----------------------------------------------|--------------|------|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | 1.2 | 3.6 | V |
| I _{DR} | Data Retention Current | V _{DD} = 1.2V, $\overline{CS1} \geq V_{DD} - 0.2V$ | Com. Ind. Auto. typ. ⁽¹⁾ | 3 7 20 | μA |
| t _{SDR} | Data Retention Setup Time | See Data Retention Waveform | 0 | — | ns |
| t _{RDR} | Recovery Time | See Data Retention Waveform | t _{RC} | — | ns |

Note: 1. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CS1}$ Controlled)



ORDERING INFORMATION

IS62WV5128DALL (1.65V-2.2V)

Industrial Range: -40°C to +85°C

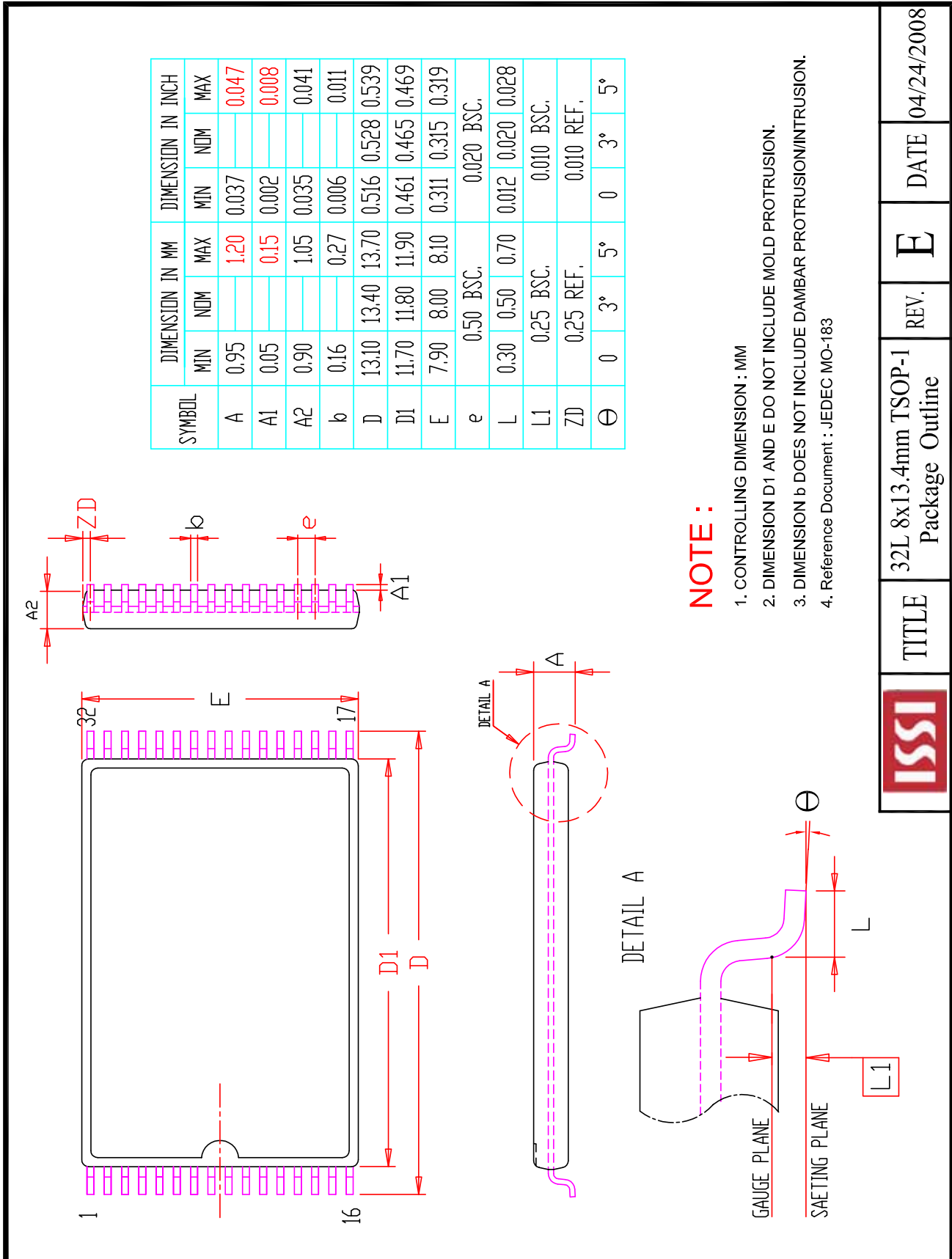
| Speed (ns) | Order Part No. | Package |
|------------|-----------------------|----------------------------------------|
| 55 | IS62WV5128DALL-55TLI | TSOP, TYPE I, Lead-free (8 x 20 mm) |
| 55 | IS62WV5128DALL-55T2LI | TSOP, TYPE II, Lead-free |
| 55 | IS62WV5128DALL-55HLI | sTSOP, TYPE I, Lead-free (8 x 13.4 mm) |
| 55 | IS62WV5128DALL-55BI | mini BGA (6mmx8mm) |
| | IS62WV5128DALL-55BLI | mini BGA (6mmx8mm), Lead-free |

ORDERING INFORMATION

IS62WV5128BLL (2.3V - 3.6V)

Industrial Range: -40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|------------|-----------------------|----------------------------------------|
| 45 | IS62WV5128DBLL-45TLI | TSOP, TYPE I, Lead-free (8 x 20 mm) |
| 45 | IS62WV5128DBLL-45QLI | SOP, Lead-free |
| 45 | IS62WV5128DBLL-45T2LI | TSOP, TYPE II, Lead-free |
| 45 | IS62WV5128DBLL-45HLI | sTSOP, TYPE I, Lead-free (8 x 13.4 mm) |
| 45 | IS62WV5128DBLL-45BI | mini BGA (6mmx8mm) |
| 45 | IS62WV5128DBLL-45BLI | mini BGA (6mmx8mm), Lead-free |

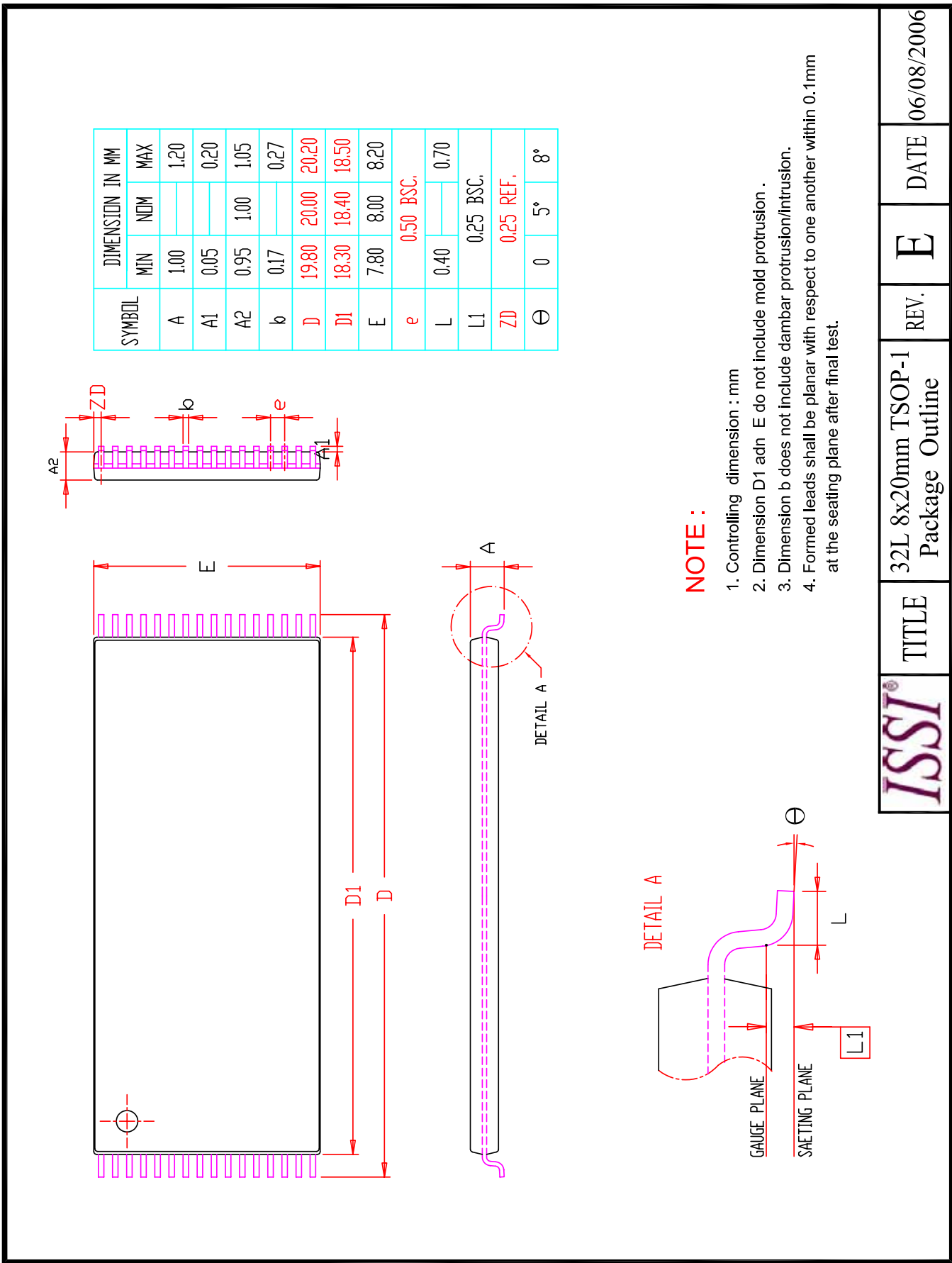


| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|--------|-----------------|-------|-------|-------------------|-------|-------|
| | MIN | NDM | MAX | MIN | NDM | MAX |
| A | 0.95 | | 1.20 | 0.037 | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.008 |
| A2 | 0.90 | | 1.05 | 0.035 | | 0.041 |
| b | 0.16 | | 0.27 | 0.006 | | 0.011 |
| D | 13.10 | 13.40 | 13.70 | 0.516 | 0.528 | 0.539 |
| D1 | 11.70 | 11.80 | 11.90 | 0.461 | 0.465 | 0.469 |
| E | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| L | 0.30 | 0.50 | 0.70 | 0.012 | 0.020 | 0.028 |
| L1 | 0.25 BSC. | | | 0.010 BSC. | | |
| ZD | 0.25 REF. | | | 0.010 REF. | | |
| Θ | 0 | 3° | 5° | 0 | 3° | 5° |

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183

| | | | | | | |
|--|-------|----------------------------------------|------|---|------|------------|
| | TITLE | 32L 8x13.4mm TSOP-1 Package Outline | REV. | E | DATE | 04/24/2008 |
|--|-------|----------------------------------------|------|---|------|------------|



| SYMBOL | DIMENSION IN MM | | |
|--------|-----------------|-----------|-------|
| | MIN | NOM | MAX |
| A | 1.00 | | 1.20 |
| A1 | 0.05 | | 0.20 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | | 0.27 |
| D | 19.80 | 20.00 | 20.20 |
| D1 | 18.30 | 18.40 | 18.50 |
| E | 7.80 | 8.00 | 8.20 |
| e | | 0.50 BSC. | |
| L | 0.40 | | 0.70 |
| L1 | | 0.25 BSC. | |
| ZD | | 0.25 REF. | |
| Θ | 0 | 5° | 8° |

NOTE :

1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.



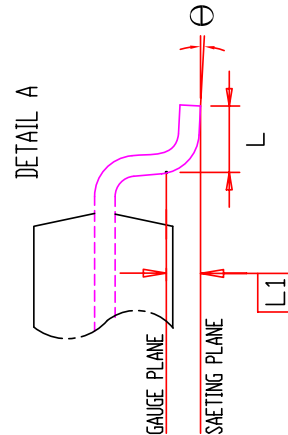
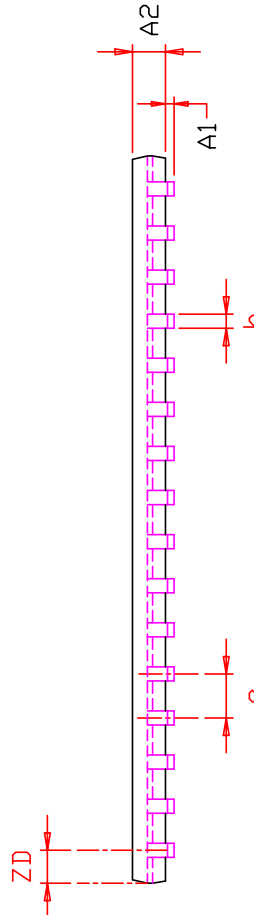
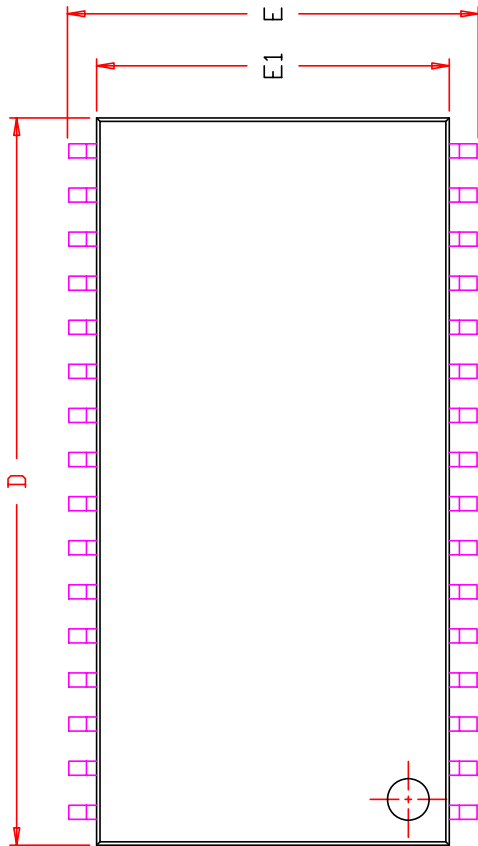
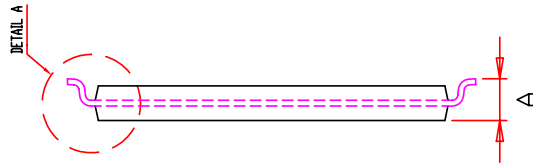
32L 8x20mm TSOP-1
Package Outline

REV.

E

DATE

06/08/2006

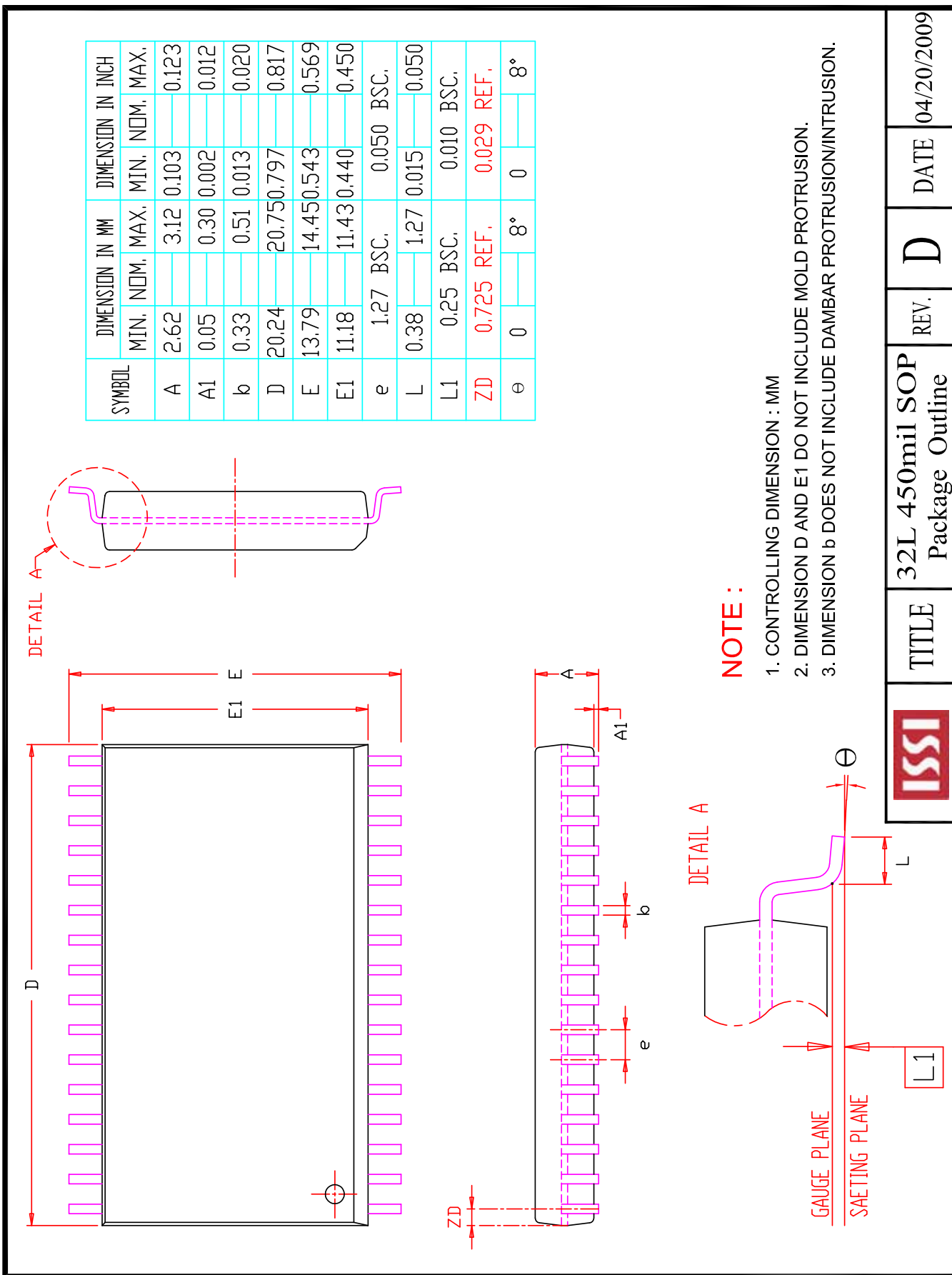


NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

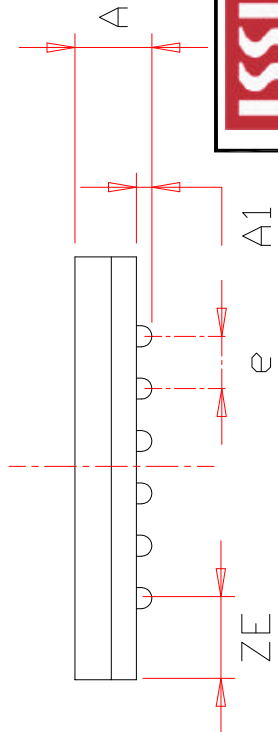
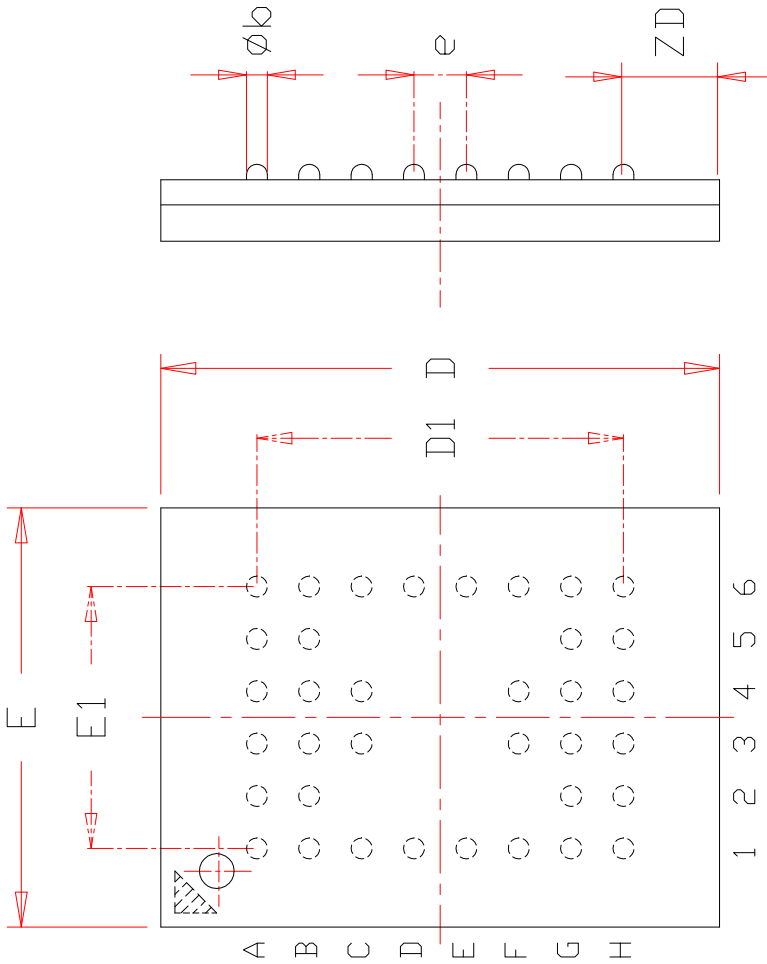
| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|--------|-----------------|-------|-------|-------------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.00 | | 1.20 | 0.039 | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| b | 0.30 | | 0.52 | 0.012 | | 0.020 |
| D | 20.82 | 20.95 | 21.08 | 0.820 | 0.825 | 0.830 |
| E | 11.56 | 11.76 | 11.96 | 0.455 | 0.463 | 0.471 |
| E1 | 10.03 | 10.16 | 10.29 | 0.395 | 0.400 | 0.405 |
| e | 1.27 BSC. | | | 0.050 BSC. | | |
| L | 0.40 | 0.50 | 0.60 | 0.016 | 0.020 | 0.024 |
| L1 | 0.25 BSC. | | | 0.010 BSC. | | |
| ZD | 0.95 REF. | | | 0.037 REF. | | |
| ϕ | 0 | | 8° | 0 | | 8° |

| | | | | | | |
|--|-------|--------------------------------------|------|---|------|------------|
| | TITLE | 32L 400mil TSOP-2 Package Outline | REV. | E | DATE | 06/23/2009 |
|--|-------|--------------------------------------|------|---|------|------------|



| | | | | | | |
|---------------------------------------------------------------------------------------|-------|-----------------------------------|------|---|------|------------|
|  | TITLE | 32L 450mil SOP Package Outline | REV. | D | DATE | 04/20/2009 |
|---------------------------------------------------------------------------------------|-------|-----------------------------------|------|---|------|------------|

TOP VIEW



| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|----------|-----------------|------|------|-------------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 1.20 | | | 0.047 |
| A1 | 0.20 | | 0.30 | 0.008 | | 0.012 |
| ϕb | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| D1 | 5.25 BSC. | | | 0.207 BSC. | | |
| E | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| E1 | 3.75 BSC. | | | 0.148 BSC. | | |
| e | 0.75 BSC. | | | 0.030 BSC. | | |
| ZD | 1.375 REF. | | | 0.054 REF. | | |
| ZE | 1.125 REF. | | | 0.044 REF. | | |

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207



TITLE

**36/48L 6x8mm TF-BGA
 Package Outline**

REV.

E

DATE

08/12/2008