

NCP3712ASN, SZNCP3712ASN

Over Voltage Protected High Side Switch

This switch is primarily intended to protect loads from transients by isolating the load from the transient energy rather than absorbing it.

Features

- Capable of Switching Loads of up to 200 mA without External Rboost
- Switch Shuts Off in Response to an Over Voltage Input Transient
- Features Active Turn Off for Fast Input Transient Protection
- Flexible Over Voltage Protection Threshold Set with External Zener
- Automatic Recovery after Transient Decays Below Threshold
- Withstands Input Transients up to 105 V Peak
- Guaranteed Off State with $\overline{\text{Enbl}}$ Input
- ESD Resistant in Accordance with the 2000 V Human Body Model
- Extremely Low Saturation Voltage
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices

Applications Include:

- High Voltage Transient Isolation
- Power Switching to Electronic Modules
- DC Power Distribution in Line Operated Equipment
- Buffering Sensitive Circuits from Poorly Regulated Power Supplies
- Pre-conditioning of Voltage Regulator Input Voltage

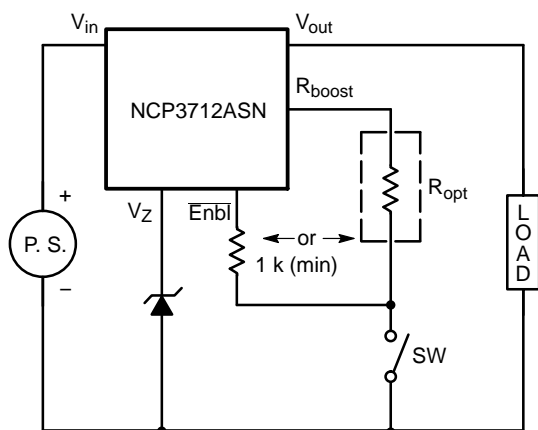


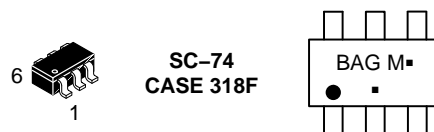
Figure 1. Typical Application Circuit



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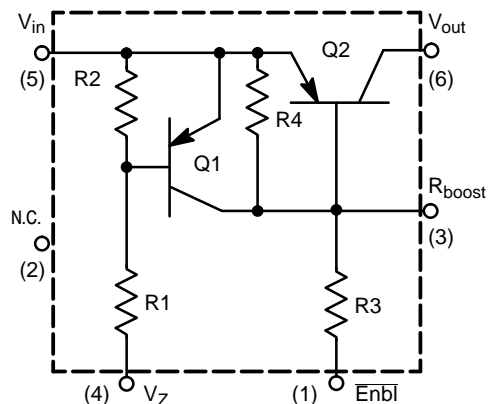
MARKING DIAGRAM



BAG = Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

INTERNAL CIRCUIT DIAGRAM/ PIN CONFIGURATION



ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------------------------|--------------------|-------------------------|
| NCP3712ASNT1G SZNCP3712ASNT1G | SC-74 (Pb-Free) | 3000 / Tape & Reel |
| NCP3712ASNT3G SZNCP3712ASNT3G | SC-74 (Pb-Free) | 10,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MAXIMUM RATINGS (T_J = 25°C unless otherwise noted) (Note 1)

| Rating | Symbol | Value | Unit |
|--|----------------------|------------------------------------|-------|
| Input-to-Output Voltage | V _{io} | 105 | V |
| Reverse Input-to-V _Z Voltage | V _{in(rev)} | -9.0 | V |
| Reverse Input-to-Rboost Voltage | V _{in(rev)} | -5.0 | V |
| Output Load Current – Continuous | I _{load} | -300 | mA |
| Enbl Input Current – Continuous | I _{enbl} | 5.0 | mA |
| V _Z Input Current – Continuous | I _Z | 3.0 | mA |
| Rboost Input Current – Continuous | I _{boost} | 10 | mA |
| Junction Temperature | T _J | 125 | °C |
| Operating Ambient Temperature Range | T _A | -40 to +85 | °C |
| Storage Temperature Range | T _{stg} | -65 to +150 | °C |
| Device Power Dissipation (Minimum Footprint) | P _D | 300 | mW |
| Derate Above 25°C | - | 2.4 | mW/°C |
| Latchup Performance: | Positive Negative | I _{Latchup} 200 200 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- This device contains ESD protection and exceeds the following tests:
 Human Body Model 1500 V per MIL-STD-883, Method 3015.
 Machine Model Method 150 V.

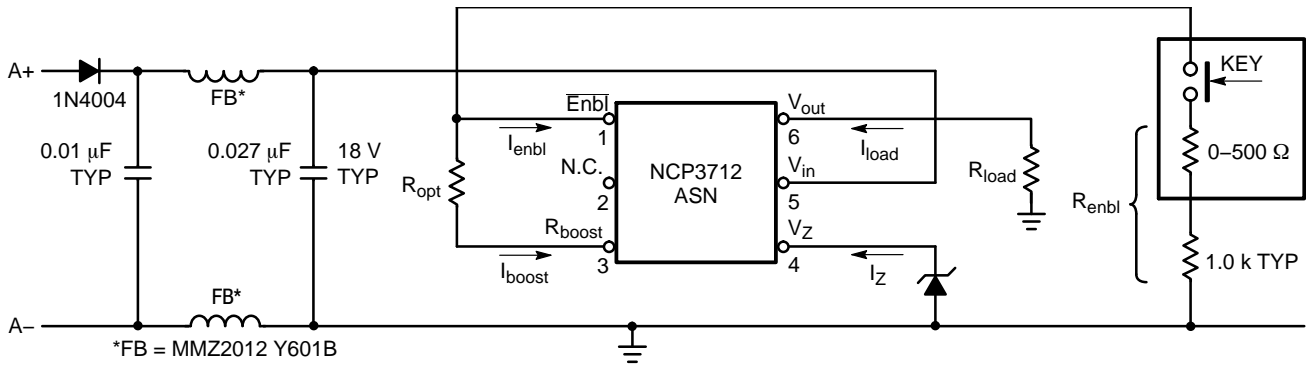


Figure 2. Typical Applications Circuit for Load Dump Transient Protection

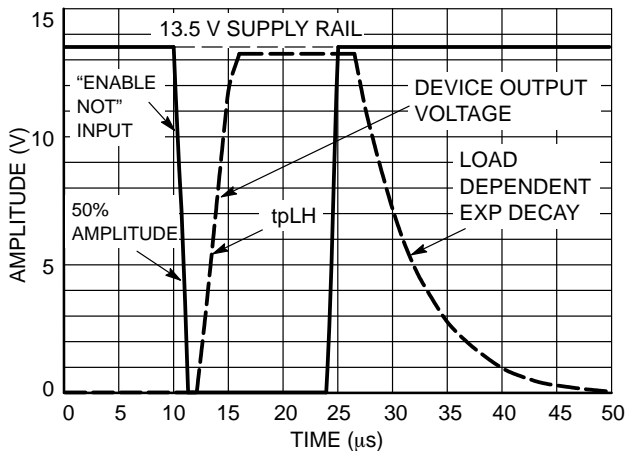


Figure 3. Enable NOT Switching Waveforms

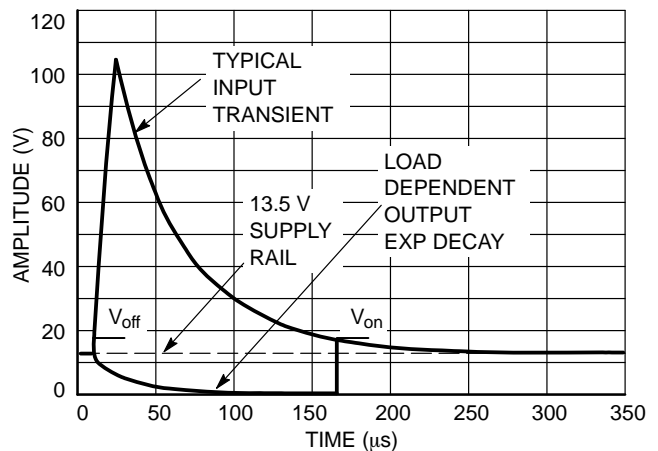


Figure 4. Load Dump Waveforms

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ELECTRICAL CHARACTERISTICS ($V_{in} = 12.5 V_{DC}$ Ref to Gnd, $T_A = 25^\circ C$ unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|-----------------|------|------|------|--------------|
| OFF CHARACTERISTICS | | | | | |
| Input-Output Breakdown Voltage (@ $I_{out} = 200 \mu A$) | $V_{(BRio)}$ | 105 | - | - | Vdc |
| Output Reverse Breakdown Voltage (@ $I_{out} = -1.0 mA$ Pulse) | $V_{(-BRout)}$ | - | -0.7 | - | Vdc |
| Output Leakage Current ($V_{in} = V_{enbl} = 30 V$, $T_A = 25^\circ C$) | $I_{load(off)}$ | - | - | -100 | μA_{dc} |
| Guaranteed "Off" State "ENBL NOT" Voltage ($I_O \leq 100 \mu A$) | $V_{enbl(off)}$ | 13 | - | - | Vdc |
| Required "Off" State I_z Current ($R_{load} = 100 \Omega$) | $I_{z(off)}$ | 150 | - | - | μA_{dc} |
| $V_{in(off)}$ ($V_Z = 16 V$, $I_{load} = 100 mA$, $R_{enbl} = 1500 \Omega$) | V_{off} | 15.5 | - | 18.7 | Vdc |

ON CHARACTERISTICS

| | | | | | |
|--|--------------|-----|-----|------|------------|
| Input-Output On Voltage ($I_O = 100 mA$, $I_{enbl} = -3.0 mA$) | $V_{io(on)}$ | - | 0.2 | 0.5 | Vdc |
| Output Load Current — Continuous ($I_{enbl} = -3.0 mA$, $V_{io(on)} = 0.5 V_{dc}$) ($I_{boost} = -9.0 mA$, $V_{io(on)} = 0.5 V_{dc}$) ($I_{boost} = -9.0 mA$, $V_{io(on)} = 0.6 V_{dc}$) | $I_{o(on)}$ | - | - | -200 | $m A_{dc}$ |
| $V_{in(on)}$ ($V_Z = 16 V$, $I_{load} = 100 mA$, $R_{enbl} = 1500 \Omega$) | V_{on} | 8.5 | - | 10.5 | Vdc |
| "ENBL NOT" Input Current ($I_O = 100 mA$, $V_{io(on)} = 0.35 V_{dc}$, $R_{enbl} = 1500 \Omega$) | I_{enbl} | - | - | -1.0 | $m A_{dc}$ |

SWITCHING CHARACTERISTICS

| | | | | | |
|---|------------------------|---|-----|---|---------|
| Propagation Delay Time: Hi to Lo Prop Delay; Fig. 3 ($V_{in} = V_{enbl} = 13.5 V$) Lo to Hi Prop Delay; Fig. 3 ($V_{in} = 13.5 V$, $V_{enbl} = 0 V$) | t_{PHL} t_{PLH} | - | 1.5 | - | μS |
| Transition Times: Fall Time; Fig. 4 ($V_{in} = V_{enbl} = 13.5 V$) Rise Time; Fig. 4 ($V_{in} = V_{enbl} = 0 V$) | t_f t_r | - | 75 | - | $n S$ |

INTERNAL RESISTORS

| | | | | | |
|-------------------------|----|-----|-----|-----|-----------|
| Input Leakage Resistor | R2 | 7.0 | 10 | 13 | $k\Omega$ |
| Input Resistor | R1 | 3.3 | 4.7 | 6.1 | $k\Omega$ |
| Output Leakage Resistor | R4 | 1.4 | 2.4 | 3.2 | $k\Omega$ |
| Enable Input Resistor | R3 | 1.4 | 2.4 | 3.2 | $k\Omega$ |

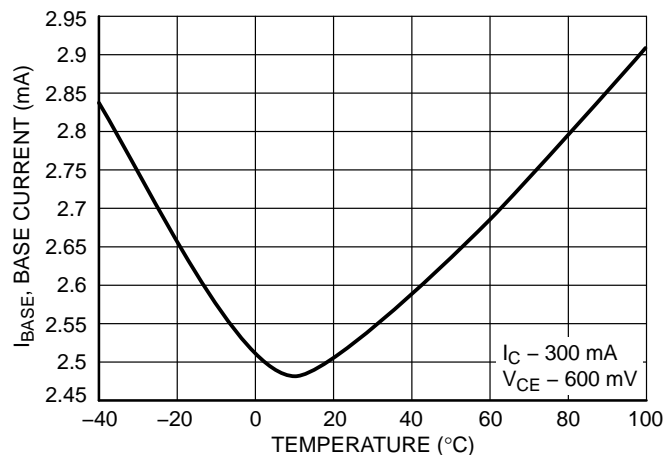


Figure 5. Q2 Base Current vs Temperature with Pin 4 Open

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

SC-74
CASE 318F
ISSUE P

DATE 07 OCT 2021



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
2. CONTROLLING DIMENSION: INCHES
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.

| DIM | MILLIMETERS | | | INCHES | | |
|----------------|-------------|------|------|--------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.90 | 1.00 | 1.10 | 0.035 | 0.039 | 0.043 |
| A1 | 0.01 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.25 | 0.37 | 0.50 | 0.010 | 0.015 | 0.020 |
| c | 0.10 | 0.18 | 0.26 | 0.004 | 0.007 | 0.010 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 1.30 | 1.50 | 1.70 | 0.051 | 0.059 | 0.067 |
| e | 0.85 | 0.95 | 1.05 | 0.034 | 0.037 | 0.041 |
| H _E | 2.50 | 2.75 | 3.00 | 0.099 | 0.108 | 0.118 |
| L | 0.20 | 0.40 | 0.60 | 0.008 | 0.016 | 0.024 |
| M | 0* | --- | 10* | 0* | --- | 10* |

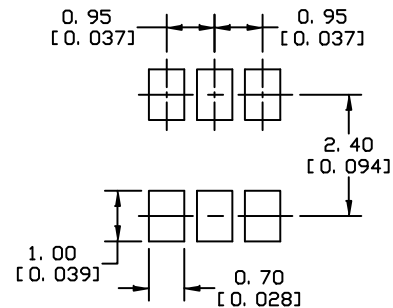
GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

SOLDERING FOOTPRINT

- | | | | | | |
|---|--|---|--|---|---|
| <p>STYLE 1: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. ANODE 6. CATHODE</p> | <p>STYLE 2: PIN 1. NO CONNECTION 2. COLLECTOR 3. EMITTER 4. NO CONNECTION 5. COLLECTOR 6. BASE</p> | <p>STYLE 3: PIN 1. EMITTER 1 2. BASE 1 3. COLLECTOR 2 4. EMITTER 2 5. BASE 2 6. COLLECTOR 1</p> | <p>STYLE 4: PIN 1. COLLECTOR 2 2. EMITTER 1/EMITTER 2 3. COLLECTOR 1 4. EMITTER 3 5. BASE 1/BASE 2/COLLECTOR 3 6. BASE 3</p> | <p>STYLE 5: PIN 1. CHANNEL 1 2. ANODE 3. CHANNEL 2 4. CHANNEL 3 5. CATHODE 6. CHANNEL 4</p> | <p>STYLE 6: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE</p> |
| <p>STYLE 7: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1</p> | <p>STYLE 8: PIN 1. EMITTER 1 2. BASE 2 3. COLLECTOR 2 4. EMITTER 2 5. BASE 1 6. COLLECTOR 1</p> | <p>STYLE 9: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2</p> | <p>STYLE 10: PIN 1. ANODE/CATHODE 2. BASE 3. EMITTER 4. COLLECTOR 5. ANODE 6. CATHODE</p> | <p>STYLE 11: PIN 1. EMITTER 2. BASE 3. ANODE/CATHODE 4. ANODE 5. CATHODE 6. COLLECTOR</p> | |

| | | |
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