NAU8820
Low Power 24-bit Stereo Audio Codec with High Current Outputs

emPowerAudio™

Description

The NAU8820 is a low power, high quality CODEC for portable applications. In addition to precision 24-bit stereo ADCs and DACs, this device integrates a broad range of additional functions to simplify implementation of complete audio system solutions. The NAU8820 includes drivers for headphones, and differential or stereo line outputs, and integrates preamps for stereo differential microphones, significantly reducing external components.

Advanced on-chip digital signal processing includes a 5-band equalizer, a 3-D audio enhancer, a mixed-signal automatic level control for the microphone or line input through the ADC, and a digital limiter function for the playback path. Additional digital filtering options are available in the ADC path, to simplify implementation of specific application requirements such as 'wind noise reduction'. The digital interface can operate as either a master or a slave. Additionally, an internal fractional PLL is available to generate accurately any desired audio sample rate clock for the CODEC, using any commonly available system clock from 8MHz to 33MHz and no external parts.

The NAU8820 operates with analog supply voltages from 2.5V to 3.6V, while the digital core can operate as low as 1.65V to conserve power. The two high current auxiliary line outputs can operate using separate supply rails for increased output capability and design flexibility, and may be used for cap-less headphone drive. Internal register controls enable flexible power saving modes by powering down sub-sections of the chip under software control.

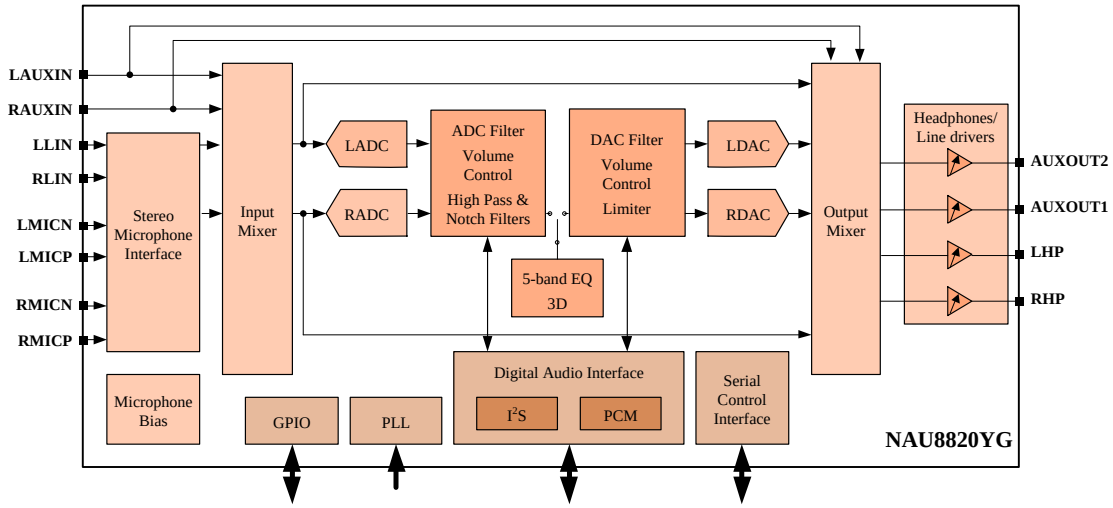
The NAU8820 is specified for operation from -40°C to +85°C. AEC-Q100 & TS16949 compliant device is available upon request.

Key Features

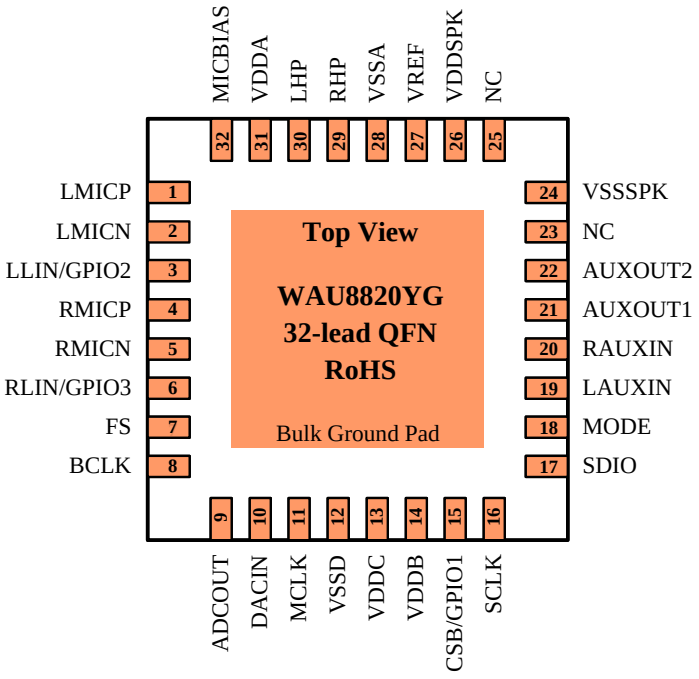
- DAC: 94dB SNR and -84dB THD ("A" weighted)
- ADC: 90dB SNR and -80dB THD ("A" weighted)
- Integrated head-phone driver: 40mW into 16Ω
- Integrated programmable microphone amplifier
- Integrated line input and high current line output
- On-chip PLL
- Integrated DSP with specific functions:
  - 5-band equalizer
  - 3-D audio enhancement
  - Automatic level control
  - Audio level limiter
  - Multiple filtering options
- Standard audio interfaces: PCM and I^2S
- Serial control interfaces with read/write capability
- Supports audio sample rates from 8kHz to 48kHz

Applications

- Personal Media Players
- Smartphones
- Personal Navigation Devices
- Portable Game Players
- Camcorders
- Digital Still Cameras
- Portable TVs
- Stereo Bluetooth Headsets



Pinout



Part Number	Dimension	Package	Package Material
NAU8820YG	5 x 5 mm	32-QFN	Pb-Free

Pin Descriptions

Pin #	Name	Type	Functionality
1	LMICP	Analog Input	Left MICP Input (common mode)
2	LMICN	Analog Input	Left MICN Input
3	LLIN/GPIO2	Analog Input / Digital I/O	Left Line Input / alternate Left MICP Input / GPIO2
4	RMICP	Analog Input	Right MICP Input (common mode)
5	RMICN	Analog Input	Right MICN Input
6	RLIN/GPIO3	Analog Input / Digital I/O	Right Line Input/ alternate Right MICP Input / Digital Output In 4-wire mode: Must be used for GPIO3
7	FS	Digital I/O	Digital Audio DAC and ADC Frame Sync
8	BCLK	Digital I/O	Digital Audio Bit Clock
9	ADCOUT	Digital Output	Digital Audio ADC Data Output
10	DACIN	Digital Input	Digital Audio DAC Data Input
11	MCLK	Digital Input	Master Clock Input
12	VSSD	Supply	Digital Ground
13	VDDC	Supply	Digital Core Supply
14	VDDB	Supply	Digital Buffer (Input/Output) Supply
15	CSB/GPIO1	Digital I/O	3-Wire MPU Chip Select or GPIO1 multifunction input/output
16	SCLK	Digital Input	3-Wire MPU Clock Input / 2-Wire MPU Clock Input
17	SDIO	Digital I/O	3-Wire MPU Data Input / 2-Wire MPU Data I/O
18	MODE	Digital Input	Control Interface Mode Selection Pin
19	LAUXIN	Analog Input	Left Auxiliary Input
20	RAUXIN	Analog Input	Right Auxiliary Input
21	AUXOUT1	Analog Output	Headphone Ground / Mono Mixed Output / Line Output
22	AUXOUT2	Analog Output	Headphone Ground / Line Output
23	NC		Not Internally Connected
24	VSSSPK	Supply	AUXOUT Line/Speaker Pre-amp Driver Analog Ground
25	NC		Not Internally Connected
26	VDDSPK	Supply	AUXOUT Line/Speaker Pre-amp Driver Analog Power Supply
27	VREF	Reference	Decoupling for Midrail Reference Voltage
28	VSSA	Supply	Analog Ground
29	RHP	Analog Output	Headphone Positive Output / Line Output Right
30	LHP	Analog Output	Headphone Negative Output / Line Output Left
31	VDDA	Supply	Analog Power Supply
32	MICBIAS	Analog Output	Microphone Bias

Notes

1. The 32-QFN package includes a bulk ground connection pad on the underside of the chip. This bulk ground should be thermally tied to the PCB as much as possible, and electrically tied to the analog ground (VSSA, pin 28).
2. Unused analog input pins should be left as no-connection.
3. Unused digital input pins should be tied to ground.
4. Pins designated as NC (Not Internally Connected) should be left as no-connection

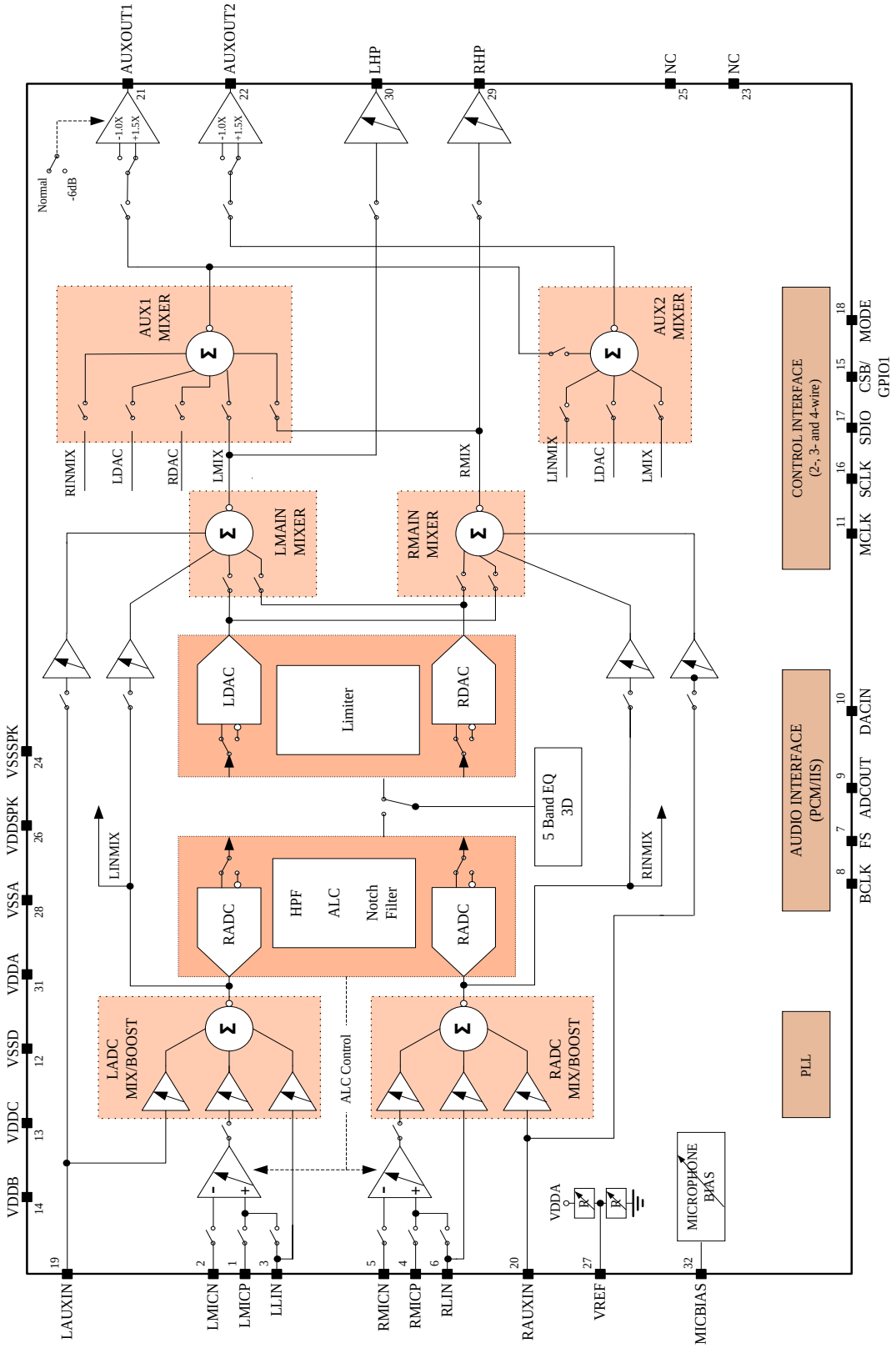


Figure 1: NAU8820 Block Diagram

Electrical Characteristics

Conditions: VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V, MCLK = 12.288MHz, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data, 64X oversampling rate, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Analog to Digital Converter (ADC)						
Full scale input signal [1]	V_{INFS}	PGABST = 0dB PGAGAIN = 0dB		1.0 0		Vrms dBV
Signal-to-noise ratio	SNR	Gain = 0dB, A-weighted	tbd	90		dB
Total harmonic distortion [2]	THD+N	Input = -3dB FS input		-80	tbd	dB
Channel separation		1kHz input signal		103		dB
Digital to Analog Converter (DAC) driving RHP / LHP with 10kΩ / 50pF load						
Full-scale output [4]		Output boost disabled PGA gains = 0dB AUX1BST = 1 AUX2BST = 1		VDDA / 3.3		V_{rms}
		Output boost enabled PGA gains = 0dB AUX1BST = 0 AUX2BST = 0		1.5 * (VDDA / 3.3)		V_{rms}
Signal-to-noise ratio	SNR	A-weighted	88	94		dB
Total harmonic distortion [2]	THD+N	R_L = 10kΩ; full-scale signal		-84	tbd	dB
Channel separation		1kHz input signal		96		dB
Output Mixers						
Maximum PGA gain into mixer				+6		dB
Minimum PGA gain into mixer				-15		dB
PGA gain step into mixer		Guaranteed monotonic		3		dB
Analog Outputs (RHP / LHP)						
Maximum programmable gain				+6		dB
Minimum programmable gain				-57		dB
Programmable gain step size		Guaranteed monotonic		1		dB
Mute attenuation		1kHz full scale signal		85		dB
Headphone Output (RHP / LHP with 32Ω load)						
0dB full scale output voltage				AVDD / 3.3		V_{rms}
Signal-to-noise ratio	SNR	A-weighted		92		dB
Total harmonic distortion [2]	THD+N	R_L = 16Ω, P_o = 20mW, VDDA = 3.3V		80		dB
		R_L = 32Ω, P_o = 20mW, VDDA = 3.3V		85		dB
AUXOUT1 / AUXOUT2 with 10kΩ / 50pF load						
Full scale output [3]		AUX1BST = 0 AUX2BST = 0		VDDSPK / 3.3		V_{rms}
		AUX1BST = 1 AUX2BST = 1		(VDDSPK / 3.3) * 1.5		V_{rms}
Signal-to-noise ratio	SNR			87		dB
Total harmonic distortion [2]	THD+N			-83		dB
Channel separation		1kHz signal		99		dB
Power supply rejection ratio (50Hz - 22kHz)	PSRR			53		dB

Electrical Characteristics, cont'd.

Conditions: VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V, MCLK = 12.288MHz,
T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Microphone Inputs (LMICP, LMICN, RMICP, RMICN, LLIN, RLIN) and Programmable Gain Amplifier (PGA)						
Full scale input signal [1]		PGABST = 0dB PGAGAIN = 0dB		1.0 0		Vrms dBV
Programmable gain			-12		35.25	dB
Programmable gain step size		Guaranteed Monotonic		0.75		dB
Mute Attenuation				120		dB
Input resistance		Inverting Input PGA Gain = 35.25dB PGA Gain = 0dB PGA Gain = -12dB Non-inverting Input		 1.6 47 75 94		 kΩ kΩ kΩ kΩ
Input capacitance				10		pF
PGA equivalent input noise		0 to 20kHz, Gain set to 35.25dB		120		µV
Input Boost Mixer						
Gain boost		Boost disabled Boost enabled		0 20		dB dB
Gain range LLIN / RLIN or LAUXIN / RAUXIN to boost/mixer			-12		6	dB
Gain step size to boost/mixer				3		dB
Auxiliary Analog Inputs (LAUXIN, RAUXIN)						
Full scale input signal [1]		Gain = 0dB		1.0 0		Vrms dBV
Input resistance		Aux direct-to-out path, only Input gain = +6.0dB Input gain = 0.0dB Input gain = -12dB		 20 40 159		 kΩ kΩ kΩ
Input capacitance				10		pF

Electrical Characteristics, cont'd.

Conditions: VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V, MCLK = 12.288MHz,
T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Automatic Level Control (ALC) & Limiter: ADC path only						
Target record level			-22.5		-1.5	dBFS
Programmable gain			-12		35.25	dB
Gain hold time [4]	t_{HOLD}	Doubles every gain step, with 16 steps total	0 / 2.67 / 5.33 / … / 43691			ms
Gain ramp-up (decay) [4]	t_{DCY}	ALC Mode ALC = 0	4 / 8 / 16 / … / 4096			ms
		Limiter Mode ALC = 1	1 / 2 / 4 / … / 1024			ms
Gain ramp-down (attack) [4]	t_{ATK}	ALC Mode ALC = 0	1 / 2 / 4 / … / 1024			ms
		Limiter Mode ALC = 1	0.25 / 0.5 / 1 / … / 128			ms
Mute Attenuation				120		dB
Microphone Bias						
Bias voltage	$V_{MICBIAS}$	See Figure 4	0.50, 0.60,0.65, 0.70, 0.75, 0.85, or 0.90			VDDA VDDA
Bias current source	$I_{MICBIAS}$			3		mA
Output noise voltage	V_n	1kHz to 20kHz		14		nV/√Hz
Digital Input/Output						
Input HIGH level	V_{IL}		0.7 * VDDC			V
Input LOW level	V_{IH}				0.3 * VDDC	V
Output HIGH level	V_{OH}	I_{Load} = 1mA	0.9 * VDDC			V
Output LOW level	V_{OL}	I_{Load} = -1mA			0.1 * VDDC	V
Input capacitance				10		pF

Notes

1. Full Scale is relative to the magnitude of VDDA and can be calculated as FS = VDDA/3.3.
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurements is at 3dB below full scale, unless otherwise noted.
3. With default register settings, SPKVDD should be 1.5xVDDA (but not exceeding maximum recommended operating voltage) to optimize available dynamic range in the AUXOUT1 and AUXOUT2 line output stages. Output DC bias level is optimized for SPKVDD = 5.0Vdc (boost mode) and VDDA = 3.3Vdc.
4. Time values scale proportionally with MCLK. Complete descriptions and definitions for these values are contained in the detailed descriptions of the ALC functionality.

Absolute Maximum Ratings

Condition	Min	Max	Units
VDDB, VDDC, VDDA supply voltages	-0.3	+3.61	V
VDDSPK supply voltage (default register configuration)	-0.3	+5.80	V
VDDSPK supply voltage (optional low voltage configuration)	-0.3	+3.61	V
Core Digital Input Voltage range	VSSD – 0.3	VDDC + 0.30	V
Buffer Digital Input Voltage range	VSSD – 0.3	VDDB + 0.30	V
Analog Input Voltage range	VSSA – 0.3	VDDA + 0.30	V
Industrial operating temperature	-40	+85	°C
Storage temperature range	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Digital supply range (Core)	VDDC	1.65		3.60	V
Digital supply range (Buffer)	VDDB	1.65		3.60	V
Analog supply range	VDDA	2.50		3.60	V
Speaker supply (SPKBST=0)	VDDSPK	2.50		5.50	V
Speaker supply (SPKBST=1)	VDDSPK	2.50		5.50	V
Ground	VSSD VSSA VSSSPK		0		V

1. VDDA must be ≥ VDDC.
2. VDDB must be ≥ VDDC.

1 General Description

The NAU8820 is a stereo device with identical left and right channels that share common support elements. The left and right channels are identical, except for the mixing options and gain options available for each of the two auxiliary outputs.

1.1 Analog Inputs

All inputs, except for the wide range programmable amplifier (PGA), have available analog input gain conditioning of -15dB through +6dB in 3dB steps. All inputs also have individual muting functions with excellent channel isolation and off-isolation from all outputs. All inputs are suitable for full quality, high bandwidth signals.

Each of the left-right stereo channels includes a low noise differential PGA amplifier, programmable for high-gain input. This may be used for a microphone level through line level source. Gain may be set from +35.25db through -12dB at the analog difference-amplifier type programmable amplifier input stage. A separate additional 20dB analog gain is available on this input path, between the PGA output and ADC mixer input. The output of the ADC mixer may be routed to the ADC and/or analog bypass to the analog output sections.

Each channel also has a line level input. This input may be routed to the input PGA, and/or directly to the ADC input mixer.

Each channel has a separate additional auxiliary input. This is a line level input which may be routed the ADC input mixer and/or directly to the analog output mixers.

1.2 Analog Outputs

There are four high current analog audio outputs. These are very flexible outputs that can be used individually or in stereo pairs for a wide range of end uses. However, these outputs are optimized for specific functions and are described in this section using the functional names that are applicable to those optimized functions.

Each output receives its signal source from built-in analog output mixers. These mixers enable a wide range of signal combinations, including muting of all sources. Additionally, each output has a programmable gain function, output mute function, and output disable function.

The RHP and LHP headphone outputs are optimized for driving a stereo pair of headphones, and are powered from the main analog voltage supply rail, VDDA. These outputs may be coupled using traditional DC blocking series capacitors. Alternatively, these may be configured in a no-capacitor DC coupled design using a virtual ground at ½ VDDA provided by an AUXOUT analog output. Gain of each headphone output can be separately varied in 1dB steps from +6dB through -57dB.

The AUXOUT1 and AUXOUT2 analog outputs can be coupled to a wide range of input signal mixing options, and support two gain choices. Gain may either be unity for 3.3V operation, or 1.5x for 5V operation. The auxiliary outputs are powered from the VDDSPK supply rail and VSSSPK ground return path. The supply rail may be the same as VDDA, or may be a separate voltage up to 5.0Vdc. These separate supply rails enable these outputs to have increased output range and power capabilities, and facilitate system design through enabling power supply and routing separate from VDDA.

Important: **For analog outputs depopping purpose, when powering up speakers, headphone, AUXOUTs, certain delays are generated after enabling sequence. However, the delays are created by MCLK and sample rate register. For correct operation, sending I2S signal no earlier than 250ms after speaker or headphone enabled and MCLK appearing.**

ADC, DAC, and Digital Signal Processing

Each left and right channel has an independent high quality ADC and DAC associated with it. These are high performance, 24-bit delta-sigma converters that are suitable for a very wide range of applications.

The ADC and DAC functions are each individually supported by powerful analog mixing and routing. The ADC output may be routed to the digital output path and/or to the input of the DAC in a digital passthrough mode. The ADC and DAC blocks are also supported by advanced digital signal processing subsystems that enable a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is with 24-bit precision, as to minimize processing artifacts and maximize the audio dynamic range supported by the NAU8820.

The ADCs are supported by a wide range, mixed-mode Automatic Level Control (ALC), a high pass filter, and a notch filter. All of these features are optional and highly programmable. The high pass filter function is intended for DC-blocking or low frequency noise reduction, such as to reduce unwanted ambient noise or "wind noise" on a microphone input. The notch filter may be programmed to greatly reduce a specific frequency band or frequency, such as a 50Hz, 60Hz, or 217Hz unwanted noise.

The DACs are supported by a programmable limiter/DRC (Dynamic Range Compressor). This is useful to optimize the output level for various applications and for use with small loudspeakers. This is an optional feature that may be programmed to limit the maximum output level and/or boost an output level that is too small.

Digital signal processing is also provided for a 3D Audio Enhancement function, and for a 5-Band Equalizer. These features are optional, and are programmable over wide ranges. This pair of digital processing features may be applied jointly to either the ADC audio path or to the DAC audio path, but not to both paths simultaneously.

1.3 Voltage Reference and Microphone Bias

Built-in power management includes a high stability voltage reference. This is used as an internal reference, and to generate a high quality, programmable microphone bias supply voltage that is well isolated from the supply rails. This microphone bias supply is suitable for both conventional electret (ECM) type microphone, and to power the newer MEMS all-silicon type microphones.

1.4 Digital Interfaces

Command and control of the device is accomplished using a 2-wire/3-wire/4-wire serial control interface. This is a simple, but highly flexible interface that is compatible with many commonly used command and control serial data protocols and host drivers.

Digital audio input/output data streams are transferred to and from the device separately from command and control. The digital audio data interface supports either I2S or PCM audio data protocols, and is compatible with commonly used industry standard devices that follow either of these two serial data formats.

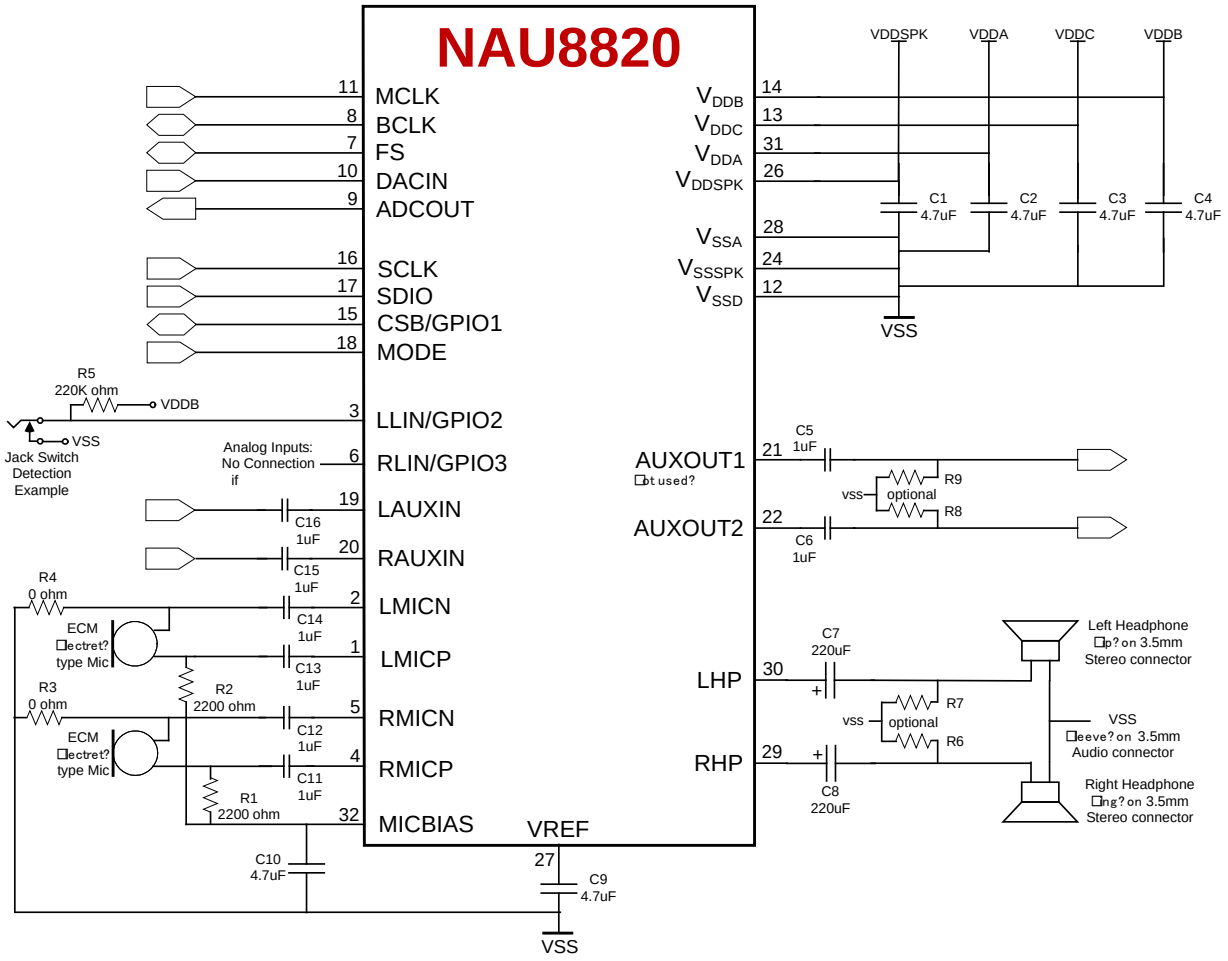
1.5 Clock Requirements

The clocking signals required for the audio signal processing, audio data I/O, and control logic may be provided externally, or by optional operation of a built-in PLL (Phase Locked Loop). An external master clock (MCLK) signal must be active for analog audio logic paths to align with control register updates, and is required as the reference clock input for the PLL, if the PLL is used.

The PLL is provided as a low cost, zero external component count optional method to generate required clocks in almost any system. The PLL is a fractional-N divider type design, which enables generating accurate desired audio sample rates derived from a very wide range of commonly available system clocks.

The frequency of the system clock provided as the PLL reference frequency may be any stable frequency in the range between 8MHz and 33MHz. Because the fractional-N multiplication factor is a very high precision 24-bit value, any desired sample rate supported by the NAU8820 can be generated with very high accuracy, typically limited by the accuracy of the external reference frequency. Reference clocks and sample rates outside of these ranges are also possible, but may involve performance tradeoffs and increased design verification.

2 Application Information



2.1 Typical Application Schematic

Figure 2: Schematic with recommended external components for typical application with AC-coupled headphones and stereo electret (ECM) style microphones.

Note 1: All non-polar capacitors are assumed to be low ESR type parts, such as with MLC construction or similar. If capacitors are not low ESR, additional 0.1ufd and/or 0.01ufd capacitors may be necessary in parallel with the bulk 4.7ufd capacitors on the supply rails.

Note 2: Load resistors to ground on outputs may be helpful in some applications to insure a DC path for the output capacitors to charge/discharge to the desired levels. If the output load is always present and the output load provides a suitable DC path to ground, then the additional load resistors may not be necessary. If needed, such load resistors are typically a high value, but a value dependent upon the application requirements.

Note 3: To minimize pops and clicks, large polarized output capacitors should be a low leakage type.

Note 4: Depending on the microphone device and PGA gain settings, common mode rejection can be improved by choosing the resistors on each node of the microphone such that the impedance presented to any noise on either microphone wire is equal.

Note 5: Unused analog input pins should be left as no-connection.

Note 6: Unused digital input pins should be tied to ground.

2.2 Power Consumption

The NAU8820 has flexible power management capability which allows sections not being used to be powered down, to draw minimum current in battery-powered applications. The following table shows typical power consumption in different operating conditions. The "off" condition is the initial power-on state with all subsystems powered down, and with no applied clocks.

Mode	Conditions	VDDA = 3V	VDDC = 1.8V	VDDB = 3V	Total Power
		mA	mA	mA	mW
OFF		0.008	0.001	0.0003	0.025
Sleep	VREF maintained @ 300kΩ, no clocks,	0.008	0.001	0.0003	0.025
	VREF maintained @ 75kΩ, no clocks,	0.014	0.001	0.0003	0.045
	VREF maintained @ 5kΩ, no clocks,	0.259	0.001	0.0003	0.781
Stereo Record	8kHz, 0.9Vrms input signal	6.44	1.07	0.10	21.5
	8kHz, 0.9Vrms input signal, PLL on	7.42	1.33	0.10	24.9
Stereo Playback	16Ω HP, 44.1kHz, quiescent	7.25	6.10	0.03	32.8
	16Ω HP, 44.1kHz, quiescent, PLL on	9.77	7.53	0.025	42.9
	16Ω HP, 44.1kHz, 0.6 Vrms sine wave	21.3	6.28	0.015	75.2
	16Ω HP, 44.1kHz, 0.6Vrms sine, PLL on	23.8	7.72	0.015	85.3

Table 1: Typical Power Consumption in Various Application Modes.

2.3 Supply Currents of Specific Blocks

The NAU8820 can be programmed to enable/disable various analog blocks individually, and the current to some of the major blocks can be reduced with minimum impact on performance. The table below shows the change in current consumed with different register settings. Sample rate settings affect current consumption of VDDC supply. Lower sampling rates draw lower current.

Register		Function	Bit	VDDA current increase/ Decrease when enabled
Dec	Hex			
1	01	Power Management 1	REFIMP[1:0]	+100µA for 80kΩ and 300kΩ +260µA for 3kΩ
			IOBUFEN[2]	+100µA
			ABIASEN[3]	+600µA
			MICBIASEN[4]	+540µA
			PLLEN[5]	+2.5 mA +1/5mA from VDDC with clocks applied
			AUX2MXEN[6]	+200µA
			AUX1MXEN[7]	+200µA
			DCBUFEN[8]	+140µA
2	02	Power Management 2	LADCEN[0]	+2.3 mA with 64X OSR +3.3 mA with 128X OSR
			RADCEN[1]	+2.3 mA with 64X OSR +3.3 mA with 128X OSR
			LPGAEN[2]	+300µA
			RPGAEN[3]	+300µA
			LBSTEN[4]	+650µA
			RBSTEN[5]	+650µA
			SLEEP[6]	Same as PLLEN (R1[5])
			LHPEN[7]	+800µA
			RHPEN[8]	+800µA
3	03	Power Management 3	LDACEN[0]	+1.6 mA with 64X OSR +1.7 mA with 128X OSR
			RDACEN[1]	+1.6 mA with 64X OSR +1.7 mA with 128X OSR
			LMIXEN[2]	+250µA
			RMIXEN[3]	+250µA
			AUXOUT2EN[7] AUXOUT1EN[8]	+225µA +225µA
58	3A	Power Management 4	IBIADJ[1:0]	-1.2mA with IBIADJ at 11
			REGVOLT[2:3]	
			MICBIASM[4]	
			LPADC[6]	-1.1mA with no SNR decrease @ 8kHz
			LPIPBST[7]	-600µA with no SNR decrease @ 8kHz
			LPDAC[8]	-1.1mA with 1.4dB SNR decrease @ 44.1kHz

Table 2: VDDA 3.3V Supply Current in Various Modes

3 Appendix A: Digital Filter Characteristics

Parameter	Conditions	Min	Typ	Max	Units
ADC Filter					
Passband	+/- 0.015dB	0		0.454	fs
	-6dB		0.5		fs
Passband Ripple				+/-0.015	dB
Stopband		0.546			fs
Stopband Attenuation	f > 0.546*fs	-60			dB
Group Delay			28.25		1/fs
ADC High Pass Filter					
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		Hz
	-0.1dB		21.6		Hz
DAC Filter					
Passband	+/- 0.035dB	0		0.454	fs
	-6dB		0.5		fs
Passband Ripple				+/-0.035	dB
Stopband		0.546			fs
Stopband Attenuation	f > 0.546*fs	-55			dB
Group Delay			28		1/fs

Table 3: Digital Filter Characteristics

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1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region
3. Note that this delay applies only to the filters and does not include other latencies, such as from the serial data interface

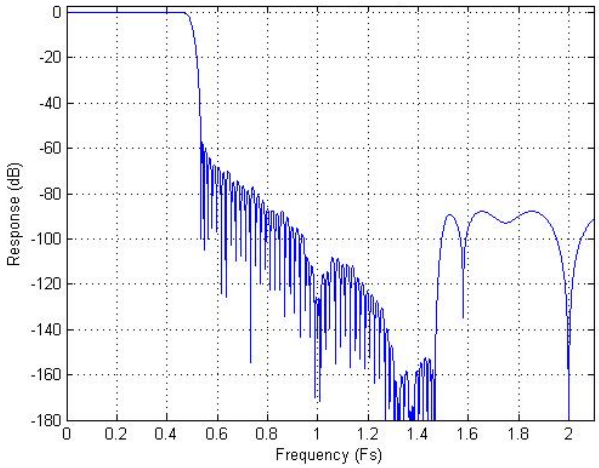


Figure 3: DAC Filter Frequency Response

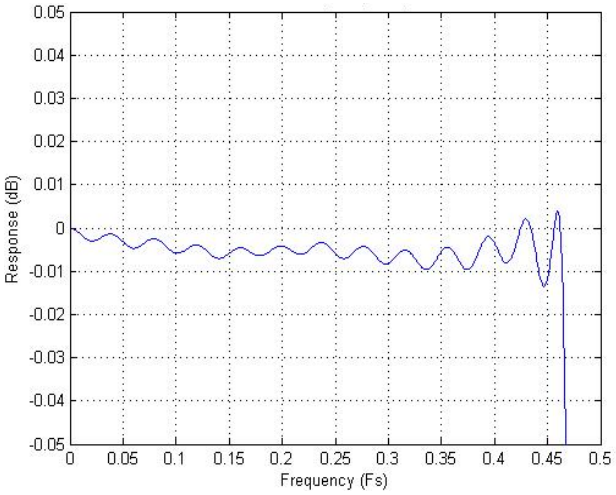


Figure 4: DAC Filter Ripple

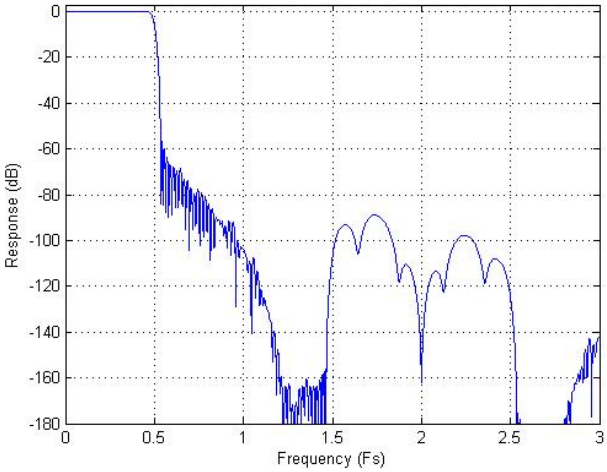


Figure 5: ADC Filter Frequency Response

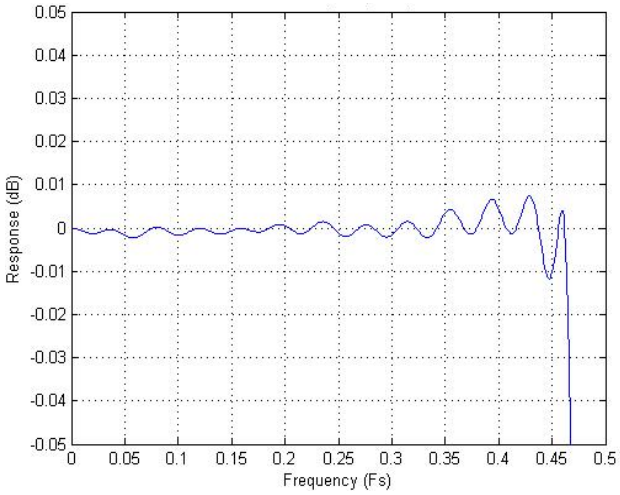


Figure 6: ADC Filter Ripple

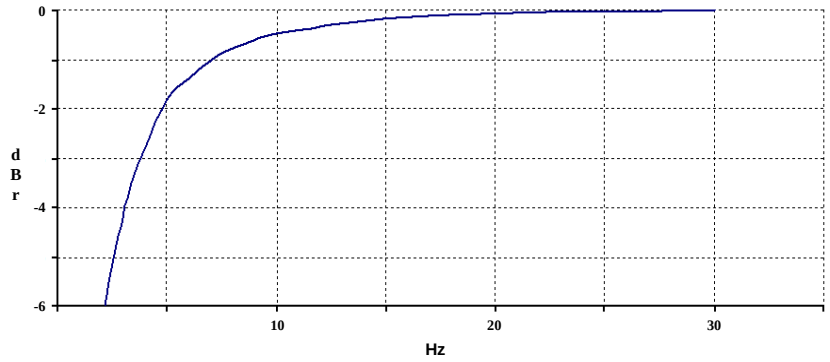


Figure 7: ADC Highpass Filter Response, Audio Mode

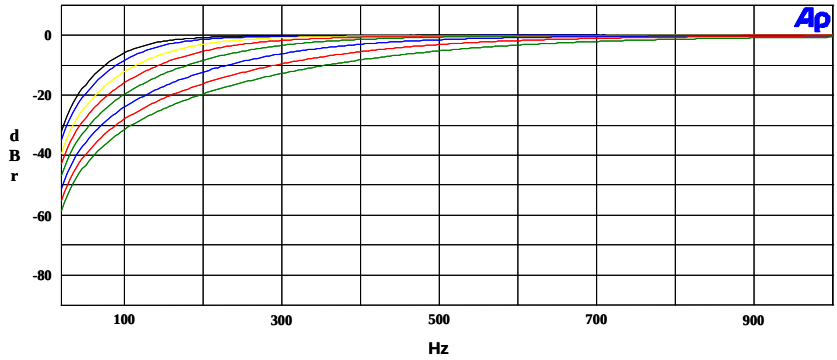


Figure 8: ADC Highpass Filter Response, HPF enabled, FS = 48kHz

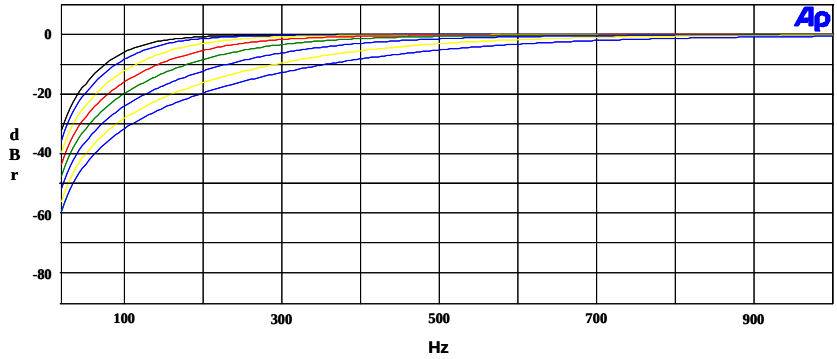


Figure 9: ADC Highpass Filter Response, HPF enabled, FS = 24kHz

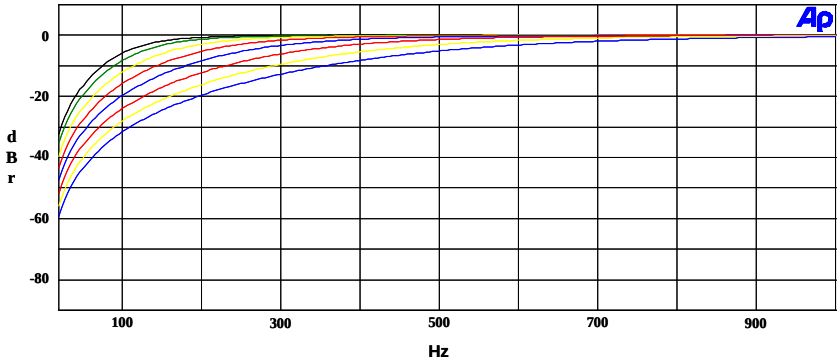


Figure 10: ADC Highpass Filter Response, HPF enabled, FS = 12kHz

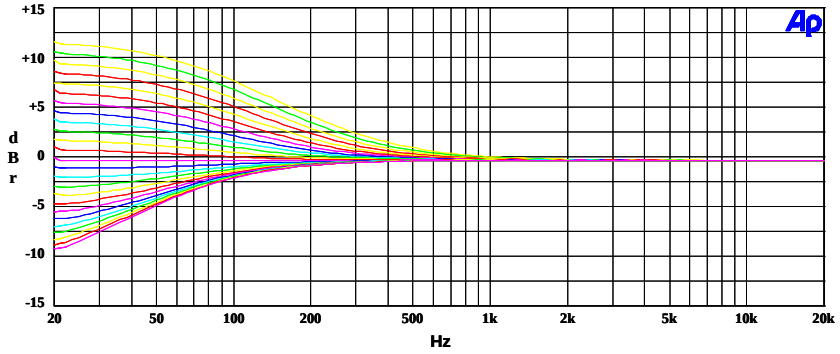


Figure 11: EQ Band 1 Gains for Lowest Cut-Off Frequency

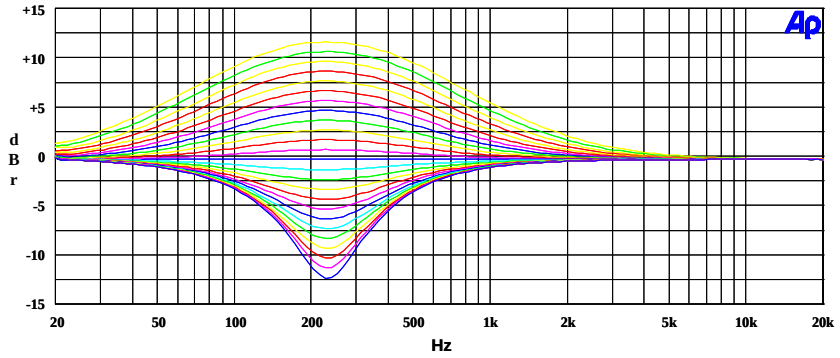


Figure 12: EQ Band 2 Peak Filter Gains for Lowest Cut-Off Frequency with EQ2BW = 0

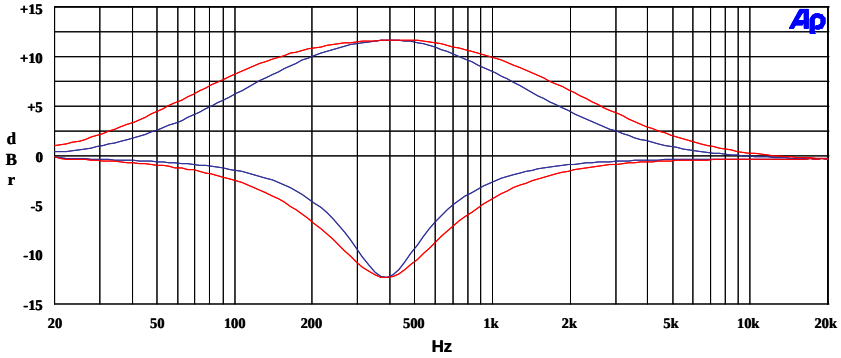


Figure 13: EQ Band 2, EQ2BW = 0 versus EQ2BW = 1

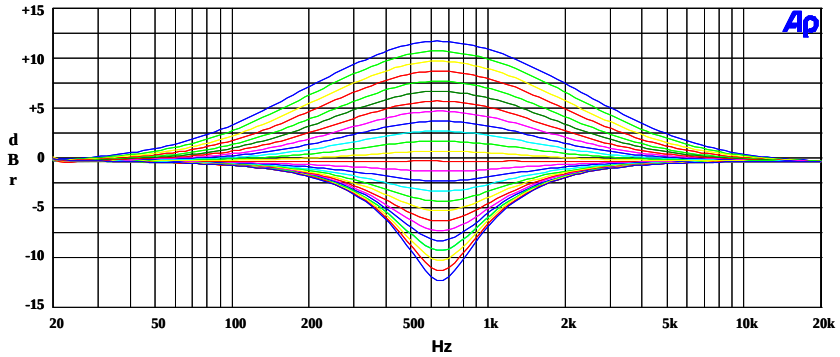


Figure 14: EQ Band 3 Peak Filter Gains for Lowest Cut-Off Frequency with EQ3BW = 0

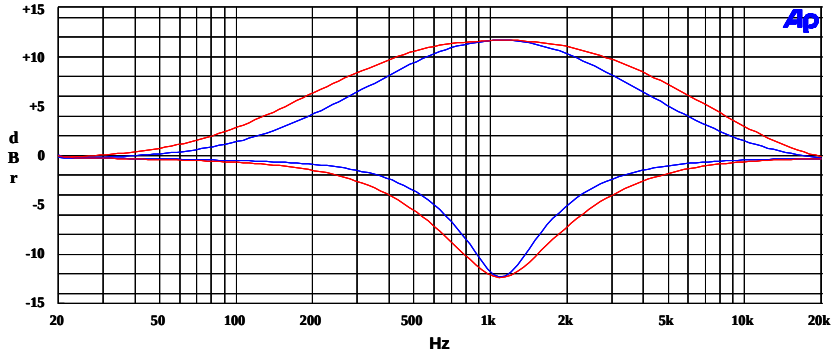


Figure 15: EQ Band 3, EQ3BW = 0 versus EQ3BW = 1

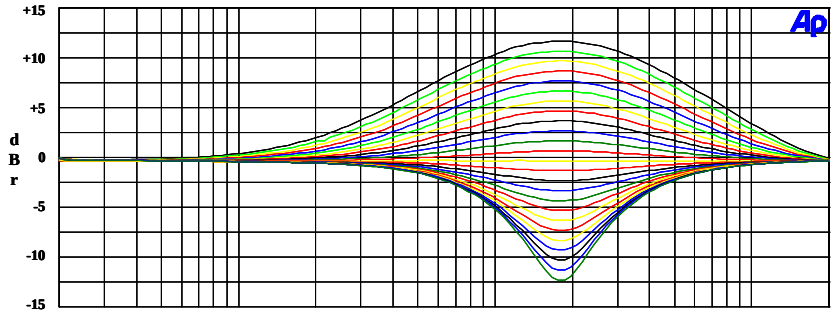


Figure 16: EQ Band 4 Peak Filter Gains for Lowest Cut-Off Frequencies with EQ4BW = 0

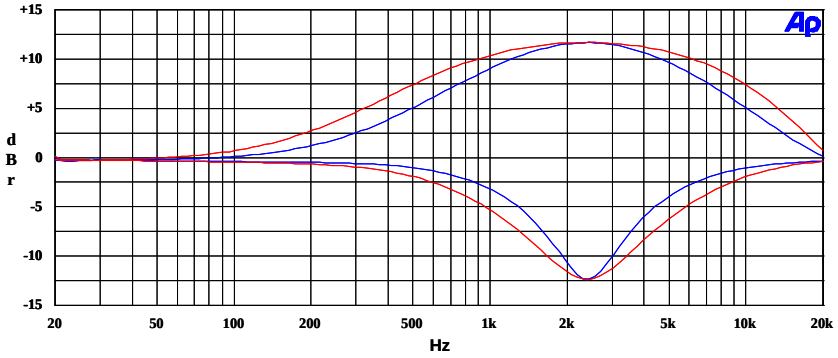


Figure 17: EQ Band 4, EQ4BW = 0 versus EQ4BW =1

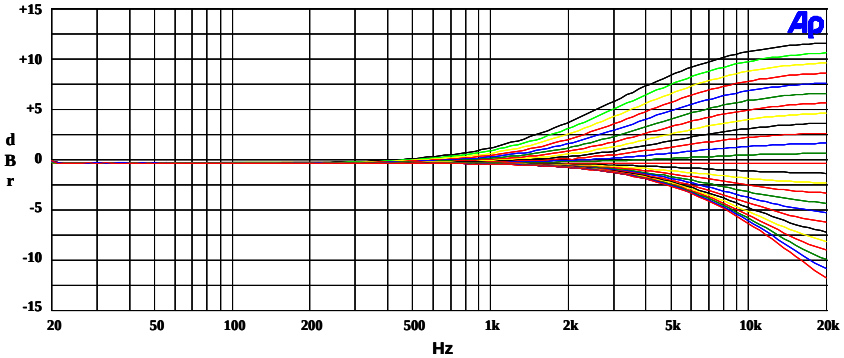


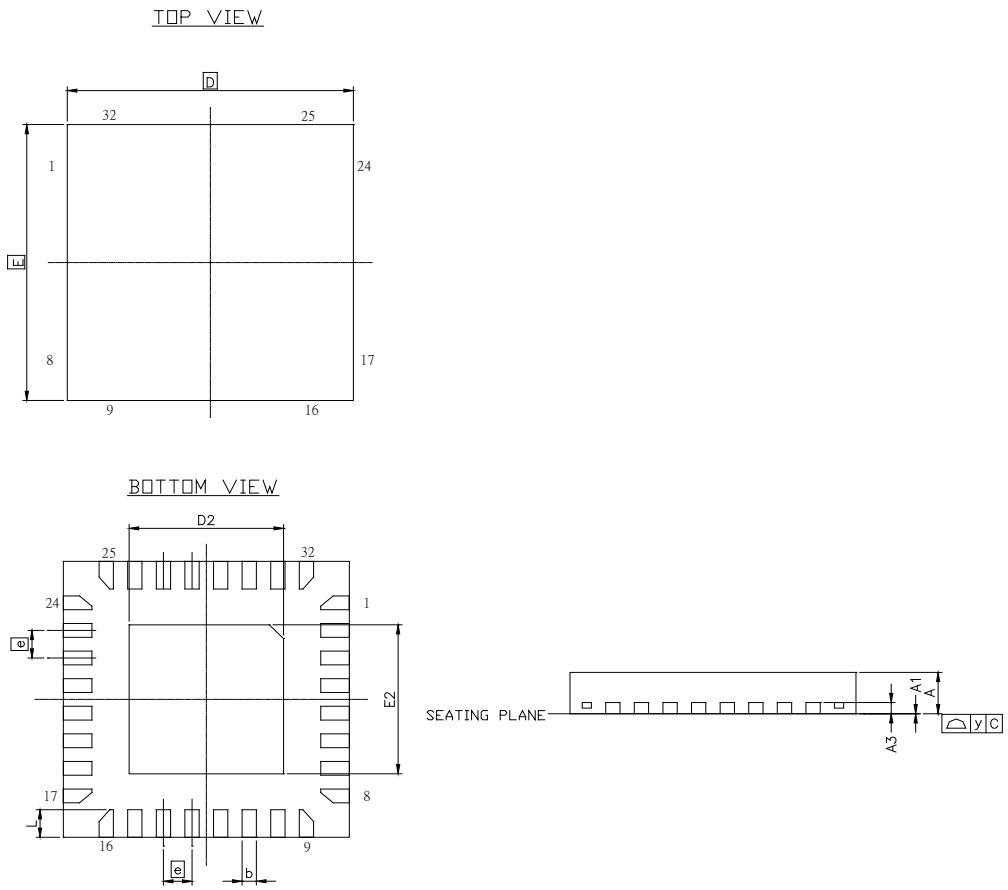
Figure 18: EQ Band 5 Gains for Lowest Cut-Off Frequency

4 Appendix D: Register Overview

DEC	HEX	NAME	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0	00	Software Reset	RESET (SOFTWARE)									
1	01	Power Management 1	DCBUFEN	AUX1MXEN	AUX2MXEN	PLLEN	MICBIASEN	ABIASEN	IOBUFEN	REFIMP		000
2	02	Power Management 2	RHPEN	NHPEN	SLEEP	RBSTEN	LBSTEN	RPGAEN	LPGAEN	RADCEN	LADCEN	000
3	03	Power Management 3	AUXOUT1EN	AUXOUT2EN	Reserved	Reserved	BIASGEN	RMIXEN	LMIXEN	RDACEN	LDACEN	000
General Audio Controls												
4	04	Audio Interface	BCLKP	LRP	WLEN		AIFMT		DACPHS	ADCPHS	MONO	050
5	05	Companding	Reserved			CMB8	DACCM		ADCCM		ADDAP	000
6	06	Clock Control 1	CLKM	MCLKSEL			BCLKSEL			Reserved	CLKIOEN	140
7	07	Clock Control 2	4WSPIEN	Reserved				SMPLR			SCLKEN	000
8	08	GPIO	Reserved			GPIO1PLL		GPIO1PL	GPIO1SEL			000
9	09	Jack Detect 1	JCKMIDEN		JCKDEN	JCKDIO		Reserved				000
10	0A	DAC Control	Reserved		SOFTMT	Reserved		DACOS	AUTOMT	RDACPL	LDACPL	000
11	0B	Left DAC Volume	LDACVU	LDACGAIN								0FF
12	0C	Right DAC Volume	RDACVU	RDACGAIN								0FF
13	0D	Jack Detect 2	Reserved	JCKDOEN1				JCKDOEN0				000
14	0E	ADC Control	HPFEN	HPFAM	HPF			ADCOS	Reserved	RADCPL	LADCPL	100
15	F	Left ADC Volume	LADCVU	LADCGAIN								0FF
16	10	Right ADC Volume	RADCVU	RADCGAIN								0FF
17	11	Reserved										
Equalizer												
18	12	EQ1-low cutoff	EQM	Reserved	EQ1CF		EQ1GC					12C
19	13	EQ2-peak 1	EQ2BW	Reserved	EQ2CF		EQ2GC					02C
20	14	EQ3-peak 2	EQ3BW	Reserved	EQ3CF		EQ3GC					02C
21	15	EQ4-peak3	EQ4BW	Reserved	EQ4CF		EQ4GC					02C
22	16	EQ5-high cutoff	Reserved		EQ5CF		EQ5GC					02C
23	17	Reserved										
DAC Limiter												
24	18	DAC Limiter 1	DACLIMEN	DACLIMDCY				DACLIMATK				032
25	19	DAC Limiter 2	Reserved		DACLIMTHL			DACLIMBST				000
26	1A	Reserved										
Notch Filter												
27	1B	Notch Filter 1	NFCU1	NFCEN	NFCA0[13:7]							000
28	1C	Notch Filter 2	NFCU2	Reserved	NFCA0[6:0]							000
29	1D	Notch Filter 3	NFCU3	Reserved	NFCA1[13:7]							000
30	1E	Notch Filter 4	NFCU4	Reserved	NFCA1[6:0]							000
31	1F	Reserved										
ALC and Noise Gate Control												
32	20	ALC Control 1	ALCEN		Reserved	ALCMXGAIN			ALCMNGAIN			038
33	21	ALC Control 2	Reserved	ALCHT				ALCSL				00B
34	22	ALC Control 3	ALCM	ALCDCY				ALCATK				032
35	23	Noise Gate	Reserved				ALCTBLSEL	ALCNEN	ALCNTH			010
Phase Locked Loop												
36	24	PLL N	Reserved				PLLMCLK	PLLN				008
37	25	PLL K 1	Reserved			PLLK[23:18]						00C
38	26	PLL K 2	PLLK[17:9]									093
39	27	PLL K 3	PLLK[8:0]									0E9
40	28	Mic Bias Mode	Reserved								MICBIASM	000
Miscellaneous												
41	29	3D control	Reserved					3DDEPTH				000
42	2A	Reserved										
43	2B	Reserved										
44	2C	Input Control	MICBIASV		RLINRPGA	RMICNRPGA	RMICPRPGA	Reserved	LLINLPGA	LMICNLPGA	LMICPLPGA	033
45	2D	Left Input PGA Gain	LPGAU	LPGAZC	LPGAMT	LPGAGAIN						010
46	2E	Right Input PGA Gain	RPGAU	RPGAZC	RPGAMT	RPGAGAIN						010
47	2F	Left ADC Boost	LPGABST	Reserved	LPGABSTGAIN			Reserved	LAUXBSTGAIN			100
48	30	Right ADC Boost	RPGABST	Reserved	RPGABSTGAIN			SPKSTAGE	RAUXBSTGAIN			100
49	31	Output Control	Reserved		LDACRMX	RDACLMX	AUX1BST	AUX2BST	SPKBST	TSEN	AOUTIMP	002
50	32	Left Mixer	LAUXMXGAIN			LAUXLMX	LBYPMXGAIN			LBYPLMX	LDACLMX	001
51	33	Right Mixer	RAUXMXGAIN			RAUXRMX	RBYPMXGAIN			RBYPRMX	RDACRMX	001
52	34	LHP Volume	LHPVU	LHPZC	LHPMUTE	LHPGAIN						039
53	35	RHP Volume	RHPVU	RHPZC	RHPMUTE	RHPGAIN						039
54	36	Reserved										
55	37	Reserved										
56	38	AUX2 Mixer	Reserved		AUXOUT2MT	Reserved		AUX1MIX>2	LADCAUX2	LMIXAUX2	LDACAUX2	001
57	39	AUX1 Mixer	Reserved		AUXOUT1MT	AUX1HALF	LMIXAUX1	LDACAUX1	RADCAUX1	RMIXAUX1	RDACAUX1	001
58	3A	Power Management 4	LPDAC	LPIPBST	LPADC	Reserved	MICBIASM	REGVOLT		IBADJ		000
PCM Time Slot and ADCOUT Impedance Option Control												
59	3B	Left Time Slot	LTSLOT[8:0]									000
60	3C	Misc	PCMTSEN	TRI	PCM8BIT	PUDEN	PUDPE	PUDPS	Reserved	RTSLOT[9]	LTSLOT[9]	020
61	3D	Right Time Slot	RTSLOT[8:0]									000
Silicon Revision and Device ID												
62	3E	Device Revision #	Reserved	REV								xxx
63	3F	Device ID	ID									01A

Package Dimensions

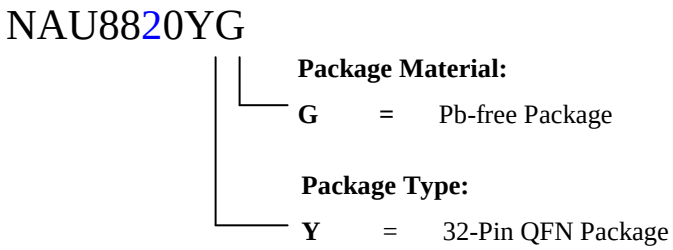
32-lead Plastic QFN; 5X5mm^2, 1.0mm thickness, 0.5mm lead pitch



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
D2	2.60	2.70	2.80	0.1024	0.1063	0.1102
E	5.00 BSC			0.197 BSC		
E2	2.60	2.70	2.80	0.1024	0.1063	0.1102
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		

5 Ordering Information

Nuvoton Part Number Description



Version History

VERSION	DATE	PAGE	DESCRIPTION
A0.0	February, 2008	NA	Preliminary Revision
A0.6	May 2008	NA	Preliminary Revision
A0.86	September 2008	NA	Preliminary Revision
Rev1.0	Mar. 05, 2009	NA	Correct minor errata; minor text improvements
Rev 1.1	Jan.15, 2014	1	Updated AECQ100 description
Rev 1.2	March 2016	9	Add Important Notice
Rev 1.3	June 28, 2016	20	Update package information

Table 4: Version History

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

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