User's Guide

TPS54320 Step-Down Converter Evaluation Module User's Guide

Table of Contents

List of Figures

List of Tables

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

This user's guide contains background information for the TPS54320 as well as support documentation for the TPS54320 evaluation module (HPA513). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54320.

1.1 Background

The TPS54320 dc/dc converter is designed to provide up to a 3 A output. The TPS54320 implements split input power rails with separate input voltage inputs for the power stage and control circuitry. The power stage input (PVIN) is rated for 1.6 V to 17 V while the control input (VIN) is rated for 4.5 to 17 V. The TPS54320 provides both inputs but is designed and tested using the PVIN connected to VIN. Rated input voltage and output current range for the evaluation module are given in Table 1-1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54320 regulator. The switching frequency is externally set at a nominal 480 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS54320 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS54320 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54320 provides adjustable slow start, tracking and undervoltage lockout inputs. The absolute maximum input voltage is 20 V for the TPS54320.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS54320	VIN = 8 V to 17 V (VIN start voltage = 6.806 V)	0 A to 3 A

1.2 Performance Specification Summary

A summary of the TPS54320 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of 12 V and an output voltage of 3.3 V, unless otherwise specified. The TPS54320 is designed and tested for V_{IN} = 8 V to 17 V with the VIN and PVIN pins connect together with the JP1 jumper. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. TPS54320 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range (PVIN = VIN)			8	12	17	V
V_{IN} start voltage				6.806		V
V_{IN} stop voltage				4.824		V
Output voltage set point				3.3		V
Output current range	V_{IN} = 8 V to 17 V		0		3	A
Line regulation	I_O = 3 A, V_{IN} = 8 V to 17 V			± 0.02		%
Load regulation	V_{IN} = 12 V, I_O = 0 A to 3 A			± 0.02		%
Load transient response	I_O = 0.75 A to 1.5 A	Voltage change		90		mV
		Recovery time		70		µs
	I_O = 1.5 A to 0.75 A	Voltage change		80		mV
		Recovery time		70		µs
Loop bandwidth	V_{IN} = 12 V, I_O = 3 A			32.1		kHz
Phase margin	V_{IN} = 12 V , I_O = 3 A			82		°
Input ripple voltage	I_O = 3 A			480		mV_{PP}
Output ripple voltage	I_O = 3 A			10		mV_{PP}
Output rise time				3.5		ms
Operating frequency				480		kHz
Maximum efficiency	TPS54320EVM-513, V_{IN} = 8 V, I_O = 0.9 A			94.9		%

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54320. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

The output voltage is set by the resistor divider network of R8 and R9. R9 is fixed at 10 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R8. Changing the value of R8 can change the output voltage above 0.8 V. The value of R8 for a specific output voltage can be calculated using Equation 1.

$$R8 = \frac{10\ k\Omega\left(V_{OUT} - 0.8\ V\right)}{0.8\ V} \tag{1}$$

Table 1-3 lists the R8 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 135 ns, and the maximum duty cycle is less than 95%. The values given in Table 1-3 are standard values, not the exact value calculated using Equation 1.

Table 1-3. Output Voltages Available

Output Voltage (V)	R_8 Value (kΩ)
1.8	12.4
2.5	21.5
3.3	31.6
5	52.3

1.3.2 Slow Start Time

The slow start time can be adjusted by changing the value of C7. Use Equation 2 to calculate the required value of C7 for a desired slow start time

$$C7(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref(V)} \tag{2}$$

The EVM is set for a slow start time of 3.5 msec using C7 = 0.01 µF.

1.3.3 Track In

The TPS54320 can track an external voltage during start up. The J5 connector is provided to allow connection to that external voltage. Ratio-metric or simultaneous tracking can be implemented using resistor divider R5 and R6. See the TPS54320 data sheet (SLVS982) for details.

1.3.4 Adjustable UVLO

The under voltage lock out (UVLO) can be adjusted externally using R1 and R2. The EVM is set for a start voltage of 6.528 V and a stop voltage of 6.190 V using R1 = 511 kΩ and R2 = 100 kΩ. Use Equation 3 and Equation 4 to calculate the required resistor values for different start and stop voltages.

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \tag{3}$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \tag{4}$$

1.3.5 Input Voltage Rails

The EVM is designed to accommodate different input voltage levels for the power stage and control logic. During normal operation, the PVIN and VIN inputs are connected together using a jumper across JP1. The single input voltage is supplied at J1. If desired, these two input voltage rails may be separated by removing the jumper across JP1. Two input voltages, which could be at different voltages, must then be provided at both J1 and J2.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54320 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input / Output Connections

The TPS54320 is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying 2 A must be connected to J1 through a pair of 20 AWG wires. The jumper across JP1 must be in place. See Section 1.3.5 for split input voltage rail operation. The load must be connected to J3 through a pair of 20 AWG wires. The maximum load current capability must be 3 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP8 is used to monitor the output voltage with TP9 as the ground reference.

Table 2-1. EVM Connectors and Test Points

Reference Designator	Function
J1	PVIN input voltage connector. (see Table 1-1 for V_{IN} range).
J2	VIN input voltage connector. Not normally used.
J3	V_{OUT}, 3.3 V at 3 A maximum.
J4	2-pin header for tracking output and ground.
J5	2-pin header for tracking voltage input and ground.
JP1	PVIN to VIN jumper. Normally closed to tie VIN to PVIN for common rail voltage operation.
JP2	2-pin header for enable. Connect EN to ground to disable, open to enable.
TP1	PVIN test point at PVIN connector.
TP2	GND test point at PVIN connector.
TP3	VIN test point at VIN connector.
TP4	GND test point at VIN connector.
TP5	PH test point.
TP6	Slow start / track in test point.
TP7	Test point between voltage divider network and output. Used for loop response measurements.
TP8	Output voltage test point at V_{OUT} connector.
TP9	GND test point at V_{OUT} connector.
TP10	PWRGD test point.

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 0.9 A and then decreases as the load current increases towards full load. Figure 2-1 shows the efficiency for the TPS54320 at an ambient temperature of 25°C.

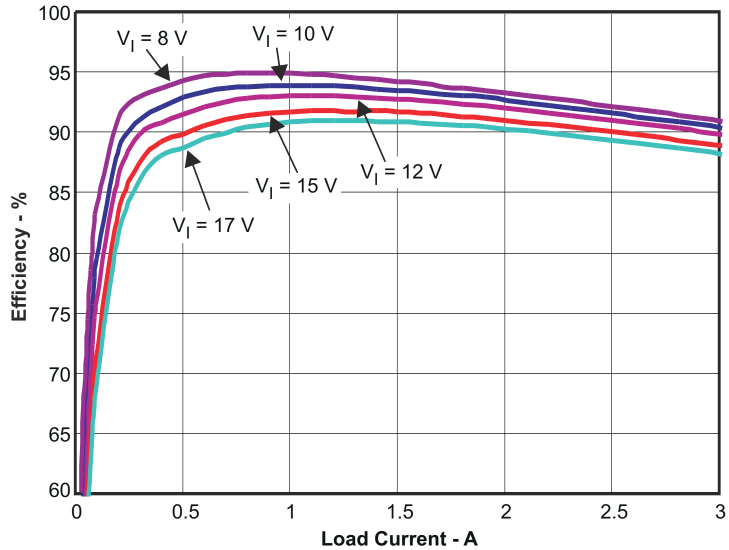

Figure 2-1. TPS54320 Efficiency

Figure 2-2 shows the efficiency for the TPS54320 at lower output currents below 0.20 A at an ambient temperature of 25°C.

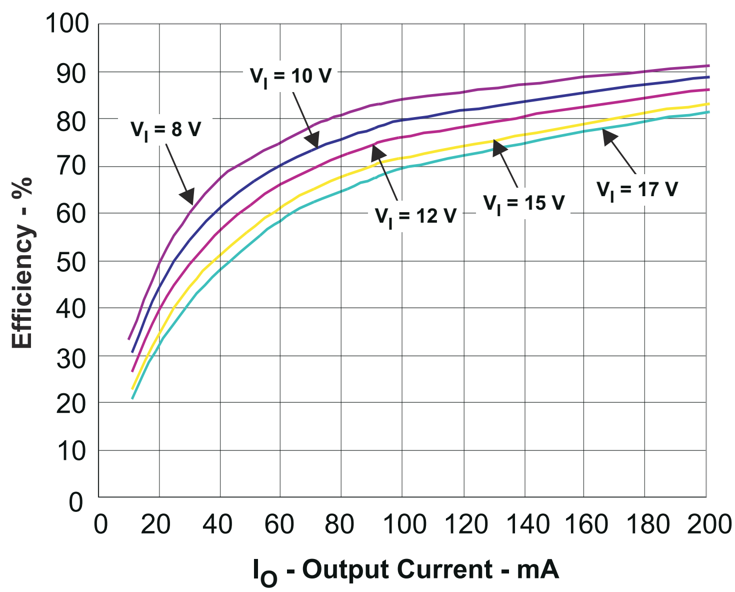

Figure 2-2. TPS54320 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

Figure 2-3 shows the load regulation for the TPS54320.

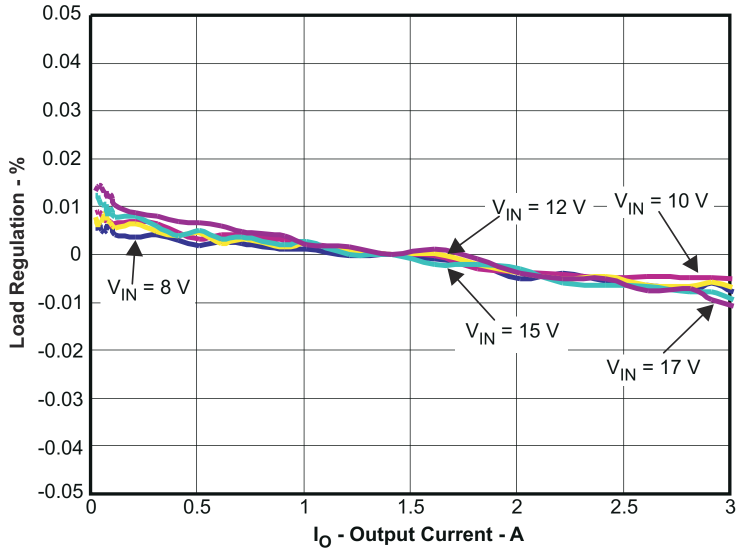

Figure 2-3. TPS54320 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 2-4 shows the line regulation for the TPS54320.

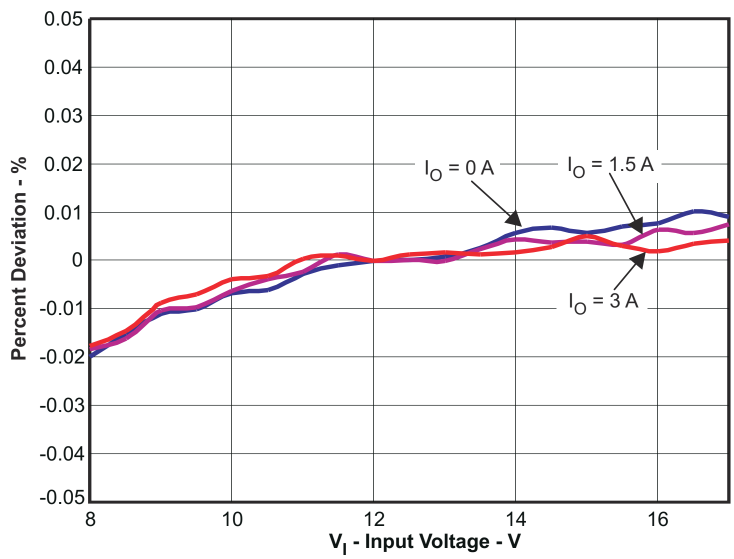

Figure 2-4. TPS54320 Line Regulation

2.5 Load Transients

Figure 2-5 shows the TPS54320 response to load transients. The current step is from 25% to 50% of maximum rated load at 12 V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

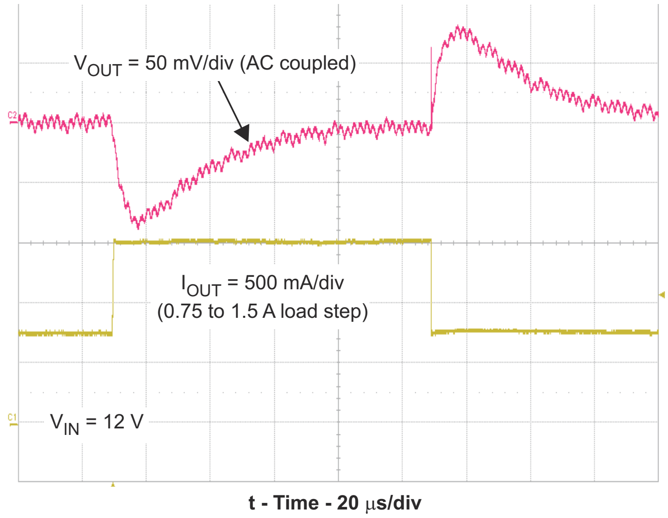

Figure 2-5. TPS54320 Transient Response

2.6 Loop Characteristics

Figure 2-6 shows the TPS54320 loop-response characteristics. Gain and phase plots are shown for V_{IN} of 12 V. Load current for the measurement is 3 A.

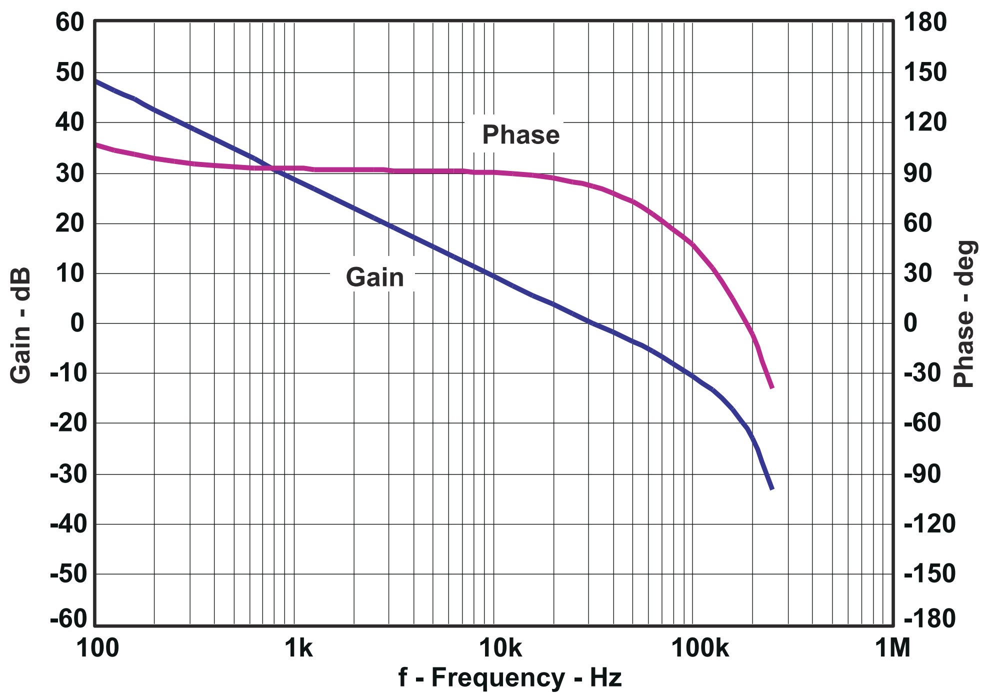

Figure 2-6. TPS54320 Loop Response

2.7 Output Voltage Ripple

Figure 2-7 shows the TPS54320 output voltage ripple. The output current is the rated full load of 3 A and V_{IN} = 12 V. The ripple voltage is measured directly across the output capacitors with a low inductance probe. Measuring at the output test points, TP8 and TP9, can pick up some radiated noise and give an erroneous measurement.

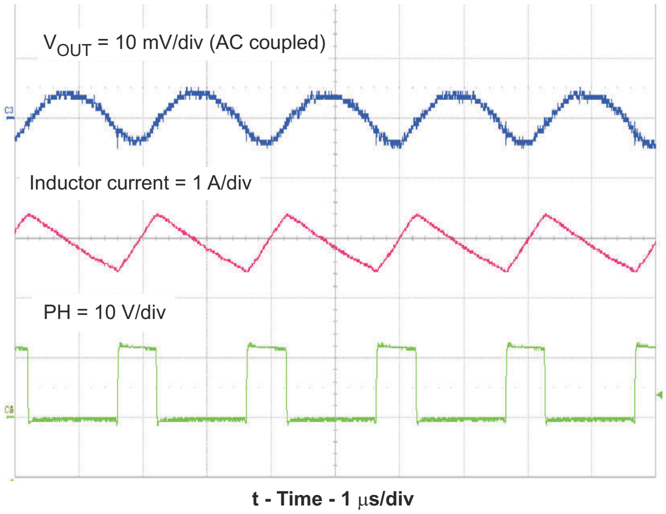

Figure 2-7. TPS54320 Output Ripple

2.8 Input Voltage Ripple

Figure 2-8 shows the TPS54320 input voltage. The output current is the rated full load of 3 A and V_{IN} = 12 V. The ripple voltage is measured directly across the input capacitors.

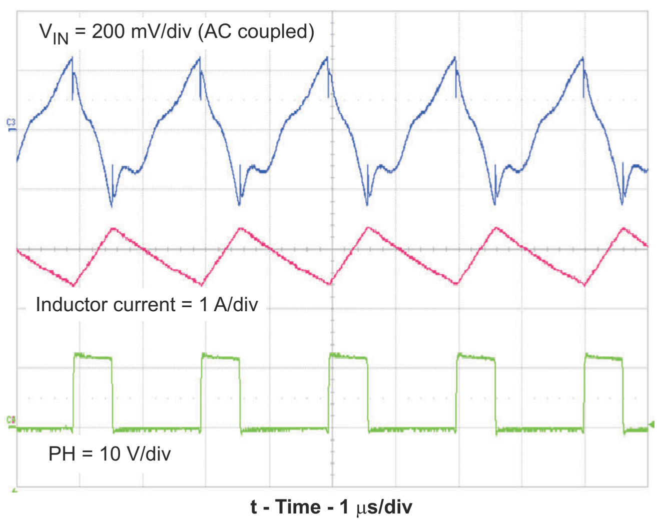

Figure 2-8. TPS54320 Input Ripple

2.9 Powering Up

Figure 2-9 and Figure 2-10 show the start-up waveforms for the TPS54320. In Figure 2-9, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R1 and R2 resistor divider network. In Figure 2-10, the input voltage is initially applied and the output is inhibited by using a jumper at JP2 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 3.3 V. The input voltage for these plots is 12 V and the load is 1.1Ω.

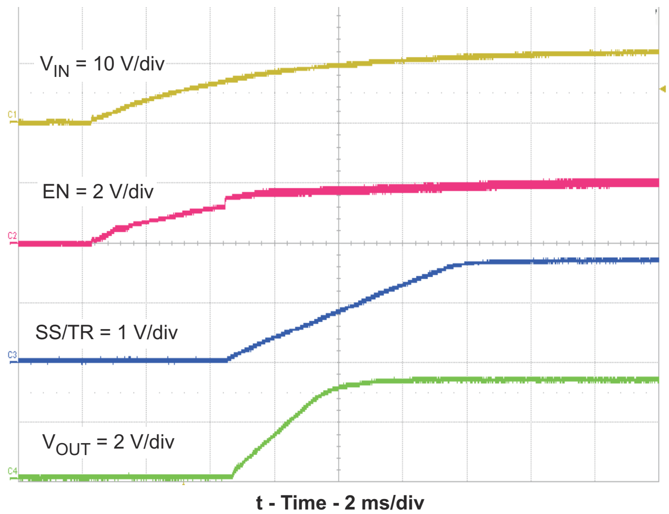

Figure 2-9. TPS54320 Start-Up Relative to V_{IN}

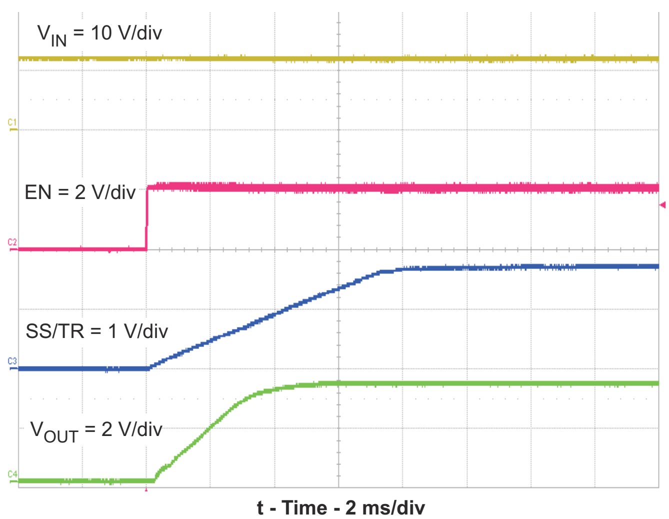

Figure 2-10. TPS54320 Start-Up Relative to Enable

2.10 Thermal Characteristics

This section shows a thermal image of the TPS54320 running at 12 V input and 3 A load. there is no air flow and the ambient temperature is 25°C. The peak temperature of the IC (59.5°C) is well below the maximum recommended operating condition listed in the data sheet of 150°C.

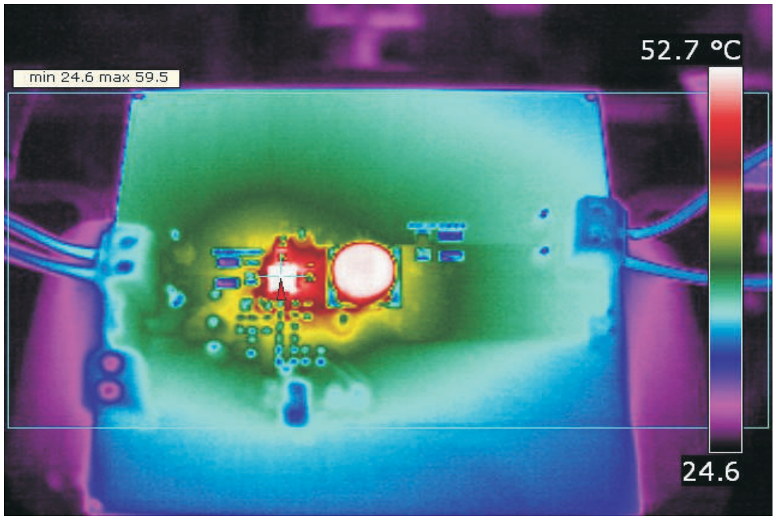

Figure 2-11. TPS54320 Thermal Image

3 Board Layout

This section provides a description of the TPS54320, board layout, and layer illustrations.

3.1 Layout

The board layout for the TPS54320 is shown in Figure 3-1 through Figure 3-3. The topside layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for PVIN, VIN, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54320 and a large area filled with ground. The bottom ground layer contains a ground plane only. The top side ground traces are connected to the bottom ground plane with multiple vias placed around the board including nine vias directly under the TPS54320 device to provide a thermal path from the top-side ground plane to the bottom-side ground plane.

The input decoupling capacitors (C2, and C3) and bootstrap capacitor (C5) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace at the J3 output connector. For the TPS54320, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply. Critical analog circuits such as the voltage setpoint divider, frequency set resistor, slow start capacitor and compensation components are terminated to ground using a wide ground trace separate from the power ground pour.

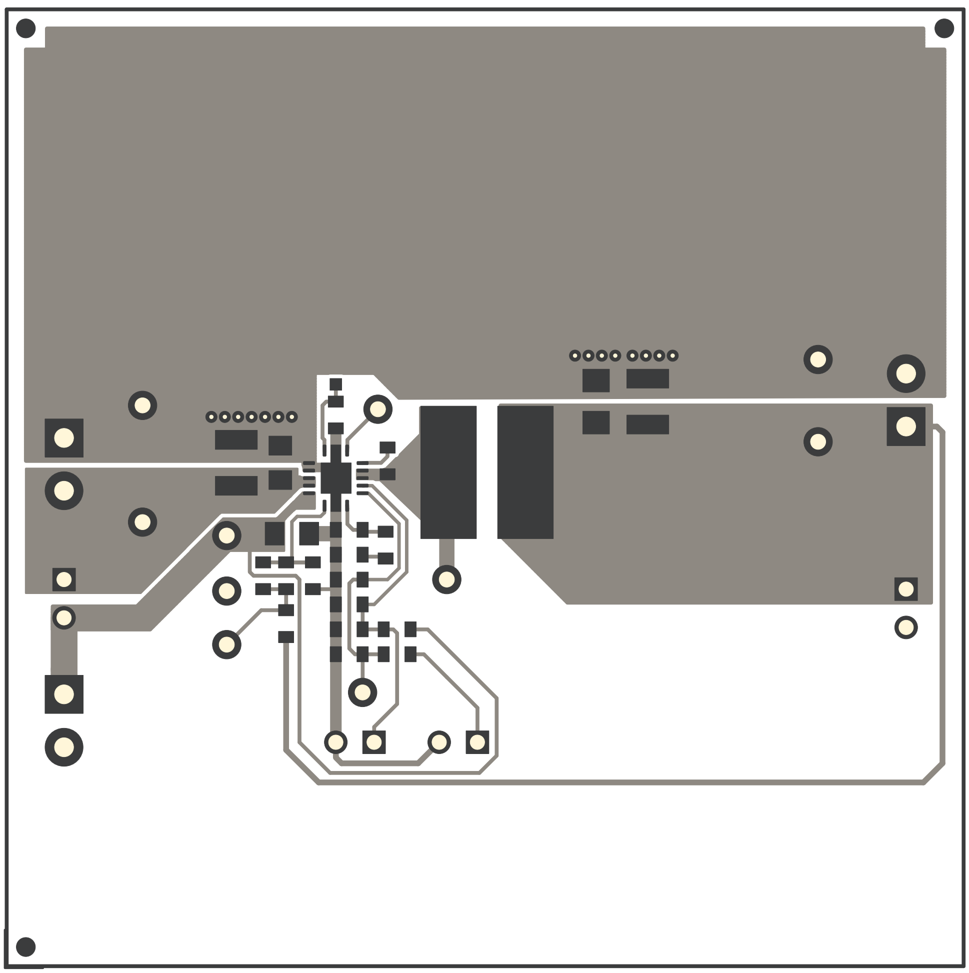

Figure 3-1. TPS54320 Top-Side Layout

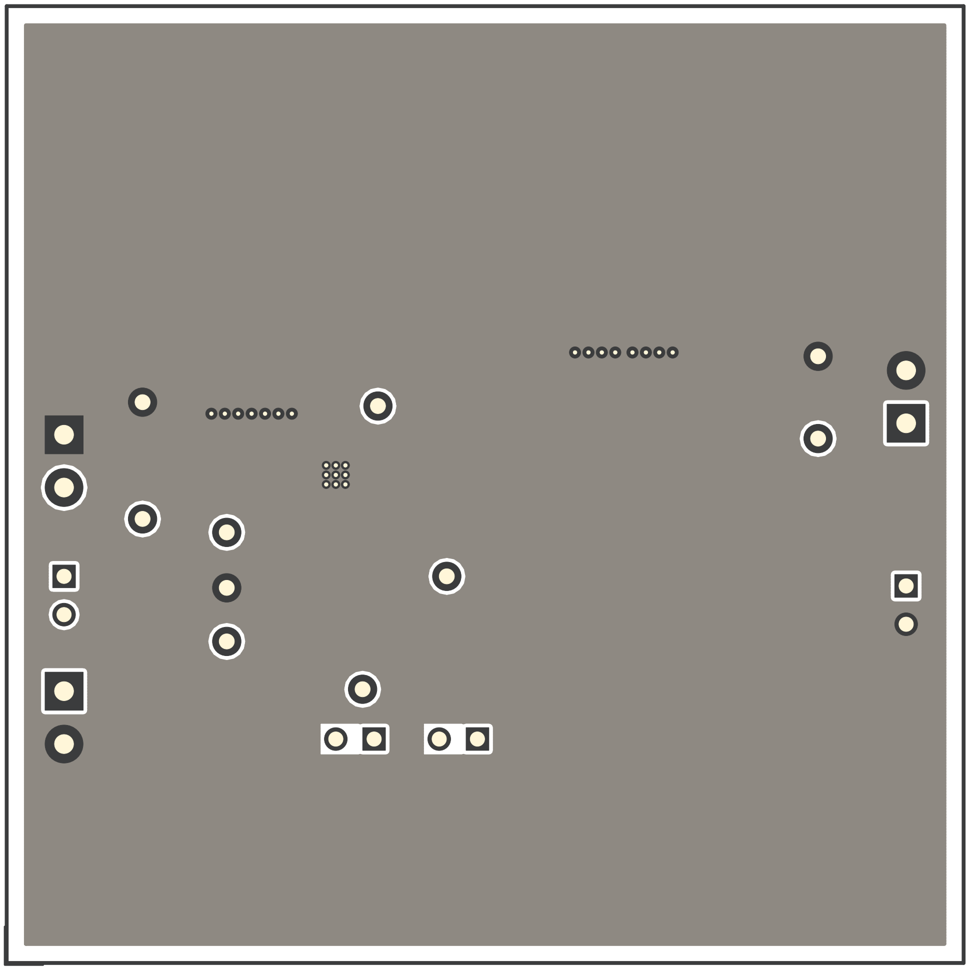

Figure 3-2. TPS54320 Bottom-Side Layout

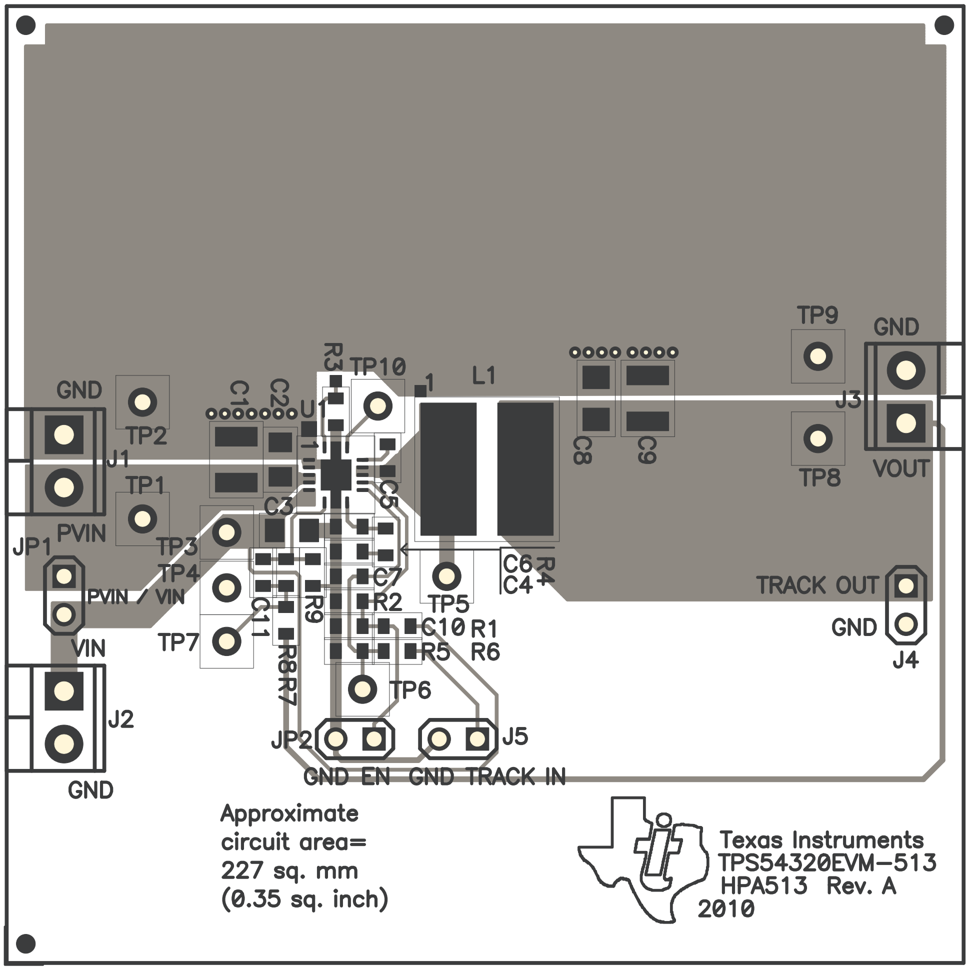

Figure 3-3. TPS54320 Top-Side Assembly

3.2 Estimated Circuit Area

The estimated printed circuit board area for the components used in this design is 0.35 in^2 (227 mm^2). This area does not include test point or connectors.

4 Schematic and Bill of Materials

This section presents the TPS54320 schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS54320.

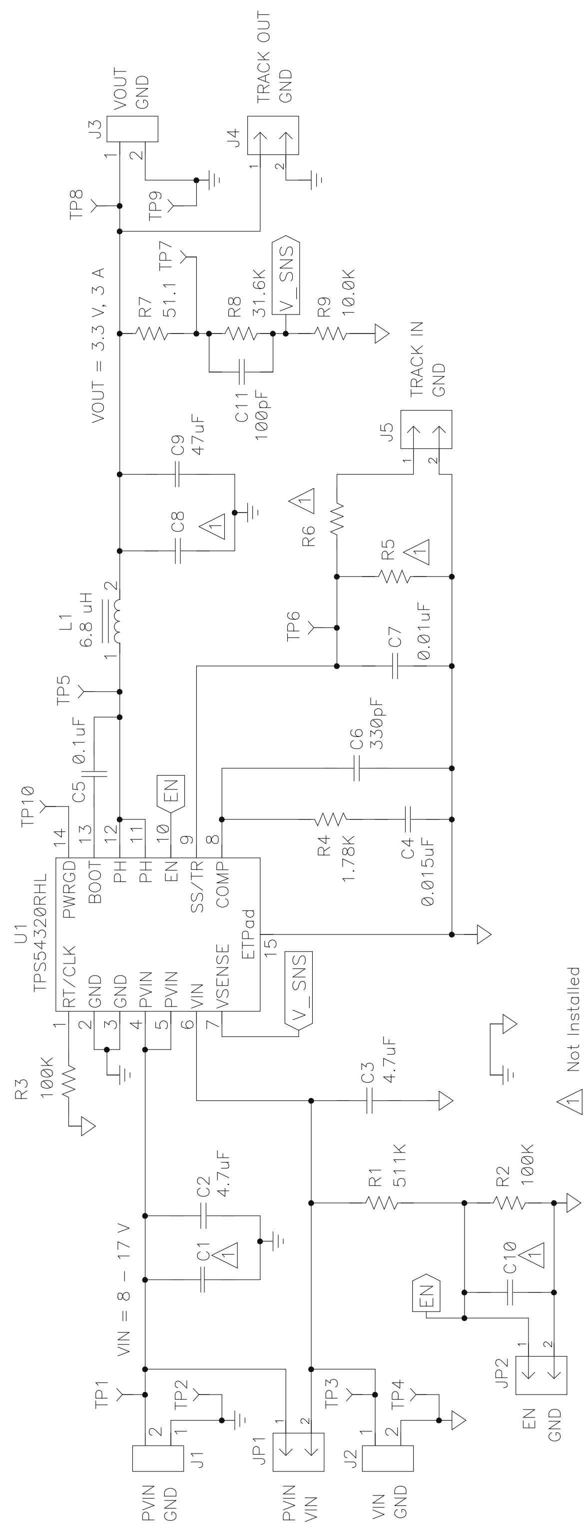

Figure 4-1. TPS54320EVM-513 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS54320.

Table 4-1. TPS54320 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
2	C2, C3	4.7μF	Capacitor, Ceramic, 25V, X5R, 10%	0805	Std	Std
1	C4	0.015μF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	C5	0.1μF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
1	C6	330pF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std
1	C7	0.01μF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std
1	C9	47μF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	Std	Std
1	C11	100pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	Std	Std
1	L1	6.8 μH	Inductor, SMT, 3.6A, 24 milliohm	8.7 mm x 8.6 mm	VLP8040T-6R8M	TDK
1	R1	511KΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R2, R3	100KΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	1.78KΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	51.1Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	31.6KΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	10.0KΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1	TPS54320RHL	IC, 17V Input, 3A Output, Sync. Step Down Switcher with Integrated FET	QFN14	TPS54320RHL	TI

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2010) to Revision A (October 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated the user's guide title	2

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d’usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。 http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered “Radio Frequency Products” in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry’s Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス· インスツルメンツ株式会社

東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265