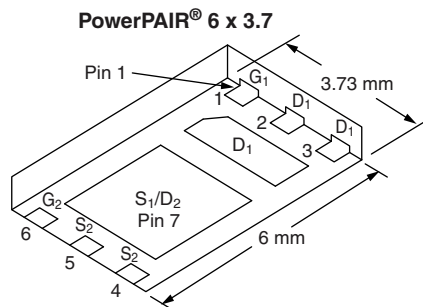




## N-Channel 30 V (D-S) MOSFETs

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
Channel-1	30	0.0093 at V <sub>GS</sub> = 10 V	16 <sup>a</sup>	7.7 nC
		0.0130 at V <sub>GS</sub> = 4.5 V	16 <sup>a</sup>	
Channel-2	30	0.0039 at V <sub>GS</sub> = 10 V	35 <sup>a</sup>	21.2 nC
		0.0053 at V <sub>GS</sub> = 4.5 V	35 <sup>a</sup>	



Ordering Information: SiZ730DT-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

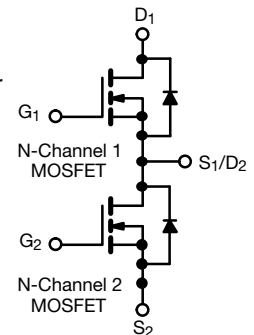
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFETs
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS  
COMPLIANT  
HALOGEN  
FREE

### APPLICATIONS

- System Power
  - Notebook
  - Server
- POL
- Synchronous Buck Converter



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)

Parameter	Symbol	Channel-1	Channel-2	Unit	
Drain-Source Voltage	V <sub>DS</sub>	30		V	
Gate-Source Voltage	V <sub>GS</sub>	± 20			
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	16 <sup>a</sup>	35 <sup>a</sup>	A
		T <sub>C</sub> = 70 °C	16 <sup>a</sup>	35 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	12.9 <sup>b, c</sup>	26.4 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	10.3 <sup>b, c</sup>	21.1 <sup>b, c</sup>	
Pulsed Drain Current (t = 300 μs)	I <sub>DM</sub>	70	100		
Continuous Source Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	16 <sup>a</sup>	35 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	3.2 <sup>b, c</sup>	3.8 <sup>b, c</sup>	
Single Pulse Avalanche Current	I <sub>AS</sub>	16	30		
Single Pulse Avalanche Energy	E <sub>AS</sub>	13	45	mJ	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	27	48	W
		T <sub>C</sub> = 70 °C	17	31	
		T <sub>A</sub> = 25 °C	3.9 <sup>b, c</sup>	4.6 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	2.5 <sup>b, c</sup>	3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260			

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Channel-1		Channel-2		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient <sup>b, f</sup>	R <sub>thJA</sub>	24	32	20	27	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	3.5	4.6	2	2.6	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 67 °C/W for channel-1 and 65 °C/W for channel-2.

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1	30			V	
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-2	30				
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1		34		mV/°C	
		$I_D = 250\text{ }\mu\text{A}$	Ch-2		32			
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1		-5			
		$I_D = 250\text{ }\mu\text{A}$	Ch-2		-5			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1		2.2	V	
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-2	1		2.2		
Gate Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch-1			$\pm 100$	nA	
			Ch-2			$\pm 100$		
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-1			1	$\mu\text{A}$	
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-2			1		
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1			5		
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-2			5		
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	15			A	
		$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-2	20				
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	Ch-1		0.0075	0.0093	$\Omega$	
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2		0.0032	0.0039		
		$V_{GS} = 4.5\text{ V}, I_D = 13\text{ A}$	Ch-1		0.0105	0.0130		
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	Ch-2		0.0043	0.0053		
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$	Ch-1		48		S	
		$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$	Ch-2		80			
<b>Dynamic<sup>a</sup></b>								
Input Capacitance	$C_{iss}$	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		830		pF	
			Ch-2		2370			
Output Capacitance	$C_{oss}$		Channel-2 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		185		
				Ch-2		475		
Reverse Transfer Capacitance	$C_{rss}$	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		Ch-1		80		nC
				Ch-2		220		
Total Gate Charge	$Q_g$		Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-1		15.6	24	
				Ch-2		43	65	
Gate-Source Charge	$Q_{gs}$	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$		Ch-1		7.7	12	
				Ch-2		21.2	32	
Gate-Drain Charge	$Q_{gd}$		Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	Ch-1		2.6		
				Ch-2		7		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		Ch-1	0.2	1	2	$\Omega$
				Ch-2	0.2	0.8	1.6	

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .



<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
<b>Dynamic<sup>a</sup></b>								
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		10	20	ns	
			Ch-2		20	40		
Rise Time	$t_r$		Ch-1		15	30		
			Ch-2		18	35		
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		15	30		
			Ch-2		30	60		
Fall Time	$t_f$		Ch-1		7	15		
			Ch-2		10	20		
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		5	10		
			Ch-2		10	20		
Rise Time	$t_r$		Ch-1		15	30		
			Ch-2		15	30		
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		17	35		
			Ch-2		30	60		
Fall Time	$t_f$		Ch-1		7	15		
			Ch-2		10	20		
<b>Drain-Source Body Diode Characteristics</b>								
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	Ch-1			16	A	
			Ch-2			35		
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$		Ch-1			70		
			Ch-2			100		
Body Diode Voltage	$V_{SD}$	$I_S = 10\text{ A}$ , $V_{GS} = 0\text{ V}$	Ch-1		0.8	1.2	V	
		$I_S = 10\text{ A}$ , $V_{GS} = 0\text{ V}$	Ch-2		0.78	1.2		
Body Diode Reverse Recovery Time	$t_{rr}$	Channel-1 $I_F = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		15	30	ns	
			Ch-2		25	50		
Body Diode Reverse Recovery Charge	$Q_{rr}$		Channel-2 $I_F = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		6	12	nC
				Ch-2		15	32	
Reverse Recovery Fall Time	$t_a$		Ch-1		9		ns	
			Ch-2		13			
Reverse Recovery Rise Time	$t_b$		Ch-1		6			
			Ch-2		12			

Notes:

- a. Guaranteed by design, not subject to production testing.  
 b. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

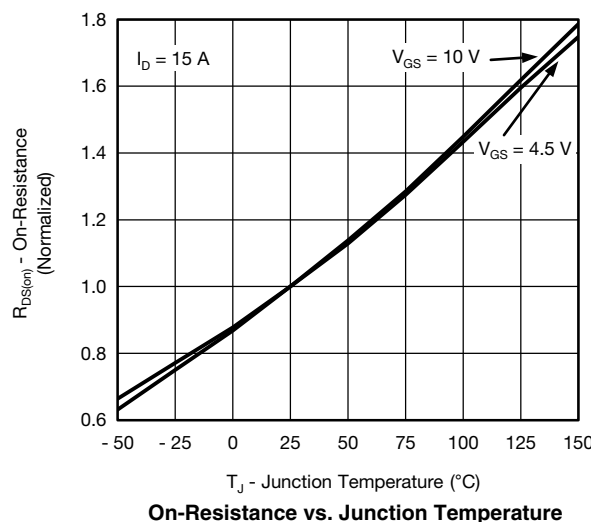
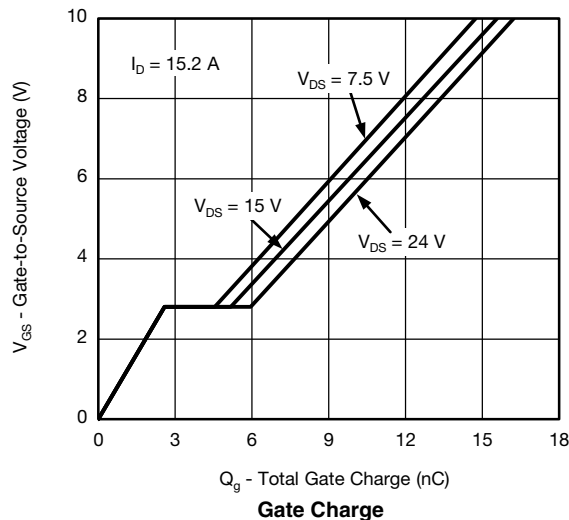
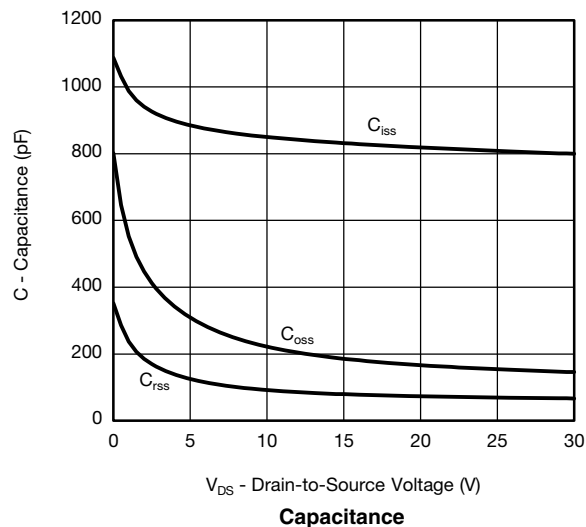
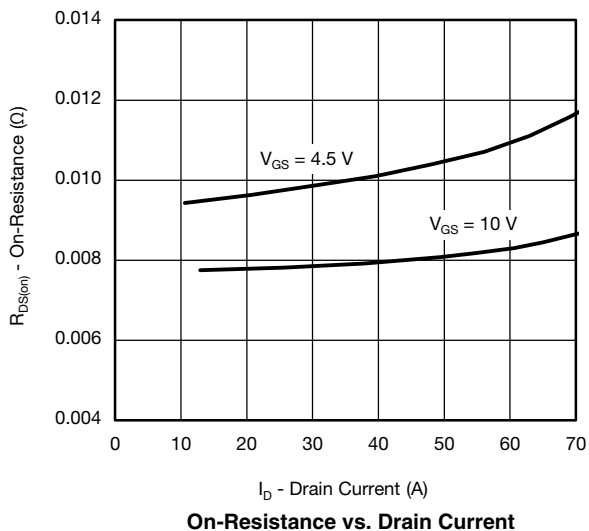
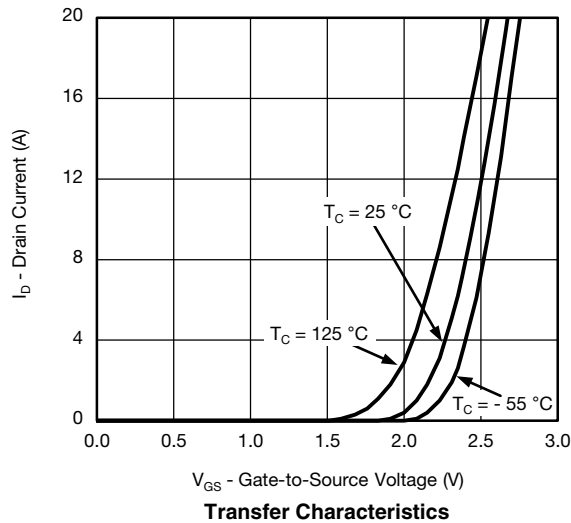
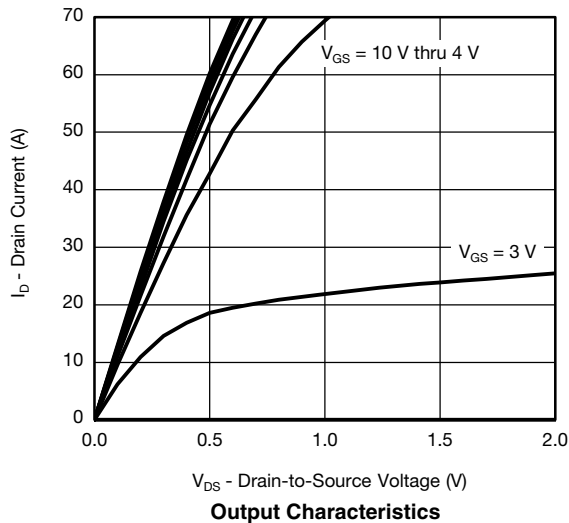
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# SiZ730DT

Vishay Siliconix

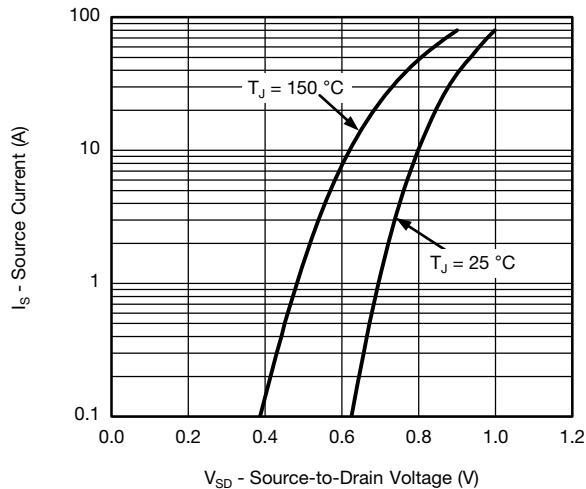


## CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

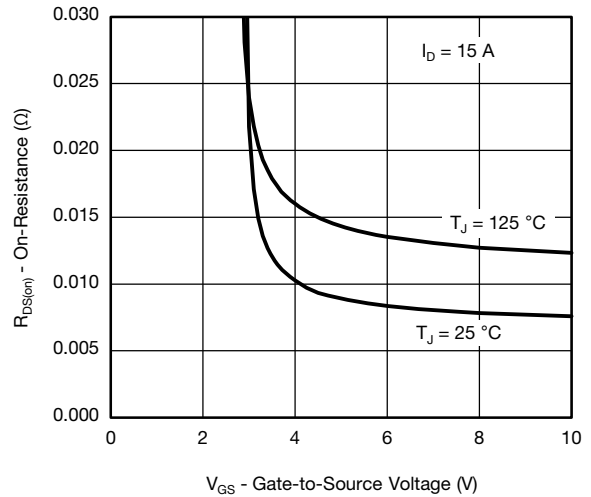




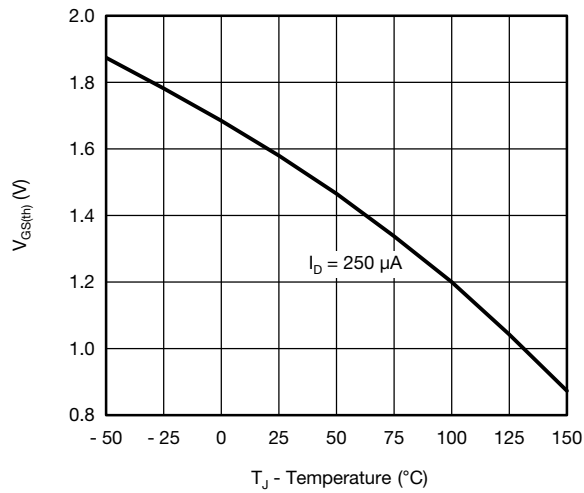
**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



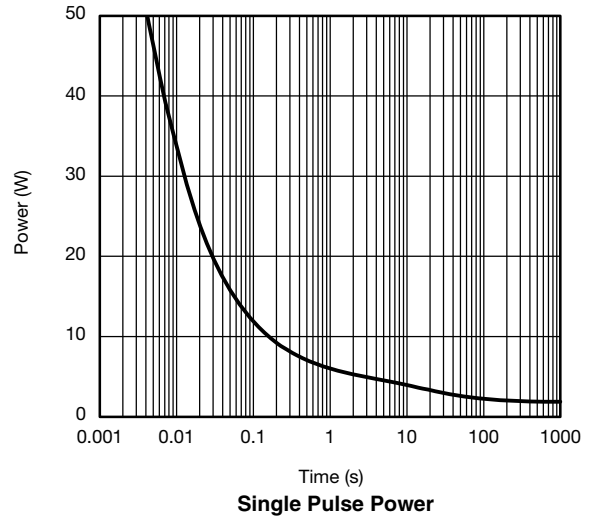
Source-Drain Diode Forward Voltage



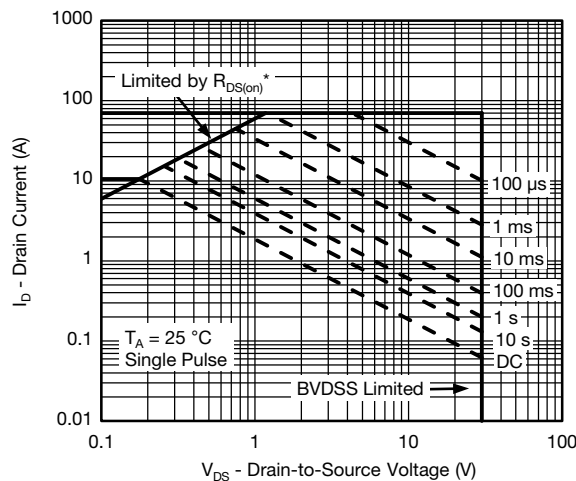
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



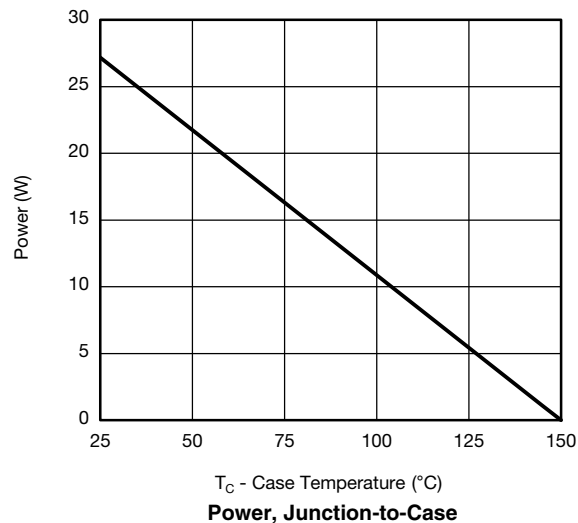
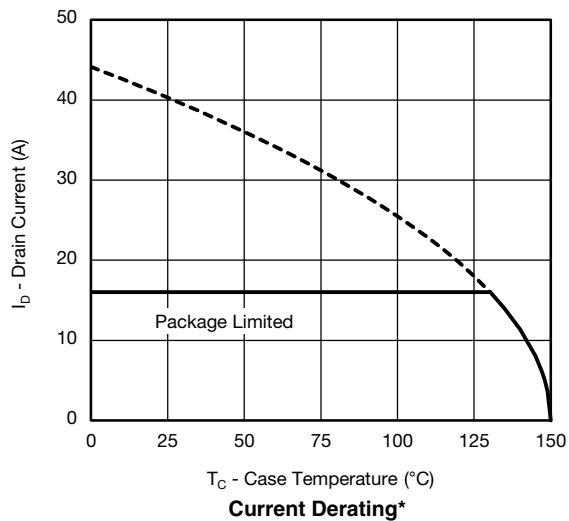
Safe Operating Area, Junction-to-Ambient

# SiZ730DT

Vishay Siliconix



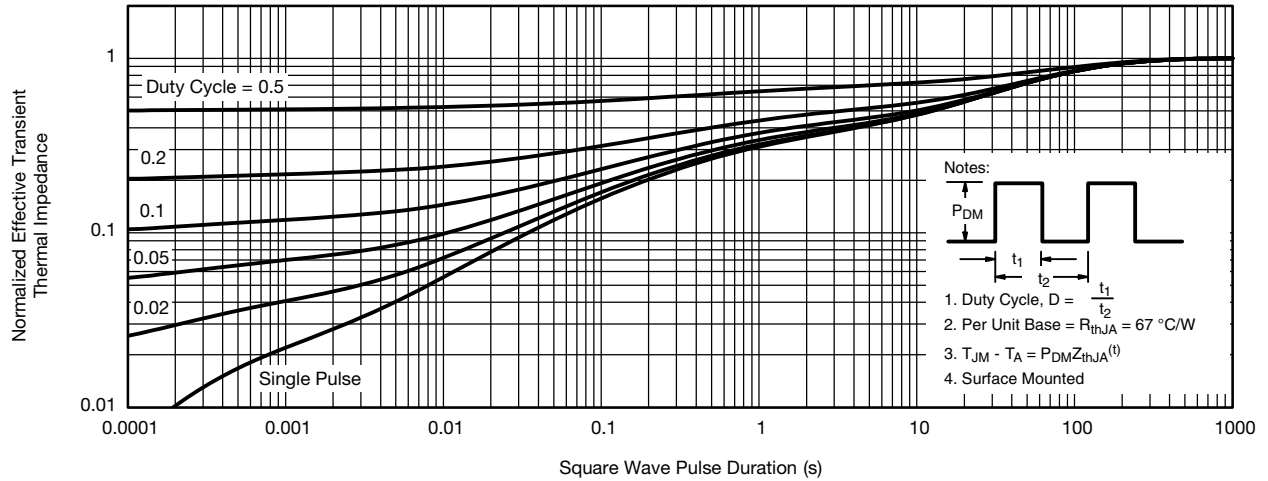
## CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



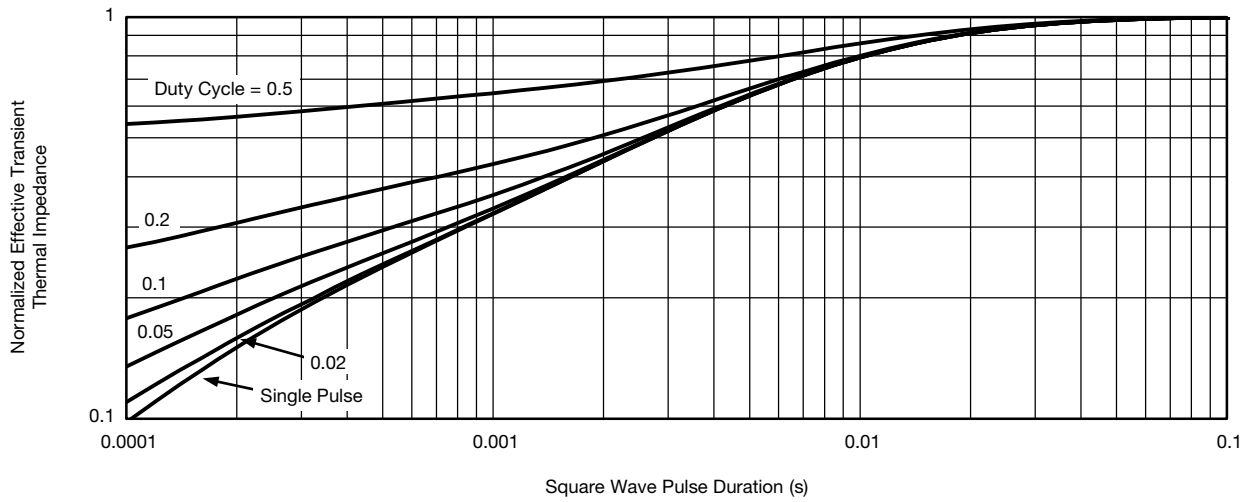
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



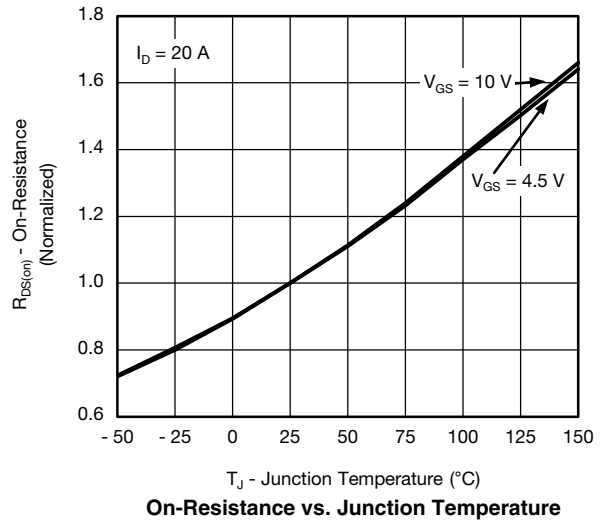
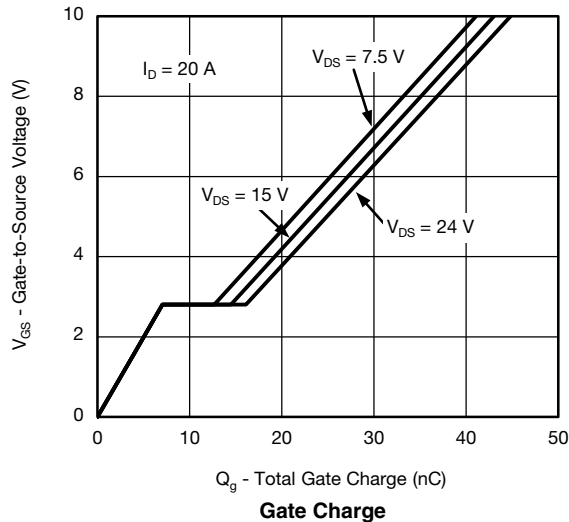
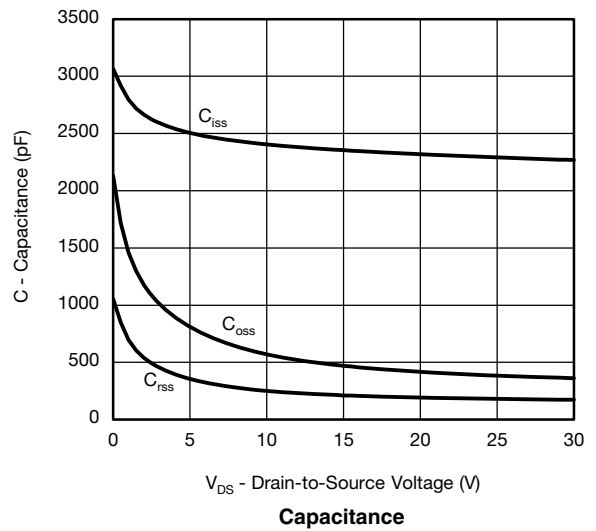
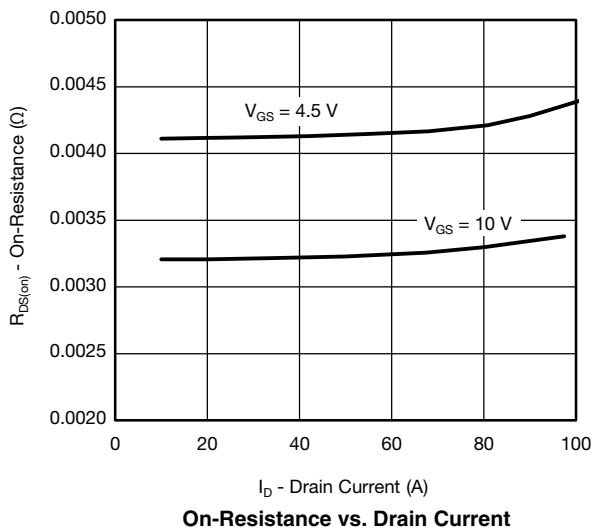
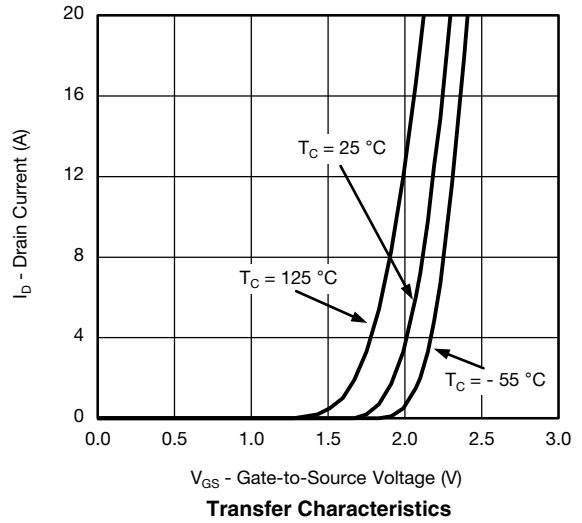
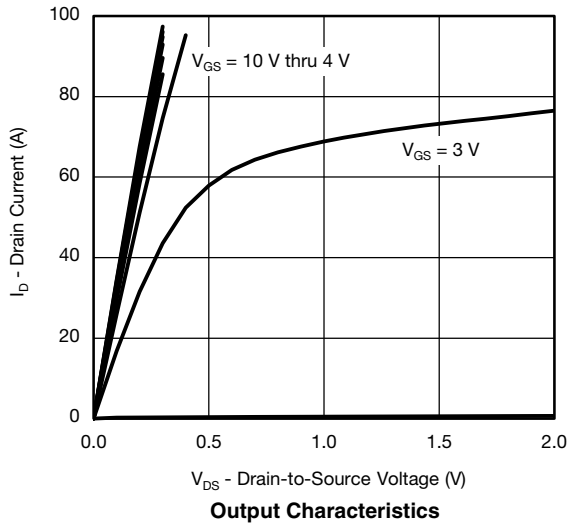
**Normalized Thermal Transient Impedance, Junction-to-Case**

# Si730DT

Vishay Siliconix



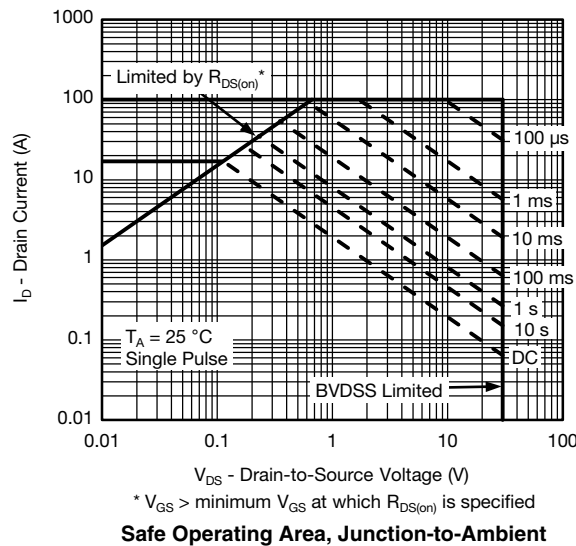
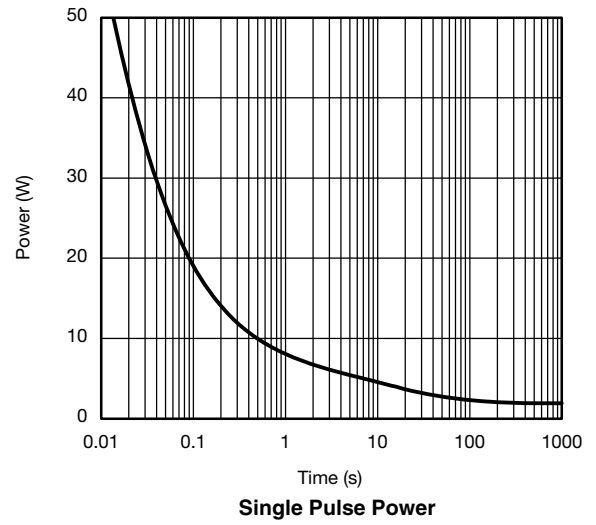
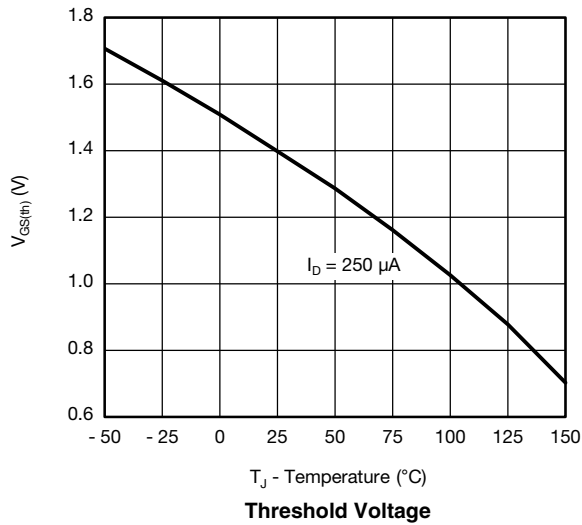
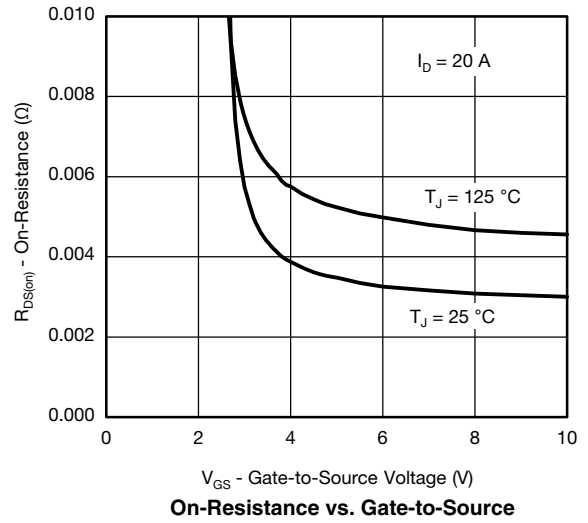
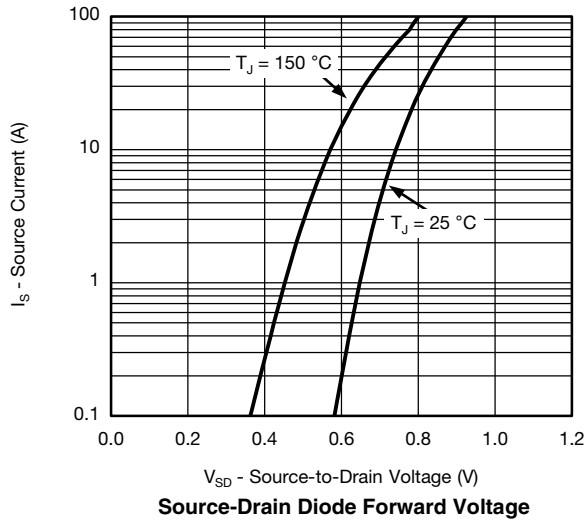
## CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





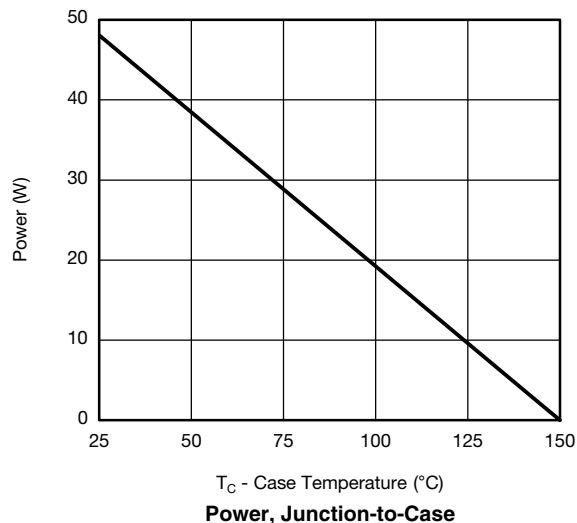
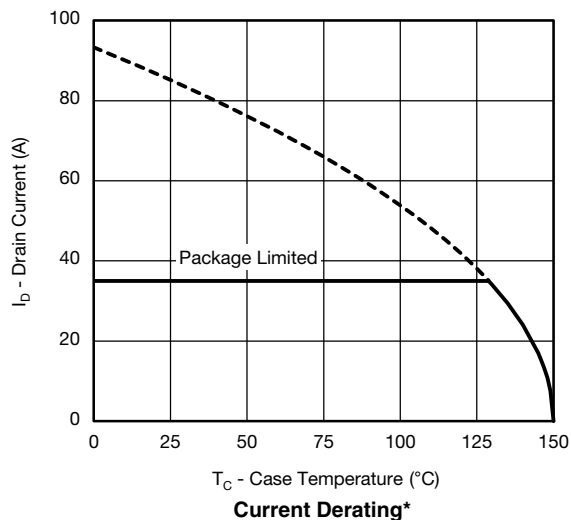


**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)





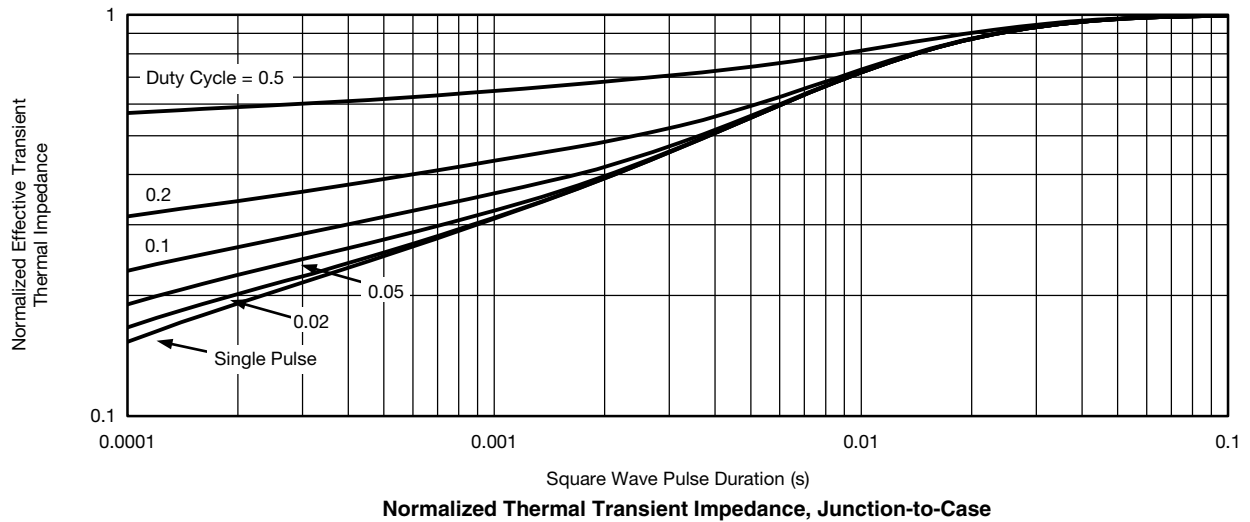
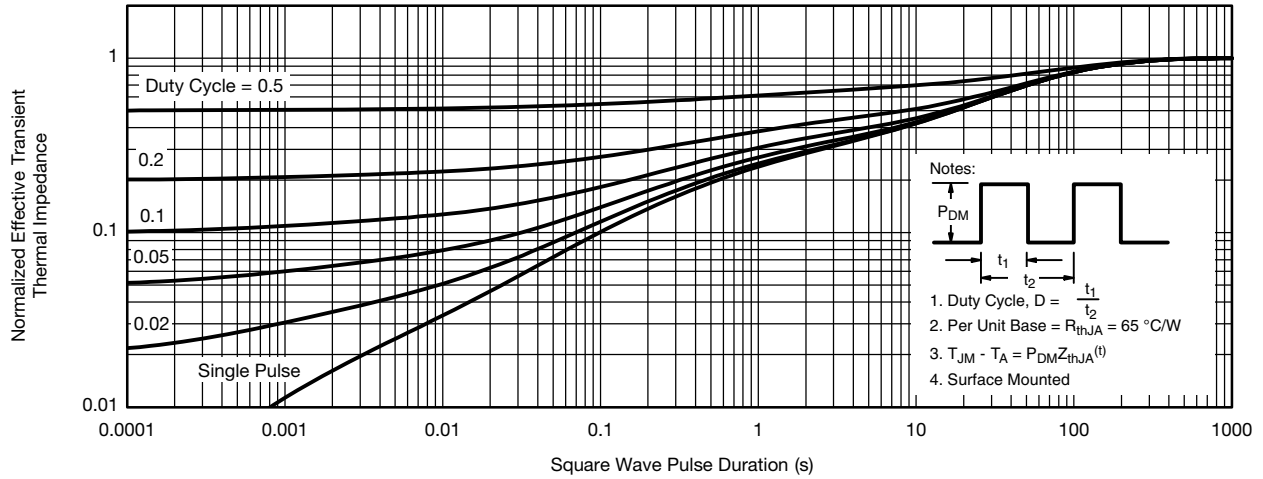
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\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

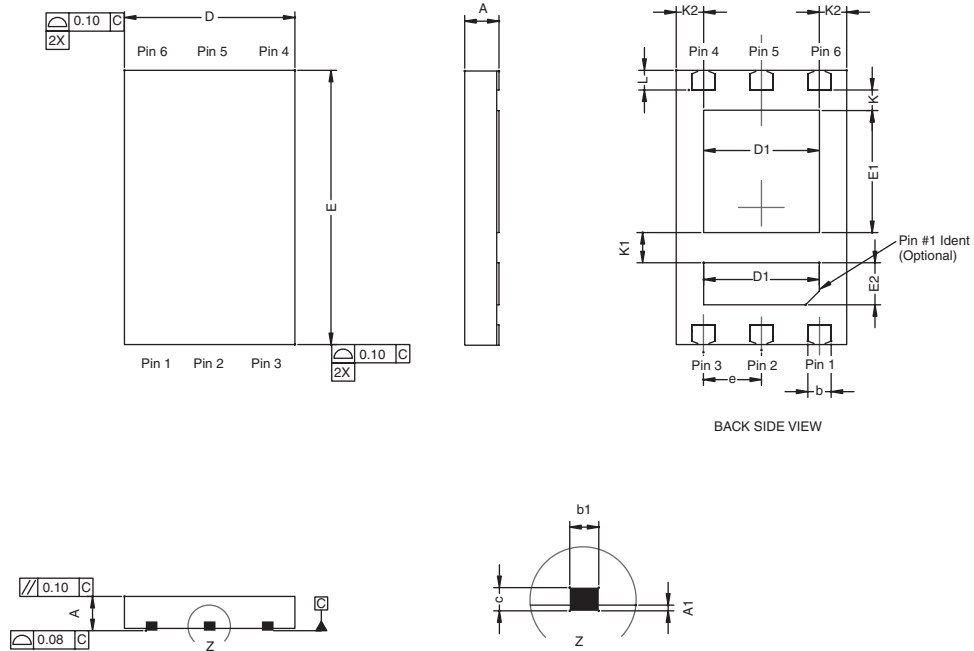


**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



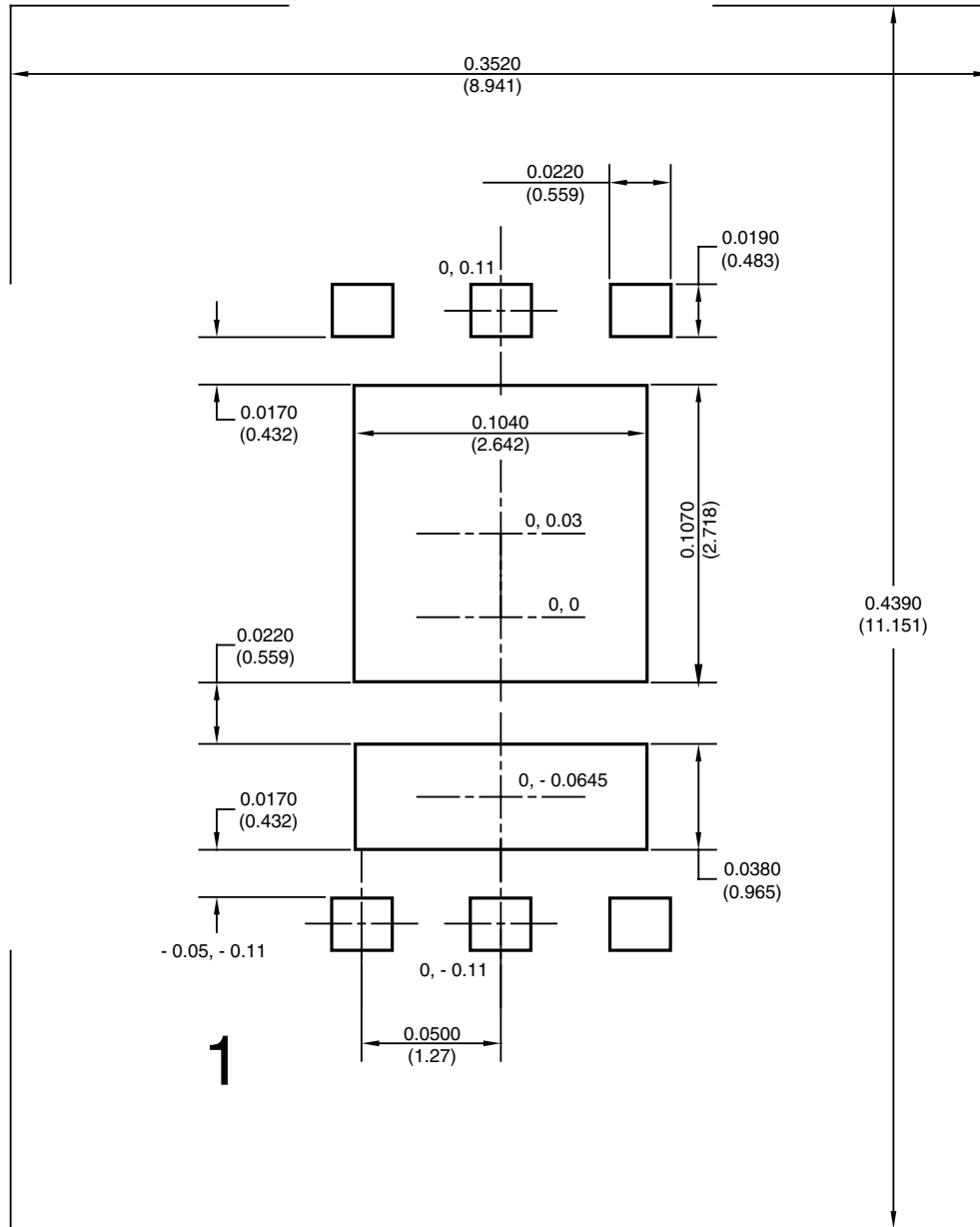
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?67648](http://www.vishay.com/ppg?67648).

### PowerPAIR™ 6 x 3.7 CASE OUTLINE



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	-	0.05	0.000	-	0.002
b	0.46	0.51	0.56	0.018	0.020	0.022
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	3.65	3.73	3.81	0.144	0.147	0.150
D1	2.41	2.53	2.65	0.095	0.100	0.104
E	5.92	6.00	6.08	0.233	0.236	0.239
E1	2.62	2.67	2.72	0.103	0.105	0.107
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.05 BSC		
K	0.45 TYP.			0.018 TYP.		
K1	0.66 TYP.			0.026 TYP.		
K2	0.60 TYP.			0.024 TYP.		
L	0.38	0.43	0.48	0.015	0.017	0.019
ECN: S-82772-Rev. B, 17-Nov-08 DWG: 5979						

## RECOMMENDED PAD FOR PowerPAIR™ 6 x 3.7



Recommended PAD for PowerPAIR 6 x 3.7  
 Dimensions in inches (mm)  
 Keep-out 0.3520 (8.94) x 0.4390 (11.151)



## **Disclaimer**

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