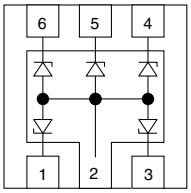
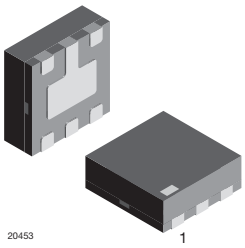
5-Line ESD Protection Diode Array in LLP75



19956



20453

FEATURES

- Ultra compact LLP75-6L package
- Low profile < 0.6 mm
- 5-line ESD protection
- Low leakage current I_R < 0.1 µA
- Low load capacitance C_D = 13 pF
- ESD immunity acc. IEC 61000-4-2
  ± 15 kV contact discharge
  ± 15 kV air discharge
- Working voltage range V_{RWM} = 5 V
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

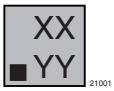
e4

RoHS COMPLIANT

HALOGEN FREE

GREEN (5-2008)

MARKING (example only)



21001

Dot = pin 1 marking
XX = date code
YY = type code (see table below)

DESIGN SUPPORT TOOLS

click logo to get started

3D Models Available

ORDERING INFORMATION

DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VESD05A5A-HSF	VESD05A5A-HSF-GS08	3000	15 000

PACKAGE DATA

DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VESD05A5A-HSF	LLP75-6L	AR	4.2 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

ABSOLUTE MAXIMUM RATINGS VESD05A5A-HSF

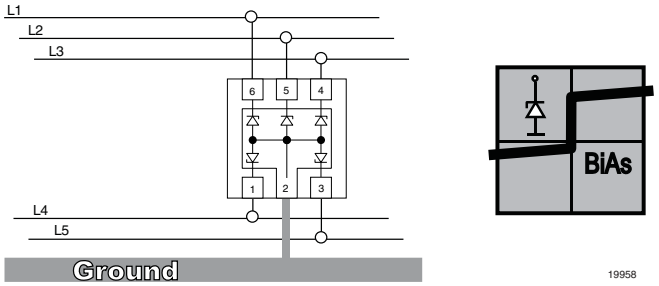
PARAMETER	TEST CONDITIONS		SYMBOL	VALUE	UNIT
Peak pulse current	BiAs-mode: each input (pin 1 to pin 6) to ground (pin 2); acc. IEC 61000-4-5; t_p = 8/20 µs; single shot		I_{PPM}	2.5	A
	BiSy-mode: each input (pin 1 to pin 6) to any other input pin. Pin 2 not connected. Acc. IEC 61000-4-5; t_p = 8/20 µs; single shot			2.5	A
Peak pulse power	BiAs-mode: each input (pin 1 to pin 6) to ground (pin 2); acc. IEC 61000-4-5; t_p = 8/20 µs; single shot		P_{PP}	33	W
	BiSy-mode: each input (pin 1 - pin 6) to any other input pin. Pin 2 not connected. Acc. IEC 61000-4-5; t_p = 8/20 µs; single shot			43	W
ESD immunity	acc. IEC61000-4-2; 10 pulses BiAs-mode: each input (pin 1 to pin 6) to ground (pin 2)	Contact discharge	V_{ESD}	± 15	kV
		Air discharge		± 15	kV
ESD immunity	acc. IEC 61000-4-2 ; 10 pulses BiSy-mode: each input (pin 1 to pin 6) to any other input pin. Pin 2 not connected.	Contact discharge	V_{ESD}	± 10	kV
		Air discharge		± 10	kV
Operating temperature	Junction temperature		T_J	-40 to +125	°C
Storage temperature			T_{STG}	-55 to +150	°C

For technical questions, contact: ESDprotection@vishay.com

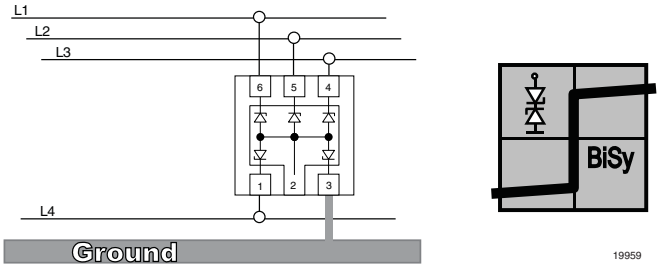
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APPLICATION NOTE:

a. With the VESD05A5A-HSF 5 different signal or data lines can be clamped to ground. Due to the different clamping levels in forward and reverse direction the VESD05A5A-HSF clamping behavior is bidirectional and asymmetrical (BiAs).



b. If symmetrical clamping behaviour is required the VESD05A5A-HSF can also be used as a bidirectional symmetrical protection device protecting up to 4 lines. In this case pin no. 2 must not be connected.



ELECTRICAL CHARACTERISTICS VESD05A5A-HSF (Between pin 1, 3, 4, 5 or 6, and pin 2) (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITIONS/REMARKS**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	5	lines
Reverse stand-off voltage	Max. reverse working voltage	V_{RWM}	-	-	5	V
Reverse voltage	at I_R = 0.1 µA	V_R	5	-	-	V
Max. reverse current	at V_R = 5 V	I_R	-	< 0.01	0.1	µA
Reverse breakdown voltage	at I_R = 1 mA	V_{BR}	6	6.7	7.5	V
Reverse clamping voltage	at I_{PP} = 1 A	V_C	-	9	10	V
	at I_{PP} = I_{PPM} = 2.5 A	V_C	-	12	13	V
Forward clamping voltage	at I_{PP} = 1 A	V_F	-	2	2.5	V
	at I_{PP} = I_{PPM} = 2.5 A	V_F	-	3.2	4	V
Line capacitance	at V_R = 0 V; f = 1 MHz	C_D	-	13	15	pF
	at V_R = 2.5 V; f = 1 MHz	C_D	-	8	-	pF

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TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

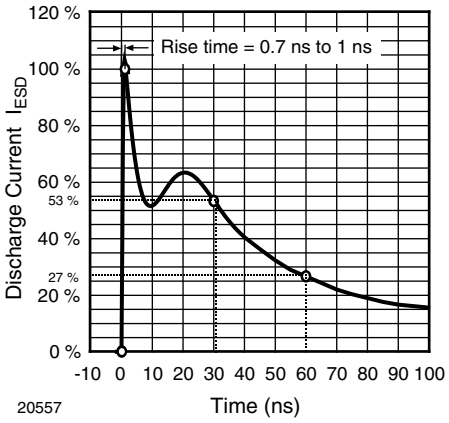


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω/150 pF)

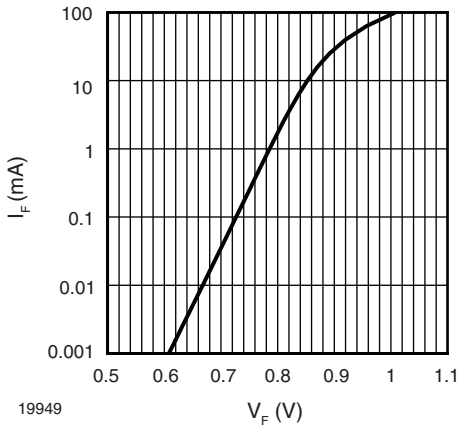


Fig. 4 - Typical Forward Current I_F vs. Forward Voltage V_F

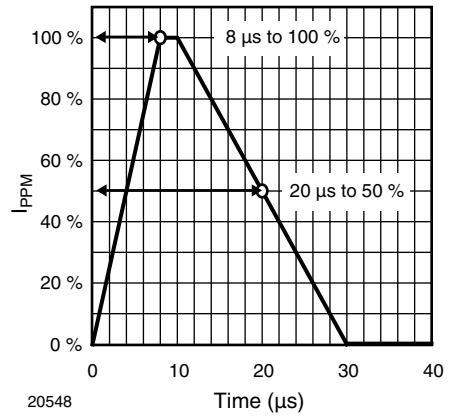


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

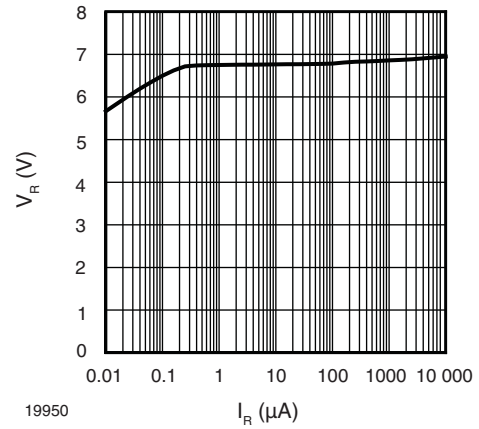


Fig. 5 - Typical Reverse Voltage V_R vs. Reverse Current I_R

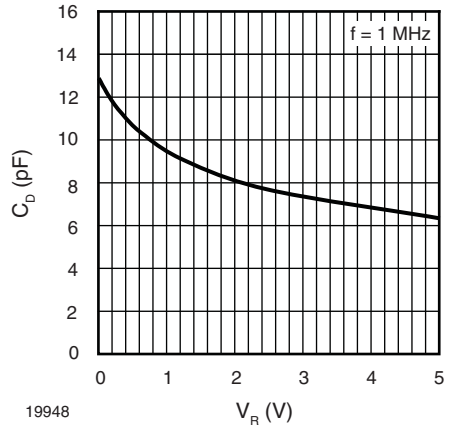


Fig. 3 - Typical Capacitance C_D vs. Reverse Voltage V_R

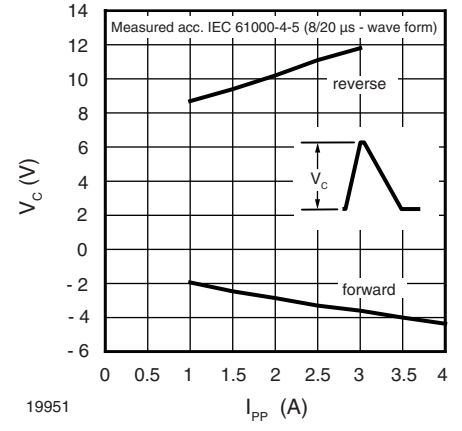


Fig. 6 - Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

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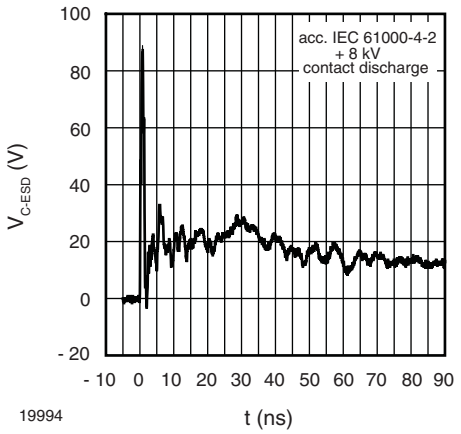


Fig. 7 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

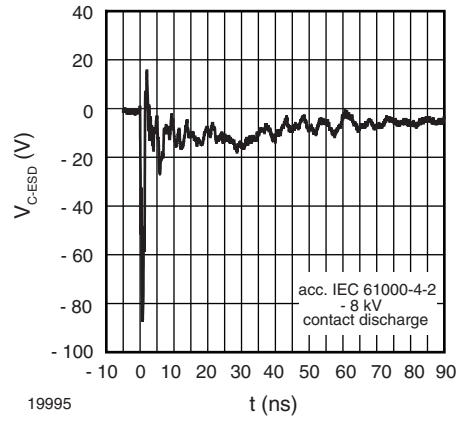


Fig. 8 - Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

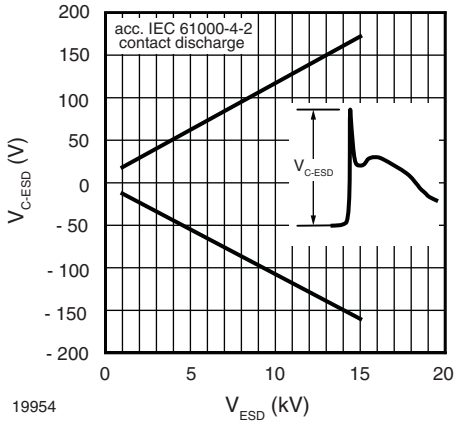
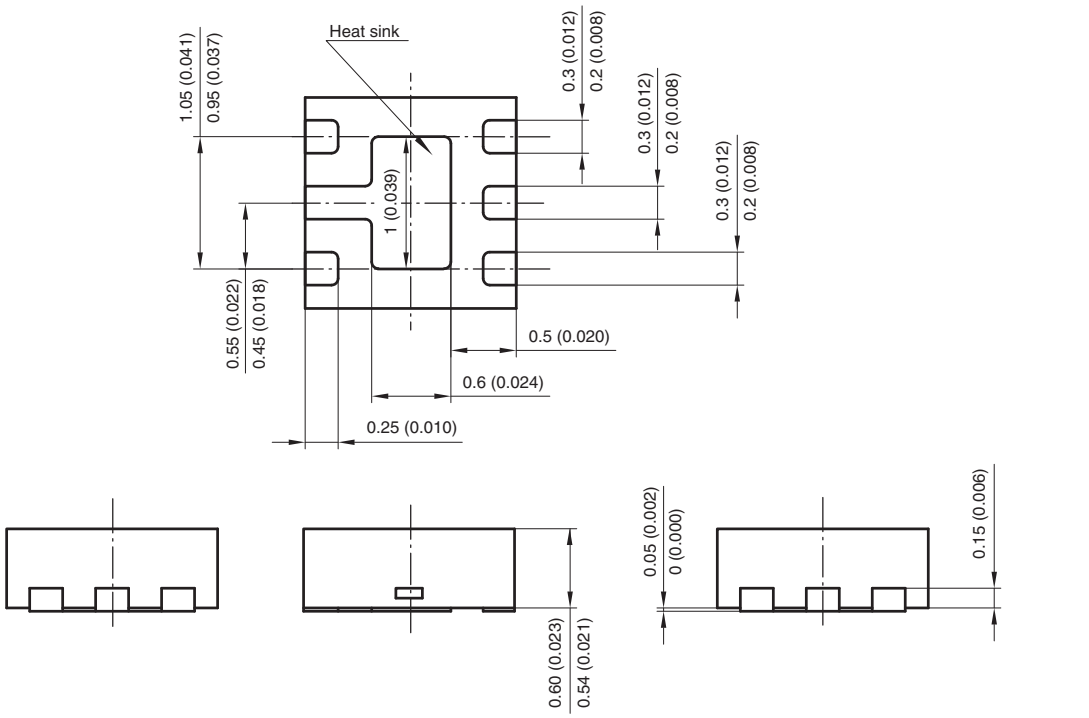
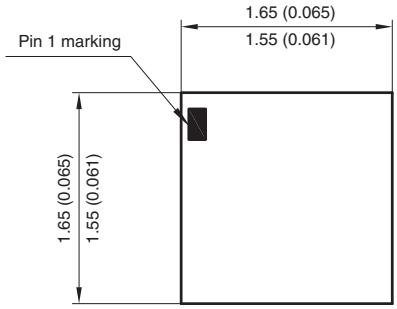


Fig. 9 - Typical max. Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)

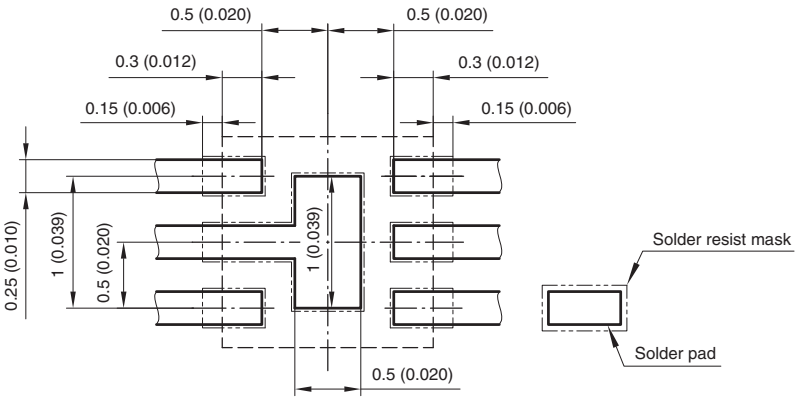
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PACKAGE DIMENSIONS in millimeters (Inches): **LLP75-6L**



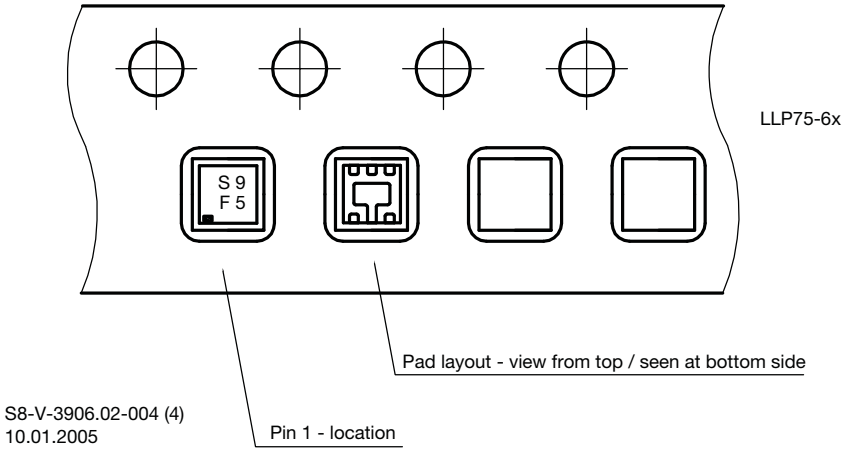


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Rev. 4 - Date: 21. March 2006
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