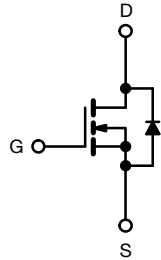
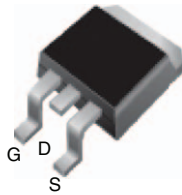


D Series Power MOSFET



RoHS
COMPLIANT
HALOGEN
FREE

| PRODUCT SUMMARY | |
|---|-----------------------|
| V_{DS} (V) at T_J max. | 450 |
| $R_{DS(on)}$ max. (Ω) at 25 °C | $V_{GS} = 10$ V 0.6 |
| Q_g max. (nC) | 30 |
| Q_{gs} (nC) | 4 |
| Q_{gd} (nC) | 7 |
| Configuration | Single |

D²PAK (TO-263)


N-Channel MOSFET

FEATURES

- Optimal design
 - Low area specific on-resistance
 - Low input capacitance (C_{iss})
 - Reduced capacitive switching losses
 - High body diode ruggedness
 - Avalanche energy rated (UIS)
- Optimal efficiency and operation
 - Low cost
 - Simple gate drive circuitry
 - Low figure-of-merit (FOM): $R_{on} \times Q_g$
 - Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Consumer electronics
 - Displays (LCD or plasma TV)
- Server and telecom power supplies
 - SMPS
- Industrial
 - Welding
 - Induction heating
 - Motor drives
- Battery chargers

ORDERING INFORMATION

| | |
|---------------------------------|-----------------------------|
| Package | D ² PAK (TO-263) |
| Lead (Pb)-free and Halogen-free | SiHB10N40D-GE3 |

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)


| PARAMETER | SYMBOL | LIMIT | UNIT |
|---|------------------|----------------|------|
| Drain-Source Voltage | V_{DS} | 400 | V |
| Gate-Source Voltage | V_{GS} | ± 30 | |
| Gate-Source Voltage AC ($f > 1$ Hz) | | 30 | |
| Continuous Drain Current ($T_J = 150$ °C) | V_{GS} at 10 V | $T_C = 25$ °C | A |
| | | $T_C = 100$ °C | |
| Pulsed Drain Current ^a | I_{DM} | 23 | |
| Linear Derating Factor | | 1.2 | W/°C |
| Single Pulse Avalanche Energy ^b | E_{AS} | 194 | mJ |
| Maximum Power Dissipation | P_D | 147 | W |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +150 | °C |
| Drain-Source Voltage Slope | dV/dt | $T_J = 125$ °C | V/ns |
| Reverse Diode dV/dt ^d | | 0.6 | |
| Soldering Recommendations (Peak temperature) ^c | for 10 s | 300 | °C |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 2.3$ mH, $R_g = 25$ Ω , $I_{AS} = 13$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, starting $T_J = 25$ °C.



| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------------|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | R_{thJA} | - | 62 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 0.85 | |

| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|---------------------|---|---|------|------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 400 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 250\text{ }\mu\text{A}$ | | - | 0.53 | - | V/°C |
| Gate-Source Threshold Voltage (N) | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 3 | - | 5 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 30\text{ V}$ | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 1 | μA |
| | | $V_{DS} = 320\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | | - | - | 10 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 5\text{ A}$ | - | 0.5 | 0.6 | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = 50\text{ V}, I_D = 5\text{ A}$ | | - | 2.7 | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$ | | - | 526 | - | pF |
| Output Capacitance | C_{oss} | | | - | 59 | - | |
| Reverse Transfer Capacitance | C_{rss} | | | - | 9 | - | |
| Effective Output Capacitance, Energy Related ^a | $C_{o(er)}$ | $V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 320\text{ V}$ | | - | 66 | - | |
| Effective Output Capacitance, Time Related ^b | $C_{o(tr)}$ | | | - | 84 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 5\text{ A}, V_{DS} = 320\text{ V}$ | - | 15 | 30 | nC |
| Gate-Source Charge | Q_{gs} | | | - | 4 | - | |
| Gate-Drain Charge | Q_{gd} | | | - | 7 | - | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 400\text{ V}, I_D = 10\text{ A}, V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$ | | - | 12 | 24 | ns |
| Rise Time | t_r | | | - | 18 | 36 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 18 | 36 | |
| Fall Time | t_f | | | - | 14 | 28 | |
| Gate Input Resistance | R_g | $f = 1\text{ MHz}, \text{open drain}$ | | 0.9 | 1.8 | 3.6 | Ω |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 10 | A |
| Pulsed Diode Forward Current | I_{SM} | | | - | - | 40 | |
| Diode Forward Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 5\text{ A}, V_{GS} = 0\text{ V}$ | | - | - | 1.2 | V |
| Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$ | | - | 230 | - | ns |
| Reverse Recovery Charge | Q_{rr} | | | - | 1.6 | - | μC |
| Reverse Recovery Current | I_{RRM} | | | - | 14 | - | A |

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
- b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

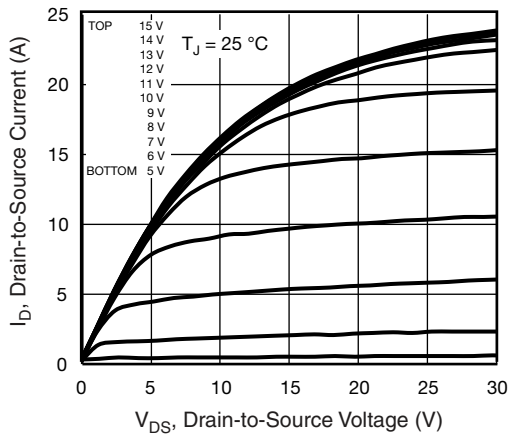


Fig. 1 - Typical Output Characteristics

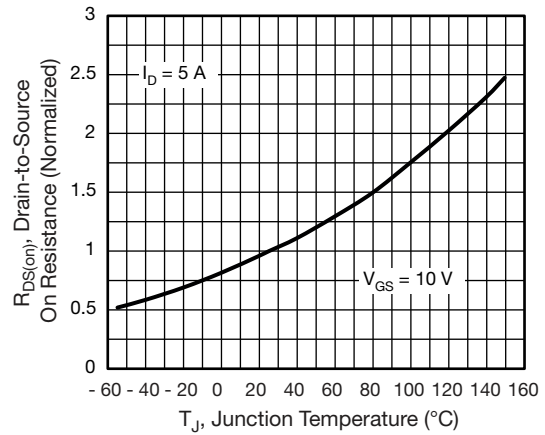


Fig. 4 - Normalized On-Resistance vs. Temperature

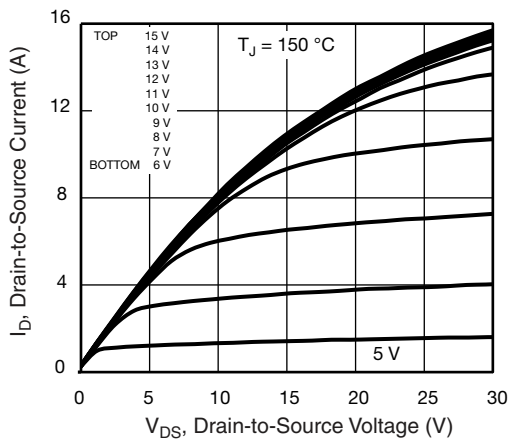


Fig. 2 - Typical Output Characteristics

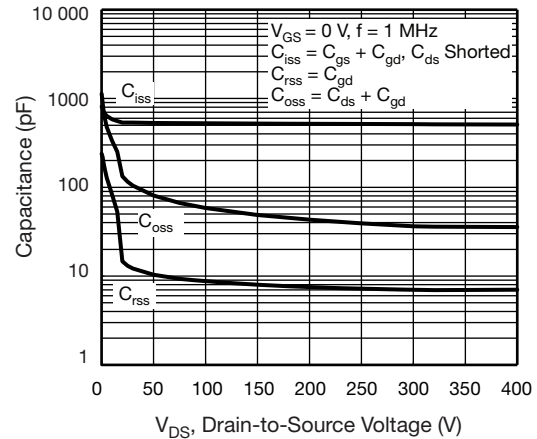


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

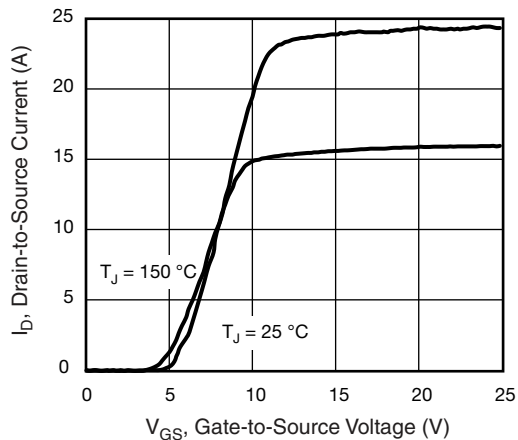


Fig. 3 - Typical Transfer Characteristics

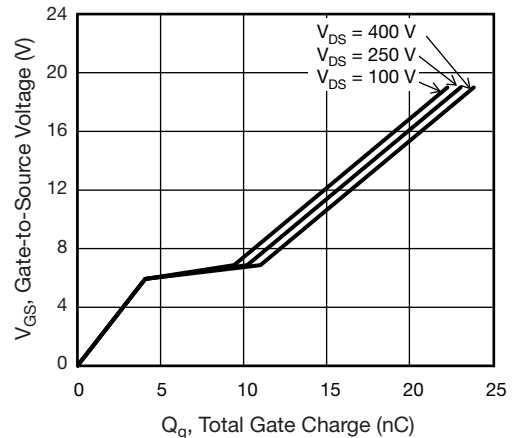


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

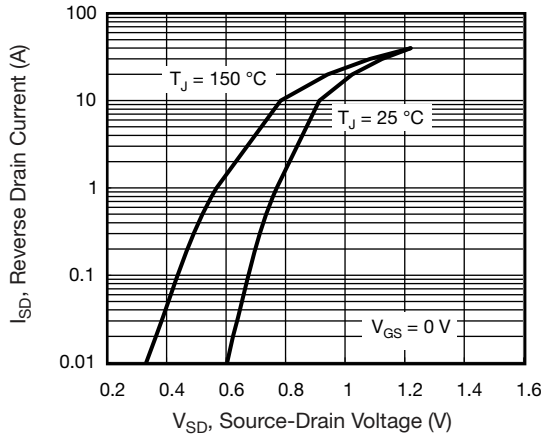


Fig. 7 - Typical Source-Drain Diode Forward Voltage

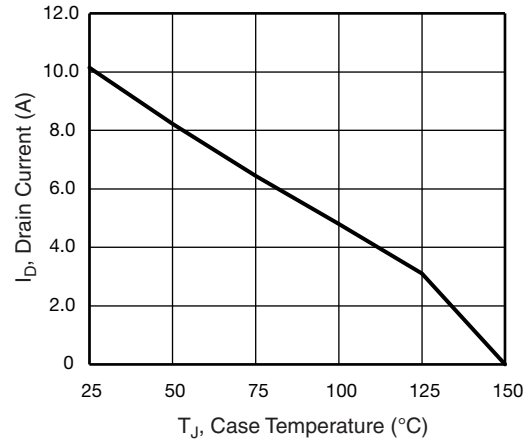


Fig. 9 - Maximum Drain Current vs. Case Temperature

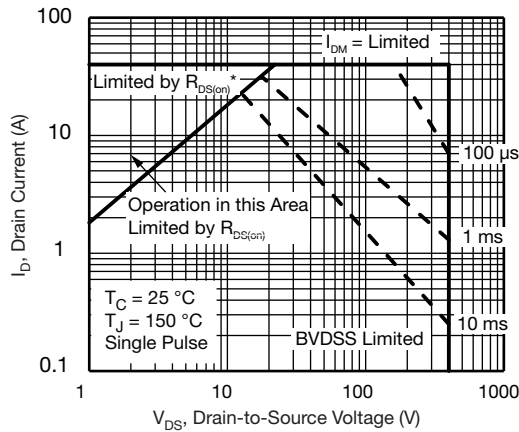


Fig. 8 - Maximum Safe Operating Area

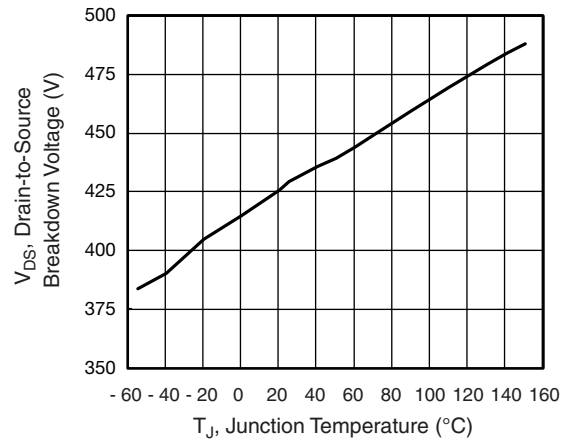


Fig. 10 - Temperature vs. Drain-to-Source Voltage

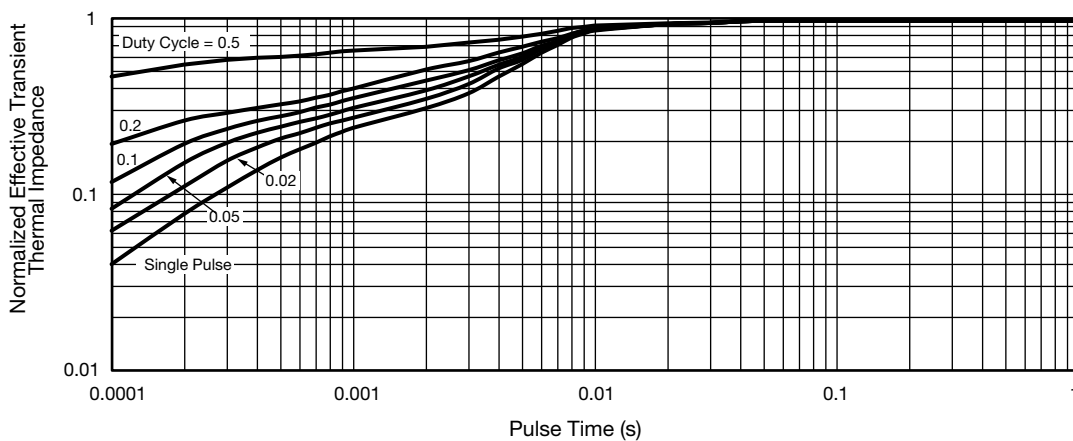


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

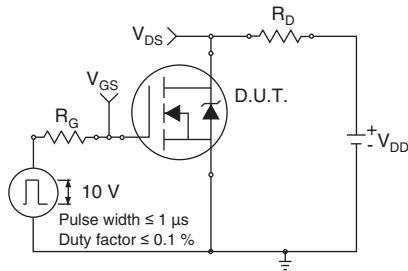


Fig. 12 - Switching Time Test Circuit

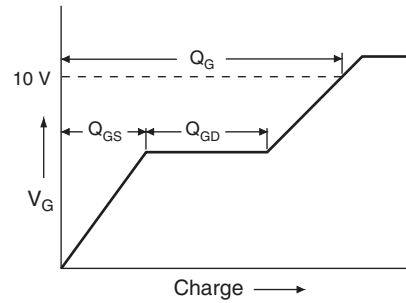


Fig. 16 - Basic Gate Charge Waveform

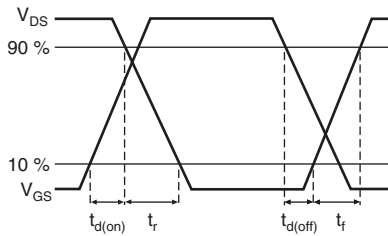


Fig. 13 - Switching Time Waveforms

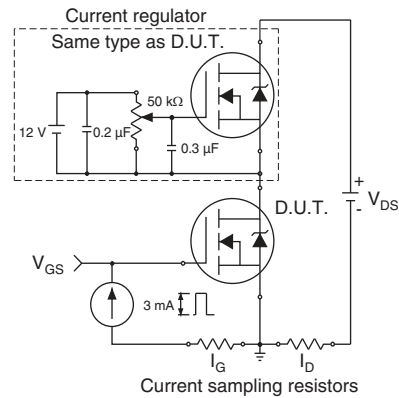


Fig. 17 - Gate Charge Test Circuit

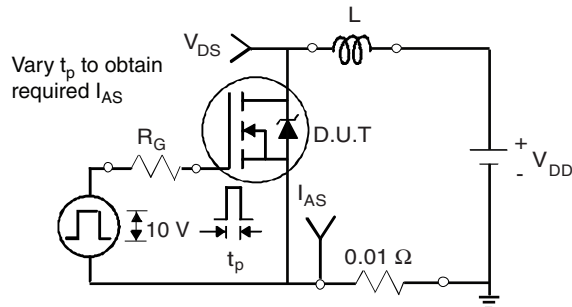


Fig. 14 - Unclamped Inductive Test Circuit

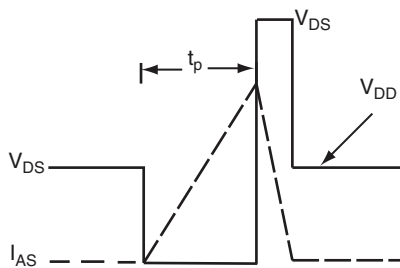


Fig. 15 - Unclamped Inductive Waveforms

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 18 - For N-Channel

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